TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

64 GBIT (8G × 8 BIT) CMOS NAND E^2PROM (Triple-Level-Cell)

DESCRIPTION

The TC58NVG6T2FTA00 is a single 3.3 V 64 Gbit (79,054,700,544 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) organized as (8192 + 1024) bytes × 258 pages × 4156 blocks. The device has four 9216-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 9216-byte increments. The Erase operation is implemented in a single block unit (2064 Kbytes + 258 Kbytes:9216 bytes x 258 pages).

The TC58NVG6T2FTA00 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization

	TC58NVG6T2FTA00
Memory cell array	9216 × 1047.1171875K × 8
Register	9216 × 8
Page size	9216 bytes
Block size	(2064K + 258K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read,
  Multi Page Program, Multi Block Erase, Multi Page Read

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 4000 blocks
  Max 4156 blocks

- Power supply
  V_{CC} = 2.7 V to 3.6 V

- Access time

Cell array to register	110 μs max
Serial Read Cycle	25 ns min

- Program/Erase time

Auto Page Program	2000 μs/page typ.
Auto Block Erase	3 ms/block typ.

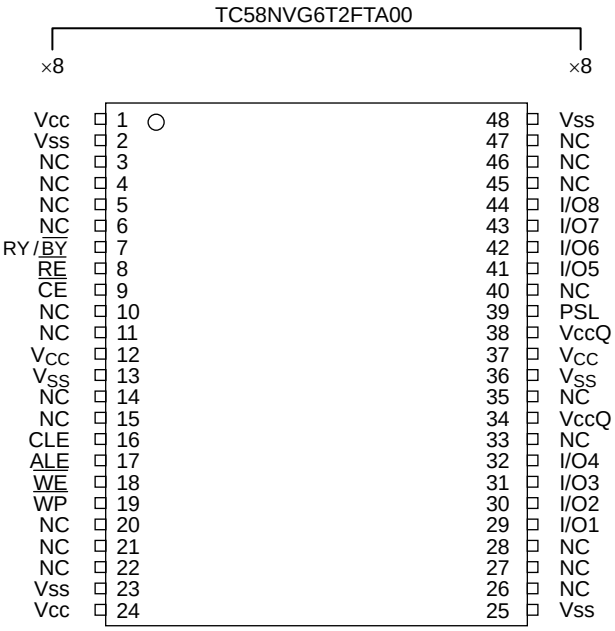
- Operating current

Read (25 ns cycle)	50 mA max.
Program (avg.)	50mA max.
Erase (avg.)	50 mA max.
Standby	100 μA max

- Package
  TSOP I 48-P-1220-0.50C (Weight: 0.53 g typ.)

- FOR RELIABILITY GUIDANCE, PLEASE REFER TO THE APPLICATION NOTES AND COMMENTS (15).
  60 bit ECC for each 1K bytes is required.

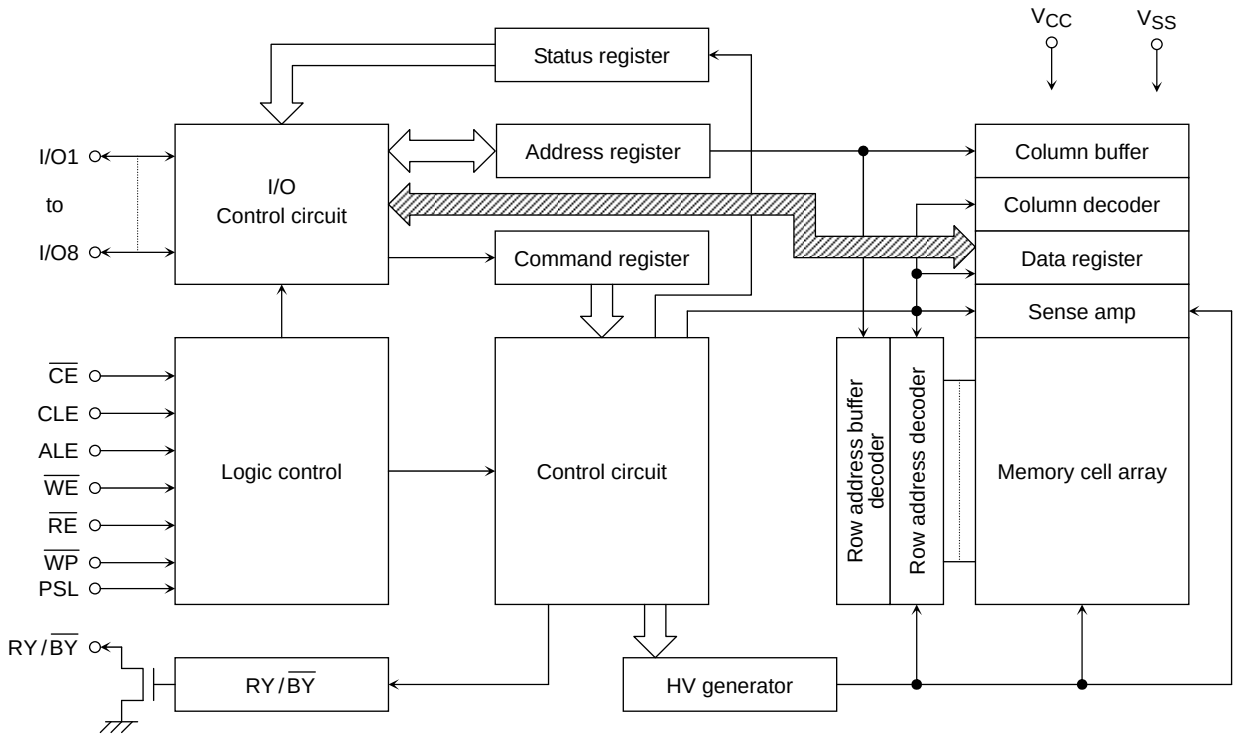
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O1 ~ I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
PSL	Power on select
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
V_{CC}	Power supply
V_{CCQ}	I/O port power supply
V_{SS}	Ground
N.C	No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 V to V_{CC} + 0.3 V (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS*

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	4000	—	4156	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (11) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over the device lifetime.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage		2.7 V	—	3.6 V	V
V_{IH}	High Level input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	0.8 x Vcc	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	−0.3*	—	0.2 x Vcc	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO0} *	Power On Reset Current	PSL = GND or NU	—	—	30	mA
		PSL = Vcc,FFh command input after Power On	—	—	30	mA
I_{CCO1}	Serial Read Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 50 ns	—	—	50	mA
I_{CCO2}	Programming Current	—	—	—	50	mA
I_{CCO3}	Erasing Current	—	—	—	50	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0 V/V_{CC}, PSL=0V/Vcc/NU	—	—	100	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	—	0.4	V
I_{OL} (RY/$\overline{BY}$)	Output current of RY/$\overline{BY}$ pin	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	8	—	mA

* Refer to application note(2) for detail

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	0	—	ns
t_{CLS2}	CLE Setup Time	30	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	$\overline{CE}$ Setup Time	8	—	ns
t_{CS2}	$\overline{CE}$ Setup Time	20	—	ns
t_{CH}	$\overline{CE}$ Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	0	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	10	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns
t_{WHW} *	$\overline{WE}$ High Hold Time from final address to first data	200	—	ns
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	$\overline{RE}$ Access Time	—	20	ns
t_{REAID}	$\overline{RE}$ Access Time for ID Read	—	22	ns
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low	10	—	ns
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns
t_{RHOH}	Data Output Hold Time from $\overline{RE}$ High	25	—	ns
t_{RLOH}	Data Output Hold Time from $\overline{RE}$ Low	5	—	ns
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	30	ns
t_{CLHZ}	CLE High to Output High Impedance	—	30	ns
t_{REH}	$\overline{RE}$ High Hold Time	10	—	ns
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low for data output	400	—	ns
t_{WHRS}	$\overline{WE}$ High to $\overline{RE}$ Low for Status & ID Read	180	—	ns
t_{R1}	Memory Cell Array to Starting Address	—	70	μs
t_{R2}	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	25	μs
t_{R3}	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	15	μs
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	10/10/30/200	μs

* tWHW is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ falling edge of first data cycle.

AC TEST CONDITIONS

PARAMETER	CONDITION
	2.7 V ≤ V_{CC} ≤ 3.6 V
Input level	0 V to Vcc
Input pulse rise and fall time	3ns
Input comparison level	Vcc/2
Output data comparison level	Vcc/2
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY / $\overline{BY}$ pin.
(Refer to Application Note (7) toward the end of this document.)

PROGRAMMING AND ERASING CHARACTERISTICS
(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	2000	6000	μs	
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)	—	—	10	μs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	10000	μs	(2)
$t_{DCBSYW3}$	Data Cache Busy Time in Write Cache (following 1Ah)	—	10	6000	μs	(3)
N	Number of Partial Program Cycles in the Same Page	—	—	—		(1)
t_{BERASE}	Block Erasing Time	—	3	10	ms	

(1) Refer to Application Note (10) toward the end of this document.

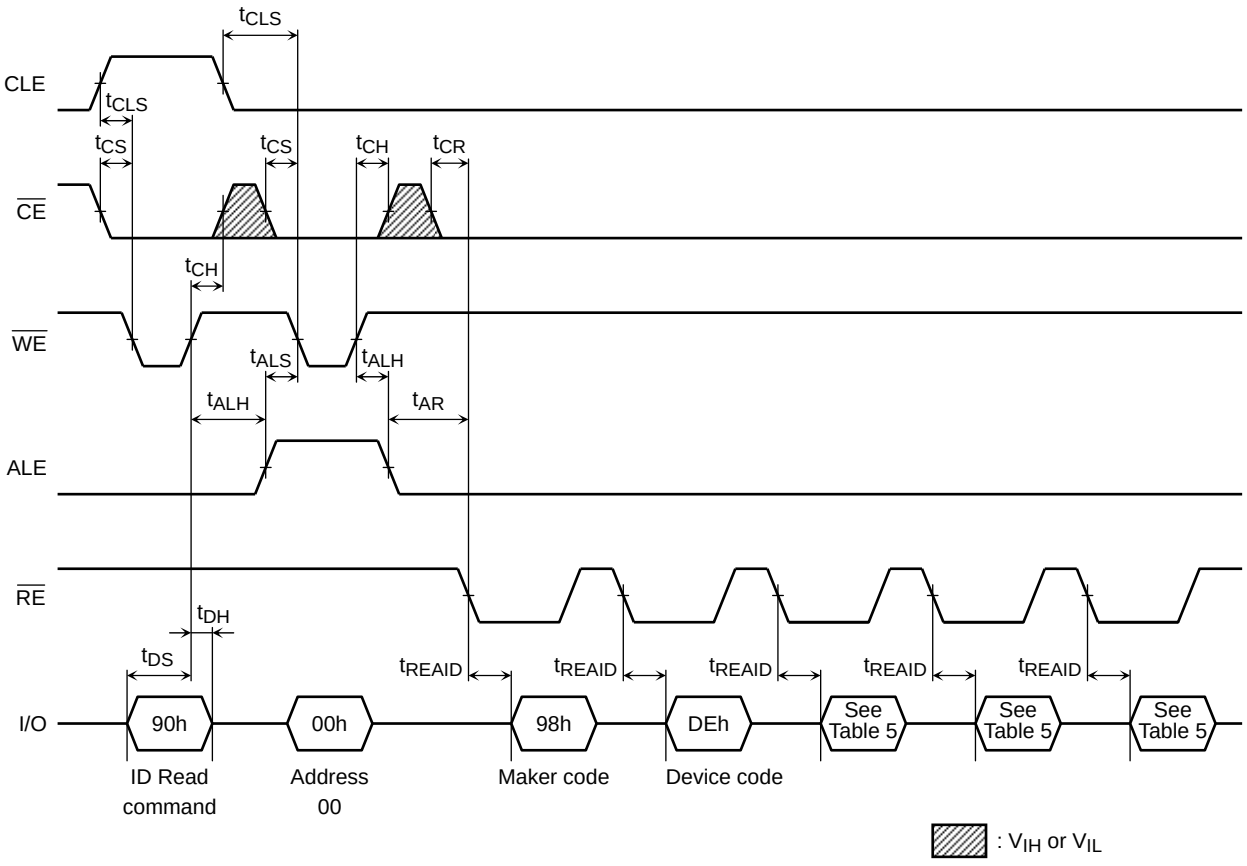
(2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

(3) In case of Program Operation with Data Cache, $t_{DCBSYW3}$ depends on the timing between internal programming time and data in time.

Data Output

When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25 ns MIN). On this condition, waveforms look like normal serial read mode.
When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.
Data Output can be output synchronously with the clock after 05h+Address*5cycle+E0h sequence.

ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

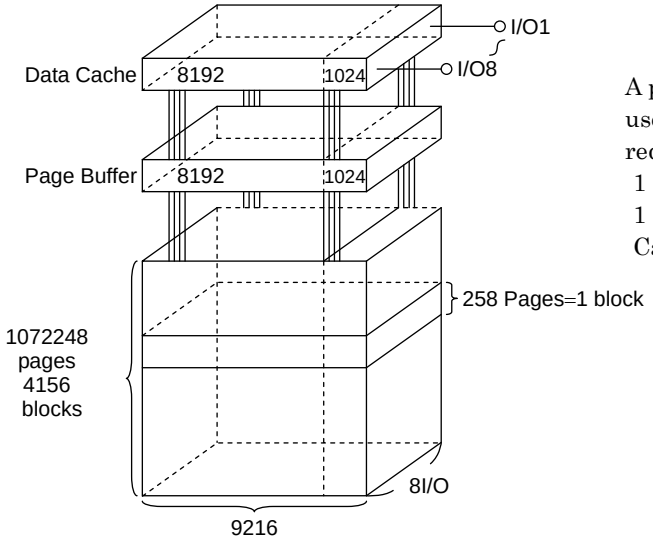
The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vcc with an appropriate resister.

Power on Select: PSL

The PSL signal is used to select whether the device initialization should take place during the device power on or during the first Reset. Please refer to the application note (2) for details.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 9216 bytes in which 8192 bytes are used for main memory storage and 1024 bytes are for redundancy or for other uses.
1 page = 9216 bytes
1 block = 9216 bytes × 258 pages = (2064K + 258K)bytes
Capacity = 9216 bytes × 258 pages × 4156 blocks

An address is read in via the I/O port over five consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	CA13	CA12	CA11	CA10	CA9	CA8
Third cycle	L	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7
Fifth cycle	L	L	L	PA19	PA18	PA17	PA16	PA15

CA0 to CA13: Column address
PA0 to PA19: Page address

PA0 to PA6: WL address in a block
PA7 to PA19: Block address

Note)

(a) Block address (PA7 to PA19) can only be selected between Block 0 and Block 4155.

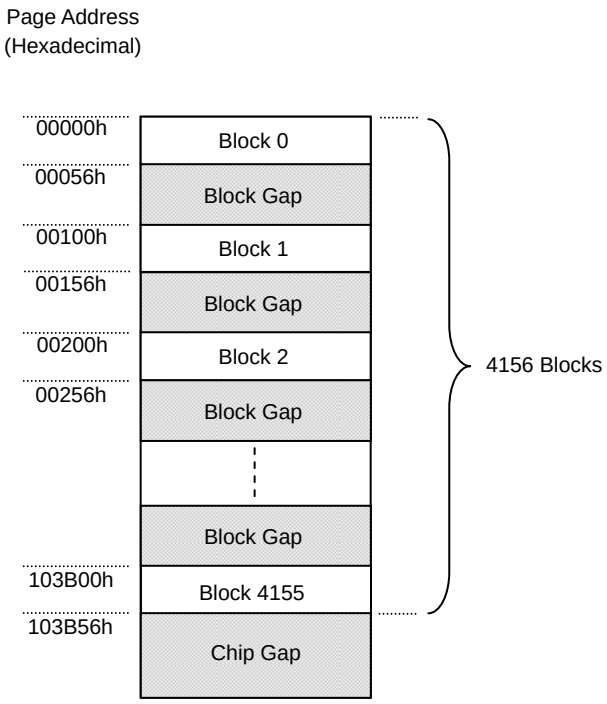
(b) WL address in a block (PA0 to PA6) can only be selected between WL 0 and WL 85.

(c) There are Lower/Middle/Upper address in a WL, which is selected 01/02/03h command.

Input of the address other than specified above is invalid.
If those unspecified addresses are inputted in program or erase operation, the device will output a fail status to respond to status read command.
In case of read operation, some invalid data will be outputted by the device.
Please refer to Application Note (12) toward the end of this document for block management.

Block Arrangement

The device has block gaps and chip gap(s). Block arrangement is as follows.



Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1	PSL *3
Command Input	H	L	L	⌐└⌐	H	*	0V/ V_{CC}/ NU
Data Input	L	L	L	⌐└⌐	H	H	0V/ V_{CC}/ NU
Address input	L	H	L	⌐└⌐	H	*	0V/ V_{CC}/ NU
Serial Data Output	L	L	L	H	¬└¬	*	0V/ V_{CC}/ NU
During Program (Busy)	*	*	*	*	*	H	0V/ V_{CC}/ NU
During Erase (Busy)	*	*	*	*	*	H	0V/ V_{CC}/ NU
During Read (Busy)	*	*	H	*	*	*	0V/ V_{CC}/ NU
	*	*	L	H (*2)	H (*2)	*	0V/ V_{CC}/ NU
Program, Erase Inhibit	*	*	*	*	*	L	0V/ V_{CC}/ NU
Standby	*	*	H	*	*	0 V/V_{CC}	0V/ V_{CC}/ NU

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (8) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

*3: PSL must be tied to either 0V or Vcc, or left unconnected (NU).

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Data Out & Column Address Change in Serial Data Output	05	E0	
Next page Read with WL address increment	31	—	
Next page Read w/o WL address increment	3F	—	
Set 1st Program Mode	09		
Set 2nd Program Mode	0D		
Lower page select	01		
Middle page select	02		
Upper page select	03		
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Program with Data Cache	80	15	
Multi Page Program	80	11	
Input data to page Buffer	80	1A	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	O
Status Read for Multi-Page Program	71	—	O
Reset	FF	—	O

HEX data bit assignment

(Example)

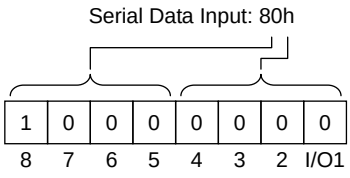


Table 4 shows the operation states for Read mode,when tREH is long.

Table 4. Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L: V_{IL},

ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

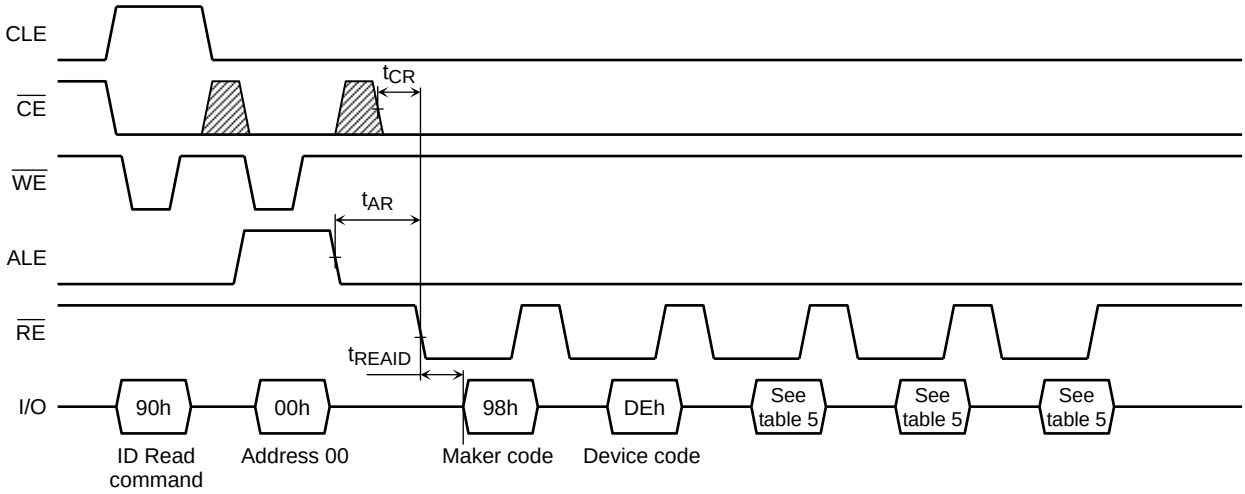


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	0	1	1	1	1	0	DEh
3rd Data	Chip Number, Cell Type	—	—	—	—	—	—	—	—	See table
4th Data	Page Size, Block Size, Redundant Size, Organization	—	—	—	—	—	—	—	—	See table
5th Data	Extended Block	—	—	—	—	—	—	—	—	See table

2nd Data

Description		I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Memory Density per each /CE	8 Gbits	1	1	0	1	0	0	1	1	D3h
	16 Gbits	1	1	0	1	0	1	0	1	D5h
	32 Gbits	1	1	0	1	0	1	1	1	D7h
	64 Gbits	1	1	0	1	1	1	1	0	DEh
	128 Gbits	0	0	1	1	1	0	1	0	3Ah
	256 Gbits	0	0	1	1	1	1	0	0	3Ch

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number per each /CE	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 level cell 4 level cell 8 level cell 16 level cell					0 0 1 1	0 1 0 1		
Reserved		0 or 1	0	0 or 1	0 or 1				

4th Data

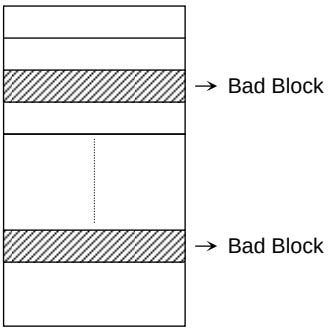
	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	2 KB 4 KB 8 KB Reserved							0 0 1 1	0 1 0 1
Block Size (without redundant area)	Default Value	1		0	0				
	Reserved			0 or 1	0 or 1				
Redundant area size	Default Value		0			0	0		
	Reserved					0 or 1	0 or 1		

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number per each /CE	1 2 4 8					0 0 1 1	0 1 0 1		
Reserved		0 or 1	0 or 1	0 or 1	0 or 1			0 or 1	0 or 1

(11) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



At the time of shipment, the bad block information is marked on each bad block. Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information, if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

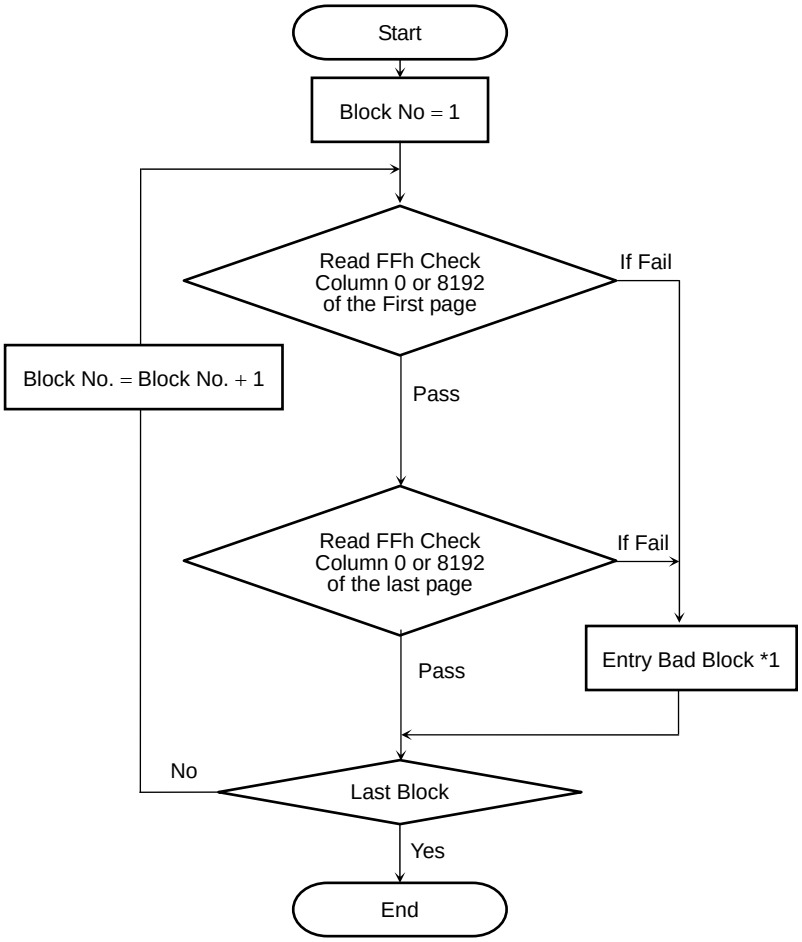
A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	4000	—	4156	Block

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in both the 1st and the last page.



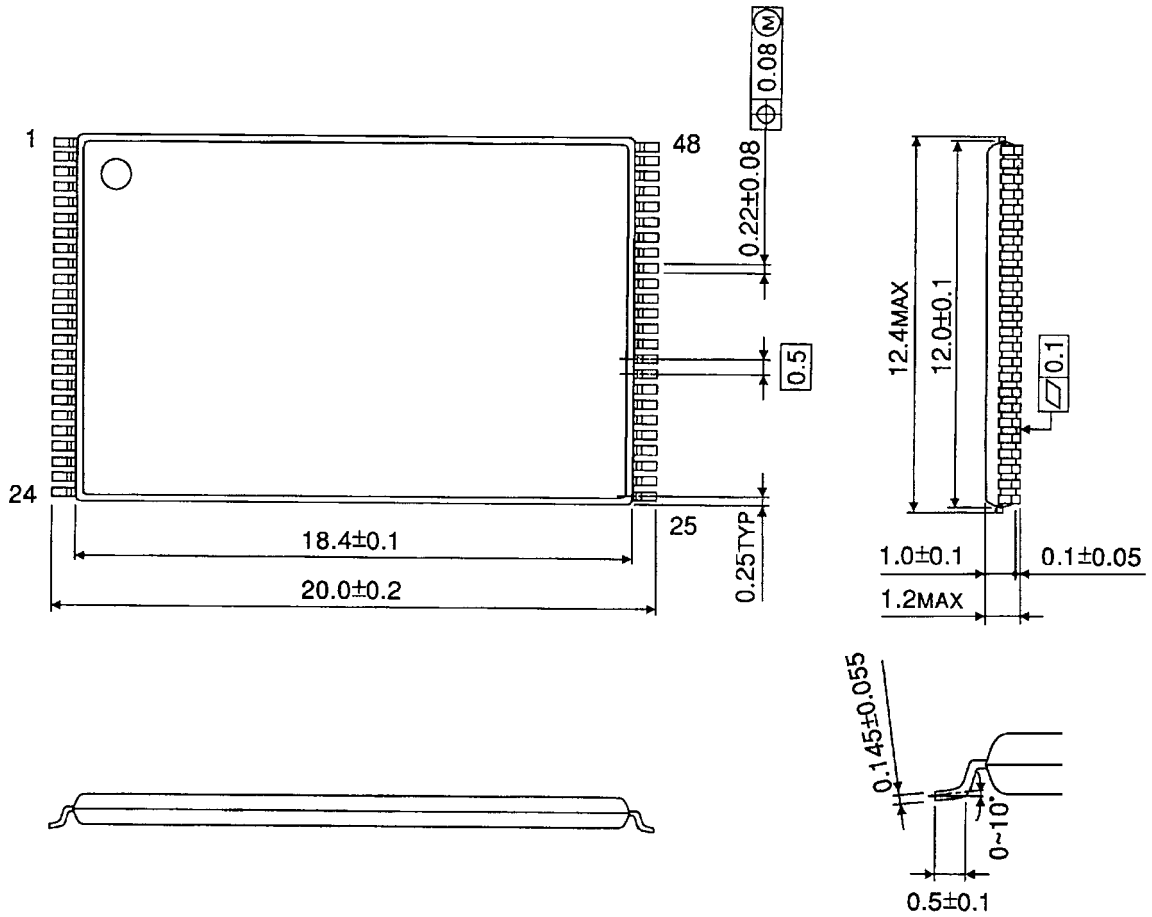
*1:No erase operation is allowed to detected bad blocks.

*2:Bad column detection shoud be operated before detecting bad block information and Bad Columns should be skipped when bad block information is read.

(for example) In case of Column 0 or 8192 is Bad Column, it should be checked the next Column(Column 1 or 8193).

Package Dimensions

TSOP I 48-P-1220-0.50 Unit : mm



Weight: 0.53 g (typ.)

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