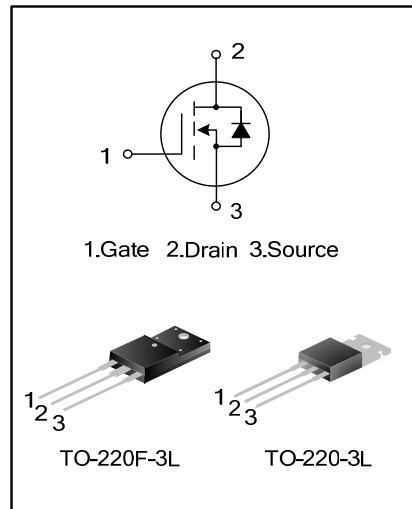


**8A, 600V N-CHANNEL MOSFET**

**GENERAL DESCRIPTION**

SVF8N60T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

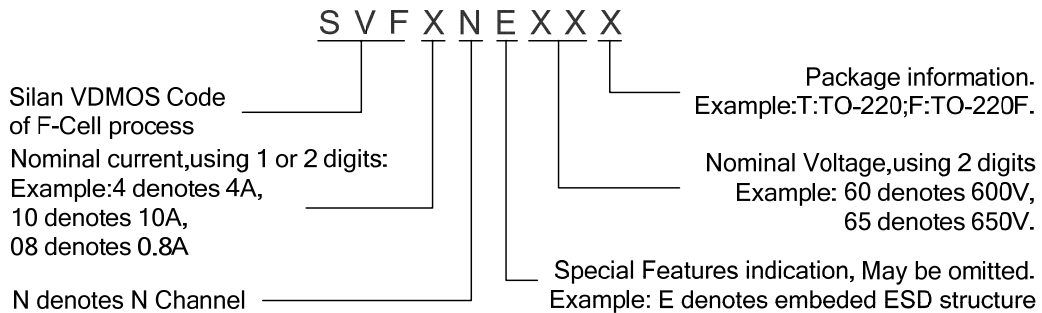
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



**FEATURES**

- \* 8A,600V, $R_{DS(on)(typ.)}=0.96\Omega@V_{GS}=10V$
- \* Low gate charge
- \* Low Crss
- \* Fast switching
- \* Improved dv/dt capability

**NOMENCLATURE**



**ORDERING INFORMATION**

Part No.	Package	Marking	Material	packing
SVF8N60T	TO-220-3L	SVF8N60T	Pb free	Tube
SVF8N60F	TO-220F-3L	SVF8N60F	Pb free	Tube

**ABSOLUTE MAXIMUM RATINGS** ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)

Characteristics	Symbol	Rating		Unit
		SVF8N60T	SVF8N60F	
Drain-Source Voltage	$V_{DS}$	600		V
Gate-Source Voltage	$V_{GS}$	$\pm 30$		V
Drain Current	$I_D$	$T_C=25^{\circ}\text{C}$		A
		$T_C=100^{\circ}\text{C}$		
Drain Current Pulsed	$I_{DM}$	32.0		A
Power Dissipation( $T_C=25^{\circ}\text{C}$ ) -Derate above $25^{\circ}\text{C}$	$P_D$	147	48	W
		1.18	0.38	W/ $^{\circ}\text{C}$
Single Pulsed Avalanche Energy (Note 1)	$E_{AS}$	450		mJ
Operation Junction Temperature Range	$T_J$	$-55 \sim +150$		$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	$-55 \sim +150$		$^{\circ}\text{C}$

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Rating		Unit
		SVF8N60T	SVF8N60F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.85	2.6	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.50	120	$^{\circ}\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS** ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{VDSS}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	600	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=600\text{V}, V_{GS}=0\text{V}$	--	--	1.0	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30\text{V}, V_{DS}=0\text{V}$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=4.0\text{A}$	--	0.96	1.2	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHZ}$	--	910	--	pF
Output Capacitance	$C_{oss}$		--	105	--	
Reverse Transfer Capacitance	$C_{rss}$		--	2.43	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300\text{V}, R_G=25\Omega,$ $I_D=8.0\text{A}$  (Note 2,3)	--	29.00	--	ns
Turn-on Rise Time	$t_r$		--	71.33	--	
Turn-off Delay Time	$t_{d(off)}$		--	34.93	--	
Turn-off Fall Time	$t_f$		--	32.80	--	
Total Gate Charge	$Q_g$	$V_{DS}=480\text{V}, I_D=8.0\text{A},$ $V_{GS}=10\text{V}$  (Note 2,3)	--	14.83	--	nC
Gate-Source Charge	$Q_{gs}$		--	5.90	--	
Gate-Drain Charge	$Q_{gd}$		--	4.00	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	8.0	A
Pulsed Source Current	$I_{SM}$		--	--	32.0	
Diode Forward Voltage	$V_{SD}$	$I_S=8.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_S=8.0A, V_{GS}=0V,$ $di_F/dt=100A/\mu S$	--	520.65	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	3.72	--	$\mu C$

**Notes:**

1.  $L=30mH, I_{AS}=5.0A, V_{DD}=110V, R_G=25\Omega$ , starting  $T_J=25^\circ C$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

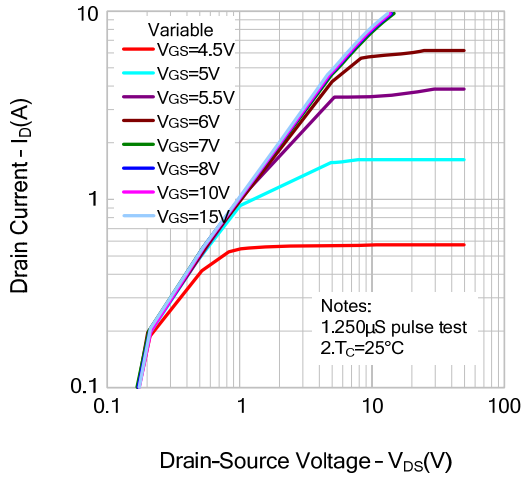


Figure 2. Transfer Characteristics

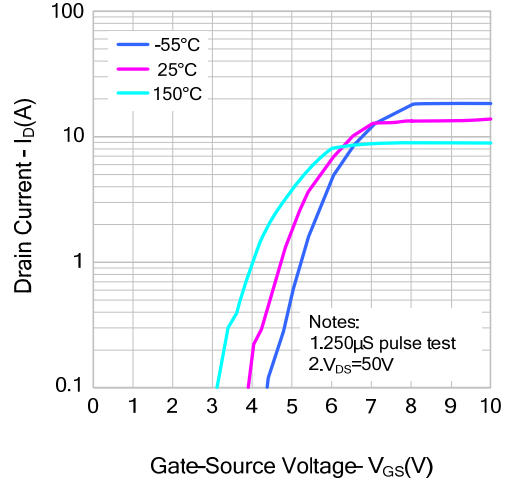


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

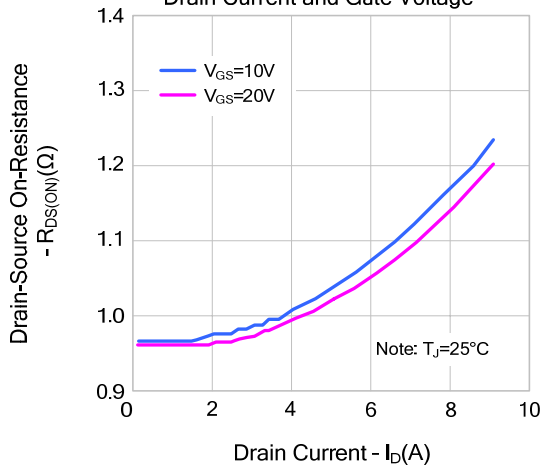


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

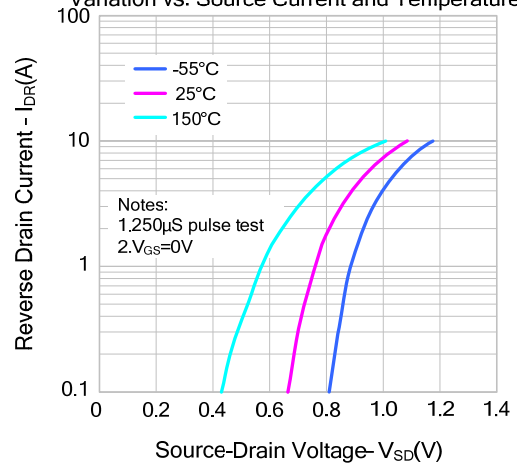


Figure 5. Capacitance Characteristics

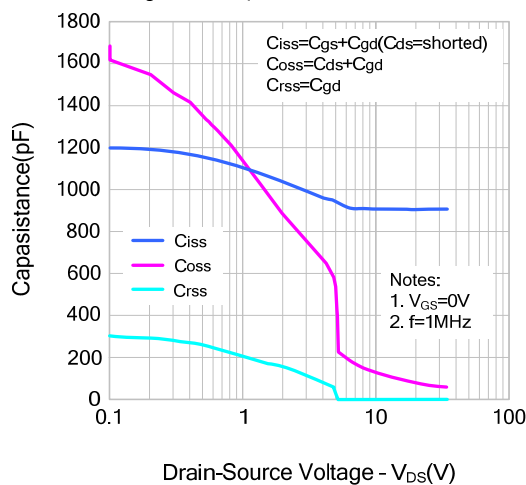
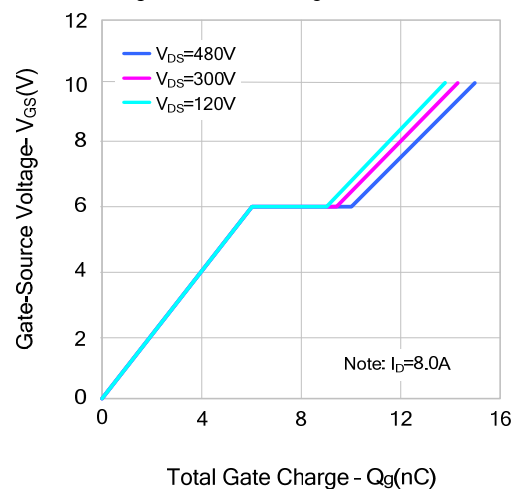


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS(continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

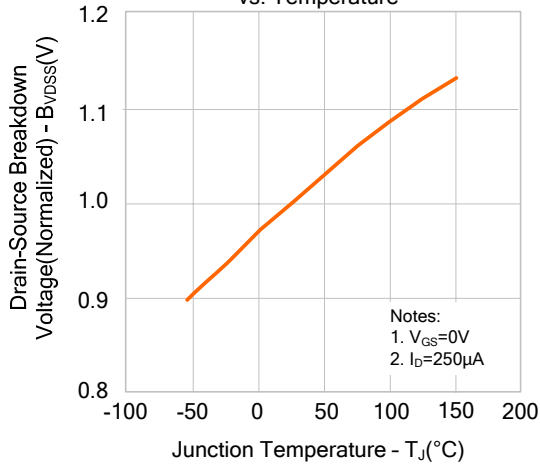


Figure 8. On-resistance Variation vs. Temperature

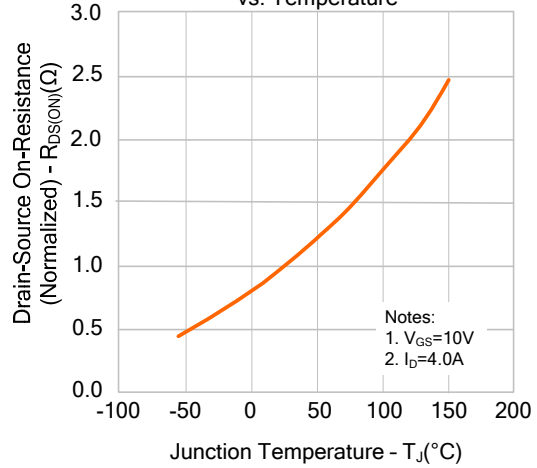


Figure 9-1. Max. Safe Operating Area(SVF8N60T)

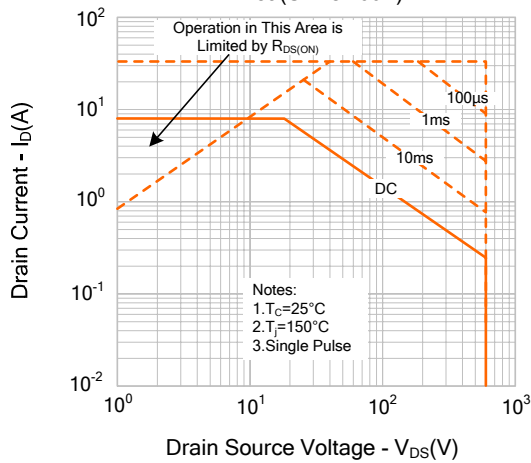


Figure 9-2. Max. Safe Operating Area(SVF8N60F)

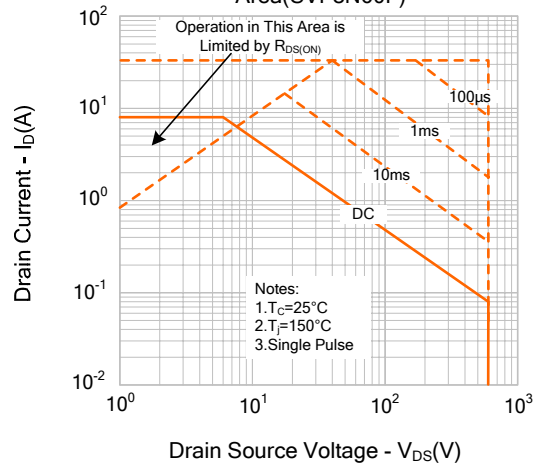
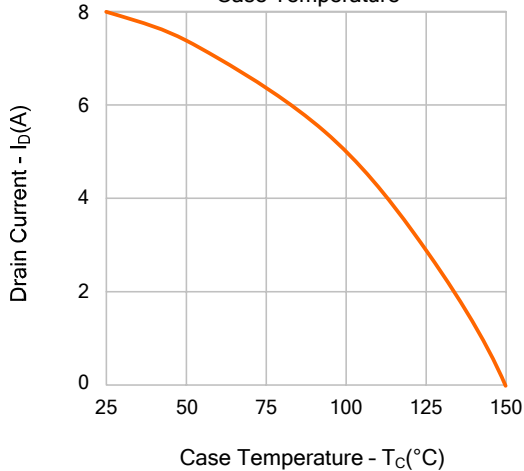
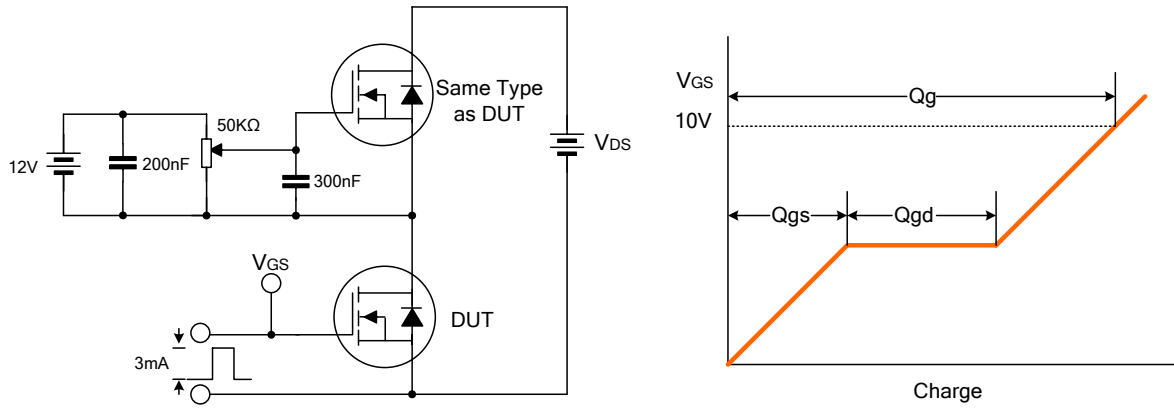


Figure 10. Maximum Drain Current vs. Case Temperature

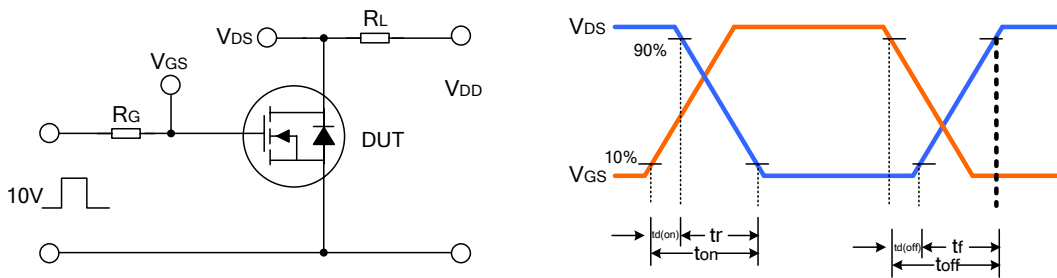


**TYPICAL TEST CIRCUIT**

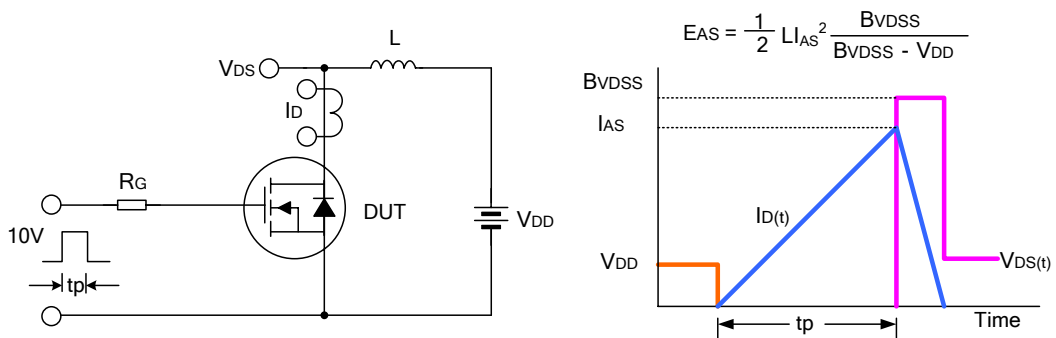
Gate Charge Test Circuit & Waveform



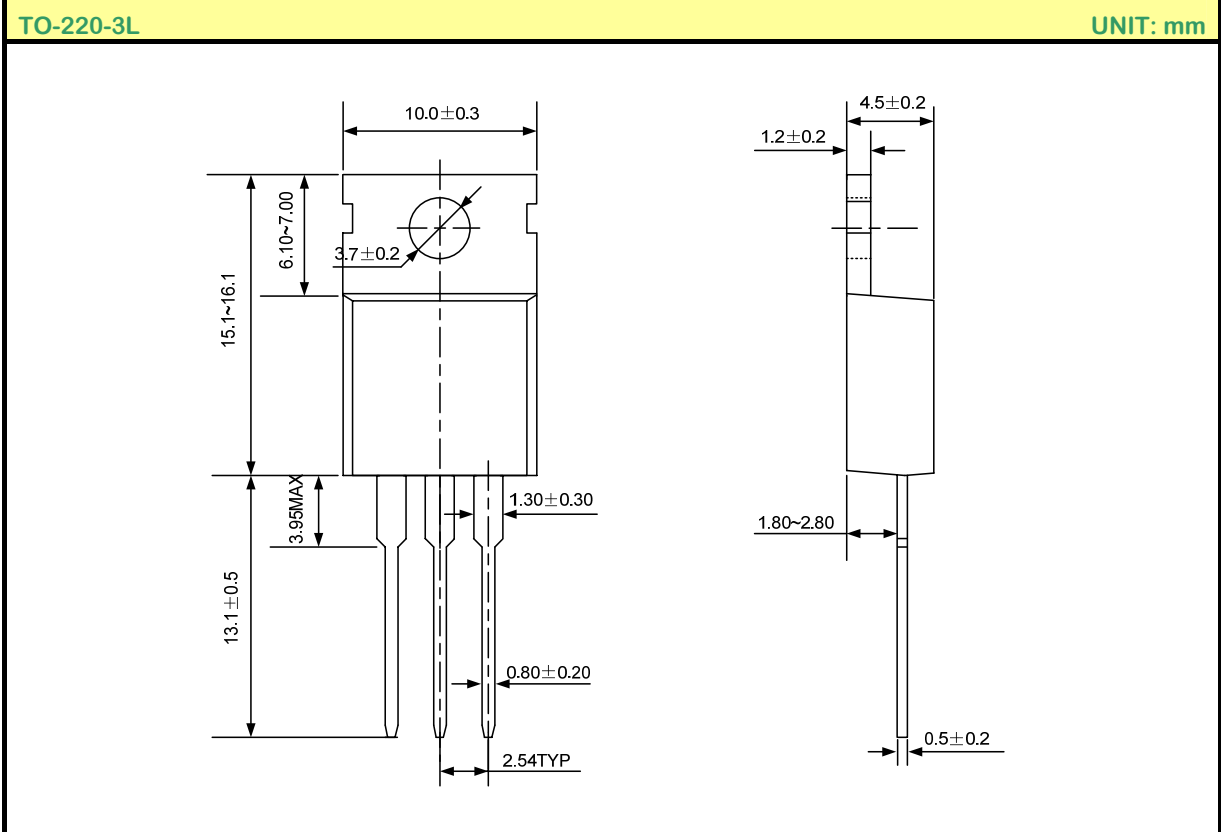
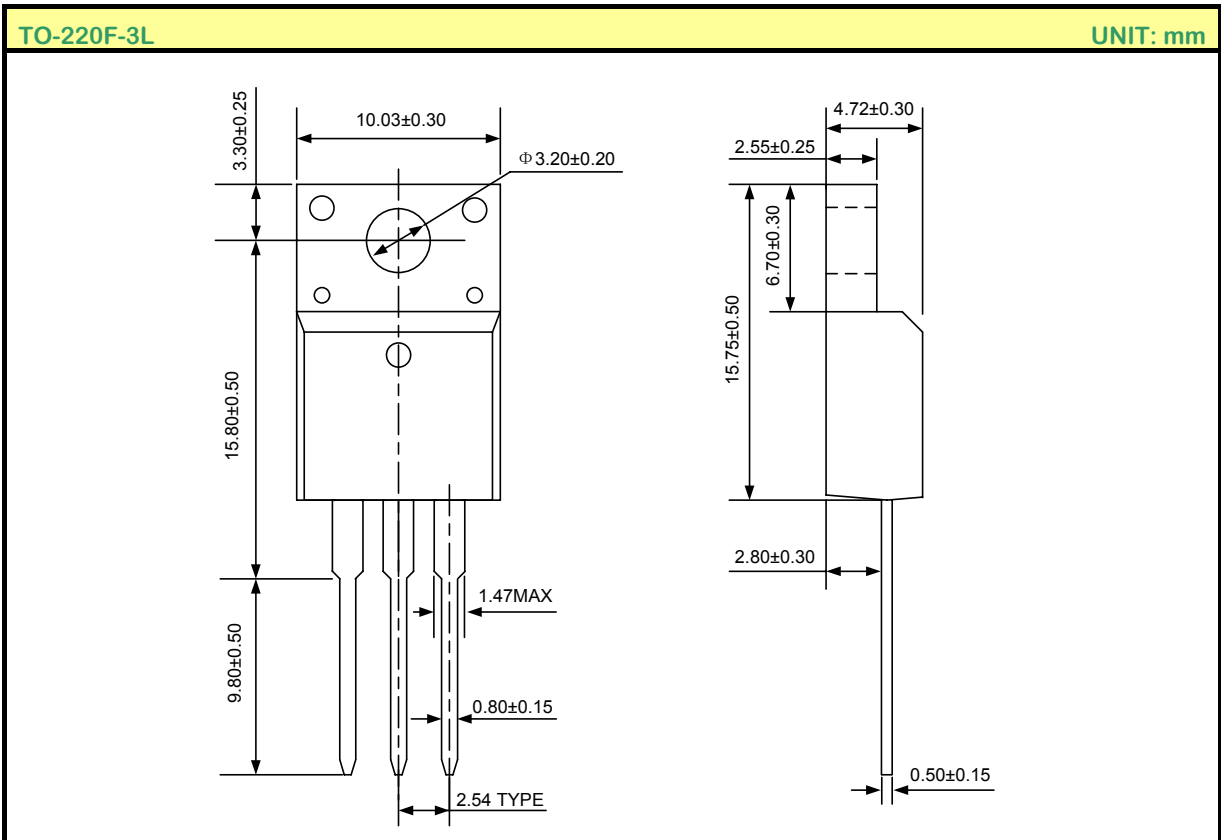
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE





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- Silan will supply the best possible product for customers!

## ATTACHMENT

### Revision History

Date	REV	Description	Page
2011.02.11	1.0	Original	
2011.08.30	1.1	Modify "PACKAGE OUTLINE"	
2012.06.04	1.2	Modify the values of $T_{rr}$ and $Q_{rr}$	
2012.06.15	1.3	Modify the typ. value of $R_{DS(on)}$	