■ GENERAL DESCRIPTION

The MSM70V000 series is the gate array LSI based on the master slice method using the high performance silicon gate 1.5 micron HCMOS process with the dual-layer metal structure.

This series has the features to easily realize functions of the schmitt trigger, crystal/ceramic or CR oscillator, pull-up/pull-down input circuit, and clock driver through the input/output cells, without using any internal gate, which are greatly required by customers.

In addition, the I/O interface is able to convert levels of both CMOS and TTL for all input/output buffers.

Ten types of master chips are prepared according to the combination of the number of gates and the number of pads (the number of pins), which are the MSM70V000, MSM-71V000, MSM72V000, MSM73V000, MSM74V000, MSM79V000, MSM75V000, MSM-76V000, MSM77V000, and MSM78V000.

These series have 700, 1,000, 1,568, 2,000, 2,400, 3,289, 4,290, 6,000, 8,118, and 10,008 2-input gates converted into NAND/NOR ones respectively; and 74, 74, 74, 88, 88, 94, 112, 138, 178 and 188 pads respectively.

It is possible to programmably construct pads for input, output, bi-direction, V_{DD}, and V_{SS} only with metal connection.

The LSI development using the series is fully supported by completed OKI CAD system, from the design through the prototype evaluation.

Since the system fully supports the design using the engineering work station (DAISY, MENTOR, VALID and FutureNet) which has now been popular, OKI is ready to supply floppy disks for the library package.

■ FEATURES

- Short development period
  (Ordinarily 4 weeks after the simulation is completed)
- 1.5 μm silicon gate and dual-layer metal HCMOS
  (Effective gate length: 1.0 microns)
- High speed and low power dissipation
  (Internal basic gate: 1.1 nS/10 μW)
- Full-support with CAD system (including EWS)
- Basic two pairs of PMOS/NMOS cell configurations
- Wide range integration (700 to 10,000 gates)
- Various types of packages
  - 24- to 64-pin DIP
  - 20- to 84-pin PLCC
  - 24- to 160-pin FLAT
  - 72- to 208-pin PGA (including the plastic PGA)
- Various types of functional blocks
  (316 types are already registered)
  - Internal block: 144 types
  - Hardware macro block: 31 types
  - I/O block: 57 types
  - Macro functional block: 84 types
    (TTL MSI equivalent)
- All pins of schmitt input circuit are available.
  (Both CMOS and TTL levels are available.)
- All pins of pull-up or pull-down MOS (100 KΩ) are available.
- The oscillation circuit can be mounted. (Maximum 40 MHz)
- The output buffer circuit can be configurated for the maximum of 18 mA sink current.
- All pins on the pad can be configurated input, output, and bi-directional.
- The internal bus and LSSD circuits can be available.
  LSSD: Level Sensitive Scan Design
- The locations of V_{DD} and V_{SS} pins for power supply can be moved and the number of the pins can be increased easily as an option.

■ MASTER CHIP CONFIGURATION

Item	Symbol	MSM 70V000	MSM 71V000	MSM 72V000	MSM 73V000	MSM 74V000
Number of unit cells (2-input gate)	N_{UC}	700	1000	1568	2000	2400
Total number of pads	N_{PAD}	74	74	74	88	88
Maximum number of I/O pads (input/output/bi-direction) (*1)	$N_{I/O}$	66	66	66	80	80
Number of V_{DD} pads (*1)	N_{VDD}	(*2) 4	(*2) 4	(*2) 4	(*2) 4	(*2) 4
Number of V_{SS} pads (*1)	N_{VSS}	(*2) 4	(*2) 4	(*2) 4	(*2) 4	(*2) 4

Item	Symbol	MSM 79V000	MSM 75V000	MSM 76V000	MSM 77V000	MSM 78V000
Number of unit cells (2-input gate)	N_{UC}	3289	4290	6000	8118	10008
Total number of pads	N_{PAD}	94	112	138	178	188
Maximum number of I/O pads (input/output/bi-direction) (*1)	$N_{I/O}$	86	104	130	166	172
Number of V_{DD} pads (*1)	N_{VDD}	4	4	4	(*2) 4	8
Number of V_{SS} pads (*1)	N_{VSS}	4	4	4	(*2) 8	8

Note: *1 The number of I/O, V_{DD} and V_{SS} pads may be different according to the number of output buffers simultaneous switching and the types of packages used.

Each number of $N_{I/O}$, N_{VDD} and N_{VSS} in the above table shows OKI's recommendable standard specification.

Conditions: $N_{I/O} + N_{VDD} + N_{VSS} \leq N_{PAD}$

*2 In above table, the number of V_{DD} and V_{SS} means fixed pads which are located at four corners of the chip, and they can not be used for any signals.

■ ELECTRICAL CHARACTERISTICS

● Absolute maximum rating

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}	Ta = 25°C V_{SS} = 0 V	-0.5 to +7	V
Input voltage	V_I		-0.5 to V_{DD} +0.5	V
Output voltage	V_O		-0.5 to V_{DD} +0.5	V
Input current	I_I		-10 to +10	mA
Output current	I_O		-20 to +20	mA
Storage temperature	T_{stg}	—	-65 to +150	°C

● Operation range

(V_{SS} = 0 V)

Item	Symbol	Rated value		Unit
Power supply voltage	V_{DD}	3 to 6		V
Operating temperature	T_{OPR}	-40 to +85		°C
On-chip Oscillation frequency	f_{OSC}	"BSCC" block	100 to 500K (*1)	Hz
		"BLCC" block	32K to 10M (*2)	
		"BHCC" block	10M to 20M (*2)	
		"BVCC" block	20M to 40M(*2)	

Note: *1 CR oscillator (using the BSCC block)

*2 Ceramic or crystal resonator

- **Recommended operating conditions**

(V_{SS} = 0 V)

Item	Symbol	Rated value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{DD}	4.5	5.0	5.5	V
Operating temperature	T_{OPR}	-40	+25	+85	°C
"H" level input voltage (*1)	V_{IHA}	2.2	–	V_{DD} +0.3	V
	V_{IHB}	3.5	–	V_{DD} +0.3	
	V_{IHC}	2.4	–	V_{DD} +0.3	
	V_{IHD}	4.0	–	V_{DD} +0.3	
"L" level input voltage (*2)	V_{ILA}	V_{SS} -0.3	–	0.8	V
	V_{ILB}	V_{SS} -0.3	–	1.5	
	V_{ILC}	V_{SS} -0.3	–	0.6	
	V_{ILD}	V_{SS} -0.3	–	1.0	
Output sink current	I_{OL}	–	6	18(*3)	mA
Output load capacity	C_L	–	20	100	pF

Note: *1 The V_{IHA} and V_{ILA} are TTL-level normal input buffers.
The V_{IHB} and V_{ILB} are CMOS-level normal input buffers.
The V_{IHC} and V_{ILC} are TTL-level schmitt input buffers.
The V_{IHD} and V_{ILD} are CMOS-level schmitt input buffers.

*2 The V_{SS} -1.5 V is acceptable for the minimum value of the V_{IL} under the condition of the pulse width $\leq$ 10 ns.

*3 The Max. IOL value can be realized by connecting three output buffers in parallel.

• DC characteristics

(V_{DD} = 5 V ± 10%, V_{SS} = 0 V, Ta = −40 to +85°C)

Item	Symbol	Condition		Specified value			Unit
				Min.	Typ.	Max.	
TTL-level schmitt trigger input threshold	V_{T+}			1.2	1.7	2.3	V
	V_{T-}			0.8	1.3	1.9	
CMOS-level schmitt trigger input threshold	V_{T+}			2.4	3.1	3.8	V
	V_{T-}			1.1	1.8	2.4	
"H" level output voltage	V_{OH}		I_{OH} = −6.0 mA	2.4	4.2	V_{DD}	V
"L" level output voltage	V_{OL}		I_{OL} = 6.0 mA	V_{SS}	0.24	0.5	V
"H" level input current	I_{IH}		V_{IH} = V_{DD}	–	0.01	1.0	μA
		With the pull-down	V_{IH} = V_{DD}	10	40	120	
"L" level input current	I_{IL}		V_{IL} = V_{SS}	−1.0	−0.01	–	μA
		With the pull-up	V_{IL} = V_{SS}	−120	−40	−10	
3-state output leak current (including Open Drain)	I_{OZH}		V_{OH} = V_{DD}	–	0.01	10	μA
	I_{OZL}		V_{OH} = V_{SS}	−10	−0.01	–	
Stand-by current	I_{DDS}	Output open	V_{IH} = V_{DD} V_{IL} = V_{SS}	–	0.1	100	μA

• Input/Output terminal capacity

Item	Symbol	Condition	Rated value			Unit
			Min.	Typ.	Max.	
Input terminal	C_I	V_{DD} = V_I = V_O = V_{SS} f = 1 MHz Ta = 25°C	–	6	–	pF
Output terminal	C_O		–	9	–	pF
Bi-directional terminal	C_{IO}		–	10	–	pF

Note: The terminal capacity represents an average including the pin capacity of package and the pad capacity inside chip.

• AC characteristics

(V_{DD} = 5 V, V_{SS} = 0 V, Ta = 25°C)

Item	Symbol	Functional block name	Condition	Rated value			Unit
				Min.	Typ.	Max.	
Internal-gate delay time	tpd	INV	FO = 3, ℓ = 1 mm ℓ: Metal length	0.7	1.1	1.5	nS
		2ND		0.8	1.3	1.8	
TTL-level input-buffer delay time	tpdi	BFIN	V_{IH} = 3 V, V_{IL} = 0 V FO = 3, ℓ = 3 mm	2.1	3.2	4.3	nS
CMOS-level input-buffer delay time	tpdi	BFIC	V_{IH} = V_{DD}, V_{IL} = 0 V FO = 3, ℓ = 3 mm	1.6	2.5	3.4	nS
Output buffer delay time	tpdo	BN	V_{OH} = V_{OL} = 1.5 V C_L = 20 pF	2.3	3.5	4.7	nS
Output-buffer rise transition time	tr	BN	Output amplitude of 10 to 90% C_L = 20 pF	3.4	5.2	7.0	nS
Output-buffer fall transition time	tf	BN	Output amplitude of 90 to 10% C_L = 20 pF	1.6	2.5	3.4	nS

■ STANDARD NUMBER OF POWER-SUPPLY PINS AND STANDARD PIN LAYOUT FOR EACH PACKAGE

Package		Name of series (number of pad)							Standard number of pins				Standard PINOUT (pin number)		
Type	No. of pins	70V 71V 72V (74)	73V 74V (88)	79V (94)	75V (112)	76V (138)	77V (178)	78V (188)	Max. I/O	V_{DD}	V_{SS}	N.C. (*1)	V_{DD}	V_{SS}	N.C. (*1)
DIP	24	●	●	●					22	1	1		24	12	
	28	●	●	●					25	1	2		28	7 21	
	40	●	●	●	●				37	1	2		40	10 30	
	42	●	●	●	●				39	1	2		42	11 32	
	48	●	●	●	●				45	1	2		48	12 36	
Shrink DIP	42S	●	●	○					39	1	2		42	11 32	
	64S	●	●	●	●	●	●		60	2	2		32 64	16 48	
FLAT	24	●	●						22	1	1		24	12	
	32	●	●						30	1	1		32	16	
	44	●	●	●					40	2	2		17 39	6 28	
	56	●	●	●	●				52	2	2		21 49	7 35	
	60	●	●	●	○				56	2	2		23 53	8 39	
	64	○	●	●					60	2	2		26 58	10 42	
	80	●							66	4	4	6	1 23 42 64	3 21 44 62	2 22 32 41 43 63
			●	●	●	●	●	●	72	4	4		13 32 54 73	12 31 53 72	
	100		●						80	4	4	12	1 29 52 80	3 27 54 78	2 5 14 25 28 31 40 53 56 67 74 79
				●					86	4	4	6	16 40 67 91	15 39 66 90	3 28 50 53 56 79
					●	●	●		92	4	4		16 40 67 91	15 39 66 90	
							●		92	4	4		3 27 54 78	2 28 53 79	
								●	92	4	4		16 40 68 91	15 39 67 90	
	128					○	○	○	120	4	4		(*2)	(*2)	
	136					○	○	○	124	6	6		(*2)	(*2)	
	144						○	○	132	6	6		(*2)	(*2)	
	160						○	○	144	8	8		(*2)	(*2)	

(To be continued)

Note: *1 N.C. ---------- Non Connection

*2 to be determined

Package		Name of series (number of pad)							Standard number of pins				Standard PINOUT (pin number)		
Type	No. of pins	70V 71V 72V (74)	73V 74V (88)	79V (94)	75V (112)	76V (138)	77V (178)	78V (188)	Max. I/O	V_{DD}	V_{SS}	N.C. (*1)	V_{DD}	V_{SS}	N.C. (*1)
PLCC	20	●							18	1	1		1	11	
	28	●	●						26	1	1		1	15	
	44	●	●	●	●				40	2	2		1 23	12 34	
	68	●							64	2	2		27 61	10 44	
			●										1 35	18 52	
				●	●	●			60	4	4		1 19 35 53	18 34 52 68	
							●	●	56	4	8		13 30 47 64	3 6 20 23 37 40 54 57	
	84		●						76	4	4		11 33 53 75	12 32 54 74	
				●	●	●			76	4	4		1 23 43 65	22 42 64 84	
							●	●	72	4	8		16 37 58 79	3 7 24 28 45 49 66 70	
PGA	72					●	●	●	60	4	8		43 51 59 67	7 17 27 37 46 54 62 70	
	88			●	●				80	4	4		7 19 43 74	30 54 64 84	
						●							7 19 31 43	54 64 74 84	
	108			○					86	4	4	14	(*2)	(*2)	(*2)
					○				100						
	132				●				104	4	4	20	21 47 59 81	8 34 69 91	(*3)
						●	●	●	118	6	8		4 17 30 43 56 78	11 24 37 50 62 73 84 95	
	176						●	●	160	8	8		146 150 154 158 162 166 170 174	148 152 156 160 164 168 172 176	
	208							●	172	12	8	16	3 19 35 51 74 88 102 116 175 185 195 205	125 132 137 144 149 156 161 168	7 8 23 24 39 40 55 56 69 83 97 111 129 141 153 165

Note: *3 Total of 7, 9, 13, 16, 20, 22, 25, 26, 33, 35, 42, 46, 48, 52, 89, 96, 98, 107, 116, 125

■ FUNCTIONAL BLOCK (MACRO CELL)

The functional block means the fundamental block required to construct the LSI circuit and the cell pattern for each block is designed and registered. Therefore each detailed AC data is also determined.

The functional block is classified into the two types: the I/O interface block that is used for the interface with the peripherals of chip, and the internal basic block used in the array.

For details, see the logic functional block library data sheet (Doc. No. L70KV and HM70KV).

- **Internal basic block table (144 types)**

Type	No.	Functional block name	Logic function	No. of unit cell	Notes
Inverters	1	INV	Invert gate	1	
	2	INV2	Dual invert gates	1	
NAND gates	3	2ND	2-input NAND gate	1	
	4	3ND	3-input NAND gate	2	
	5	4ND	4-input NAND gate	2	
	6	5ND	5-input NAND gate	4	
	7	6ND	6-input NAND gate	5	
	8	7ND	7-input NAND gate	5	
	9	8ND	8-input NAND gate	6	
	10	2ND2	Dual 2-input NAND gates	2	
NOR gates	11	2NR	2-input NOR gate	1	
	12	3NR	3-input NOR gate	2	
	13	4NR	4-input NOR gate	2	
	14	5NR	5-input NOR gate	4	
	15	6NR	6-input NOR gate	5	
	16	7NR	7-input NOR gate	5	
	17	8NR	8-input NOR gate	6	
	18	2NR2	Dual 2-input NOR gates	2	
AND gates	19	2AD	2-input AND gate	2	
	20	3AD	3-input AND gate	2	
	21	4AD	4-input AND gate	3	
	22	5AD	5-input AND gate	4	
	23	6AD	6-input AND gate	4	

(To be continued)

- **Internal basic block table (144 types)**

Type	No.	Functional block name	Logic function	No. of unit cell	Notes
AND gates	24	7AD	7-input AND gate	5	
	25	8AD	8-input AND gate	5	
	26	2AD2	Dual 2-input AND gates	3	
OR gates	27	2OR	2-input OR gate	2	
	28	3OR	3-input OR gate	2	
	29	4OR	4-input OR gate	3	
	30	5OR	5-input OR gate	4	
	31	6OR	6-input OR gate	4	
	32	7OR	7-input OR gate	5	
	33	8OR	8-input OR gate	5	
	34	2OR2	Dual 2-input OR gates	3	
Exclusive gates	35	EXR	Exclusive OR gate	3	
	36	ENR	Exclusive NOR gate	3	
AND-OR/ NOR gates	37	220	2-input 2-wide AND-OR gate	3	
	38	330	3-input 3-wide AND-OR gate	6	
	39	440	4-input 4-wide AND-OR gate	10	
	40	22AR	2-input 2-wide AND-NOR gate	2	
	41	G101	2-1 input 2 wide AND-NOR gate	2	
	42	G102	2-1-1 input 3 wide AND-NOR gate	2	
	43	G103	3-1 input 2 wide AND-NOR gate	2	
	44	G104	2 input OR into 2-1 input 2 wide AND-NOR gate	2	
	45	G107	2 input 3 wide AND-NOR gate	3	
	46	G108	2 input 4 wide NAD-NOR gate	4	
	47	G109	2 input 6 wide AND-NOR gate	8	
	48	G110	2 input 8 wide AND-NOR gate	11	
	49	G111	3 input 2 wide AND-NOR gate	3	
	50	G114	4 input 2 wide AND-NOR gate	4	
	51	G117	2 input AND and 2 input NOR into 2 input NOR gate	3	
OR-AND/ NAND gates	52	G201	2-1 input 2 wide OR-NAND gate	2	
	53	G202	2-1-1 input 3 wide OR-NAND gate	2	

(To be continued)

- **Internal basic block table (144 types)**

Type	No.	Functional block name	Logic function	No. of unit cell	Notes
OR-AND/ NAND gates	54	G203	3-1 input 2 wide OR-NAND gate	2	
	55	G204	2 input AND into 2-1 input 2 wide OR-NAND gate	2	
	56	G205	2 input 2 wide OR-NAND gate	2	
	57	G207	2 input 3 wide OR-NAND gate	3	
	58	G208	2 input 4 wide OR-NAND gate	4	
	59	G209	2 input 6 wide OR-NAND gate	8	
	60	G210	2 input 8 wide OR-NAND gate	11	
	61	G211	3 input 2 wide OR-NAND gate	3	
	62	G214	4 input 2 wide OR-NAND gate	4	
	63	G217	2 input OR and 2 input NAND into 2 input NAND gate	3	
Internal drivers	64	D1A	Internal through driver -1	2	F0≤35
	65	D2A	Internal through driver -2	3	F0≤60
	66	D3A	Internal through driver -3	9	F0≤80
	67	G301	Internal through driver -4	1	F0≤15
	68	G302	Internal through driver -5	2	F0≤25
	69	G304	Internal through driver -6	3	F0≤45
	70	D1N	Internal invert driver -1	3	F0≤35
	71	D2N	Internal invert driver -2	4	F0≤60
	72	D3N	Internal invert driver -3	7	F0≤80
	73	G402	Internal invert driver -4	1	F0≤20
	74	G403	Internal invert driver -5	2	F0≤30
	75	G404	Internal invert driver -6	2	F0≤35
	76	CB4	Internal through and invert driver	6	F0≤45
	77	D2ND	2-input NAND driver	3	F0≤35
	78	D2AD	2-input AND driver	3	F0≤40
Internal tristate drivers	79	TBD1	Internal through tristate bus driver -1	4	F0≤12
	80	TBD2	Internal through tristate bus driver -2	5	F0≤30
	81	TBD3	Internal through tristate bus driver -3	7	F0≤60
	82	TB01	Internal through tristate bus driver -1 (Low enable)	4	F0≤12

(To be continued)

- **Internal basic block table (144 types)**

Type	No.	Functional block name	Logic function	No. of unit cell	Notes
Internal bus drivers	83	TB11	Internal invert tristate bus driver -1	4	F0≤12
	84	BHD1	Bus hold -1	3	
Latches	85	LTND	S-R NAND latch	3	
	86	LTNR	S-R NOR latch	3	
	87	L101	S-R latch with enable	4	
	88	L102	S-R latch with clear	4	
	89	DLT	D-type latch with reset	4	(1)
	90	DLT1	D-type latch	3	(1)
	91	L203	D-type latch with $\overline{\text{reset}}$	4	(1)
	92	L204	D-type latch	3	(2)
	93	L205	D-type latch with $\overline{\text{reset}}$	4	(2)
D-type flip flops	94	DFF	D-type flip flop	6	(3)
	95	DFR	D-type flip flop with reset	8	(3)
	96	F112	D-type flip flop with reset	7	(3)
	97	F113	D-type flip flop with set	7	(3)
	98	DF	D-type flip flop with set/reset	9	(3)
	99	F114	D-type flip flop with set/reset	8	(3)
	100	F115	D-type flip flop with $\overline{\text{reset}}$	7	(3)
	101	F116	D-type flip flop with $\overline{\text{set}}$	7	(3)
	102	DF1	D-type flip flop with $\overline{\text{set}}$/$\overline{\text{reset}}$	8	(3)
	103	F121	D-type flip flop	6	(4)
	104	F125	D-type flip flop with $\overline{\text{reset}}$	7	(4)
	105	F126	D-type flip flop with $\overline{\text{set}}$	7	(4)
	106	F127	D-type flip flop with $\overline{\text{set}}$/$\overline{\text{reset}}$	8	(4)
J-K flip flops	107	JKFF	J-K flip flop	10	(3)
	108	F211	J-K flip flop	9	(3)
	109	JKFR	J-K flip flop with reset	11	(3)
	110	F212	J-K flip flop with reset	10	(3)
	111	F213	J-K flip flop with set	10	(3)
	112	JKF	J-K flip flop with set/reset	13	(3)
	113	F214	J-K flip flop with set/reset	11	(3)

(To be continued)

- **Internal basic block table (144 types)**

Type	No.	Functional block name	Logic function	No. of unit cell	Notes
J-K flip flops	114	F215	J-K flip flop with $\overline{\text{reset}}$	10	(3)
	115	F216	J-K flip flop with $\overline{\text{set}}$	10	(3)
	116	JKF1	J-K flip flop with $\overline{\text{set}}$/$\overline{\text{reset}}$	11	(3)
	117	F221	J-K flip flop	9	(4)
	118	F225	J-K flip flop with $\overline{\text{reset}}$	10	(4)
	119	F226	J-K flip flop with $\overline{\text{set}}$	10	(4)
	120	F227	J-K flip flop with $\overline{\text{set}}$/$\overline{\text{reset}}$	11	(4)
Toggle flip flops	121	TFR	Toggle flip flop with reset	8	(3)
	122	F312	Toggle flip flop with reset	7	(3)
	123	F313	Toggle flip flop with set	7	(3)
	124	F314	Toggle flip flop with set/reset	8	(3)
	125	TFR1	Toggle flip flop with $\overline{\text{reset}}$	7	(3)
	126	F316	Toggle flip flop with $\overline{\text{set}}$	7	(3)
	127	F317	Toggle flip flop with $\overline{\text{set}}$/$\overline{\text{reset}}$	8	(3)
	128	F325	Toggle flip flop with reset	7	(4)
	129	F326	Toggle flip flop with $\overline{\text{set}}$	7	(4)
	130	F327	Toggle flip flop with $\overline{\text{set}}$/$\overline{\text{reset}}$	8	(4)
	131	TFRE	Toggle flip flop with $\overline{\text{enable}}$/reset	10	(3)
	132	TFE	Toggle flip flop with $\overline{\text{enable}}$/set/reset	12	(3)
	133	F401	Toggle flip flop with enable/set/reset	10	(3)
	134	F402	Toggle flip flop with $\overline{\text{enable}}$/$\overline{\text{set}}$/$\overline{\text{reset}}$	10	(4)
Flip flops with LSSD	135	LDFR	D-type flip flop with reset and LSSD	10	(3)
	136	LDF	D-type flip flop with set/reset and LSSD	11	(3)
	137	LJKR	J-K flip flop with reset and LSSD	13	(3)
	138	LJKF	J-K flip flop with set/reset and LSSD	15	(3)
Fix gates	139	HFX	Fixed high level gate	1	
	140	LFX	Fixed low level gate	1	
	141	G901	Fixed high and low level gate	1	
Delay gates	142	G701	Delay gate (Typical delay: 10 ns)	6	
	143	G702	Delay gate (Typical delay: 20 ns)	11	
	144	G703	Delay gate (Typical delay: 30 ns)	5	

Note: 1. Negative edge latch
2. Positive edge latch
3. Positive edge trigger
4. Negative edge trigger

• Hardware-macro block table (31 types) <HM70KV>

Type	No.	Macro code	Logic function	No. of unit cell	Notes
Selectors	1	2SE	2-line to 1-line data selector	4	¼ 157
	2	2SE4	Quadruple 2-line to 1-line data selectors	11	74158
	3	4SE	4-line to 1-line data selector	8	½ 153
	4	8SE	8-line to 1-line data selector	18	74151
Decoders	5	4DE	2-line to 4-line decoder with enable	9	74139
	6	4DE1	2-line to 4-line decoder	6	
	7	8DE	3-line to 8-line decoder with enable	20	74138
	8	8DE1	3-line to 8-line decoder	15	
Latches/ registers	9	4LT	4-bit data latch	11	
	10	4LT1	4-bit data latch with reset	13	
	11	8LT	8-bit data latch	21	
	12	8LT1	8-bit data latch with reset	25	
	13	4DF	Quadruple D-type flip flops	19	
	14	4DF1	Quadruple D-type flip flops with reset	23	
Counters	15	4CU	Synchronous 4-bit binary counter with synchronous reset	45	74163
	16	4CU1	Synchronous 4-bit binary counter with synchronous reset (without data load)	38	<74163>
	17	4CD	Synchronous 4-bit binary up/down counter with down/up mode control	66	74191
	18	4CD1	Synchronous 4-bit binary up/down counter with down/up mode control and set/reset (without data load)	56	<74191>
	19	4RU	4-bit binary up counter with reset	23	74393
	20	4RD	4-bit binary down counter with set	23	
Shift registers	21	4SR	4-bit shift register with reset	23	
	22	4SR1	4-bit shift register with reset and data load	32	74395
	23	8SR	8-bit shift register with reset	45	74164
	24	8SR1	8-bit shift register with reset and data load	62	
Arithmetic elements	25	1FA	1-bit carry save full adder	7	
	26	2FA	2-bit full adder	15	7482
	27	4FA1	4-bit binary full adder with fast carry	38	74283
	28	4CM1	4-bit equal-to comparator	14	
	29	4CM2	4-bit magnitude comparator (A>B)	22	
	30	8PG	8-bit partiy generator	18	
RAM cells	31	R41	4-bit by 1-word RAM cell	14	

- **I/O interface block table (57 types)**

This functional block realizes the TTL-CMOS level conversion as well as the oscillator, schmitt trigger circuit, and pull-up/pull-down that are greatly demanded by customers.

It is not necessary to add the extra cell in the array.

As much as 57 types of blocks are registered at present.

Purpose	Normal	With pull-up	With pull-down
Input buffer	10 types	10 types	10 types
Output buffer	4 types	–	–
Bi-directional buffer	6 types	6 types	6 types
Oscillation circuit	5 types	–	–

Type	No.	Functional block name	Logic function	No. of buffer cell	Interface level	
Input buffer	1	BFIN	Through input buffer	1	TTL	
	2	BFIC	Through input buffer	1		CMOS
	3	BCK	Through clock input buffer	1	TTL	
	4	BCKN	Invert clock input buffer	1	TTL	
	5	BST	Invert schmitt trigger input buffer	1	TTL	
	6	BSC	Invert schmitt trigger input buffer	1		CMOS
	7	BSTB	Invert schmitt trigger clock input buffer	1	TTL	
	8	BSCB	Invert schmitt trigger clock input buffer	1		CMOS
	9	BSTD	Through schmitt trigger clock input buffer	1	TTL	
	10	BSCD	Through schmitt trigger clock input buffer	1		CMOS
Input buffer with pull-up	11	UFIN	Through input buffer with pull up	1	TTL	
	12	UFIC	Through input buffer with pull up	1		CMOS
	13	UCK	Through clock input buffer with pull up	1	TTL	
	14	UCKN	Invert clock input buffer with pull up	1	TTL	
	15	UST	Invert schmitt trigger input buffer with pull up	1	TTL	
	16	USC	Invert schmitt trigger input buffer with pull up	1		CMOS
	17	USTB	Invert schmitt trigger clock input buffer with pull up	1	TTL	
	18	USCB	Invert schmitt trigger clock input buffer with pull up	1		CMOS
	19	USTD	Through schmitt trigger clock input buffer with pull up	1	TTL	

(To be continued)

- **I/O interface block table (57 types)**

Type	No.	Functional block name	Logic function	No. of buffer cell	Interface level	
Input buffer with pull-up	20	USCD	Through schmitt trigger clock input buffer with pull up	1		CMOS
Input buffer with pull-down	21	DFIN	Through input buffer with pull down	1	TTL	
	22	DFIC	Through input buffer with pull down	1		CMOS
	23	DCK	Through clock input buffer with pull down	1	TTL	
	24	DCKN	Invert clock input buffer with pull down	1	TTL	
	25	DST	Invert schmitt trigger input buffer with pull down	1	TTL	
	26	DSC	Invert schmitt trigger input buffer with pull down	1		CMOS
	27	DSTB	Invert schmitt trigger clock input buffer with pull down	1	TTL	
	28	DSCB	Invert schmitt trigger clock input buffer with pull down	1		CMOS
	29	DSTD	Through schmitt trigger clock input buffer with pull down	1	TTL	
	30	DSCD	Through schmitt trigger clock input buffer with pull down	1		CMOS
Oscillator circuit	31	BSTC	Invert schmitt trigger input buffer with schmitt output	2	TTL	
	32	BSCC	Invert schmitt trigger input buffer with schmitt output	2		CMOS
	33	BLCC	Invert input buffer with oscillator output	2		CMOS
	34	BHCC	Invert input buffer with oscillator output	2		CMOS
	35	BVCC	Invert input buffer with oscillator output	2		CMOS
Output buffer	36	BN	Through push pull output buffer	1	TTL	CMOS
	37	BODN	Through open drain output buffer	1	TTL	CMOS
	38	BODP	Through current force output buffer	1	TTL	CMOS
	39	BT	Through 3-state output buffer	1	TTL	CMOS
Bi-directional buffer	40	BC	Through common I/O buffer (BFIN and BT)	1	TTL	
	41	BCIC	Through common I/O buffer (BFIC and BT)	1		CMOS
	42	BCST	Through output and invert schmitt trigger input common I/O buffer (BSTB and BT)	1	TTL	

(To be continued)

- **I/O interface block table (57 types)**

Type	No.	Functional block name	Logic function	No. of buffer cell	Interface level	
Bi-directional buffer	43	BCSC	Through output and invert schmitt trigger input common I/O buffer (BSCB and BT)	1		CMOS
	44	BCSD	Through common I/O buffer with schmitt input (BSTD and BT)	1	TTL	
	45	BCSE	Through common I/O buffer with schmitt input (BSCD and BT)	1		CMOS
Bi-directional buffer with pull-up	46	UBC	Through common I/O buffer with pull up (UFIN and BT)	1	TTL	
	47	UCIC	Through common I/O buffer with pull up (UFIC and BT)	1		CMOS
	48	UCST	Through output and invert schmitt trigger input with pull up common I/O buffer (USTB and BT)	1	TTL	
	49	UCSC	Through output and invert schmitt trigger input with pull up common I/O buffer (USCB and BT)	1		CMOS
	50	UCSD	Through common I/O buffer with schmitt input and pull up (USTD and BT)	1	TTL	
	51	UCSE	Through common I/O buffer with schmitt input and pull up (USCD and BT)	1		CMOS
Bi-directional with pull-down	52	DBC	Through common I/O buffer with pull down (DFIN and BT)	1	TTL	
	53	DCIC	Through common I/O buffer with pull down (DFIC and BT)	1		CMOS
	54	DCST	Through output and invert schmitt trigger input with pull down common I/O buffer (DSTB and BT)	1	TTL	
	55	DCSC	Through output and invert schmitt trigger input with pull down common I/O buffer (DSCB and BT)	1		CMOS
	56	DCSD	Through common I/O buffer with schmitt input and pull down (DSTD and BT)	1	TTL	
	57	DCSE	Through common I/O buffer with schmitt input pull down (DSCD and BT)	1		CMOS

(To be continued)

■ SOFT MACRO BLOCK (MACRO FUNCTION)

The circuit equivalent to the TTL 74/74LS MSI (10 to 150 gates) is called the soft macro, which is previously designed and registered using the functional block. At the present time eight-four types of the circuits are prepared which are frequently used.

- Decoder: 12
- Comparator: 4
- Selector/Multiplexer: 7
- Latch: 12
- Counter: 20
- ALU/Carry: 12
- Shift register: 16

The soft macro especially designed for users in addition to the ones listed below can be easily prepared.

For details, see the data sheet (Doc. No. MS70K).

- Soft macro block table (84 types)

No.	Marcro code	Logic function	Equivalent TTL code	No. of unit cells (gate)	Note
1	<0042>	BCD-TO-DECIMAL DECODER	7442	24	
2	<0085>	4-BIT MAGNITUDE COMPARATOR	7485	64	
3	<0091>	8-BIT SHIFT REGISTER	7491	52	*
4	<0092>	DIVIDE-BY-TWELVE COUNTER	7492	42	
5	<0093>	4-BIT BINARY COUNTER	7493	35	
6	<0094>	4-BIT SHIFT REGISTER	7494	52	*
7	<0095>	4-BIT SHIFT REGISTER	7495	41	*
8	<0138>	3-LINE TO 8-LINE DECODER/ DEMULTIPLEXER	74138	22	
9	<0139>	2-LINE TO 4-LINE DECODER/ DEMULTIPLEXER	1/2 74139	11	
10	<0148>	8-LINE TO 3-LINE PRIORITY ENCODER	74148	28	
11	<0151>	8-LINE TO 1-LINE DATA SELECTOR/ MULTIPLEXER	74151	26	
12	<0152>	8-LINE TO 1-LINE DATA SELECTOR/ MULTIPLEXER	74152	24	
13	<0153>	DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS	74153	23	
14	<0155>	DUAL 2-LINE TO 4-LINE DECODERS/ DEMULTIPLEXERS	74155	21	

(To be continued)

No.	Macro code	Logic function	Equivalent TTL code	No. of unit cells (gate)	Remarks
15	<0157>	QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS	74157	15	
16	<0158>	QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS	74158	17	
17	<0160>	SYNCHRONOUS 4-BIT BCD COUNTER WITH ASYNCHRONOUS CLEAR	74160	73	*
18	<0161>	SYNCHRONOUS 4-BIT BINARY COUNTER WITH ASYNCHRONOUS CLEAR	74161	71	*
19	<0162>	SYNCHRONOUS 4-BIT BCD COUNTER WITH SYNCHRONOUS CLEAR	74162	67	*
20	<0163>	SYNCHRONOUS 4-BIT BINARY COUNTER WITH SYNCHRONOUS CLEAR	74163	65	*
21	<0164>	8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER	74164	73	
22	<0165>	PARALLEL LOAD 8-BIT SHIFT REGISTER	74165	95	*
23	<0166>	8-BIT SHIFT REGISTER	74166	92	*
24	<0169>	SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER	74169	81	*
25	<0175>	QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR	74175	35	
26	<0181>	ARITHMETIC LOGIC UNIT/ FUNCTION	74181	109	
27	<0182>	LOOK-AHEAD CARRY GENERATOR	74182	33	
28	<0190>	SYNCHRONOUS 4-BIT BCD UP/DOWN COUNTER WITH DOWN/UP MODE CONTROL	74190	98	*
29	<0191>	SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER WITH DOWN/UP MODE CONTROL	74191	93	*
30	<0192>	SYNCHRONOUS 4-BIT BCD UP/DOWN DUAL CLOCK COUNTER WITH CLEAR	74192	97	*
31	<0193>	SYNCHRONOUS 4-BIT BINARY UP/DOWN DUAL CLOCK COUNTER WITH CLEAR	74193	93	*
32	<0194>	4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER	74194	78	*

(To be continued)

No.	Macro code	Logic function	Equivalent TTL code	No. of unit cells (gate)	Note
33	<0195>	4-BIT PARALLEL-ACCESS SHIFT REGISTER	74195	52	*
34	<0259>	8-BIT ADDRESSABLE LATCHES	74259	71	
35	<0280>	9-BIT ODD/EVEN PARITY GENERATOR/CHECKER	74280	25	
36	<0283>	4-BIT BINARY FULL ADDER WITH FAST CARRY	74283	54	
37	<0298>	QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE	74298	38	*
38	<0393>	4-BIT BINARY COUNTER	1/2 74393	33	
39	<0043>	EXCESS-3 TO DECIMAL DECODER	7443	24	
40	<0044>	EXCESS-3 GRAY TO DECIMAL DECODER	7444	24	
41	<0100>	4-BIT LATCHES	1/2 74100	16	
42	<0131>	3-LINE TO 8-LINE DECODER WITH ADDRESS LATCHES	74131	37	
43	<0147>	10-LINE TO 4-LINE PRIORITY ENCODER	74147	29	
44	<0150>	16-LINE TO 1-LINE DATA SELECTOR/ MULTIPLEXER	74150	81	*
45	<0154>	4-LINE TO 16-LINE DECODER/ DEMULTIPLEXER	74154	71	
46	<0168>	SYNCHERONOUS DECADE UP/DOWN COUNTER	74168	88	
47	<0170>	4 BY 4 REGISTER FILES	(74170)	123	
48	<0179>	4-BIT PARALLEL ACCESS SHIFT REGISTER	74179	59	*
49	<0180>	9-BIT ODD/EVEN PARITY GENE-RATORS/CHECKERS	74180	30	
50	<0183>	CARRY SAVE FULL ADDER	1/2 74183	18	*
51	<0196>	PRESETTABLE DECADE COUNTER/ LATCH	74196	71	*
52	<0197>	PRESETTABLE 4-BIT BINARY COUNTER/LATCH	74197	68	*
53	<0198>	8-BIT SHIFT REGISTER	74198	119	*
54	<0199>	8-BIT SHIFT REGISTER	74199	95	*
55	<0244>	QUADRUPLE INTERNAL 3-STATE BUS BUFFER	1/2 74244	21	

(To be continued)

No.	Macro code	Logic function	Equivalent TTL code	No. of unit cells (gate)	Note
56	<0278>	4-BIT CASCADABLE PRINORITY REGISTERS	74278	35	
57	<0350>	4-BIT SHIFTER (WITHOUT 3-STATE)	(74350)	42	
58	<0381>	ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR	74381	147	
59	<0390>	DECADE COUNTER	1/2 74390	39	*
60	<0541>	OCTAL INTERNAL 3-STATE BUS BUFFER	74541	43	
61	<0049>	BCD TO 7 SEGMENT DECODER	(7449)	52	
62	<0082>	2-BIT FULL ADDER	7482	26	
63	<0096>	5-BIT SHIFT REGISTER	7496	58	*
64	<0137>	3-LINE TO 8–LINE DECODER WITH ADDRESS LATCHES	74137	36	
65	<0167>	BCD SYNCHRONOUS RATE MULTIPLIER	74167	68	
66	<0173>	4-BIT REGISTER (WITHOUT 3-STATE)	(74173)	46	*
67	<0178>	4-BIT SHIFT REGISTER	74178	51	*
68	<0261>	2 BY 4 PARALLEL BINARY MULTIPLIER	74261	71	
69	<0295>	4 BIT SHIFT REGISTER (WITHOUT 3-STATE)	(74295)	38	*
70	<0373>	OCTAL D-TYPE LATCHES (WITHOUT 3-STATE)	(74373)	34	
71	<0374>	OCTAL D-TYPE FLIP-FLOPS (WITHOUT 3-STATE)	(74374)	48	*
72	<0377>	OCTAL D-TYPE FLIP-FLOPS WITH ENABLE	74377	54	*
73	<0379>	QUADRUPLE D-TYPE FLIP-FLOPS WITH ENABLE	74379	30	
74	<0395>	4-BIT SHIFT REGISTER (WITHOUT 3-STATE)	(74395)	46	*
75	<0396>	4 BY 2 STORAGE REGISTER	74396	56	
76	<0518>	8-BIT EQUAL-TO COMPARATOR	(74518)	31	*
77	<A175>	QUADRUPLE D-TYPE FLIP-FLOPS (WITHOUT CLEAR)	(74175)	24	

(To be continued)

No.	Macro code	Logic function	Equivalent TTL code	No. of unit cells (gate)	Note
78	<A374>	OCTAL D-TYPE FLIP-FLOPS (WITH CLEAR / WITHOUT 3-STATE)	(74374)	64	*
79	<A160>	SYNCHRONOUS 4-BIT BCT COUNTER WITH ASYNCHRONOUS CLEAR (WITHOUT DATA LOAD)	(74160)	54	*
80	<A161>	SYNCHRONOUS 4-BIT BINARY COUNTER WITH ASYNCHRONOUS CLEAR (WITHOUT DATA LOAD)	(74161)	54	*
81	<A162>	SYNCHRONOUS 4-BIT BCD COUNTER WITH SYNCHRONOUS CLEAR (WITHOUT DATA LOAD)	(74162)	50	*
82	<A163>	SYNCHRONOUS 4-BIT BINARY COUNTER WITH SYNCHRONOUS CLEAR (WITHOUT DATA LOAD)	(74163)	50	*
83	<A373>	OCTAL D-TYPE LATCHES WITH 3-STATE	74373	77	
84	<B374>	OCTAL D-TYPE FLIP-FLOPS WITH 3-STATE	74374	91	

Note: * These are so designed to be easy for use than standard 74L and 74LS TTL by expanding their output.

The logic function of standard TTL's filling in ( ) is a little bit different from that of macro blocks.