



Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications

() Final Specifications

Module	13.3" WXGA Color TFT-LCD
Model Name	B133EW06 V0

Customer	Date
_____	_____
Checked & Approved by	Date
_____	_____
<p>Note: This Specification is subject to change without notice.</p>	

Approved by	Date
<u>Kendra Wang</u>	<u>7/1/2008</u>
Prepared by	Date
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<p>NBBU Marketing Division / AU Optronics corporation</p>	



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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/03/19	All	First Edition for Customer		
0.2 2008/06/16	18,19	Signal Description/Pin Assignment		
	21	Power ON/OFF Sequence		
	25	Drawing update		
	29~32	EDID description		
0.1 2008/07/01	21	Power ON/OFF Sequence		



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lamp Reflector edge. Instead, press at the far ends of the LED lamp Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) The LCD module is designed so that the LED in it is supplied by Limited Current Circuit (IEC60950 or UL1950). Do not connect the LED in Hazardous Voltage Circuit.



Product Specification

AU OPTRONICS CORPORATION

2. General Description

B133EW06 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver) without backlight inverter. All input signals are LVDS interface compatible.

B133EW06 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

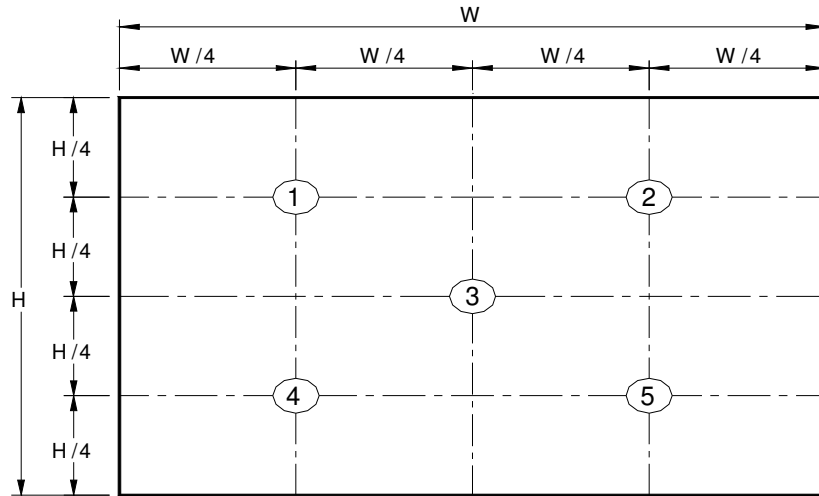
Items	Unit	Specifications			
Screen Diagonal	[mm]	337.8 (13.3W")			
Active Area	[mm]	286.08 (H) X 178.8 (V)			
Pixels H x V		1280x3(RGB) x 800			
Pixel Pitch	[mm]	0.2235 x 0.2235			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED=19mA) Note: ILED is lamp current	[cd/m ²]	200 typ.(5 points average) 170 min.(5 points average) (Note1)			
Luminance Uniformity		1.25 max. (5 points) 1.60 max. (13 points)			
Contrast Ratio		600 typ			
Response Time	[ms]	16 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.0 typ.,4.25 max.(Mosaic Pattern)			
Weight	[Grams]	290 max.			
Physical Size	[mm]		L	W	T
		Max	296.5	203.5	3.5
		Typical	296.0	203.0	-
		Min			-
Electrical Interface		one channel LVDS			
Surface Treatment		Glare, Hardness 3H,			
Support Color		262K colors (RGB 6-bit)			
Temperature Range Operating Storage (Non-Operating)	[°C]	0 to +50			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

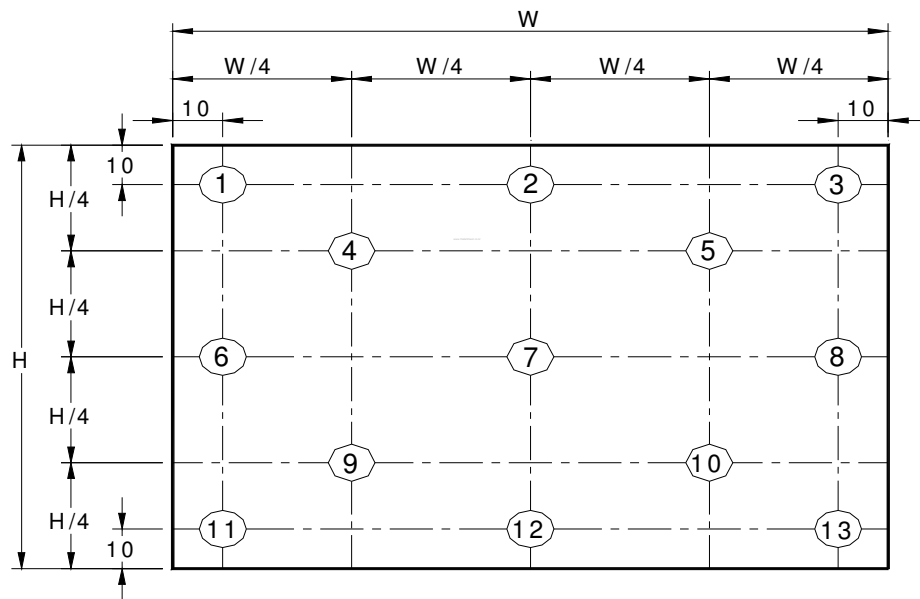
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I _{LED} =19mA	[cd/m ²]	5 points average	170	200	-	1, 4, 5.
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	30 30	40 40	- -	8
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	10 20	15 25	- -	
Luminance Uniformity		5 Points	-	-	1.25	1
Luminance Uniformity		13 Points	-	-	1.6	2
CR: Contrast Ratio			400	600	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	4	8	8
	[msec]	Falling	-	12	17	
	[msec]	Rising + Falling	-	16	25	
Chromaticity of color Coordinates (CIE 1931)		Red x		TBD		2,8
		Red y		TBD		
		Green x		TBD		
		Green y		TBD		
		Blue x		TBD		
		Blue y		TBD		
		White x	0.283	0.313	0.343	
	White y	0.299	0.329	0.359		
NTSC	%	CIE 1931	-	45	-	

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



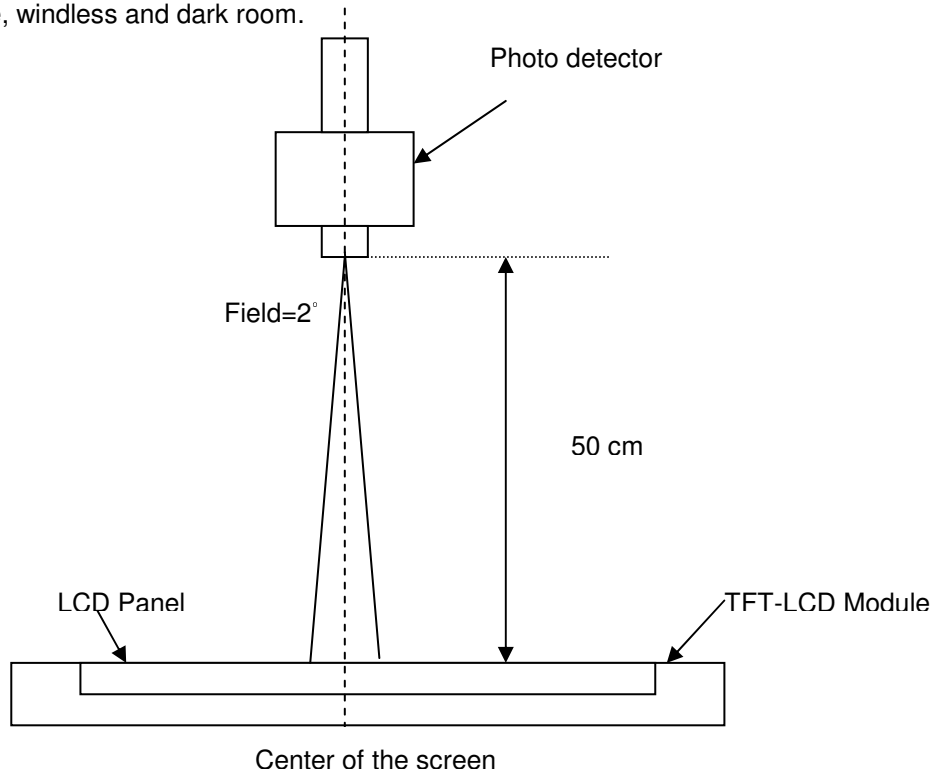
Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points , $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

$L (x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

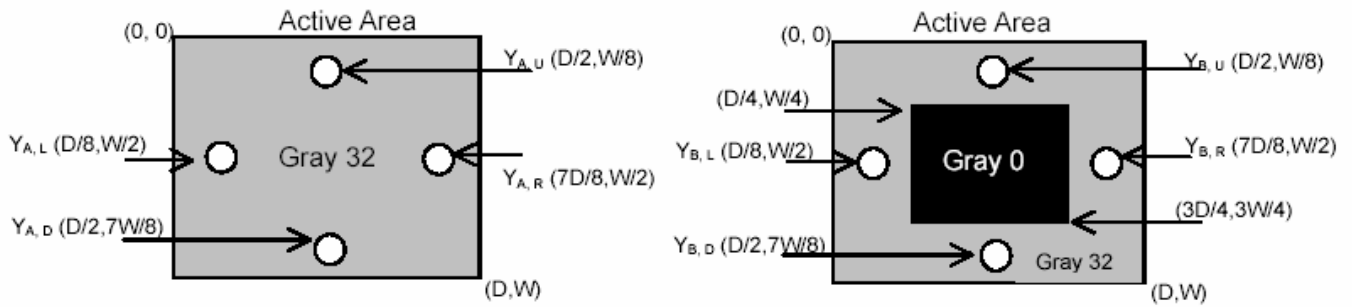
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

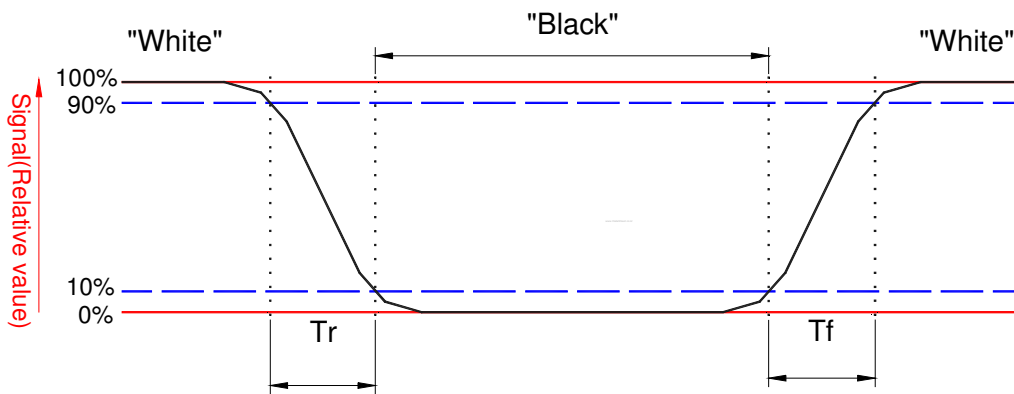
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



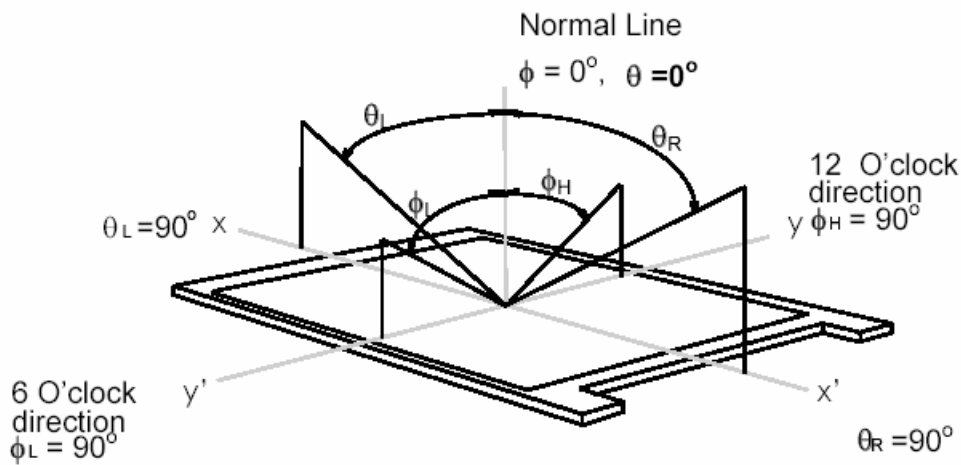
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



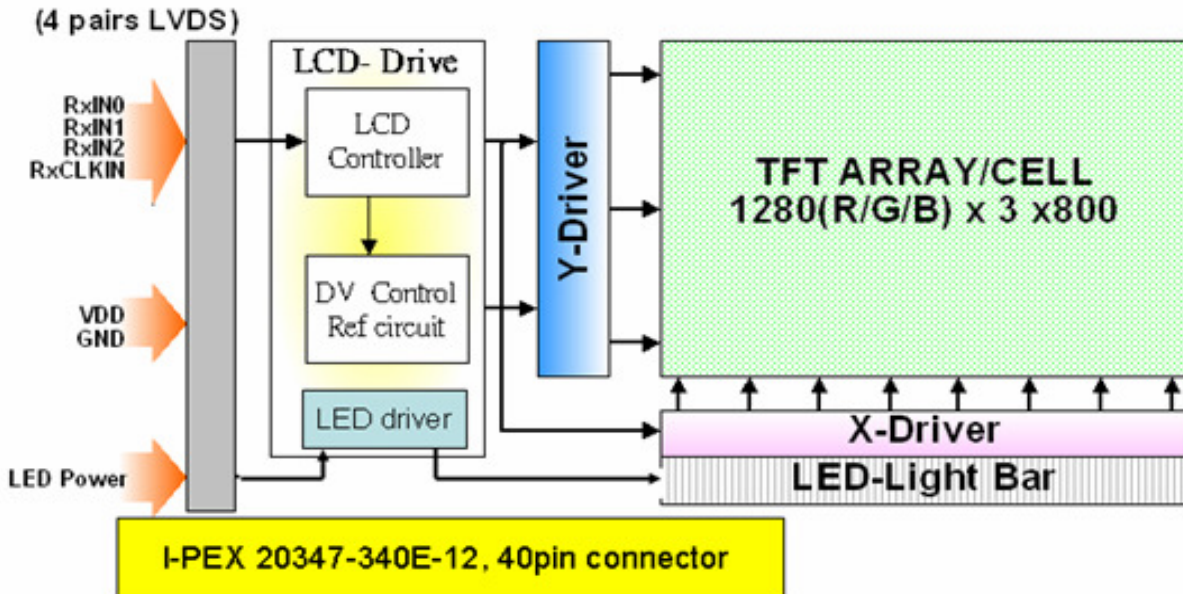
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 13.3 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
LED Current	ILED	-	35	[mA] rms	Note 1,2

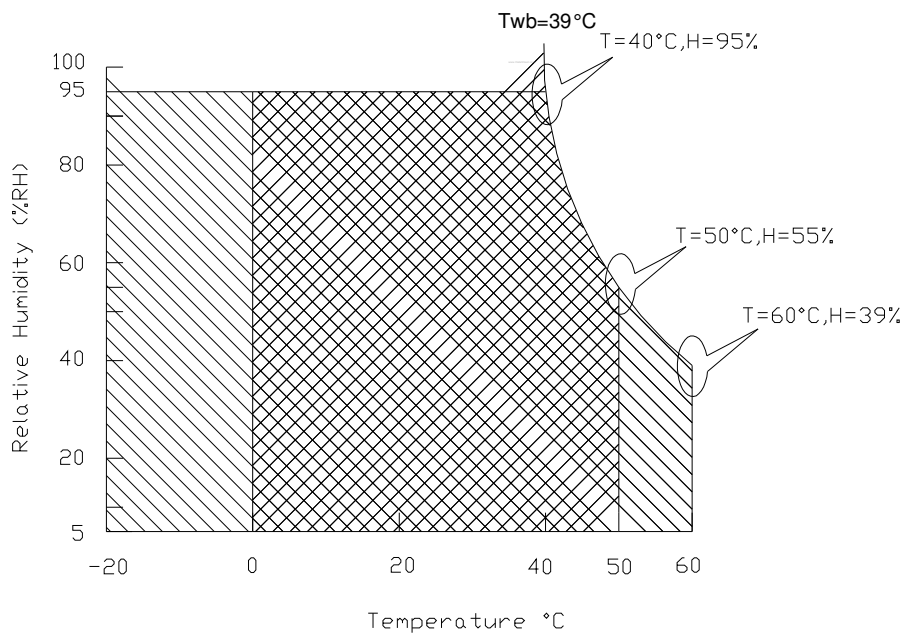
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25°C)

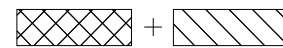
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range



5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

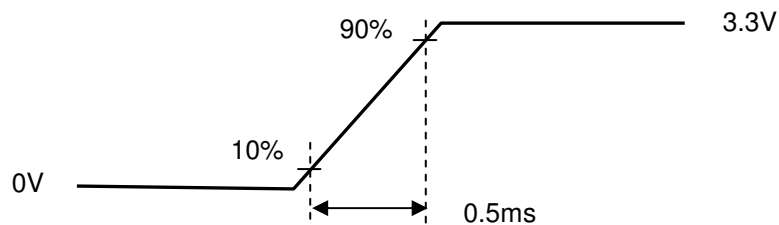
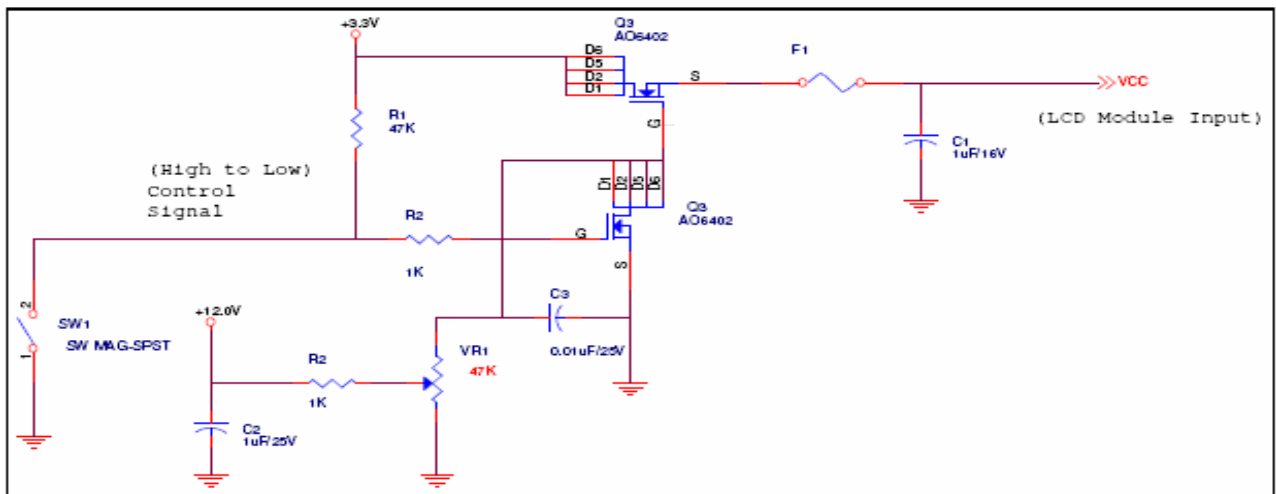
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	0.70	0.75	[Watt]	Note 1/2
IDD	IDD Current	-	215	250	[mA]	Note 1/2
IRush	Inrush Current	-	0.7	1.5	[A]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Mosaic Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

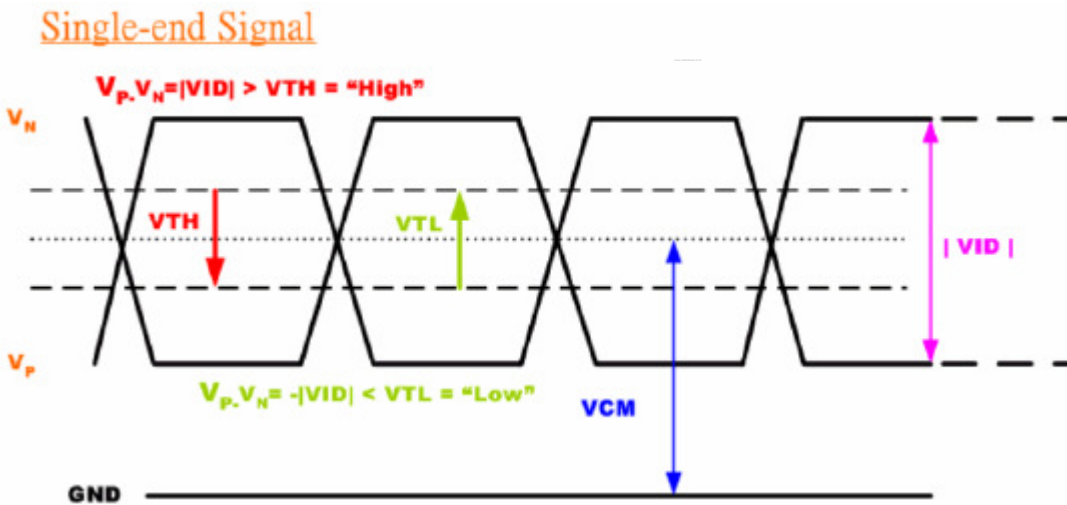
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	+100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	0.8	2.0	[V]

Note: LVDS Signal Waveform

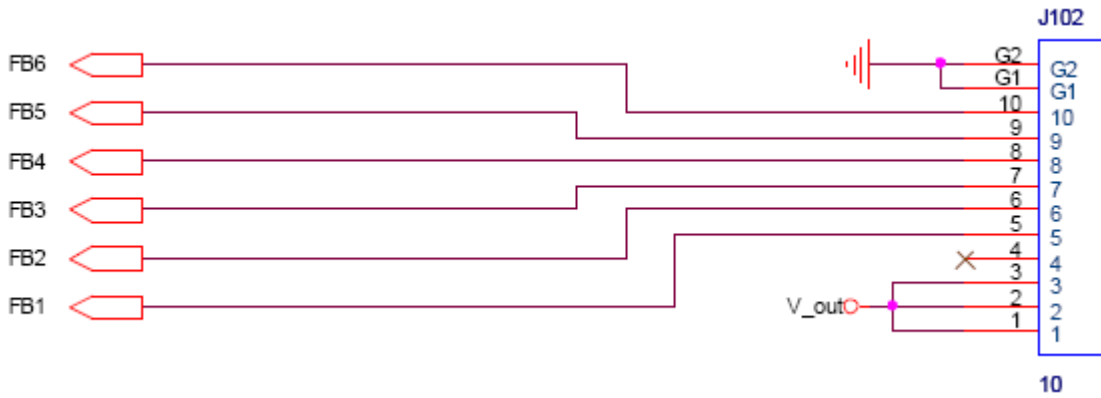


5.2 Backlight Unit

Parameter guideline for LED

Parameter	Min	Typ	Max	Units	Units
White Luminance 5 points average	170	200	-	[cd/m ²]	Ta=25 °C
LED current (ILED)	-	18	-	[mA]	Ta=25 °C
LED Power consumption	-	3.3	3.5	[Watt]	Ta=25 °C

Light bar PIN assignment:

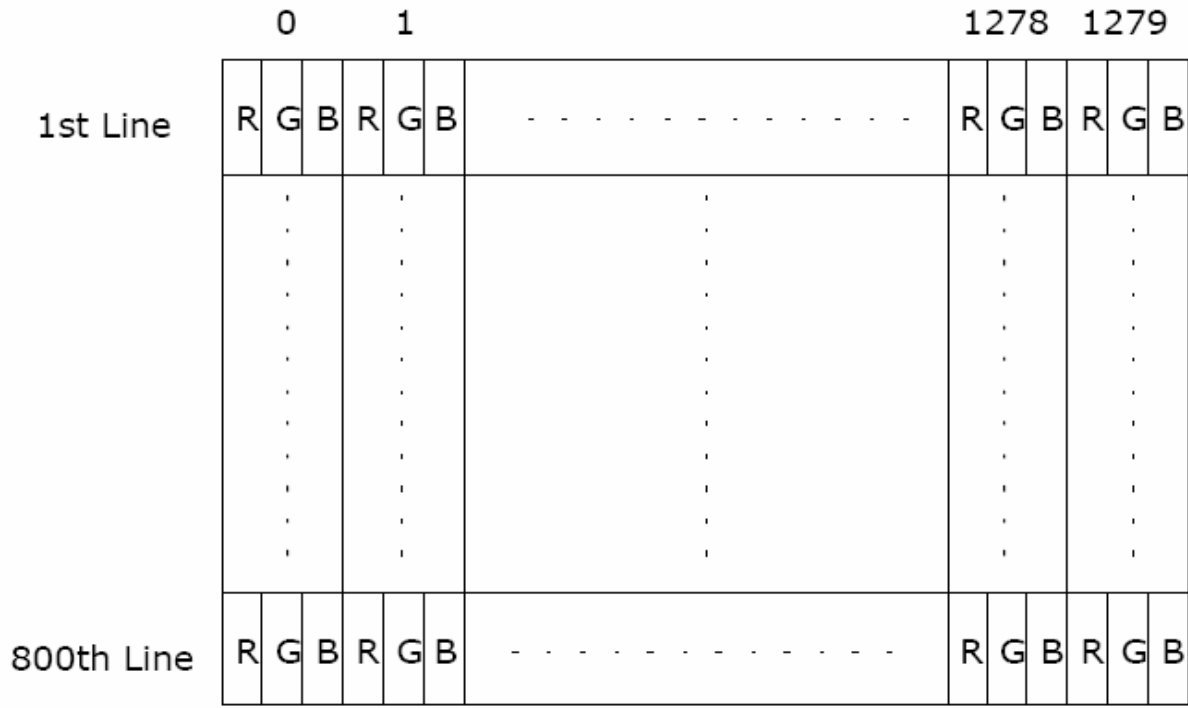


PIN NO.	Pin assignment	Function
1	VOUT	LED Anode (Positive)
2	VOUT	LED Anode (Positive)
3	VOUT	LED Anode (Positive)
4	NC	NC
5	FB1	LED Cathode (Negative)
6	FB2	LED Cathode (Negative)
7	FB3	LED Cathode (Negative)
8	FB4	LED Cathode (Negative)
9	FB5	LED Cathode (Negative)
10	FB6	LED Cathode (Negative)

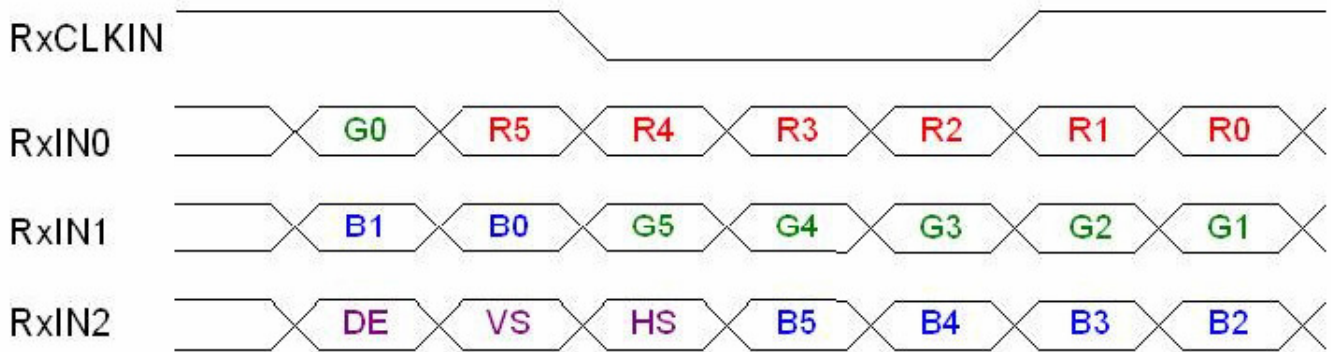
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description
VEEDID (3.3V)	+3.3V EDID Power
CLK EEDID	EDID Clock Input
DATA EEDID	EDID Data Input
RXIN0-, RXIN0+	LVDS differential data input(Red0-Red5, Green0)
RXIN1-, RXIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RXIN2-, RXIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DE)
RXCLKIN-, RXCLKIN+	LVDS differential clock input
VDD	+3.3V Power Supply
VSS	Ground

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin	Signal	Description
1	BIST/CT1	BIST/Connector Test*
2	VDD	Power Supply (3.3V typ.)
3	VDD	Power Supply (3.3V typ.)
4	V _{EDID}	DDC 3.3V power
5	CLK _{EDID}	DDC clock / SMBus clock
6	DATA _{EDID}	DDC data / SMBus data
7	Rin0-	- LVDS differential data input (R0-R5, G0)
8	Rn0+	+ LVDS differential data input (R0-R5, G0)
9	VSS	Ground
10	Rin1-	- LVDS differential data input (G1-G5, B0-B1)
11	Rn1+	+ LVDS differential data input (G1-G5, B0-B1)
12	VSS	Ground
13	Rin2-	- LVDS differential data input (B2-B5,HS,VS, DE)
14	Rn2+	+ LVDS differential data input (B2-B5,HS,VS, DE)
15	VSS	Ground
16	ClkIN-	- LVDS differential clock input
17	ClkIN+	+ LVDS differential clock input
18	VSS	Ground
19	NC	No Connection
20	NC	No Connection
21	NC	No Connection
22	NC	No Connection
23	NC	No Connection
24	NC	No Connection
25	NC	No Connection
26	NC	No Connection
27	NC	No Connection
28	NC	No Connection
29	NC	No Connection
30	VBL-	LED power return
31	VBL-	LED power return
32	VBL-	LED power return
33	NC	No Connection
34	BLIM	PWM for luminance control
35	BL_EN	BL On/Off
36	NC	No Connection

37	VBL+	6V - 20V LED power
38	VBL+	6V - 20V LED power
39	VBL+	6V - 20V LED power
40	BIST/CT2	BIST/Connector Test*

Note1: Start from right side

6.4 Interface Timing

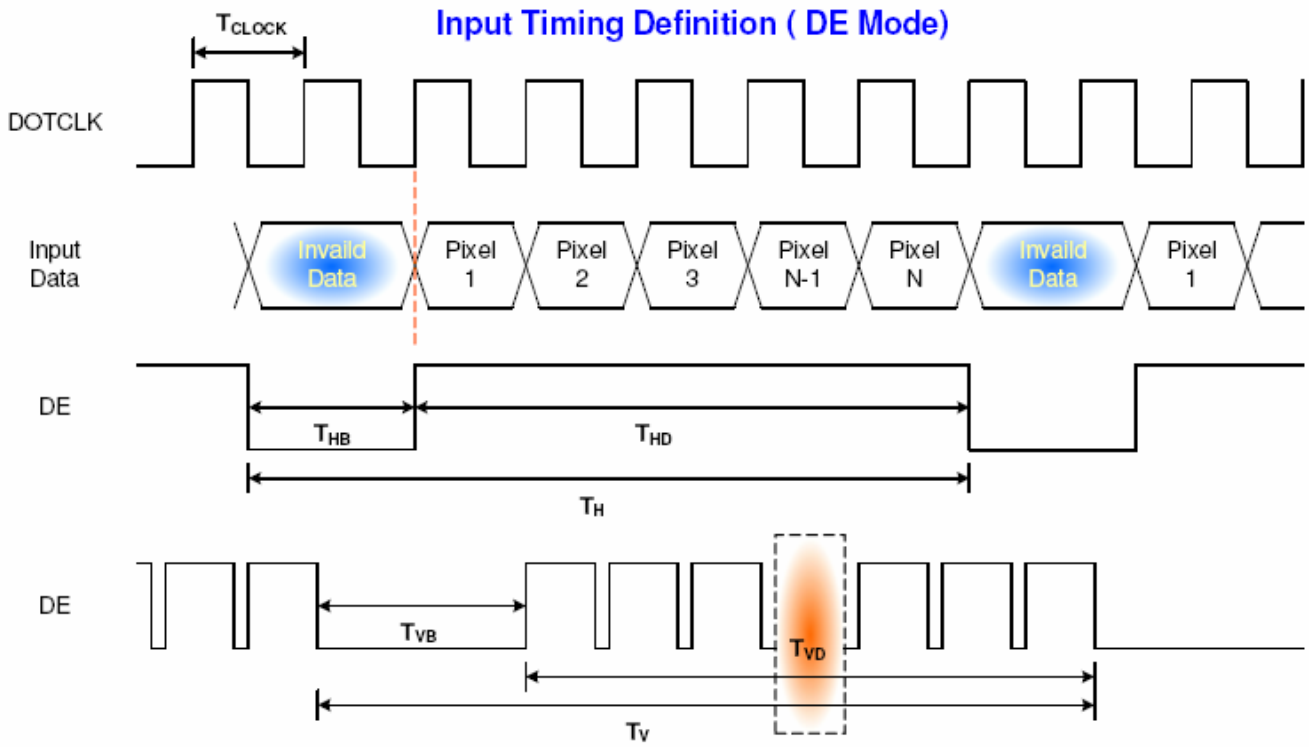
6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	50	60	-	Hz	
Clock frequency	$1/T_{\text{Clock}}$	-	69.3	72	MHz	
Vertical Section	Period	T_V	808	816	1023	T_{Line}
	Active	T_{VD}		800		
	Blanking	T_{VB}	8	16	-	
Horizontal Section	Period	T_H	1320	1408	2047	T_{Clock}
	Active	T_{HD}		1280		
	Blanking	T_{HB}	30	135		

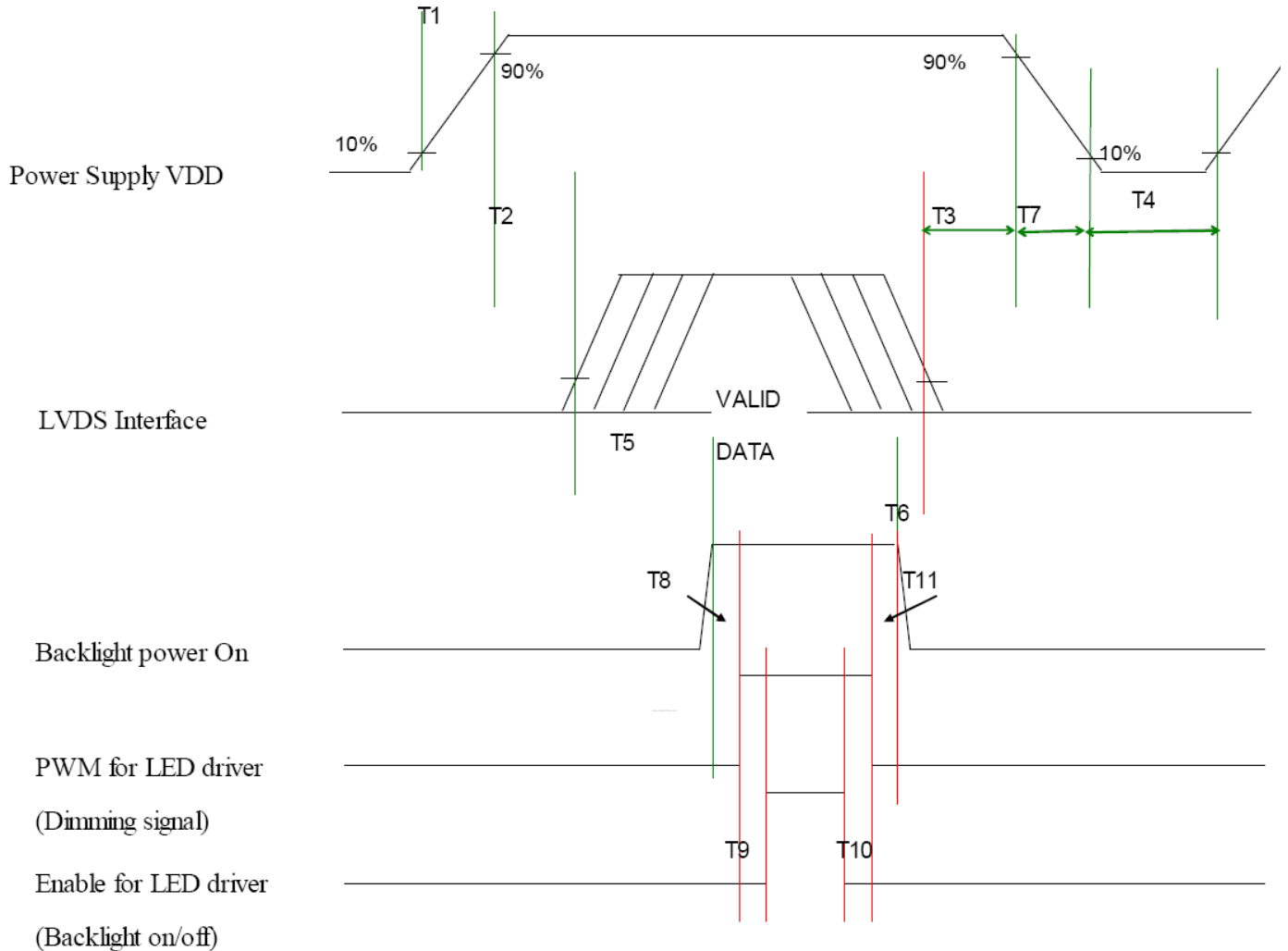
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value (ms)	
	Min.	Max.
T1	0.5	10
T2	5	50
T3	0.5	50
T4	400	-
T5	200	-
T6	200	-
T7	0	10
T8	10	---
T9	10	---
T10	0	---
T11	10	---



7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	20347-340E-12
Mating Housing/Part Number	I-PEX 20345-040T-31 or 20475-040T-## or compatible

8. Dynamic Test

8.1 Vibration Test

Test condition(Non-OP):

- Acceleration: 1.5 G
- Frequency: 10 - 500Hz half sine wave
- Sweep: 60 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test condition(Non-OP):

- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: +/-X,+/-Y,+/-Z , one time for each side

Remark:

1. Ambient condition is $25 \pm 5^{\circ}\text{C}$, Relative humidity : 40% ~ 70%
2. Non-packaged and Non-operation

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 300h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
 . Self-recoverable. No hardware failures.

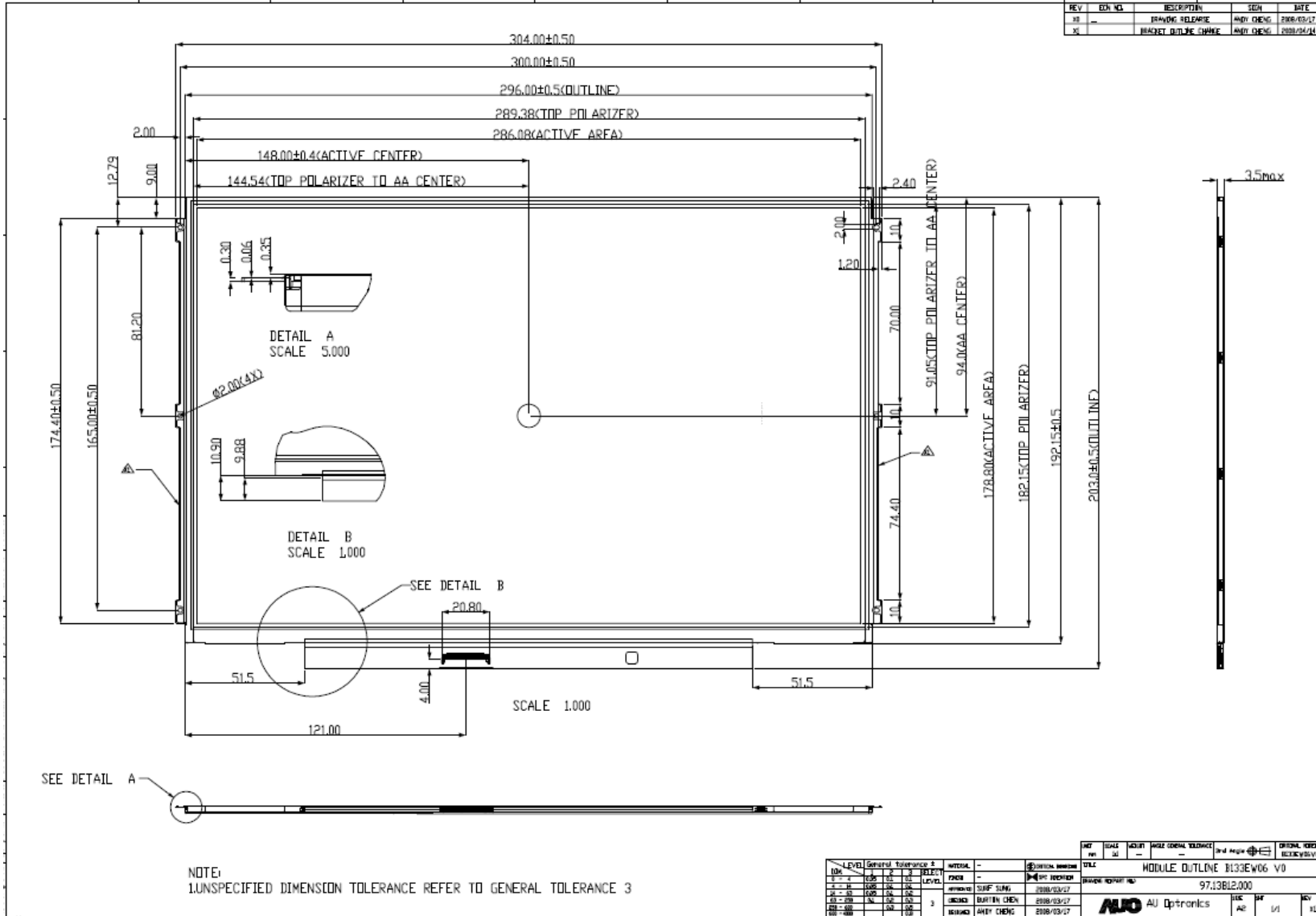


Product Specification

AU OPTRONICS CORPORATION

10. Mechanical Characteristics

10.1 LCM Outline Dimension



REV	EDN NO.	DESCRIPTION	SIGN	DATE
01		DRAWING RELEASE		2008/03/17
02		BRACKET OUTLINE CHANGE		2008/04/04

NOTE:
UNSPECIFIED DIMENSION TOLERANCE REFER TO GENERAL TOLERANCE 3

LEVEL	GENERAL TOLERANCE 4	INTERNAL	EXTERNAL	FORMAL	DATE	REVISION	DESCRIPTION
1	±0.10	±0.05	±0.10	±0.10	2008/03/17	1	INITIAL
2	±0.10	±0.05	±0.10	±0.10	2008/03/17	2	CHANG
3	±0.10	±0.05	±0.10	±0.10	2008/03/17	3	RELEAS

REV	EDN NO.	DESCRIPTION	SIGN	DATE
01		DRAWING RELEASE		2008/03/17
02		BRACKET OUTLINE CHANGE		2008/04/04

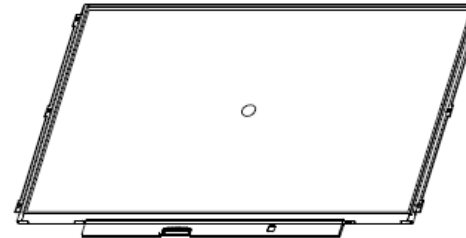
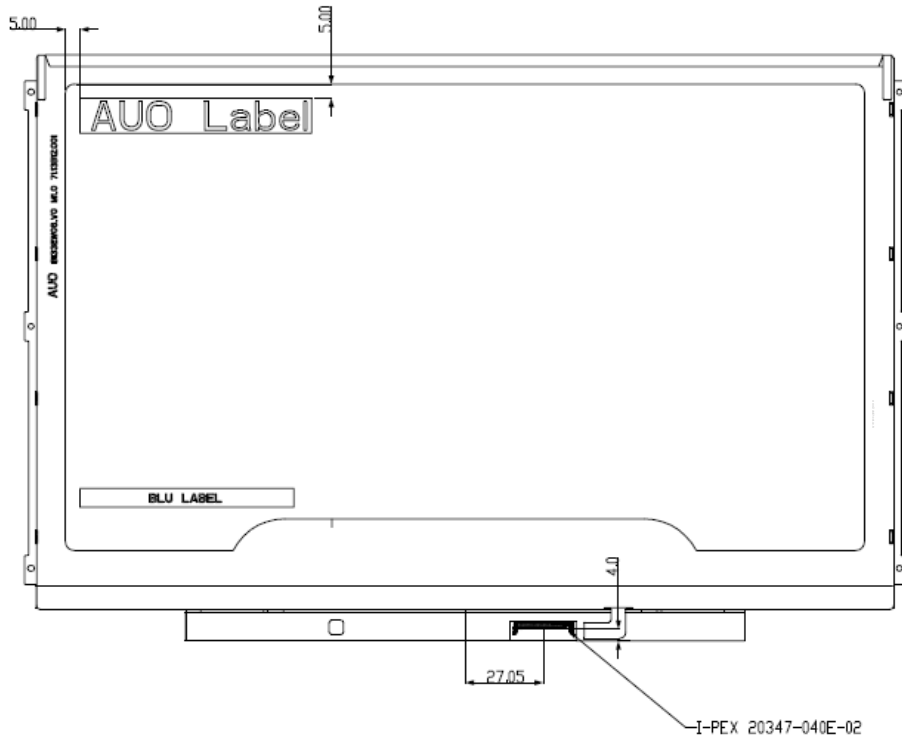
MODULE OUTLINE B133EW06 V0
97.13812.000
AUO AU Optonics



Product Specification

AU OPTRONICS CORPORATION

REV	EDN NO	DESCRIPTION	SEN	DATE
10	-	DRAWING RELEASE	ANDY CHENG	2008/03/27
11	-	BEZEL OUTLINE CHANGE	ANDY CHENG	2008/04/14



SCALE 0.500

LEVEL	General Tolerance	LEVEL	MINIUM	APPROVED	DATE
1.0	0.25	1.0	0.25	SAUF SUNG	2008/03/27
2.0	0.50	2.0	0.50	BARIN CHEN	2008/03/27
3.0	1.00	3.0	1.00	ANDY CHENG	2008/03/27

REV	SCALE	UNIT	SIZE	GENERAL TOLERANCE	3rd Angle	ORIGINAL FILE
11	24	-	-	-		1133EW06 V0
MODULE OUTLINE 1133EW06 V0						
DRAWING NUMBER: 9713BL2000						
AU Optronics						
DRG	APP	CHK	REV			
APR			2/2			
			11			

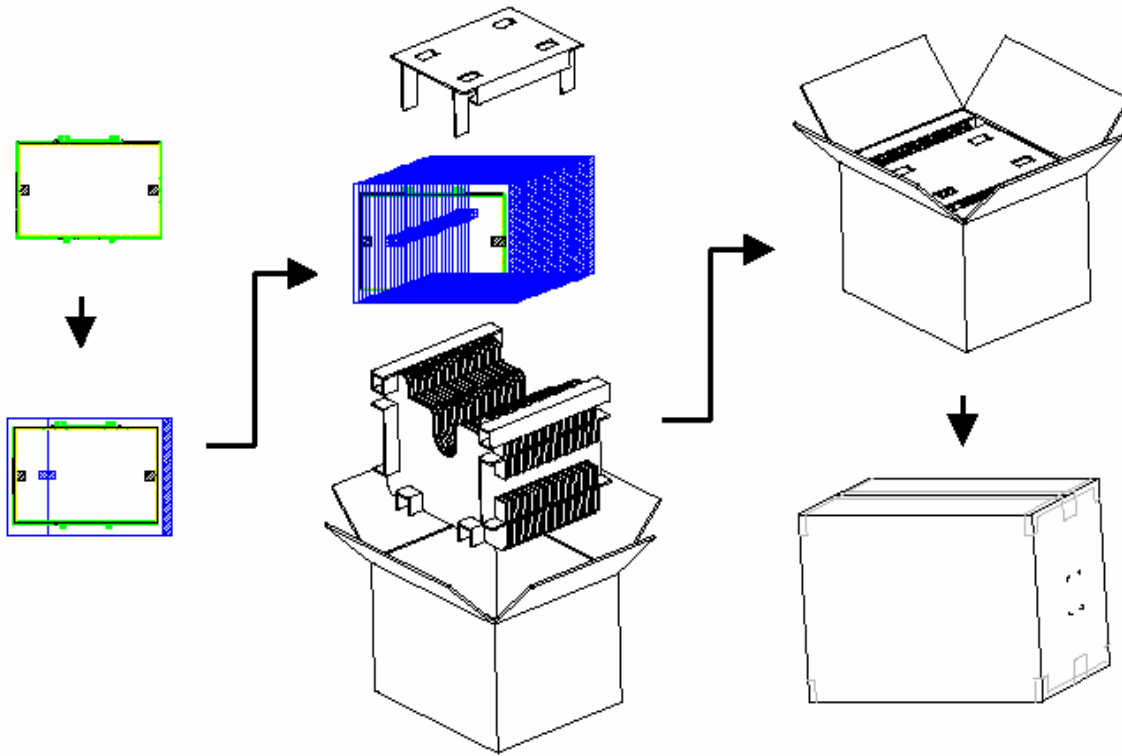
11. Shipping and Package

11.1 Shipping Label Format

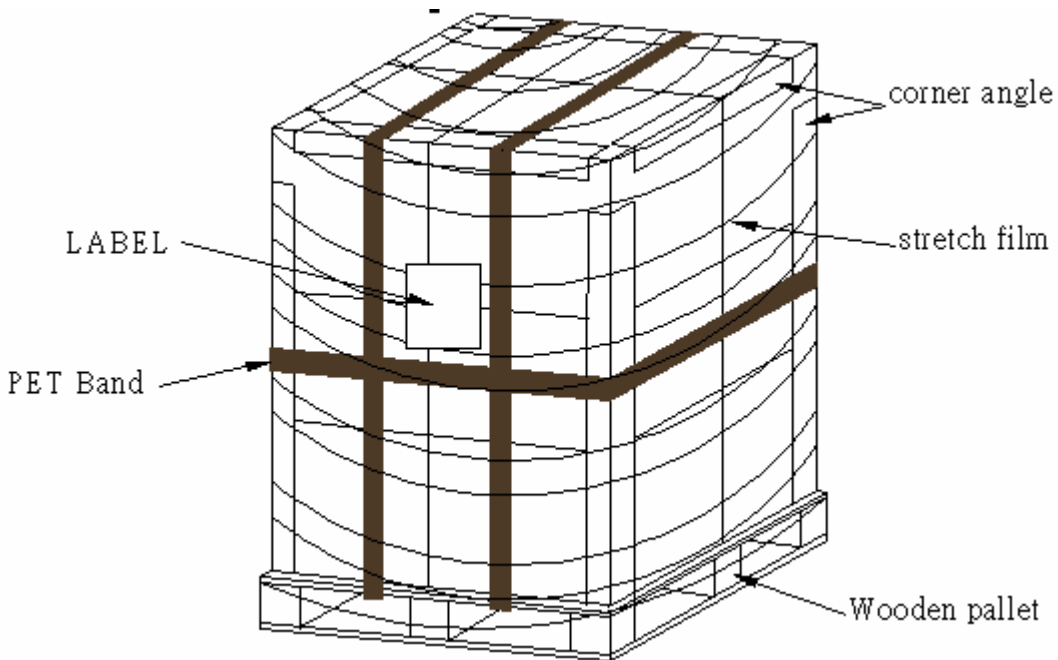
11.1 Shipping Label Format



11.2 Carton package



11.3 Shipping package of palletizing sequence





Product Specification

AU OPTRONICS CORPORATION

12. Appendix: EDID description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	24	00100100	36
0B	hex, LSB first	60	01100000	96
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	01	00000001	1
11	Year of manufacture	12	00010010	18
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	03	00000011	3
14	Video input def. (digital I/P, non-TMDS, CRGB)	80	10000000	128
15	Max H image size (rounded to cm)	1D	00011101	29
16	Max V image size (rounded to cm)	12	00010010	18
17	Display Gamma (=gamma*100)-100	78	01111000	120
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	0A	00001010	10
19	Red/green low bits (Lower 2:2:2:2 bits)	50	01010000	80
1A	Blue/white low bits (Lower 2:2:2:2 bits)	C5	11000101	197
1B	Red x (Upper 8 bits)	98	10011000	152
1C	Red y/ highER 8 bits	58	01011000	88
1D	Green x	52	01010010	82
1E	Green y	8E	10001110	142
1F	Blue x	27	00100111	39
20	Blue y	25	00100101	37
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1



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27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	12	00010010	18
37	Pixel Clock/10000 USB	1B	00011011	27
38	Horz active Lower 8bits	00	00000000	0
39	Horz blanking Lower 8bits	87	10000111	135
3A	HorzAct:HorzBlnk Upper 4:4 bits	50	01010000	80
3B	Vertical Active Lower 8bits	20	00100000	32
3C	Vertical Blanking Lower 8bits	10	00010000	16
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48
3E	HorzSync. Offset	30	00110000	48
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	36	00110110	54
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
42	Horizontal Image Size Lower 8bits	1E	00011110	30
43	Vertical Image Size Lower 8bits	B2	10110010	178
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16
45	Horizontal Border (zero for internal LCD)	00	00000000	0
46	Vertical Border (zero for internal LCD)	00	00000000	0
47	Signal (non-intr, norm, no stero, sep sync, neg pol)	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0
4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0



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52		00	00000000	0
53		00	00000000	0
54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	33	00110011	51
74	Manufacture P/N	33	00110011	51
75	Manufacture P/N	45	01000101	69
76	Manufacture P/N	57	01010111	87
77	Manufacture P/N	30	00110000	48
78	Manufacture P/N	36	00110110	54
79	Manufacture P/N	20	00100000	32
7A	Manufacture P/N	56	01010110	86
7B	Manufacture P/N	30	00110000	48
7C		20	00100000	32



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7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	D9	11011001	217
			SUM	5888