ASC8848; ASC8849; ASC8850; ASC8851

Multimedia SoC

Rev. 2.06 — 24 September 2011

Data sheet

1. General description

NXPs ASC8848/49/50/51 SoC is a single chip platform that is designed for embedded multimedia communication, security and entertainment applications. Powered by the most popular ARM926EJ processor and high performance NXP video hardware accelerators, ASC8848/49/50/51 SoC could provide upto 1080p @ 45fps MPEG-4 AVC (H.264) and JPEG encoding simultaneously at 1080p @ 40fps. With its built-in high performance image front-end processing engine, it can also provide better video quality than any smart sensor. Due to its highly flexible architecture, multiple stream real time encoding with up to 8x D1 (704x480) resolution is also practicable.

Version 2.0 of ASC8848/49/50/51 datasheet highlights the feature differences of ASC8848/49/50 with respect to ASC8851. It also provides details on ASC8851 pinouts.

2. Features and benefits

2.1 High Quality Media

NXPs expertise on multimedia processing and compression provides the state-of-the-art audio visual quality for entertainment and professional applications. The software based video encoding system guarantees perfect synchronization between audio and video channels.

2.1.1 H.264 Encoder

NXP H.264 encoder is compliant with H.264/MPEG-4 AVC (ISO/IEC 14496-10) video coding standard.The H.264 encoder supports the following features:

- H.264/MPEG-4 AVC Baseline Profile, Main Profile (I, P frame coding only), and High Profile (I, P frame coding only) @ Level 4.1
- CAVLC and CABAC entropy coding tools
- Full search quality motion estimation
- Up to 2 reference frames motion estimation
- 16*16, 16*8, 8*16, 8*8, 8*4, 4*8, and 4*4 motion estimation block size
- Integer, half and quarter pixel precision motion estimation
- Constant bitrate (CBR) and Variable bitrate (VBR) or constant quality
- Encoding capability up to D1 @ 240 fps or Full HD 1080p @ 45 fps
- Supports all intra prediction modes for 4 × 4, 8 × 8 and 16 × 16 block sizes
- Supports in-loop deblocking filter
- Forces intra MB insertion into inter-frames to maintain video quality for large I-frame interval
- Cb and Cr Qp can be different to Y
- Supports intra prediction in inter frames using 128 or reconstruction pixels

2.1.2 MPEG-4 Encoder

NXP MPEG-4 encoder is compliant with MPEG-4 Part 2 (ISO/IEC 14496-2) video coding standard.

The MPEG-4 encoder supports the following features:

- MPEG-4 Part 2 Simple Profile
- Error resilience tools (video packet re-synchronization)
- Full search quality motion estimation
- 16*16 and 8*8 motion estimation block size
- Integer and half pixel precision motion estimation
- Constant bit-rate (CBR) and variable bit-rate (VBR)/constant quality
- Encoding capability up to D1 @ 80 fps or Full HD 720p @ 30 fps (share the bandwidth with H.264 encoder)

2.1.3 JPEG Encoder

NXP JPEG encoder is compliant with JPEG (ISO/IEC IS 10918-1 | ITU-T Recommendation T.81) image coding standard. The JPEG encoder supports the following features:

- Baseline JPEG with JFIF support
- YCbCr 4:4:4, 4:2:2, and 4:2:0 input format
- Custom defined quality table and content adaptive Huffman table
- Encoding capability up to 80 megapixel/sec or Full HD 1080p @ 40 fps

2.2 Flexible Platform

The on-chip ARM926EJ processor and easy-to-use Video Media Library (VML) API ensure highest flexibility for system design. The highly integrated SoC platform provides a glueless interface to CMOS sensor, video decoder,video encoder, LCD module, HDMI transmitter, serial FLASH, NAND FLASH, DDR-II/III SDRAM, Gigabit Ethernet PHY, audio codec and camera control. USB 2.0 OTG and PCIe 1.1 interfaces are also available for wireless LAN connection, mass storage devices and other peripherals.

2.2.1 Video/Sensor Interface

Support various video/sensor input interfaces and rich functions on the captured frame

- .
- Support 2-channel 8-bit YCbCr 4:2:2 CCIR-656 progressive or interlace format
- Support 2-channel 8-bit YCbCr 4:2:2 format with separate SYNC signals
- Support 1-channel 16-bit YCbCr 4:2:2 format with separate or embedded SYNC signals
- Support 2-channel 2-to-1 time-multiplexed CCIR-656 8-bit YCbCr 4:2:2 progressive or interlace format
- Support 2-channel 4-to-1 time-multiplexed CCIR-656 8-bit YCbCr 4:2:2 progressive or interlace format
- Support 1-channel Bayer pattern (Bayer RGB or CMYG) raw data format up to 16-bit.
- Capture up to 8-channel video data simultaneously
- Image front-end processing (Color Filter Array, Auto White Balance, Auto Exposure, and Auto Focus, color correction, gamma correction)
- Tone mapping that can provide Wide Dynamic Range (WDR) image quality
- Automatic Contrast enhancement that can improve the image quality in high contrast environment
- Photometric and Geometric lens distortion correction
- Color adjustment (saturation, brightness, and contract control)
- Image cropping, mirror, and flip

2.2.2 Audio Interface

Support I2S format and there are four stereo input channels and one full-duplex stereo channel.

2.2.3 Image Processing

Rich image processing functions are included.

- Motion adaptive interlacing
- Arbitrary image resizing and scaling ratio (Scaling using Bi Cubic 4 Tap filter)
- Spatial (2D) noise reduction (Gaussian, Impulse, False color)
- Edge enhancement
- Frame difference motion detection with 16 arbitrary sized rectangular windows
- Privacy mask with arbitrary shape and grid size

2.2.4 Data Encryption

- DES, TDES, AES,SHA-1
- SHA-224, SHA-256, SHA-384, SHA-512

2.2.5 Host Controller

ARM926EJ is integrated with 16KB instruction cache and 16KB data cache. The operating frequency is up to 600 MHz on Linux 2.6x.

2.2.6 External Memory Interface

There are several interfaces built in for the external memory devices.

- Two 16-bit DDR-II/III 800 SDRAM channels that can support up to 1GB DDR-III per channel or up to 512MB DDR-II per channel for ASC8848/49/50 M2 version and ASC8851. [1]
- Two high-speed SPI interface to support serial flash
- Two NAND FLASH memory interface

2.2.7 Peripherals

High-speed peripheral interfaces are built in for the application needs

- USB 2.0 OTG (host/device) interface
- PCIe x1 1.1 dual mode (root complex/end point) interface
- 10/100/1000 Ethernet MAC

Low-speed peripherals include:

- Two MMC/SD/SDIO interfaces
- Four UARTs (2 full functionality / 2 simple UARTs (VPL UARTC))
- One IrDA interface (VPL IRDAC)
- 20-bit GPIOs
- 8 programmable timers (VPL TMRC)
- 1 watchdog timer (VPL WDTC)
- 1 64-bit system timer (VPL SYSC)
- Interface support for WLAN, Bluetooth, WUSB

[1] Refer to Table 2 for ASC8848/49/50 M1 version

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
ASC8848ET	TFBGA484	thin profile fine-pitch ball grid array; 484 balls	-
ASC8849ET	TFBGA484	thin profile fine-pitch ball grid array; 484 balls	-
ASC8850ET	TFBGA484	thin profile fine-pitch ball grid array; 484 balls	-

Table 2. Comparison of ASC8848/49/50 M1 and ASC8848/49/50/51 M2 features

Feature	Version	ASC8848	ASC8849	ASC8850	ASC8851
Max. sensor resolution	ASC8848/49/50 M1	1.3M	5M	12M	NA
	ASC8848/49/50/51 M2	5M	5M	12M	12M
Max number of input bits	ASC8848/49/50 M1	10 bits	16 bits	16 bits	NA
	ASC8848/49/50/51 M2	12 bits	16 bits	16 bits	16 bits
Max. number of input channels	ASC8848/49/50 M1	3	4	6	NA
	ASC8848/49/50/51 M2	3	4	6	8
Max VOC bits	ASC8848/49/50 M1	8	24	24	NA
	ASC8848/49/50/51 M2	8	24	24	24
Max HDMI output	ASC8848/49/50 M1	not supported	720p @ 60 fps	1080p @ 30 fps	NA
	ASC8848/49/50/51 M2	not supported	720p @ 60 fps	1080p @ 60 fps	1080p @ 60 fps
BT1120 output support	ASC8848/49/50 M1	No	No	No	NA
	ASC8848/49/50/51 M2	No	Yes	Yes	Yes
ARM frequency	ASC8848/49/50 M1	400 MHz	450 MHz	600 MHz	NA
	ASC8848/49/50/51 M2	400 MHz	500 MHz	600 MHz	600 MHz
H264 maximum performance	ASC8848/49/50 M1	720p @ 30 fps	SXGA @ 30 fps	1080p @ 30 fps	NA
	ASC8848/49/50/51 M2	720p @ 45 fps	SXGA @ 40 fps	1080p @ 30 fps	1080p @ 45 fps
DDR support	ASC8848/49/50 M1	1-ch 16 b DDR-II, 266 MHz up to 512 MB per channel	2-ch 16 b DDR-II, 300 MHz up to 512 MB per channel	2-ch 16 b DDR-II, 400 MHz upto 512 MB per channel	NA
	ASC8848/49/50/51 M2	1-ch 16 b @266 MHz up to 1 GB DDR-III or 512 MB DDR-II per channel	2-ch 16 b @333 MHz up to 1 GB DDR-III or 512 MB DDR-II per channel	2-ch 16 b @400 MHz up to 1 GB DDR-III or 512 MB DDR-II per channel	2-ch 16 b @400 MHz up to 1 GB DDR-III or 512 MB DDR-II per channel

Table 3. Comparison of ASC8848, ASC8849, ASC8850 & ASC8851 peripherals

Feature	ASC8848	ASC8849	ASC8850	ASC8851
DDR- II/III channels[1]	1	2	2	2
I2S channels	1	5	5	5
Ethernet	MII	RGMII/GMII/MII	RGMII/GMII/MII	RGMII/ GMII/MII
SPI interface	1	2	2	2

Table 3. Comparison of ASC8848, ASC8849, ASC8850 & ASC8851 peripherals

Feature	ASC8848	ASC8849	ASC8850	ASC8851
SD Interface	1	2	2	2
UARTs	2	4	4	4
NAND Flash	1	2	2	2

[1] DDR-II/III is supported only for ASC8848/49/50 M2 version and ASC8851 for ASC8848/49/50 M1 version only DDR-II is supported.

4. Functional diagram

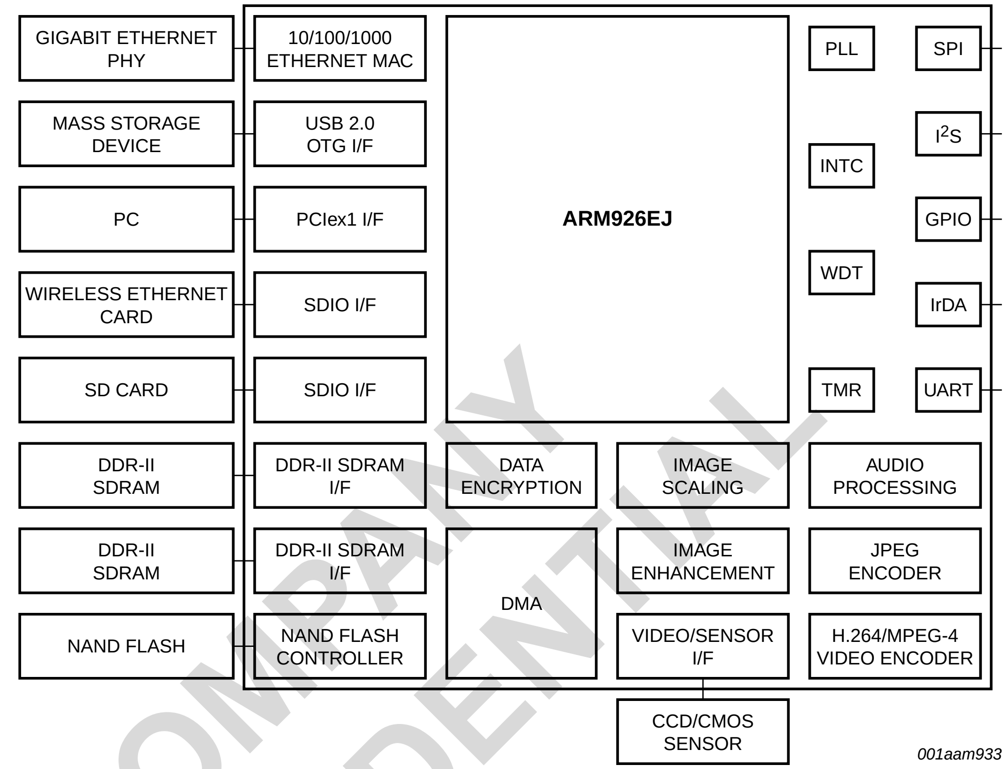
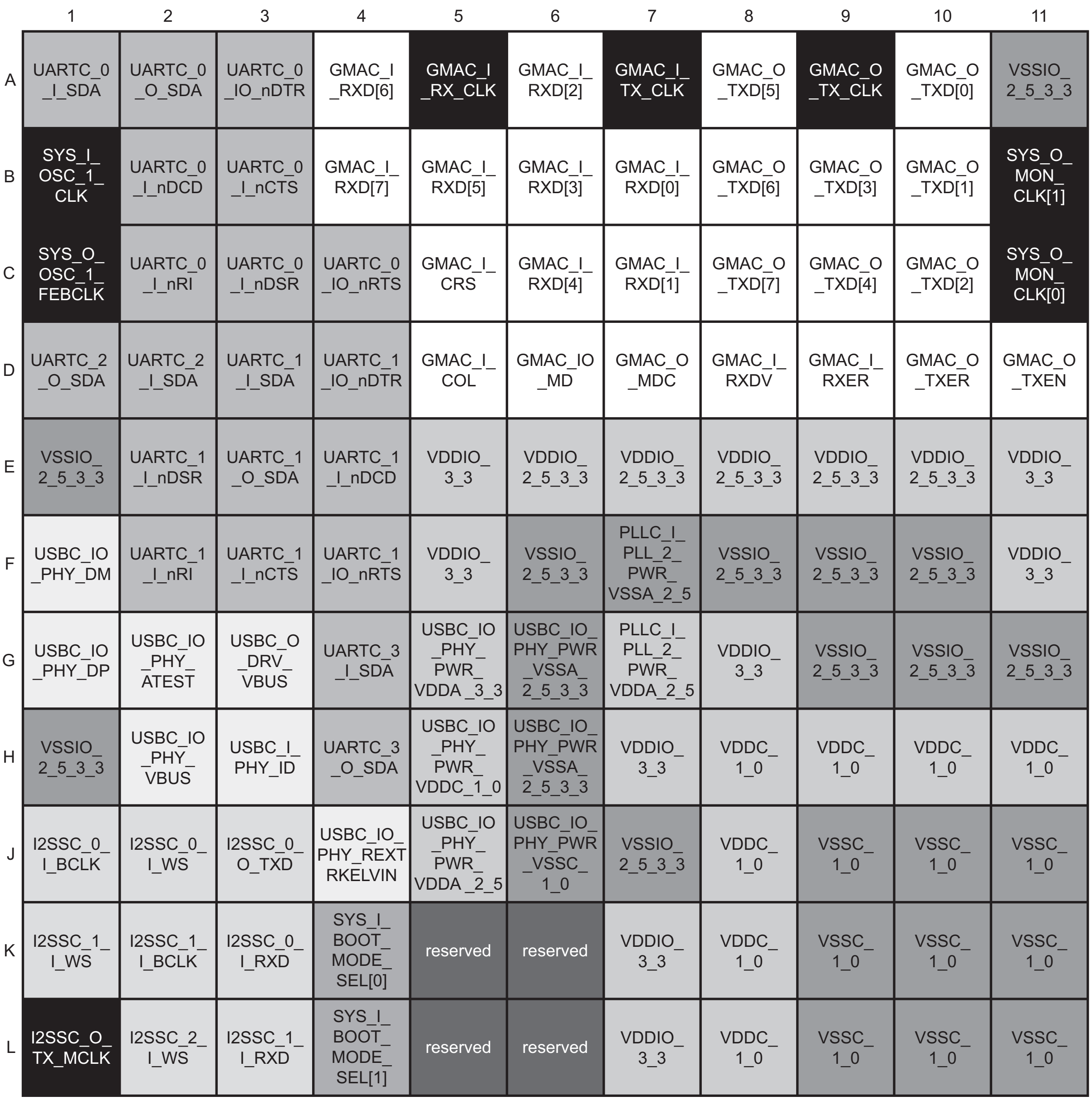


Fig 1. Functional Blocks

5. Pinning information

5.1 Pinning

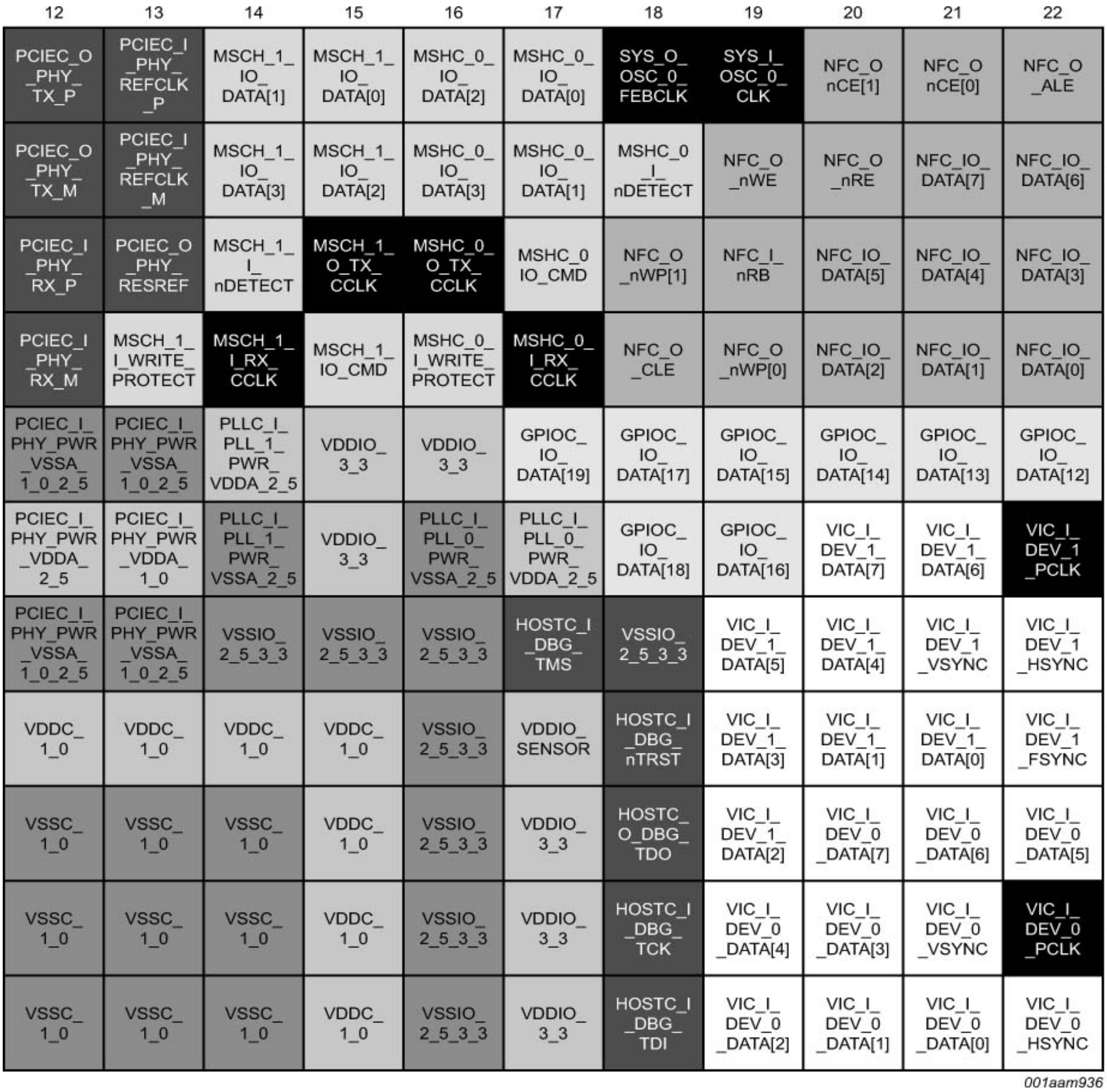
All ASC8849/50/51 SoC signals are listed in Table 6 and ASC8848 SoC signals are listed in Table 8. ASC8848/49/50 SoC has input pins (I), output pins (O), bi-directional pins (I/O), power pins (P), and ground pins (G). Some functional pins have built-in functions as specified at Table 6. Table 4 explains each I/O functions used in Table 6. The ball map is split to four quadrants as shown in Figure 2 to Figure 5.



	1	2	3	4	5	6	7	8	9	10	11
A	UARTC_0_I_SDA	UARTC_0_O_SDA	UARTC_0_IO_nDTR	GMAC_I_RXD[6]	GMAC_I_RX_CLK	GMAC_I_RXD[2]	GMAC_I_TX_CLK	GMAC_O_TXD[5]	GMAC_O_TX_CLK	GMAC_O_TXD[0]	VSSIO_2_5_3_3
B	SYS_I_OSC_1_CLK	UARTC_0_I_nDCD	UARTC_0_I_nCTS	GMAC_I_RXD[7]	GMAC_I_RXD[5]	GMAC_I_RXD[3]	GMAC_I_RXD[0]	GMAC_O_TXD[6]	GMAC_O_TXD[3]	GMAC_O_TXD[1]	SYS_O_MON_CLK[1]
C	SYS_O_OSC_1_FEBCLK	UARTC_0_I_nRI	UARTC_0_I_nDSR	UARTC_0_IO_nRTS	GMAC_I_CRS	GMAC_I_RXD[4]	GMAC_I_RXD[1]	GMAC_O_TXD[7]	GMAC_O_TXD[4]	GMAC_O_TXD[2]	SYS_O_MON_CLK[0]
D	UARTC_2_O_SDA	UARTC_2_I_SDA	UARTC_1_I_SDA	UARTC_1_IO_nDTR	GMAC_I_COL	GMAC_IO_MD	GMAC_O_MDC	GMAC_I_RXDV	GMAC_I_RXER	GMAC_O_TXER	GMAC_O_TXEN
E	VSSIO_2_5_3_3	UARTC_1_I_nDSR	UARTC_1_O_SDA	UARTC_1_I_nDCD	VDDIO_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_3_3
F	USBC_IO_PHY_DM	UARTC_1_I_nRI	UARTC_1_I_nCTS	UARTC_1_IO_nRTS	VDDIO_3_3	VSSIO_2_5_3_3	PLLC_I_PLL_2_PWR_VSSA_2_5	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VDDIO_3_3
G	USBC_IO_PHY_DP	USBC_IO_PHY_ATEST	USBC_O_DRV_VBUS	UARTC_3_I_SDA	USBC_IO_PHY_PWR_VDDA _3_3	USBC_IO_PHY_PWR_VSSA_2_5_3_3	PLLC_I_PLL_2_PWR_VDDA_2_5	VDDIO_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3
H	VSSIO_2_5_3_3	USBC_IO_PHY_VBUS	USBC_I_PHY_ID	UARTC_3_O_SDA	USBC_IO_PHY_PWR_VDDC_1_0	USBC_IO_PHY_PWR_VSSA_2_5_3_3	VDDIO_3_3	VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0
J	I2SSC_0_I_BCLK	I2SSC_0_I_WS	I2SSC_0_O_TXD	USBC_IO_PHY_REXTRKELVIN	USBC_IO_PHY_PWR_VDDA _2_5	USBC_IO_PHY_PWR_VSSC_1_0	VSSIO_2_5_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0
K	I2SSC_1_I_WS	I2SSC_1_I_BCLK	I2SSC_0_I_RXD	SYS_I_BOOT_MODE_SEL[0]	reserved	reserved	VDDIO_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0
L	I2SSC_O_TX_MCLK	I2SSC_2_I_WS	I2SSC_1_I_RXD	SYS_I_BOOT_MODE_SEL[1]	reserved	reserved	VDDIO_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0

Remark: Pin Assignment is for the M2 version. For the M1 version refer to Table 6

Fig 2. Top left view of an ASC8849 / 8850 / 8851 TFBGA-484 pin assignment



12	13	14	15	16	17	18	19	20	21	22	
PCIEC_O_PHY_TX_P	PCIEC_I_PHY_REFCLK_P	MSCH_1_IO_DATA[1]	MSCH_1_IO_DATA[0]	MSHC_0_IO_DATA[2]	MSHC_0_IO_DATA[0]	SYS_O_OSC_0_FEBCLK	SYS_I_OSC_0_CLK	NFC_O nCE[1]	NFC_O nCE[0]	NFC_O_ALE	A
PCIEC_O_PHY_TX_M	PCIEC_I_PHY_REFCLK_M	MSCH_1_IO_DATA[3]	MSCH_1_IO_DATA[2]	MSHC_0_IO_DATA[3]	MSHC_0_IO_DATA[1]	MSHC_0_I_nDETECT	NFC_O_nWE	NFC_O_nRE	NFC_IO_DATA[7]	NFC_IO_DATA[6]	B
PCIEC_I_PHY_RX_P	PCIEC_O_PHY_RESREF	MSCH_1_I_nDETECT	MSCH_1_O_TX_CCLK	MSHC_0_O_TX_CCLK	MSHC_0 IO_CMD	NFC_O_nWP[1]	NFC_I_nRB	NFC_IO_DATA[5]	NFC_IO_DATA[4]	NFC_IO_DATA[3]	C
PCIEC_I_PHY_RX_M	MSCH_1_I_WRITE_PROTECT	MSCH_1_I_RX_CCLK	MSCH_1_IO_CMD	MSHC_0_I_WRITE_PROTECT	MSHC_0_I_RX_CCLK	NFC_O_CLE	NFC_O_nWP[0]	NFC_IO_DATA[2]	NFC_IO_DATA[1]	NFC_IO_DATA[0]	D
PCIEC_I_PHY_PWR_VSSA_1_0_2_5	PCIEC_I_PHY_PWR_VSSA_1_0_2_5	PLLC_I_PLL_1_PWR_VDDA_2_5	VDDIO_3_3	VDDIO_3_3	GPIOC_IO_DATA[19]	GPIOC_IO_DATA[17]	GPIOC_IO_DATA[15]	GPIOC_IO_DATA[14]	GPIOC_IO_DATA[13]	GPIOC_IO_DATA[12]	E
PCIEC_I_PHY_PWR_VDDA_2_5	PCIEC_I_PHY_PWR_VDDA_1_0	PLLC_I_PLL_1_PWR_VSSA_2_5	VDDIO_3_3	PLLC_I_PLL_0_PWR_VSSA_2_5	PLLC_I_PLL_0_PWR_VDDA_2_5	GPIOC_IO_DATA[18]	GPIOC_IO_DATA[16]	VIC_I_DEV_1_DATA[7]	VIC_I_DEV_1_DATA[6]	VIC_I_DEV_1_PCLK	F
PCIEC_I_PHY_PWR_VSSA_1_0_2_5	PCIEC_I_PHY_PWR_VSSA_1_0_2_5	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3	HOSTC_I_DBG_TMS	VSSIO_2_5_3_3	VIC_I_DEV_1_DATA[5]	VIC_I_DEV_1_DATA[4]	VIC_I_DEV_1_VSYNC	VIC_I_DEV_1_HSYNC	G
VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_SENSOR	HOSTC_I_DBG_nTRST	VIC_I_DEV_1_DATA[3]	VIC_I_DEV_1_DATA[1]	VIC_I_DEV_1_DATA[0]	VIC_I_DEV_1_FSYNC	H
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_3_3	HOSTC_O_DBG_TDO	VIC_I_DEV_1_DATA[2]	VIC_I_DEV_0_DATA[7]	VIC_I_DEV_0_DATA[6]	VIC_I_DEV_0_DATA[5]	J
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_3_3	HOSTC_I_DBG_TCK	VIC_I_DEV_0_DATA[4]	VIC_I_DEV_0_DATA[3]	VIC_I_DEV_0_VSYNC	VIC_I_DEV_0_PCLK	K
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_3_3	HOSTC_I_DBG_TDI	VIC_I_DEV_0_DATA[2]	VIC_I_DEV_0_DATA[1]	VIC_I_DEV_0_DATA[0]	VIC_I_DEV_0_HSYNC	L

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Remark: Pin Assignment is for the M2 version. For the M1 version refer to Table 6

Fig 3. Top right view of an ASC8849 / 8850/ 8851 TFBGA-484 pin assignment

	1	2	3	4	5	6	7	8	9	10	11
M	I2SSC_O_RX_MCLK	I2SSC_2_I_RXD	I2SSC_2_I_BCLK	SYS_I_nRST	VSSIO_2_5_3_3	reserved	VDDIO_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0
N	I2SSC_3_I_RXD	I2SSC_3_I_WS	I2SSC_3_I_BCLK	VSSIO_2_5_3_3	reserved	reserved	VDDIO_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0
P	I2SSC_4_I_RXD	I2SSC_4_I_WS	I2SSC_4_I_BCLK	VSSC_1_0	reserved	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0
R	SSIC_I_RXD	SSIC_O_BCLK	WDTC_O_nRST	DDR32 SDMC_IO_PWR_VSSIO_1_8	reserved	DDR32 SDMC_IO_PWR_VSSIO_1_8	VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0
T	SSIC_O_nSEL[0]	SSIC_O_TXD	IRDAC_I_SDA	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PHY_PWR_VSSA_2_5	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8
U	SSIC_O_nSEL[1]	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 DMC_O_nRST	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8
V	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VREF_0_9	DDR32 SDMC_IO_PWR_VREF_0_9	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 DMC_O_ADDR[15]
W	DDR32 SDMC_0_O_DM[1]	DDR32 SDMC_0_IO_DQ[13]	DDR32 SDMC_I_CALI	DDR32 SDMC_0_IO_DQ[7]	DDR32 SDMC_0_IO_DQ[5]	DDR32 SDMC_O_PHY_ATEST	DDR32 SDMC_O_ADDR[2]	DDR32 SDMC_O_ADDR[4]	DDR32 SDMC_O_ADDR[8]	DDR32 SDMC_O_ADDR[6]	DDR32 SDMC_O_ADDR[14]
Y	DDR32 SDMC_0_IO_DQ[15]	DDR32 SDMC_0_IO_DQ[8]	DDR32 SDMC_0_IO_DQ[10]	DDR32 SDMC_0_IO_DQ[0]	DDR32 SDMC_0_IO_DQ[2]	DDR32 SDMC_0_O_DM[0]	DDR32 SDMC_O_BA[2]	DDR32 SDMC_O_BA[0]	DDR32 SDMC_O_ADDR[0]	DDR32 SDMC_O_ADDR[5]	DDR32 SDMC_O_ADDR[1]
AA	DDR32 SDMC_0_IO_DQ[9]	DDR32 SDMC_0_IO_DQ[11]	DDR32 SDMC_0_IO_DQ[12]	DDR32 SDMC_0_IO_DQ[6]	DDR32 SDMC_0_IO_DQ[1]	DDR32 SDMC_0_IO_DQ[3]	DDR32 SDMC_O_BA[1]	DDR32 SDMC_O_nRAS	DDR32 SDMC_O_nCAS	DDR32 SDMC_O_ADDR[10]	DDR32 SDMC_O_nWE
AB	DDR32 SDMC_0_IO_DQ[14]	DDR32 SDMC_0_IO_DQS[1]	DDR32 SDMC_0_IO_nDQS[1]	DDR32 SDMC_0_IO_DQ[4]	DDR32 SDMC_0_IO_DQS[0]	DDR32 SDMC_0_IO_nDQS[0]	DDR32 SDMC_0_O_nCS	DDR32 SDMC_0_O_ODT	DDR32 SDMC_0_O_CKE	DDR2 SDMC_O_CLK	DDR2 SDMC_O_nCLK

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Remark: Pin Assignment is for M2version. For M1 version refer to Table 6

Fig 4. Bottom left view of an ASC8849 / 8850/ 8851 TFBGA-484 pin assignment

VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_3_3	HOSTC_O_DBG_RTCK	VOC_O_DATA[23]	VOC_O_DATA[22]	VOC_O_DATA[21]	VIC_I_DEV_0_FSYNC	M
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VOC_I_CLK	VDDIO_3_3	VOC_O_DATA[20]	VOC_O_DATA[19]	VOC_O_DATA[18]	VOC_O_DATA[17]	N
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	PLLC_I_PLL_3_PWR_VSSA_2_5	PLLC_I_PLL_3_PWR_VDDA_2_5	VOC_O_DATA[16]	VOC_O_DATA[15]	VOC_O_DATA[14]	VOC_O_DATA[13]	P
VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0	GPIOC_IO_DATA[6]	GPIOC_IO_DATA[7]	GPIOC_IO_DATA[11]	VOC_O_DATA[12]	VOC_O_DATA[11]	VOC_O_DATA[10]	VOC_O_DATA[9]	R
DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PHY_VSSA_2_5	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	GPIOC_IO_DATA[9]	GPIOC_IO_DATA[8]	GPIOC_IO_DATA[10]	VOC_O_DATA[8]	VOC_O_DATA[7]	VOC_O_DATA[6]	VOC_O_PCLK	T
DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PHY_VDDA_2_5	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	VOC_O_DATA[5]	VOC_O_DATA[4]	VOC_O_DATA[3]	VOC_O_DATA[2]	U
DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VREF_0_9	DDR32 SDMC_IO_PWR_VREF_0_9	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VDDIO_1_8	DDR32 SDMC_IO_PWR_VSSIO_1_8	VOC_O_BLANK	VOC_O_DATA[1]	VOC_O_DATA[0]	V
DDR32 SDMC_O_ADDR[8]	DDR32 SDMC_O_ADDR[13]	DDR32 SDMC_O_ADDR[11]	DDR32 SDMC_1_IO_DQ[3]	DDR32 SDMC_1_IO_DQ[0]	DDR32 SDMC_IO_PHY_PWR_VDDA_2_5	DDR32 SDMC_1_IO_DQ[11]	DDR32 SDMC_1_O_DM[1]	DDR32 SDMC_IO_PWR_VSSIO_1_8	VOC_O_HSYNC	VOC_O_VSYNC	W
DDR32 SDMC_O_ADDR[3]	DDR32 SDMC_O_ADDR[7]	DDR32 SDMC_1_IO_DQ[7]	DDR32 SDMC_1_IO_DQ[5]	DDR32 SDMC_1_O_DM[0]	DDR32 SDMC_1_IO_DQ[15]	DDR32 SDMC_1_IO_DQ[9]	DDR32 SDMC_1_IO_DQ[10]	GPIOC_IO_DATA[4]	GPIOC_IO_DATA[5]	SYS_O_OSC_2_FEBCLK	Y
DDR32 SDMC_O_ADDR[12]	DDR32 SDMC_1_O_nCS	DDR32 SDMC_1_IO_DQ[6]	DDR32 SDMC_1_IO_DQ[4]	DDR32 SDMC_1_IO_DQ[1]	DDR32 SDMC_1_IO_DQ[14]	DDR32 SDMC_1_IO_DQ[13]	DDR32 SDMC_1_IO_DQ[8]	GPIOC_IO_DATA[3]	GPIOC_IO_DATA[2]	SYS_I_OSC_2_CLK	AA
DDR32 SDMC_1_O_ODT	DDR32 SDMC_1_O_CKE	DDR32 SDMC_1_IO_nDQS[0]	DDR32 SDMC_1_IO_DQS[0]	DDR32 SDMC_1_IO_DQ[2]	DDR32 SDMC_1_IO_DQ[12]	DDR32 SDMC_1_IO_nDQS[1]	DDR32 SDMC_1_IO_DQS[1]	DDR32 SDMC_IO_PWR_VSSIO_1_8	GPIOC_IO_DATA[1]	GPIOC_IO_DATA[0]	AB
12	13	14	15	16	17	18	19	20	21	22	

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Remark: Pin Assignment is for M2 version. For M1 version refer Table 6

Fig 5. Bottom right view of an ASC8849 / 8850/ 8851 TFBGA-484 pin assignment

The ball map of ASC8848 is split into four quadrants as shown in Figure 6 to Figure 9.

	1	2	3	4	5	6	7	8	9	10	11
A	UARTC_0_I_SDA	UARTC_0_O_SDA	UARTC_0_IO_nDTR	Reserved/NC	MAC_I_RX_CLK	MAC_I_RXD[2]	MAC_I_TX_CLK	Reserved/NC	Reserved/NC	MAC_O_TXD[0]	VSSIO_2_5_3_3
B	SYS_I_OSC_1_CLK	UARTC_0_I_nDCD	UARTC_0_I_nCTS	Reserved/NC	Reserved/NC	MAC_I_RXD[3]	MAC_I_RXD[0]	Reserved/NC	MAC_O_TXD[3]	MAC_O_TXD[1]	Reserved/NC
C	SYS_O_OSC_1_FEBCLK	UARTC_0_I_nRI	UARTC_0_I_nDSR	UARTC_0_IO_nRTS	MAC_I_CRS	Reserved/NC	MAC_I_RXD[1]	Reserved/NC	Reserved/NC	MAC_O_TXD[2]	SYS_O_MON_CLK[0]
D	Reserved/NC	Reserved/NC or VSSIO_2_5_3_3	UARTC_1_I_SDA	Reserved/NC	MAC_I_COL	MAC_IO_MD	MAC_O_MDC	MAC_I_RXDV	MAC_I_RXER	MAC_O_TXER	MAC_O_TXEN
E	VSSIO_2_5_3_3	Reserved/NC	UARTC_1_O_SDA	Reserved/NC	VDDIO_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_2_5_3_3	VDDIO_3_3
F	USBC_IO_PHY_DM	Reserved/NC	Reserved/NC	Reserved/NC	VDDIO_3_3	VSSIO_2_5_3_3	PLLC_I_PLL_2_PWR_VSSA_2_5	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VDDIO_3_3
G	USBC_IO_PHY_DP	USBC_IO_PHY_ATEST	USBC_O_DRV_VBUS	Reserved/NC or VSSIO_2_5_3_3	USBC_IO_PHY_PWR_VDDA _3_3	USBC_IO_PHY_PWR_VSSA _2_5_3_3	PLLC_I_PLL_2_PWR_VDDA_2_5	VDDIO_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3
H	VSSIO_2_5_3_3	USBC_IO_PHY_VBUS	USBC_I_PHY_ID	Reserved/NC	USBC_IO_PHY_PWR_VDDC_1_0	USBC_IO_PHY_PWR_VSSA_2_5_3_3	VDDIO_3_3	VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0
J	I2SSC_0_I_BCLK	I2SSC_0_I_WS	I2SSC_0_O_TXD	USBC_IO_PHY_REXTRKELVIN	USBC_IO_PHY_PWR_VDDA _2_5	USBC_IO_PHY_PWR_VSSC_1_0	VSSIO_2_5_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0
K	Reserved/NC or VSSIO_2_5_3_3	Reserved/NC or VSSIO_2_5_3_3	I2SSC_0_I_RXD	SYS_I_BOOT_MODE_SEL[0]	Reserved/NC	Reserved/NC	VDDIO_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0
L	I2SSC_O_TX_MCLK	Reserved/NC or VSSIO_2_5_3_3	Reserved/NC or VSSIO_2_5_3_3	SYS_I_BOOT_MODE_SEL[1]	Reserved/NC	Reserved/NC	VDDIO_3_3	VDDC_1_0	VSSC_1_0	VSSC_1_0	VSSC_1_0

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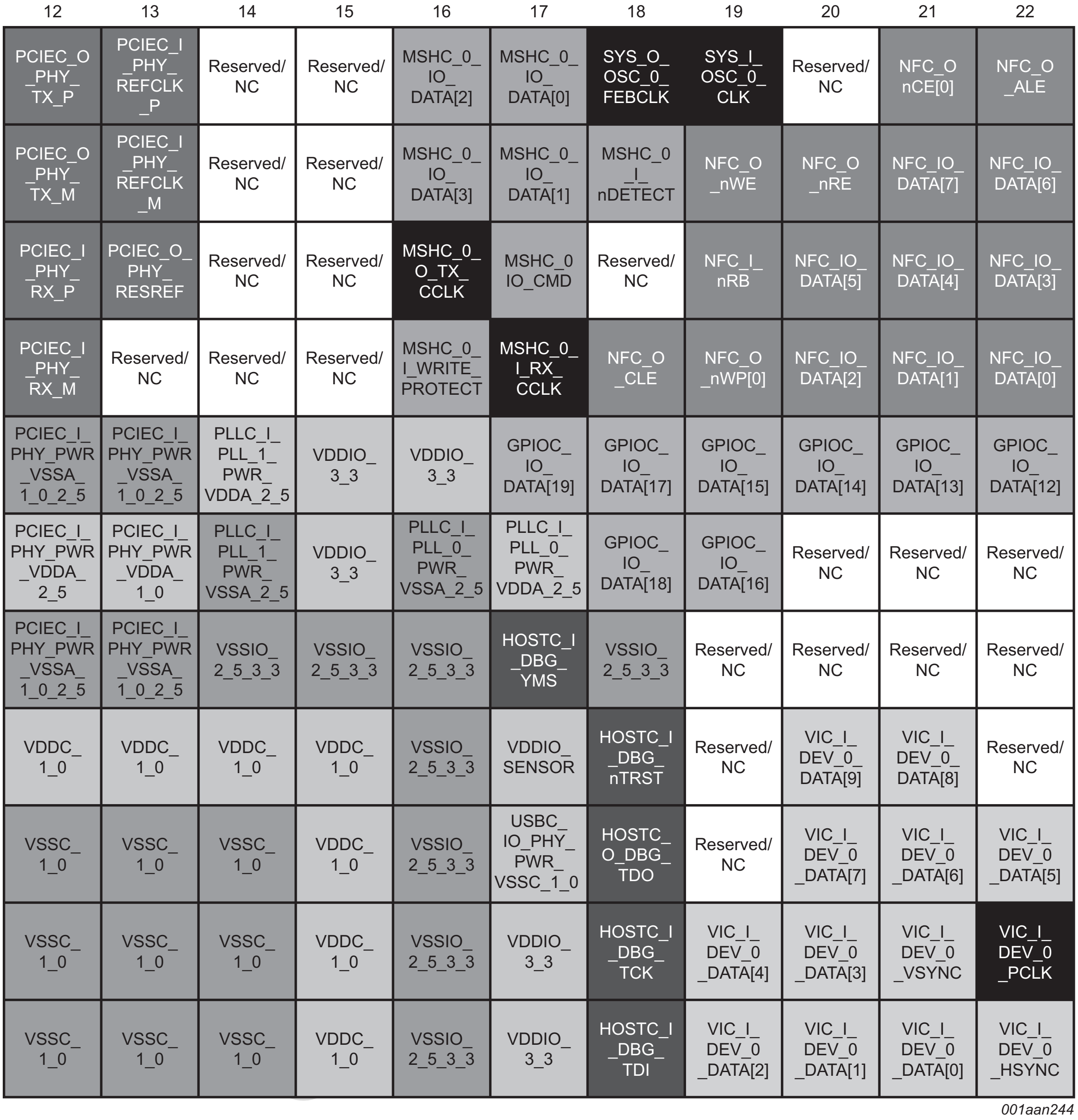
Remark: Pin Assignment is for ASC8848/49/50/51 M2 version. For ASC8848/49/50 M1 version refer Table 8

Fig 6. Top left view of an ASC8848 TFBGA- 484 pin assignment



12	13	14	15	16	17	18	19	20	21	22	
PCIEC_O_PHY_TX_P	PCIEC_I_PHY_REFCLK_P	Reserved/NC	Reserved/NC	MSHC_0_IO_DATA[2]	MSHC_0_IO_DATA[0]	SYS_O_OSC_0_FEBCLK	SYS_I_OSC_0_CLK	Reserved/NC	NFC_OnCE[0]	NFC_O_ALE	A
PCIEC_O_PHY_TX_M	PCIEC_I_PHY_REFCLK_M	Reserved/NC	Reserved/NC	MSHC_0_IO_DATA[3]	MSHC_0_IO_DATA[1]	MSHC_0_I_nDETECT	NFC_O_nWE	NFC_O_nRE	NFC_IO_DATA[7]	NFC_IO_DATA[6]	B
PCIEC_I_PHY_RX_P	PCIEC_O_PHY_RESREF	Reserved/NC	Reserved/NC	MSHC_0_O_TX_CCLK	MSHC_0 IO_CMD	Reserved/NC	NFC_I_nRB	NFC_IO_DATA[5]	NFC_IO_DATA[4]	NFC_IO_DATA[3]	C
PCIEC_I_PHY_RX_M	Reserved/NC	Reserved/NC	Reserved/NC	MSHC_0_I_WRITE_PROTECT	MSHC_0_I_RX_CCLK	NFC_O_CLE	NFC_O_nWP[0]	NFC_IO_DATA[2]	NFC_IO_DATA[1]	NFC_IO_DATA[0]	D
PCIEC_I_PHY_PWR_VSSA_1_0_2_5	PCIEC_I_PHY_PWR_VSSA_1_0_2_5	PLLC_I_PLL_1_PWR_VDDA_2_5	VDDIO_3_3	VDDIO_3_3	GPIOC_IO_DATA[19]	GPIOC_IO_DATA[17]	GPIOC_IO_DATA[15]	GPIOC_IO_DATA[14]	GPIOC_IO_DATA[13]	GPIOC_IO_DATA[12]	E
PCIEC_I_PHY_PWR_VDDA_2_5	PCIEC_I_PHY_PWR_VDDA_1_0	PLLC_I_PLL_1_PWR_VSSA_2_5	VDDIO_3_3	PLLC_I_PLL_0_PWR_VSSA_2_5	PLLC_I_PLL_0_PWR_VDDA_2_5	GPIOC_IO_DATA[18]	GPIOC_IO_DATA[16]	Reserved/NC	Reserved/NC	Reserved/NC	F
PCIEC_I_PHY_PWR_VSSA_1_0_2_5	PCIEC_I_PHY_PWR_VSSA_1_0_2_5	VSSIO_2_5_3_3	VSSIO_2_5_3_3	VSSIO_2_5_3_3	HOSTC_I_DBG_YMS	VSSIO_2_5_3_3	Reserved/NC	Reserved/NC	Reserved/NC	Reserved/NC	G
VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_SENSOR	HOSTC_I_DBG_nTRST	Reserved/NC	VIC_I_DEV_0_DATA[9]	VIC_I_DEV_0_DATA[8]	Reserved/NC	H
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	USBC_IO_PHY_PWR_VSSC_1_0	HOSTC_O_DBG_TDO	Reserved/NC	VIC_I_DEV_0_DATA[7]	VIC_I_DEV_0_DATA[6]	VIC_I_DEV_0_DATA[5]	J
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_3_3	HOSTC_I_DBG_TCK	VIC_I_DEV_0_DATA[4]	VIC_I_DEV_0_DATA[3]	VIC_I_DEV_0_VSYNC	VIC_I_DEV_0_PCLK	K
VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_3_3	HOSTC_I_DBG_TDI	VIC_I_DEV_0_DATA[2]	VIC_I_DEV_0_DATA[1]	VIC_I_DEV_0_DATA[0]	VIC_I_DEV_0_HSYNC	L

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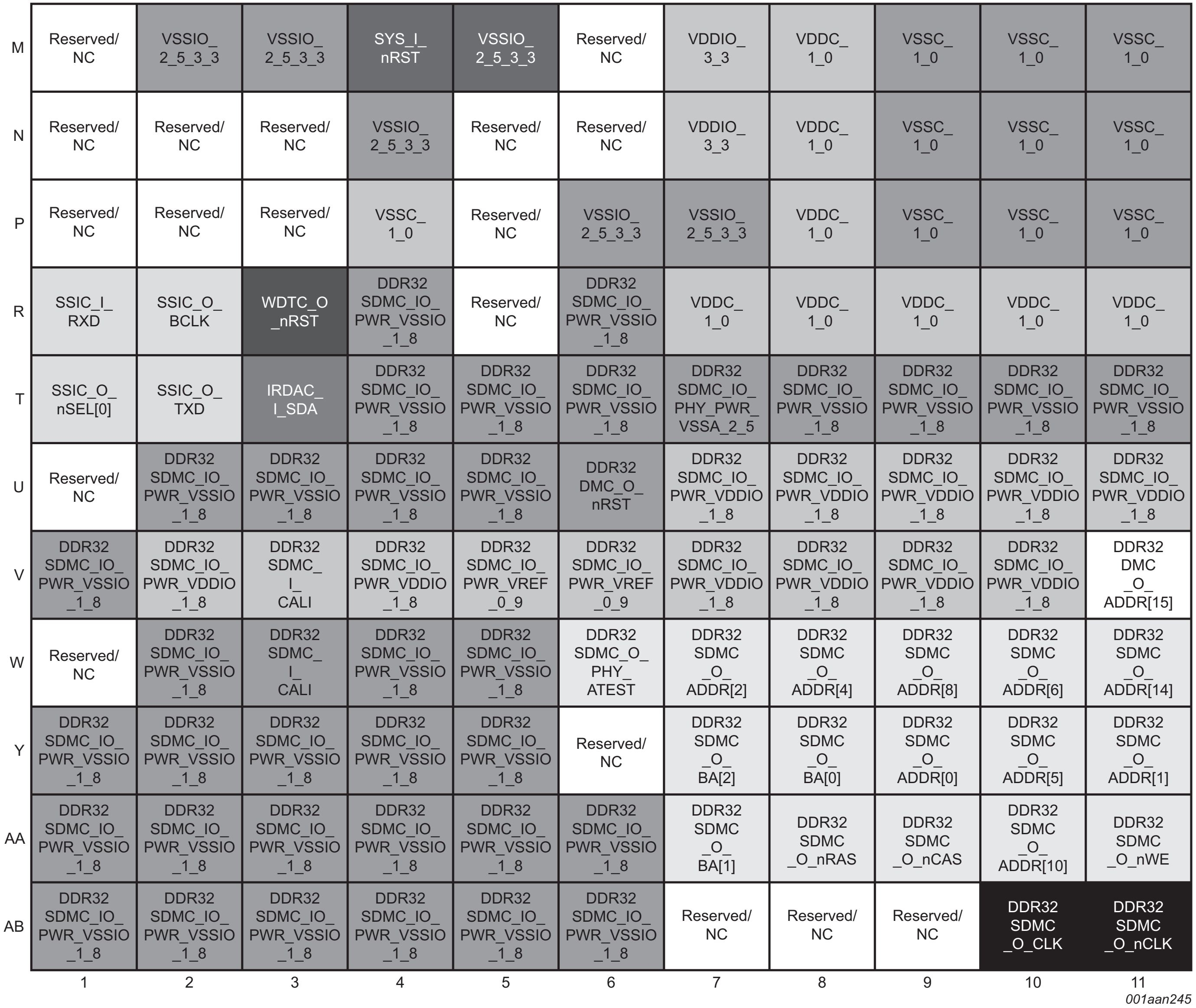
Remark: Pin Assignment is for ASC8848/49/50/51 M2 version. For ASC8848/49/50 M1 version refer Table 8

Fig 7. Top right view of an ASC8848 TFBGA - 484 Pin Assignment



M	Reserved/ NC	VSSIO_ 2_5_3_3	VSSIO_ 2_5_3_3	SYS_I_ nRST	VSSIO_ 2_5_3_3	Reserved/ NC	VDDIO_ 3_3	VDDC_ 1_0	VSSC_ 1_0	VSSC_ 1_0	VSSC_ 1_0
N	Reserved/ NC	Reserved/ NC	Reserved/ NC	VSSIO_ 2_5_3_3	Reserved/ NC	Reserved/ NC	VDDIO_ 3_3	VDDC_ 1_0	VSSC_ 1_0	VSSC_ 1_0	VSSC_ 1_0
P	Reserved/ NC	Reserved/ NC	Reserved/ NC	VSSC_ 1_0	Reserved/ NC	VSSIO_ 2_5_3_3	VSSIO_ 2_5_3_3	VDDC_ 1_0	VSSC_ 1_0	VSSC_ 1_0	VSSC_ 1_0
R	SSIC_I_ RXD	SSIC_O_ BCLK	WDTC_O _nRST	DDR32 SDMC_IO_ PWR_VSSIO _1_8	Reserved/ NC	DDR32 SDMC_IO_ PWR_VSSIO _1_8	VDDC_ 1_0	VDDC_ 1_0	VDDC_ 1_0	VDDC_ 1_0	VDDC_ 1_0
T	SSIC_O_ nSEL[0]	SSIC_O_ TXD	IRDAC_ I_SDA	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PHY_PWR_ VSSA_2_5	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8
U	Reserved/ NC	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 DMC_O_ nRST	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8
V	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_ I_ CALI	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VREF _0_9	DDR32 SDMC_IO_ PWR_VREF _0_9	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 SDMC_IO_ PWR_VDDIO _1_8	DDR32 DMC _O_ ADDR[15]
W	Reserved/ NC	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_ I_ CALI	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_O_ PHY_ ATEST	DDR32 SDMC _O_ ADDR[2]	DDR32 SDMC _O_ ADDR[4]	DDR32 SDMC _O_ ADDR[8]	DDR32 SDMC _O_ ADDR[6]	DDR32 SDMC _O_ ADDR[14]
Y	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	Reserved/ NC	DDR32 SDMC _O_ BA[2]	DDR32 SDMC _O_ BA[0]	DDR32 SDMC _O_ ADDR[0]	DDR32 SDMC _O_ ADDR[5]	DDR32 SDMC _O_ ADDR[1]
AA	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC _O_ BA[1]	DDR32 SDMC _O_nRAS	DDR32 SDMC _O_nCAS	DDR32 SDMC _O_ ADDR[10]	DDR32 SDMC _O_nWE
AB	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	DDR32 SDMC_IO_ PWR_VSSIO _1_8	Reserved/ NC	Reserved/ NC	Reserved/ NC	DDR32 SDMC _O_CLK	DDR32 SDMC _O_nCLK
	1	2	3	4	5	6	7	8	9	10	11

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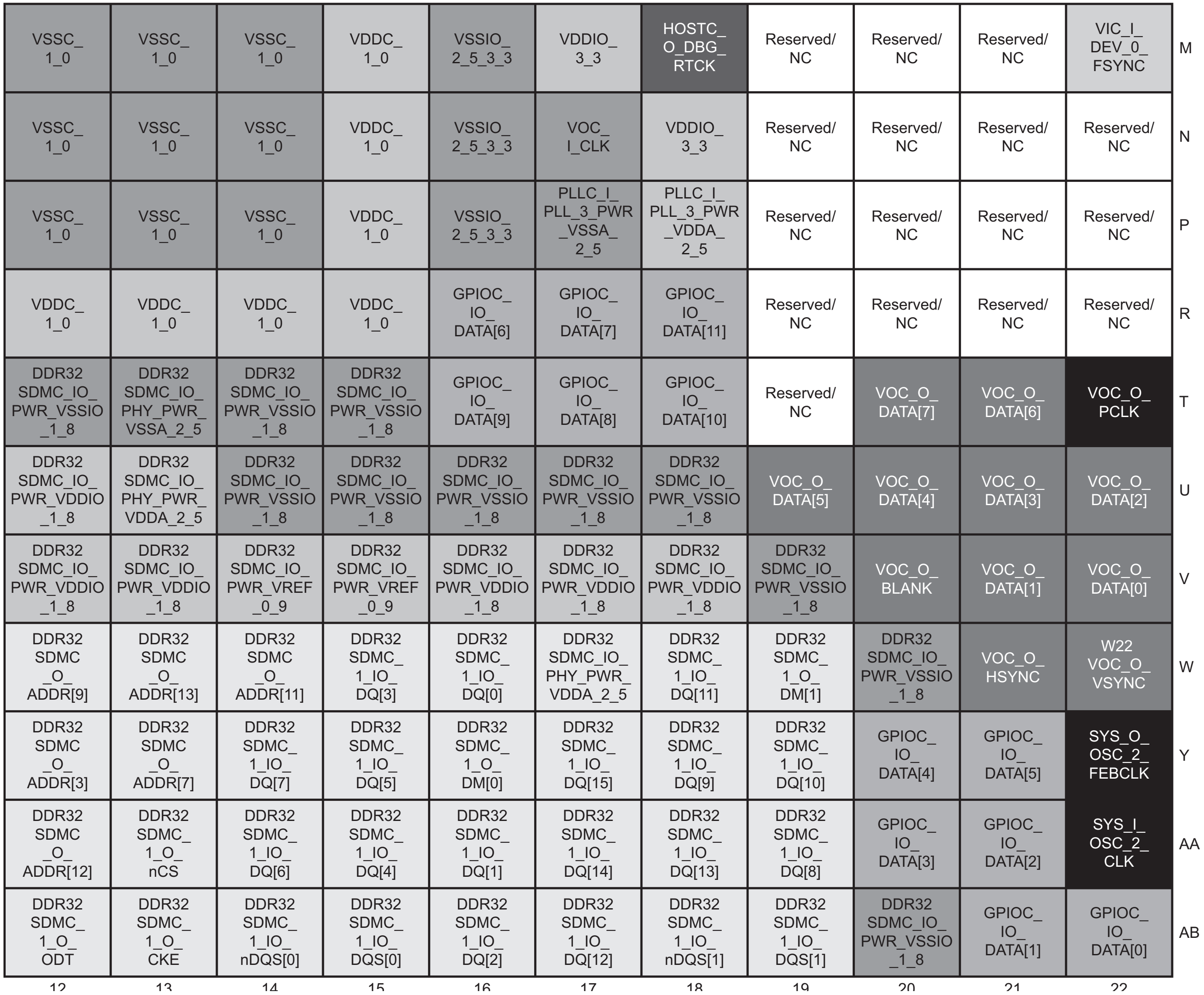
Remark: Remark: Pin Assignment is for ASC8848/49/50/51 M2 version. For ASC8848/49/50 M1 version refer Table 8

Fig 8. Bottom left view of an ASC8848 TFBGA- 484 pin assignment



	12	13	14	15	16	17	18	19	20	21	22
M	VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VDDIO_3_3	HOSTC_O_DBG_RTCK	Reserved/NC	Reserved/NC	Reserved/NC	VIC_I_DEV_0_FSYNC
N	VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	VOC_I_CLK	VDDIO_3_3	Reserved/NC	Reserved/NC	Reserved/NC	Reserved/NC
P	VSSC_1_0	VSSC_1_0	VSSC_1_0	VDDC_1_0	VSSIO_2_5_3_3	PLLC_I_PLL_3_PWR_VSSA_2_5	PLLC_I_PLL_3_PWR_VDDA_2_5	Reserved/NC	Reserved/NC	Reserved/NC	Reserved/NC
R	VDDC_1_0	VDDC_1_0	VDDC_1_0	VDDC_1_0	GPIOC_IO_DATA[6]	GPIOC_IO_DATA[7]	GPIOC_IO_DATA[11]	Reserved/NC	Reserved/NC	Reserved/NC	Reserved/NC
T	DDR32SDMC_IO_PWR_VSSIO_1_8	DDR32SDMC_IO_PHY_PWR_VSSA_2_5	DDR32SDMC_IO_PWR_VSSIO_1_8	DDR32SDMC_IO_PWR_VSSIO_1_8	GPIOC_IO_DATA[9]	GPIOC_IO_DATA[8]	GPIOC_IO_DATA[10]	Reserved/NC	VOC_O_DATA[7]	VOC_O_DATA[6]	VOC_O_PCLK
U	DDR32SDMC_IO_PWR_VDDIO_1_8	DDR32SDMC_IO_PHY_PWR_VDDA_2_5	DDR32SDMC_IO_PWR_VSSIO_1_8	DDR32SDMC_IO_PWR_VSSIO_1_8	DDR32SDMC_IO_PWR_VSSIO_1_8	DDR32SDMC_IO_PWR_VSSIO_1_8	DDR32SDMC_IO_PWR_VSSIO_1_8	VOC_O_DATA[5]	VOC_O_DATA[4]	VOC_O_DATA[3]	VOC_O_DATA[2]
V	DDR32SDMC_IO_PWR_VDDIO_1_8	DDR32SDMC_IO_PWR_VDDIO_1_8	DDR32SDMC_IO_PWR_VREF_0_9	DDR32SDMC_IO_PWR_VREF_0_9	DDR32SDMC_IO_PWR_VDDIO_1_8	DDR32SDMC_IO_PWR_VDDIO_1_8	DDR32SDMC_IO_PWR_VDDIO_1_8	DDR32SDMC_IO_PWR_VSSIO_1_8	VOC_O_BLANK	VOC_O_DATA[1]	VOC_O_DATA[0]
W	DDR32SDMC_O_ADDR[9]	DDR32SDMC_O_ADDR[13]	DDR32SDMC_O_ADDR[11]	DDR32SDMC_1_IO_DQ[3]	DDR32SDMC_1_IO_DQ[0]	DDR32SDMC_IO_PHY_PWR_VDDA_2_5	DDR32SDMC_1_IO_DQ[11]	DDR32SDMC_1_O_DM[1]	DDR32SDMC_IO_PWR_VSSIO_1_8	VOC_O_HSYNC	W22 VOC_O_VSYNC
Y	DDR32SDMC_O_ADDR[3]	DDR32SDMC_O_ADDR[7]	DDR32SDMC_1_IO_DQ[7]	DDR32SDMC_1_IO_DQ[5]	DDR32SDMC_1_O_DM[0]	DDR32SDMC_1_IO_DQ[15]	DDR32SDMC_1_IO_DQ[9]	DDR32SDMC_1_IO_DQ[10]	GPIOC_IO_DATA[4]	GPIOC_IO_DATA[5]	SYS_O_OSC_2_FEBCLK
AA	DDR32SDMC_O_ADDR[12]	DDR32SDMC_1_O_nCS	DDR32SDMC_1_IO_DQ[6]	DDR32SDMC_1_IO_DQ[4]	DDR32SDMC_1_IO_DQ[1]	DDR32SDMC_1_IO_DQ[14]	DDR32SDMC_1_IO_DQ[13]	DDR32SDMC_1_IO_DQ[8]	GPIOC_IO_DATA[3]	GPIOC_IO_DATA[2]	SYS_I_OSC_2_CLK
AB	DDR32SDMC_1_O_ODT	DDR32SDMC_1_O_CKE	DDR32SDMC_1_IO_nDQS[0]	DDR32SDMC_1_IO_DQS[0]	DDR32SDMC_1_IO_DQ[2]	DDR32SDMC_1_IO_DQ[12]	DDR32SDMC_1_IO_nDQS[1]	DDR32SDMC_1_IO_DQS[1]	DDR32SDMC_IO_PWR_VSSIO_1_8	GPIOC_IO_DATA[1]	GPIOC_IO_DATA[0]

Remark: Pin Assignment is for ASC8848/49/50/51 M2 version. For ASC8848/49/50 M1 version refer Table 8

Fig 9. Bottom right view of an ASC8848 TFBGA- 484 pin assignment

5.2 Pin description

Table 4. I/O functions

I/O function	Description
5VT	5 V - tolerant I/O
SMT	Schmitt trigger
I2P	Default 2 mA driving capability and can be programmed to 2 mA, 4 mA, 8 mA and 12 mA
I4P	Default 4 mA driving capability and can be programmed to 2 mA, 4 mA, 8 mA and 12 mA
I8P	Default 8mA driving capability and can be programmed to 2 mA, 4 mA, 8 mA and 12 mA
PD	Pulled down and can not be programmed.
PUDP	Pull-up disabled and can be programmed
PUEP	Pull-up enabled and can be programmed
PDDP	Pull-down disabled and can be programmed
PDEP	Pull-down enabled and can be programmed
OEDP	Output enable disabled and can be programmed
OEEP	Output enable enabled and can be programmed
IEEP	Input enable enabled and can be programmed
FSRP	Fast slew rate and can be programmed to slow

Table 5. Overview of ball map updates for ASC8848/49/50/51 M2 version and ASC8851

Ball	ASC8848/49/50 M1 version	ASC8848/49/50 M2 version and ASC8851
P4	SYS_I_GMAC_MODE_SEL	VSSC_1_0
R4	Reserved	DDR32SDMC_IO_PWR_VSSIO_1_8
M5	SYS_I_GMAC_TX_CLK_DIR	VSSIO_2_5_3_3
W6	DDR2SDMC_I_CMD_CALI	DDR32SDMC_O_PHY_ATEST
W17	DDR2SDMC_I_DATA_1_CALI	DDR32SDMC_IO_PHY_PWR_VDDA_2_5
W3	DDR2SDMC_I_DATA_0_CALI	DDR32SDMC_I_CALI
R7	DDR2SDMC_IO_PHY_PWR_VDDC_1_0	VDDC_1_0
T7	DDR2SDMC_IO_PHY_PWR_VSSC_1_0	DDR32SDMC_IO_PHY_PWR_VSSA_2_5
H6	USBC_IO_PHY_PWR_VSSC_1_0	USBC_IO_PHY_PWR_VSSA_2_5_3_3
J6	USBC_IO_PHY_PWR_VSSA_2_5_3_3	USBC_IO_PHY_PWR_VSSC_1_0
B11	SYS_O_MON_CLK[1][1]	SYS_O_MON_CLK[1][1]
V11	DDR2DMC_O_PHY_ATEST	DDR32DMC_O_ADDR[15]
U6	DDR2SDMC_IO_PWR_VSSIO_1_8	DDR32DMC_O_nRST
N17	VSSIO_2_5_3_3	VOC_I_CLK
H17	VDDIO_3_3	VDDIO_SENSOR

[1] Refer to Table 7 for change

Table 6. ASC8849/50/51 SoC signal descriptions

Pin name	BGA ball	Type	Function	Descriptions
Global signals				
SYS_I_OSC_0_CLK	A19	I	-	System clock 0 from oscillator or crystal (25 MHz). The feedback resistor, Rf is built in and no external resistor is required.
SYS_I_OSC_1_CLK	B1	I	-	System clock 1 from oscillator or crystal. (18.432 MHz)
SYS_I_OSC_2_CLK	AA22	I	-	System clock 2 from oscillator or crystal. (24 MHz) The feedback resistor, Rf, is built in and no external resistor is required.
SYS_I_nRST	M4	I	-	Active-low global reset input signal.
SYS_I_BOOT_MODE_SEL[0]	K4	I	-	Boot mode select. Refer to section Boot Modes 6.2.
SYS_I_BOOT_MODE_SEL[1]	L4	I	-	Boot mode select. Refer to section Boot Modes 6.2.
SYS_I_GMAC_MODE_SEL	P4	I	-	ASC8849/50 M1 version: RGMII/GMII mode select. 1: 2.5 V RGMII mode. 0: 3.3 V GMII mode.
VSSC_1_0		I	-	ASC8849/50 M2 version and 8851: Core ground supply
SYS_I_GMAC_TX_CLK_DIR	M5	I	-	ASC8849/50 M1 version: Ethernet MAC TX clock direction. 1: Input from the external Ethernet PHY. 0: Output to the external Ethernet PHY.
VSSIO_2_5_3_3		I	-	ASC8849/50 M2 version and 8851: I/O ground supply
SYS_O_OSC_0_FEBCLK	A18	O	-	Feedback crystal output of system clock 0.
SYS_O_OSC_1_FEBCLK	C1	O	-	Feedback crystal output of system clock 1.
SYS_O_OSC_2_FEBCLK	Y22	O	-	Feedback crystal output of system clock 2.
SYS_O_MON_CLK[0]	C11	O	OEEP, I2P	• Monitor clock 0. • Connect to MSHC_0_I_RX_CCLK if MSHC 0 interface is enabled.
SYS_O_MON_CLK[1]	B11	O	-	ASC8849/50 M1 version: Monitor clock 1. Connect to MSHC_1_I_RX_CCLK if MSHC 1 interface is enabled or use 90° rotated GMAC_O_TX_CLK
		O	-	ASC8849/50 M2 version and 8851: Monitor clock 1. Connect to MSHC_1_I_RX_CCLK
WDTC_O_nRST	R3	O	OEEP, PUEP, I4P	System output reset.
DDR-II/III SDRAM interface				
DDR32SDMC_O_CLK	AB10	O	-	DDR-II/III SDRAM common output clock.
DDR32SDMC_O_nCLK	AB11	O	-	DDR-II/III SDRAM common complementary output clock.

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
DDR32SDMC_IO_PWR_VSSIO_1_8	U6	G	-	ASC8849/50 M1 version: DDR-II/III SDRAM I/O ground supply.
DDR32DMC_O_NRST		G	-	ASC8849/50 M2 version and 8851: DDR-III SDRAM Reset. For DDR-II could be left floating
DDR32SDMC_O_nRAS	AA8	O	-	Active-low DDR-II/III SDRAM common row address strobe signal.
DDR32SDMC_O_nCAS	AA9	O	-	Active-low DDR-II/III SDRAM common column address strobe signal.
DDR32SDMC_O_nWE	AA11	O	-	Active-low DDR-II/III SDRAM common write enable signal.
DDR32SDMC_O_ADDR[0]	Y9	O	-	DDR-II/III SDRAM common address bus.
DDR32SDMC_O_ADDR[1]	Y11	O	-	-
DDR32SDMC_O_ADDR[2]	W7	O	-	-
DDR32SDMC_O_ADDR[3]	Y12	O	-	-
DDR32SDMC_O_ADDR[4]	W8	O	-	-
DDR32SDMC_O_ADDR[5]	Y10	O	-	-
DDR32SDMC_O_ADDR[6]	W10	O	-	-
DDR32SDMC_O_ADDR[7]	Y13	O	-	-
DDR32SDMC_O_ADDR[8]	W9	O	-	-
DDR32SDMC_O_ADDR[9]	W12	O	-	-
DDR32SDMC_O_ADDR[10]	AA10	O	-	-
DDR32SDMC_O_ADDR[11]	W14	O	-	-
DDR32SDMC_O_ADDR[12]	AA12	O	-	-
DDR32SDMC_O_ADDR[13]	W13	O	-	-
DDR32SDMC_O_ADDR[14]	W11	O	-	-
DDR2SDMC_O_PHY_ATEST	V11	O	-	ASC8849/50 M1 version: PLL analog test output.
DDR32SDMC_O_ADDR[15]		O	-	ASC8849/50 M2 version and 8851: DDR-II/III SDRAM common address bus bit15. Allows connecting higher capacity DRAM compared to M1 version otherwise could be left floating
DDR32SDMC_IO_PWR_VDDIO_1_8	U7, U8, U9, U10, U11, U12, V2, V3, V4, V7 V8, V9, V10, V12, , V16, V17, V18	P	-	DDR-II/III SDRAM I/O power supply (1.8/1.5 V).
DDR32SDMC_O_BA[0]	Y8	O	-	DDR-II/III SDRAM common internal bank select signals.
DDR32SDMC_O_BA[1]	AA7	O	-	-
DDR32SDMC_O_BA[2]	Y7	O	-	-

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
DDR2SDMC_I_CMD_CALI	W6	I	-	ASC8849/50 M1 version: PVT calibration for DDR-II SDRAM common command signal. Connected through an external resistor, 240 Ω (1 %), to 1.8 V.
DDR32SDMC_O_PHY_ATEST		O	-	ASC8849/50 M2 version and 8851: PLL analog test output.
DDR2SDMC_I_DATA_0_CALI	W3	I	-	ASC8849/50 M1 version: PVT calibration for DDR-II SDRAM 0 data bus. Connected through an external resistor, 240 Ω (1 %), to 1.8 V
DDR32SDMC_I_CALI		-	-	ASC8849/50 M2 version and 8851: PVT Calibration for DDR-II/III data and command. Connected through an external resistor, 240 Ω (1 %) to ground
DDR2SDMC_I_DATA_1_CALI	W17	I	-	ASC8849/50 M1 version: PVT calibration for DDR-II I SDRAM 1 data bus. Connected through an external resistor, 240 Ω (1 %), to 1.8 V
DDR32SDMC_IO_PHY_PWR_VDDA_2_5		I	-	ASC8849/50 M2 version and 8851: DDR-II/III PHY analog power supply (2.5 V).
DDR32SDMC_0_IO_DQ[0]	Y4	I/O	-	DDR-II/III SDRAM 0 read/write data bus.
DDR32SDMC_0_IO_DQ[1]	AA5	I/O	-	-
DDR32SDMC_0_IO_DQ[2]	Y5	I/O	-	-
DDR32SDMC_0_IO_DQ[3]	AA6	I/O	-	-
DDR32SDMC_0_IO_DQ[4]	AB4	I/O	-	-
DDR32SDMC_0_IO_DQ[5]	W5	I/O	-	-
DDR32SDMC_0_IO_DQ[6]	AA4	I/O	-	-
DDR32SDMC_0_IO_DQ[7]	W4	I/O	-	-
DDR32SDMC_0_IO_DQ[8]	Y2	I/O	-	-
DDR32SDMC_0_IO_DQ[9]	AA1	I/O	-	-
DDR32SDMC_0_IO_DQ[10]	Y3	I/O	-	-
DDR32SDMC_0_IO_DQ[11]	AA2	I/O	-	-
DDR32SDMC_0_IO_DQ[12]	AA3	I/O	-	-
DDR32SDMC_0_IO_DQ[13]	W2	I/O	-	-
DDR32SDMC_0_IO_DQ[14]	AB1	I/O	-	-
DDR32SDMC_0_IO_DQ[15]	Y1	I/O	-	-
DDR32SDMC_0_IO_DQS[0]	AB5	I/O	-	DDR-II/III SDRAM 0 data strobe signals. It is edge-aligned with write data and centered in read data. It must be connected on the board to a pull-down resistor, 430 Ω to 560 Ω (5 %). The resistor must be placed on the board within 0.3 inches of the SoC. DQS[0]: for DQ[7:0] DQS[1]: for DQ[15:8]
DDR32SDMC_0_IO_DQS[1]	AB2	I/O	-	

Table 6. ASC8849/50/51 SoC signal descriptions *...continued*

Pin name	BGA ball	Type	Function	Descriptions
DDR32SDMC_0_IO_nDQS[0]	AB6	I/O	-	DDR-II/III SDRAM 0 complementary data strobe signals for each byte of the data bus. It must be connected on the board to a pull-up resistor, 430 Ω to 560 Ω (5 %). The resistor must be placed on the board within 0.3 inches of the SoC nDQS[0]: for DQ[7:0] nDQS[1]: for DQ[15:8]
DDR32SDMC_0_IO_nDQS[1]	AB3	I/O	-	
DDR32SDMC_0_O_DM[0]	Y6	O	-	DDR-II/III SDRAM 0 output data mask signals. DM[0]: for DQ[7:0] DM[1]: for DQ[15:8].
DDR32SDMC_0_O_DM[1]	W1	O	-	-
DDR32SDMC_0_O_CKE	AB9	O	-	DDR-II/III SDRAM clock enable signal.
DDR32SDMC_0_O_nCS	AB7	O	-	Active-low DDR-II SDRAM 0 chip select signal.
DDR32SDMC_0_O_ODT	AB8	O	-	DDR-II/III SDRAM 0 on-die termination signal.
DDR32SDMC_1_IO_DQ[0]	W16	I/O	-	DDR-II/III SDRAM 1 read/write data bus.
DDR32SDMC_1_IO_DQ[1]	AA16	I/O	-	-
DDR32SDMC_1_IO_DQ[2]	AB16	I/O	-	-
DDR32SDMC_1_IO_DQ[3]	W15	I/O	-	-
DDR32SDMC_1_IO_DQ[4]	AA15	I/O	-	-
DDR32SDMC_1_IO_DQ[5]	Y15	I/O	-	-
DDR32SDMC_1_IO_DQ[6]	AA14	I/O	-	-
DDR32SDMC_1_IO_DQ[7]	Y14	I/O	-	-
DDR32SDMC_1_IO_DQ[8]	AA19	I/O	-	-
DDR32SDMC_1_IO_DQ[9]	Y18	I/O	-	-
DDR32SDMC_1_IO_DQ[10]	Y19	I/O	-	-
DDR32SDMC_1_IO_DQ[11]	W18	I/O	-	-
DDR32SDMC_1_IO_DQ[12]	AB17	I/O	-	-
DDR32SDMC_1_IO_DQ[13]	AA18	I/O	-	-
DDR32SDMC_1_IO_DQ[14]	AA17	I/O	-	-
DDR32SDMC_1_IO_DQ[15]	Y17	I/O	-	-
DDR32SDMC_1_IO_DQS[0]	AB15	I/O	-	DDR-II/DDRDDR-II/III-III SDRAM 1 data strobe signals. It is edge-aligned with write data and centered in read data. It must be connected on the board to a pull-down resistor, 430~560? (?15%). The resistor must be placed on the board within 0.3 inches of the SoC. DQS[0]: for DQ[7:0] DQS[1]: for DQ[15:8] -
DDR32SDMC_1_IO_DQS[1]	AB19		-	

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
DDR32SDMC_1_IO_nDQS[0]	AB14	I/O	-	DDR-II/III SDRAM 1 complementary data strobe signals. It is edge-aligned with write data and centered in read data. It must be connected on the board to a pull-down resistor, 430~560? (?15%). The resistor must be placed on the board within 0.3 inches of the SoC. nDQS[0]: for DQ[7:0] nDQS[1]: for DQ[15:8] -
DDR32SDMC_1_IO_nDQS[1]	AB18	I/O	-	
DDR32SDMC_1_O_DM[0]	Y16	O	-	DDR-II/III SDRAM 1 output data mask signals. DM[0]: for DQ[7:0] DM[1]: for DQ[15:8].
DDR32SDMC_1_O_DM[1]	W19	O	-	-
DDR32SDMC_1_O_CKE	AB13	O	-	DDR-II/III SDRAM 1 clock enable signal.
DDR32SDMC_1_O_nCS	AA13	O	-	Active-low DDR-II/III 1 SDRAM chip select signal.
DDR32SDMC_1_O_ODT	AB12	O	-	DDR-II/III SDRAM 1 on-die termination signal.
GPIO interface				
GPIOC_IO_DATA[0]	AB22	I/O	SMT, I8P, PUDP, PDDP, OEEP	General-purpose I/O data signals. Upon reset, GPIOC_IO_DATA[7:0] is set output mode and drives low; GPIOC_IO_DATA[19:8] is set input mode.
GPIOC_IO_DATA[1]	AB21	I/O	-	
GPIOC_IO_DATA[2]	AA21	I/O	-	
GPIOC_IO_DATA[3]	AA20	I/O	-	
GPIOC_IO_DATA[4]	Y20	I/O	-	
GPIOC_IO_DATA[5]	Y21	I/O	-	-
GPIOC_IO_DATA[6]	R16	I/O	-	-
GPIOC_IO_DATA[7]	R17	I/O	-	-
GPIOC_IO_DATA[8]	T17	I/O	SMT, I8P, PUDP, PDDP, OEDP	-
GPIOC_IO_DATA[9]	T16	I/O	-	-
GPIOC_IO_DATA[10]	T18	I/O	-	-
GPIOC_IO_DATA[11]	R18	I/O	-	-
GPIOC_IO_DATA[12]	E22	I/O	-	-
GPIOC_IO_DATA[13]	E21	I/O	-	-
GPIOC_IO_DATA[14]	E20	I/O	-	-
GPIOC_IO_DATA[15]	E19	I/O	-	-
GPIOC_IO_DATA[16]	F19	I/O	-	-
GPIOC_IO_DATA[17]	E18	I/O	-	-
GPIOC_IO_DATA[18]	F18	I/O	-	-

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
GPIOC_IO_DATA[19]	E17	I/O	-	-
JTAG interface (ARM926EJ)				
HOSTC_I_DBG_nTRST	H18	I	SMT, PUEP	Active low reset for internal synchronizer.
HOSTC_I_DBG_TCK	K18	I	SMT, IEEP, PUEP	JTAG clock input.
HOSTC_I_DBG_TMS	G17	I	SMT, PUEP	JTAG mode selection input signal.
HOSTC_I_DBG_TDI	L18	I	-	JTAG data input signal.
HOSTC_O_DBG_RTCK	M18	O	OEEP, PDEP, I4P	JTAG output clock signal.
HOSTC_O_DBG_TDO	J18	O	OEDP, PUEP, I4P	JTAG data output signal.
IrDA interface				
IRDAC_I_SDA	T3	I	-	IrDA input.
I2S interface				
I2SSC_0_I_BCLK	J1	I	IEEP, SMT	I^{2}S serial clock.
I2SSC_0_I_RXD	K3	I	-	I^{2}S receive data input signal.
I2SSC_0_I_WS	J2	I	-	I^{2}S frame synchronization signal.
I2SSC_0_O_TXD	J3	O	OEEP, I4P	I^{2}S transmit data output signal.
I2SSC_1_I_BCLK	K2	I	IEEP, SMT	I^{2}S serial clock.
I2SSC_1_I_RXD	L3	I	-	I^{2}S receive data input signal.
I2SSC_1_I_WS	K1	I	-	I^{2}S frame synchronization signal.
I2SSC_2_I_BCLK	M3	I	IEEP, SMT	I^{2}S serial clock.
I2SSC_2_I_RXD	M2	I	-	I^{2}S receive data input signal.
I2SSC_2_I_WS	L2	I	-	I^{2}S frame synchronization signal.
I2SSC_3_I_BCLK	N3	I	IEEP, SMT	I^{2}S serial clock.
I2SSC_3_I_RXD	N1	I	-	I^{2}S receive data input signal.
I2SSC_3_I_WS	N2	I	-	I^{2}S frame synchronization signal.
I2SSC_4_I_BCLK	P3	I	IEEP, SMT	I^{2}S serial clock.
I2SSC_4_I_RXD	P1	I	-	I^{2}S receive data input signal.
I2SSC_4_I_WS	P2	I	-	I^{2}S frame synchronization signal.
I2SSC_O_RX_MCLK	M1	O	OEEP, I4P	I^{2}S master clock output.
I2SSC_O_TX_MCLK	L1	O	-	I^{2}S master clock output.
10/100/1000 Ethernet MAC interface				
GMAC_I_RX_CLK	A5	I	-	Receive clock signal.
GMAC_I_TX_CLK	A7	I	-	MIII input transmit clock signal.
GMAC_I_RXDV	D8	I	-	MII/GMII: Receive data valid signal. RGMII: Receive control signal.
GMAC_I_RXER	D9	I	-	MII/GMII receive error signal.
GMAC_I_RXD[0]	B7	I	-	Receive data bus.
GMAC_I_RXD[1]	C7	I	-	MII/RGMII: [3:0]

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
GMAC_I_RXD[2]	A6	I	-	GMII: [7:0]
GMAC_I_RXD[3]	B6	I	-	-
GMAC_I_RXD[4]	C6	I	-	-
GMAC_I_RXD[5]	B5	I	-	-
GMAC_I_RXD[6]	A4	I	-	-
GMAC_I_RXD[7]	B4	I	-	-
GMAC_I_CRS	C5	I	-	MII/GMIII carrier sense signal.
GMAC_I_COL	D5	I	-	MII/GMII collision detected signal.
GMAC_IO_MD	D6	I/O	OEDP, FSRP	Management data.
GMAC_O_TX_CLK	A9	O	FSRP	GMII/RGMII output transmit clock signal. This clock is used only when TX clock is an input signal to the PHY.
GMAC_O_MDC	D7	O	OEEP, FSRP	Management data clock signal.
GMAC_O_TXEN	D11	O	-	GMII: Transmit data enable signal. RGMII: Transmit control signal
GMAC_O_TXER	D10	O	-	MGI/GMII transmit error signal.
GMAC_O_TXD[0]	A10	O	-	Transmit data bus.
GMAC_O_TXD[1]	B10	O	-	MII/RGMII: [3:0]
GMAC_O_TXD[2]	C10	O	-	GMII: [7:0]
GMAC_O_TXD[3]	B9	O	-	-
GMAC_O_TXD[4]	C9	O	-	-
GMAC_O_TXD[5]	A8	O	-	-
GMAC_O_TXD[6]	B8	O	-	-
GMAC_O_TXD[7]	C8	O	-	-
Synchronous serial interface				
SSIC_I_RXD	R1	I	-	SSI receive data signal.
SSIC_O_BCLK	R2	O	OEEP, I4P	SSI serial clock output.
SSIC_O_TXD	T2	O	OEDP, I4P	SSI transmit data signal.
SSIC_O_nSEL[0]	T1	O	OEEP, I4P, PUEP	SSI slave selection signal.
SSIC_O_nSEL[1]	U1	O	-	-
Mobile storage host control interface				
MSHC_0_I_nDETECT	B18	I	PUEP	Card detect signal.
MSHC_0_I_RX_CCLK	D17	I	IEEP	Card input sampling clock.
MSHC_0_I_WRITE_PROTECT	D16	I	PUEP	Card write protect signal.
MSHC_0_IO_CMD	C17	I/O	OEDP, SMT, PUEP, I8P	Card command signal.
MSHC_0_IO_DATA[0]	A17	I/O	-	Card data signals.
MSHC_0_IO_DATA[1]	B17	I/O	-	-
MSHC_0_IO_DATA[2]	A16	I/O	-	-

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
MSHC_0_IO_DATA[3]	B16	I/O	-	-
MSHC_0_O_TX_CCLK	C16	O	OEEP, I8P	Card clock.
MSHC_1_I_nDETECT	C14	I	PUEP	Card detect signal.
MSHC_1_I_RX_CCLK	D14	I	IEEP	Card input sampling clock.
MSHC_1_I_WRITE_PROTECT	D13	I	PUEP	Card write protect signal.
MSHC_1_IO_CMD	D15	I/O	OEDP, SMT, PUEP, I8P	Card command signal.
MSHC_1_IO_DATA[0]	A15	I/O	-	Card data signals.
MSHC_1_IO_DATA[1]	A14	I/O	-	-
MSHC_1_IO_DATA[2]	B15	I/O	-	-
MSHC_1_IO_DATA[3]	B14	I/O	-	-
MSHC_1_O_TX_CCLK	C15	O	OEEP, I8P	Card clock.
NAND FLASH interface				
NFC_I_nRB	C19	I	SMT, PUEP	NAND FLASH read/busy signal.
NFC_IO_DATA[0]	D22	I/O	OEDP, SMT, PUEP	NAND FLASH data signals.
NFC_IO_DATA[1]	D21	I/O	-	-
NFC_IO_DATA[2]	D20	I/O	-	-
NFC_IO_DATA[3]	C22	I/O	-	-
NFC_IO_DATA[4]	C21	I/O	-	-
NFC_IO_DATA[5]	C20	I/O	-	-
NFC_IO_DATA[6]	B22	I/O	-	-
NFC_IO_DATA[7]	B21	I/O	-	-
NFC_O_ALE	A22	O	OEEP, I4P	NAND FLASH address latch enable signal.
NFC_O_CLE	D18	O		NAND FLASH command latch enable signal.
NFC_O_nCE[0]	A21	O	OEEP, PUEP, I4P	NAND FLASH chip enable signals.
NFC_O_nCE[1]	A20	O	-	-
NFC_O_nRE	B20	O		NAND FLASH read enable signal.
NFC_O_nWE	B19	O		NAND FLASH write enable signal.
NFC_O_nWP[0]	D19	O		NAND FLASH write protect signals.
NFC_O_nWP[1]	C18	O	-	-
UART (modem control) interface				
UARTC_0_I_SDA	A1	I	-	Serial data input for UART0.
UARTC_0_I_nCTS	B3	I	-	Clear to send signal for UART0.
UARTC_0_I_nDSR	C3	I	-	Data set ready signal for UART0.
UARTC_0_I_nRI	C2	I	-	Ring indicator signal for UART0.
UARTC_0_I_nDCD	B2	I	-	Data carrier detect signal for UART0.
UARTC_0_IO_nRTS	C4	I/O	OEDP, SMT, I8P	Request to send signal for UART0.

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Table 6. ASC8849/50/51 SoC signal descriptions *...continued*

Pin name	BGA ball	Type	Function	Descriptions
UARTC_0_IO_nDTR	A3	I/O	OEDP, SMT, I8P	Data terminal ready signal for UART0.
UARTC_0_O_SDA	A2	O	OEDP, PUEP, I8P	Serial data output for UART0.
UARTC_1_I_SDA	D3	I	-	Serial data input for UART1.
UARTC_1_I_nCTS	F3	I	-	Clear to send signal for UART1.
UARTC_1_I_nDSR	E2	I	-	Data set ready signal for UART1.
UARTC_1_I_nRI	F2	I	-	Ring indicator signal for UART1.
UARTC_1_I_nDCD	E4	I	-	Data carrier detect signal for UART1.
UARTC_1_IO_nRTS	F4	I/O	OEDP, SMT, I8P	Request to send signal for UART1.
UARTC_1_IO_nDTR	D4	I/O	OEDP, SMT, I8P	Data terminal ready signal for UART1.
UARTC_1_O_SDA	E3	O	OEDP, PUEP, I8P	Serial data output for UART1.
UARTC_2_I_SDA	D2	I	-	Serial data input for UART2.
UARTC_2_O_SDA	D1	O	OEEP, PUEP, I8P	Serial data output for UART2.
UARTC_3_I_SDA	G4	I	-	Serial data input for UART3.
UARTC_3_O_SDA	H4	O	OEEP, PUEP, I8P	Serial data output for UART3.
Video input interface				
VIC_I_DEV_0_PCLK	K22	I	IEEP, SMT	Device 0 pixel clock input.
VIC_I_DEV_0_HSYNC	L22	I	SMT	Device 0 horizontal synchronization (line valid) signal.
VIC_I_DEV_0_VSYNC	K21	I	-	Device 0 vertical synchronization (frame valid) signal.
VIC_I_DEV_0_FSYNC	M22	I	-	Device 0 field signal.
VIC_I_DEV_0_DATA[0]	L21	I	-	Device 0 video input data bus.
VIC_I_DEV_0_DATA[1]	L20	I	-	-
VIC_I_DEV_0_DATA[2]	L19	I	-	-
VIC_I_DEV_0_DATA[3]	K20	I	-	-
VIC_I_DEV_0_DATA[4]	K19	I	-	-
VIC_I_DEV_0_DATA[5]	J22	I	-	-
VIC_I_DEV_0_DATA[6]	J21	I	-	-
VIC_I_DEV_0_DATA[7]	J20	I	-	-
VIC_I_DEV_1_PCLK	F22	I	IEEP, SMT	Device 1 pixel clock input. Unused when configured as one 16-bit device.
VIC_I_DEV_1_HSYNC	G22	I	SMT	Device 1 horizontal synchronization (line valid) signal. Unused when configured as one 16-bit device.
VIC_I_DEV_1_VSYNC	G21	I	-	Device 1 vertical synchronization (frame valid) signal. Unused when configured as one 16-bit device.

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
VIC_I_DEV_1_FSYNC	H22	I	-	Device 1 field signal. Unused when configured as one 16-bit device.
VIC_I_DEV_1_DATA[0] / VIC_I_DEV_0_DATA[8]	H21	I	-	Device 0 video input data bus [15:8] when configured as one 16-bit device.
VIC_I_DEV_1_DATA[1]/ VIC_I_DEV_0_DATA[9]	H20	I	-	Device 1 video input data bus when configured as two 8-bit devices.
VIC_I_DEV_1_DATA[2]/ VIC_I_DEV_0_DATA[10]	J19	I	-	
VIC_I_DEV_1_DATA[3]/ VIC_I_DEV_0_DATA[11]	H19	I	-	
VIC_I_DEV_1_DATA[4]/ VIC_I_DEV_0_DATA[12]	G20	I	-	
VIC_I_DEV_1_DATA[5]/ VIC_I_DEV_0_DATA[13]	G19	I	-	
VIC_I_DEV_1_DATA[6]/ VIC_I_DEV_0_DATA[14]	F21	I	-	
VIC_I_DEV_1_DATA[7]/ VIC_I_DEV_0_DATA[15]	F20	I	-	-
Video output Interface				
VOC_O_PCLK	T22	O	OEEP, FSRP, I8P	Pixel clock output.
VSSIO_2_5_3_3	N17	-	-	ASC8849/50 M1 version: I/O ground supply
VOC_I_CLK		-	-	ASC8849/50 M2 version and 8851: Optional alternate clock source for VOC PLL
VOC_O_VSYNC	W22	O	-	Vertical synchronization (frame valid) signal.
VOC_O_HSYNC	W21	O	-	Horizontal synchronization (line valid) signal.
VOC_O_BLANK	V20	O	-	Blanking signal or data enable (DE) signal.
VOC_O_DATA[0]	V22	O	-	Video output data bus
VOC_O_DATA[1]	V21	O	-	-
VOC_O_DATA[2]	U22	O	-	-
VOC_O_DATA[3]	U21	O	-	-
VOC_O_DATA[4]	U20	O	-	-
VOC_O_DATA[5]	U19	O	-	-
VOC_O_DATA[6]	T21	O	-	-
VOC_O_DATA[7]	T20	O	-	-
VOC_O_DATA[8]	T19	O	-	-
VOC_O_DATA[9]	R22	O	-	-
VOC_O_DATA[10]	R21	O	-	-
VOC_O_DATA[11]	R20	O	-	-
VOC_O_DATA[12]	R19	O	-	-
VOC_O_DATA[13]	P22	O	-	-
VOC_O_DATA[14]	P21	O	-	-
VOC_O_DATA[15]	P20	O	-	-
VOC_O_DATA[16]	P19	O	-	-

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
VOC_O_DATA[17]	N22	O	-	-
VOC_O_DATA[18]	N21	O	-	-
VOC_O_DATA[19]	N20	O	-	-
VOC_O_DATA[20]	N19	O	-	-
VOC_O_DATA[21]	M21	O	-	-
VOC_O_DATA[22]	M20	O	-	-
VOC_O_DATA[23]	M19	O	-	-
Universal serial bus (USB) interface				
USBC_I_PHY_ID	H3	I	-	USB mini-receptacle identifier. The ID detection circuitry can differentiate the following conditions: ID pin floating (>100 KΩ) ID pin shorted to ground (<10 Ω)
USBC_IO_PHY_DP	G1	I/O	5VT	USB differential data signal, D+.
USBC_IO_PHY_DM	F1	I/O	5VT	USB differential data signal, D-.
USBC_IO_PHY_REXT_RKELVIN	J4	I/O	-	USB external resistor 43.2 Ω (1 %) connection to ground for bias current in USB 2.0 PHY.
USBC_IO_PHY_VBUS	H2	I/O	5VT	USB 5V power supply pin.
USBC_IO_PHY_ATEST	G2	I/O	-	Analog test point for internal analog voltage level measurement.
USBC_O_DRV_VBUS	G3	O	OEEP, I4P	Control off-chip charge pump. 0: Do not drive VBUS 1: Drive VBUSPCI Express x1 Interface
PCI express x1 interface				
PCIEC_I_PHY_REFCLK_M	B13	I	-	Differential reference clock input, 100 MHz.
PCIEC_I_PHY_REFCLK_P	A13	I	-	Differential reference clock input, 100 MHz.
PCIEC_I_PHY_RX_M	D12	I	-	High-speed differential receive pair.
PCIEC_I_PHY_RX_P	C12	I	-	High-speed differential receive pair.
PCIEC_O_PHY_TX_M	B12	O	-	High-speed differential transmit pair.
PCIEC_O_PHY_TX_P	A12	O	-	High-speed differential transmit pair.
PCIEC_O_PHY_RESREF	C13	O	-	Reference resistor connection, 191 Ω (1 %) to ground.
Power / ground				
DDR32SDMC_IO_PHY_PWR_VDDA_2_5	U13	P	-	DDR-II PHY PLL power supply (2.5 V).
DDR32SDMC_IO_PHY_PWR_VDDC_1_0	R7	P	-	ASC8849/50 M1 version: DDR-II PHY core power supply (1.0 V).
VDDC_1_0		P	-	ASC8849/50 M2 version and 8851: Core power supply(1.0 V)
DDR32SDMC_IO_PHY_PWR_VSSA_2_5	T13	G	-	DDR-II/III PHY PLL ground supply.
DDR32SDMC_IO_PHY_PWR_VSSC_1_0	T7	G	-	ASC8849/50 M1 version: DDR-II/III PHY core ground supply.
DDR32SDMC_IO_PHY_PWR_VSSA_2_5		G	-	ASC8849/50 M2 version and 8851: DDR-II/III PHY analog ground supply.

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
DDR32SDMC_IO_PWR_VDDIO_1_8	U7, U8, U9, U10, U11, U12, V2, V3, V4, V7 V8, V9, V10, V12, V13, V16, V17, V18	P	-	DDR-II/III SDRAM I/O power supply (1.8/1.5 V).
DDR32SDMC_IO_PWR_VREF_0_9	V5, V6, V14, V15	P	-	DDR-II/III SDRAM reference power supply (0.9 V).
DDR32SDMC_IO_PWR_VSSIO_1_8	R6, T4, T5, T6, T8, T9, T10, T11, T12 T14, T15 U2, U3, U4, U5, U14, U15, U16, U17, U18, V1, V19, W20, AB20	G	-	DDR-II/III SDRAM I/O ground supply.
PCIEC_I_PHY_PWR_VDDA_1_0	F13	P	-	PCI Express PHY low-voltage power supply (1.0 V).
PCIEC_I_PHY_PWR_VDDA_2_5	F12	P	-	PCI Express PHY high-voltage power supply (2.5 V).
PCIEC_I_PHY_PWR_VSSA_1_0_2_5	E12, E13 G12, G13	G	-	PCI Express PHY ground supply.
PLLC_I_PLL_0_PWR_VDDA_2_5	F17	P	-	PLL0 analog power supply (2.5 V).
PLLC_I_PLL_0_PWR_VSSA_2_5	F16	G	-	PLL0 analog ground supply.
PLLC_I_PLL_1_PWR_VDDA_2_5	E14	P	-	PLL1 analog power supply (2.5 V).
PLLC_I_PLL_1_PWR_VSSA_2_5	F14	G	-	PLL1 analog ground supply.
PLLC_I_PLL_2_PWR_VDDA_2_5	G7	P	-	PLL2 analog power supply (2.5 V).
PLLC_I_PLL_2_PWR_VSSA_2_5	F7	G	-	PLL2 analog ground supply.
PLLC_I_PLL_3_PWR_VDDA_2_5	P18	P	-	PLL3 analog power supply (2.5 V).
PLLC_I_PLL_3_PWR_VSSA_2_5	P17	G	-	PLL3 analog ground supply.
USBC_IO_PHY_PWR_VDDC_1_0	H5	P	-	USBPHY digital power supply (1.0 V).
USBC_IO_PHY_PWR_VSSC_1_0	H6	G	-	ASC8849/50 M1 version: USBPHY digital ground supply.
USBC_IO_PHY_PWR_VSSA_2_5_3_3		G	-	ASC8849/50 M2 version and 8851: USBPHY analog ground supply.
USBC_IO_PHY_PWR_VDDA_2_5	J5	P	-	USBPHY analog power supply (2.5 V).
USBC_IO_PHY_PWR_VDDA_3_3	G5	P	-	USBPHY analog power supply (3.3 V).
USBC_IO_PHY_PWR_VSSA_2_5_3_3	G6	G	-	USBPHY analog ground supply.
USBC_IO_PHY_PWR_VSSA_2_5_3_3	J6	-	-	ASC8849/50 M1 version: USBPHY analog ground supply.
USBC_IO_PHY_PWR_VSSC_1_0		-	-	ASC8849/50 M2 version and 8851:USBPHY digital ground supply.

Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
VDDC_1_0	H8, H9, H10, H11, H12, H13, H14, H15, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R8, R9, R10, R11, R12, R13, R14, R15	P	-	Core power supply (1.0 V).
VSSC_1_0	J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14	G	-	Core ground supply.
VDDIO_2_5_3_3	E6, E7, E8, E9, E10	P	-	MII/GMII (3.3 V) / RGMII (2.5 V) I/O power supply.
VDDIO_3_3	E5, E11, E15, E16, F5, F11, F15, G8, H7, J17, K7, K17, L7, L17, M7, M17, N7, N18	P	-	I/O power supply (3.3 V).
VDDIO_3_3	H17	-	-	ASC8849/50 M1 version: I/O power supply (3.3 V).
VDDIO_SENSOR		-	-	ASC8849/50 M2 version and 8851: Sensor power supply if the level-shifters between sensor and this chip are removed

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Table 6. ASC8849/50/51 SoC signal descriptions *…continued*

Pin name	BGA ball	Type	Function	Descriptions
VSSIO_2_5_3_3	A11, E1, F6, F8, F9, F10, G9, G10, G11, G14, G15, G16 G18, H1, H16, J7, J16, K16, L16, M16, N4, N16, P6, P7, P16	G	-	I/O ground supply.
Reserved	K5, K6, L5, L6, M6, N5, N6, P5, R5	-	-	-
Reserved	R4	-	-	ASC8849/50 M1 version: Left floating for normal operation
DDR32SDMC_IO_PWR_VSSIO_1_8		-	-	ASC8849/50 M2 version and 8851: DDR-II/III SDRAM I/O ground supply.

Table 7 shows the reference voltages for each I/O. Those signals not listed below all reference VDDIO_3_3 (3.3 V).

Table 7. ASC8849/ASC8850/ASC8851 SoC pin reference voltage

Special I/O	1.0V1	1.8 V	2.5V or 3.3V	Video In I/O
USBC_I_PHY_ID	SYS_I_OSC_0_CLK	DDR32SDMC_O_CLK	GMAC_I_RX_CLK	VIC_I_DEV_0_PCLK
USBC_IO_PHY_DP	SYS_I_OSC_1_CLK	DDR32SDMC_O_nCLK	GMAC_I_TX_CLK	VIC_I_DEV_0_HSYNC
USBC_IO_PHY_DM	SYS_I_OSC_2_CLK	DDR32SDMC_O_nRAS	GMAC_I_RXDV	VIC_I_DEV_0_VSYNC
USBC_IO_PHY_REXT_RKELVIN		DDR32SDMC_O_nCAS	GMAC_I_RXER	VIC_I_DEV_0_FSYNC
USBC_IO_PHY_VBUS		DDR32SDMC_O_nWE	GMAC_I_RXD[7:0]	VIC_I_DEV_0_DATA[0]
USBC_IO_PHY_ATEST		DDR32SDMC_O_ADDR[14:0]	GMAC_I_CRS	VIC_I_DEV_0_DATA[1]
PCIEC_I_PHY_REFCLK_M		DDR32SDMC_O_BA[2:0]	GMAC_I_COL	VIC_I_DEV_0_DATA[2]
PCIEC_I_PHY_REFCLK_P		DDR32SDMC_O_PHY_ATEST	GMAC_IO_MD	VIC_I_DEV_0_DATA[3]
PCIEC_I_PHY_RX_M		DDR32SDMC_I_CALI	GMAC_O_TX_CLK	VIC_I_DEV_0_DATA[4]
PCIEC_I_PHY_RX_P		DDR32SDMC_0_IO_DQ[15:0]	GMAC_O_MDC	VIC_I_DEV_0_DATA[5]
PCIEC_O_PHY_TX_M		DDR32SDMC_0_IO_DQS[1:0]	GMAC_O_TXEN	VIC_I_DEV_0_DATA[6]
PCIEC_O_PHY_TX_P		DDR32SDMC_0_IO_nDQS[1:0]	GMAC_O_TXER	VIC_I_DEV_0_DATA[7]
PCIEC_O_PHY_RESREF		DDR32SDMC_0_O_DM[1:0]	GMAC_O_TXD[7:0]	VIC_I_DEV_1_PCLK
		DDR32SDMC_0_O_CKE		VIC_I_DEV_1_HSYNC

Table 7. ASC8849/ASC8850/ASC8851 SoC pin reference voltage

Special I/O	1.0V1	1.8 V	2.5V or 3.3V	Video In I/O
		DDR32SDMC_0_O_nCS		VIC_I_DEV_1_VSYNC
		DDR32SDMC_0_O_ODT		VIC_I_DEV_1_FSYNC
		DDR32SDMC_1_IO_DQ[15:0]		VIC_I_DEV_0_DATA[8]
		DDR32SDMC_1_IO_DQS[1:0]		VIC_I_DEV_0_DATA[9]
		DDR32SDMC_1_IO_nDQS[1:0]		VIC_I_DEV_0_DATA[10]
		DDR32SDMC_1_O_DM[1:0]		VIC_I_DEV_0_DATA[11]
		DDR32SDMC_1_O_CKE		VIC_I_DEV_0_DATA[12]
		DDR32SDMC_1_O_nCS		VIC_I_DEV_0_DATA[13]
		DDR32SDMC_1_O_ODT		VIC_I_DEV_0_DATA[14]
				VIC_I_DEV_0_DATA[15]

Table 8. ASC8848 SoC signal descriptions

Pin Name	BGA Ball	Type	Function	Description
Global signals				
SYS_I_OSC_0_CLK	A19	I	-	System clock 0 from oscillator or crystal. (25 MHz). The feedback resistor, Rf, is built in and no external resistor is required.
SYS_I_OSC_1_CLK	B1	I	-	System clock 1 from oscillator or crystal. (18.432 MHz). The feedback resistor, Rf, is built in and no external resistor is required.
SYS_I_OSC_2_CLK	AA22	I	-	System clock 2 from oscillator or crystal. (24 MHz). The feedback resistor, Rf, is built in and no external resistor is required.
SYS_I_nRST	M4	I	-	Active-low global reset input signal.
SYS_I_BOOT_MODE_SEL[0]	K4	I	-	Boot mode select. Refer to section Boot Modes 4.2.
SYS_I_BOOT_MODE_SEL[1]	L4	I	-	Boot mode select. Refer to section Boot Modes 4.2.
SYS_I_GMAC_MODE_SEL	P4	I	-	ASC8848 M1 version: RGMII/GMII mode select. 1: 2.5 V RGMII model. 0: 3.3 V GMII mode.
VSSC_1_0		I	-	ASC8848 M2: Core ground supply

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
SYS_I_GMAC_TX_CLK_DIR	M5	I	-	ASC8848 M1 version: Ethernet MAC TX clock direction. 1: Input from the external Ethernet PHY. 0: Output to the external Ethernet PHY.
VSSIO_2_5_3_3		I	-	ASC8848 M2: I/O ground supply
SYS_O_OSC_0_FEBCLK	A18	O	-	Feedback crystal output of system clock 0.
SYS_O_OSC_1_FEBCLK	C1	O	-	Feedback crystal output of system clock 1.
SYS_O_OSC_2_FEBCLK	Y22	O	-	Feedback crystal output of system clock 2.
SYS_O_MON_CLK[0]	C11	O	OEEP, I2P	1. Monitor clock 0 2. Connect to MSHC_0_I_RX_CCLK if MSHC 0 interface is enabled
WDTC_O_nRST	R3	O	OEEP, PUEP, I4P	System output reset.
DDR-II/III SDRAM interface				
DDR32SDMC_O_CLK	AB10	O	-	DDR-II/III SDRAM common output clock.
DDR32SDMC_O_nCLK	AB11	O	-	DDR-II/III SDRAM common complementary output clock.
DDR2SDMC_IO_PWR_VSSIO_1_8	U6	G	-	ASC8848 M1 version: DDR-II/III SDRAM I/O ground supply.
DDR32DMC_O_nRST		G	-	ASC8848 M2: DDR-III SDRAM Reset. For DDR-II could be left floating
DDR32SDMC_O_nRAS	AA8	O	-	Active-low DDR-II/III SDRAM common row address strobe signal.
DDR32SDMC_O_nCAS	AA9	O	-	Active-low DDR-II/III SDRAM common column address strobe signal.
DDR32SDMC_O_nWE	AA11	O	-	Active-low DDR-II/III SDRAM common write enable signal.
DDR32SDMC_O_ADDR[0]	Y9	O	-	DDR-II/III SDRAM common address bus.
DDR32SDMC_O_ADDR[1]	Y11	O	-	-
DDR32SDMC_O_ADDR[2]	W7	O	-	-
DDR32SDMC_O_ADDR[3]	Y12	O	-	-
DDR32SDMC_O_ADDR[4]	W8	O	-	-
DDR32SDMC_O_ADDR[5]	Y10	O	-	-
DDR32SDMC_O_ADDR[6]	W10	O	-	-
DDR32SDMC_O_ADDR[7]	Y13	O	-	-
DDR32SDMC_O_ADDR[8]	W9	O	-	-
DDR32SDMC_O_ADDR[9]	W12	O	-	-
DDR32SDMC_O_ADDR[10]	AA10	O	-	-
DDR32SDMC_O_ADDR[11]	W14	O	-	-
DDR32SDMC_O_ADDR[12]	AA12	O	-	-
DDR32SDMC_O_ADDR[13]	W13	O	-	-
DDR32SDMC_O_ADDR[14]	W11	O	-	

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Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
DDR2SDMC_O_PHY_ATEST	V11	O	-	ASC8848 M1 version: PLL analog test output.
DDR32SDMC_O_ADDR[15]		O	-	ASC8848 M2: DDR-II/III SDRAM common address bus bit15. Allows connecting higher capacity DRAM compared to M1 version otherwise could be left floating.
DDR32SDMC_O_BA[0]	Y8	O	-	DDR-II/III SDRAM common internal bank select signals.
DDR32SDMC_O_BA[1]	AA7	O	-	-
DDR32SDMC_O_BA[2]	Y7	O	-	-
DDR2SDMC_I_CMD_CALI	W6	I	-	ASC8848 M1 version: PVT calibration for DDR-II SDRAM common command signal. Connected through an external resistor, 240 Ω (1 %), to 1.8 V.
DDR32SDMC_O_PHY_ATEST		-	-	ASC8848 M2: PLL analog test output.
DDR2SDMC_I_DATA_1_CALI	W17	I	-	ASC8848 M1 version: PVT calibration for DDR-II SDRAM 1 data bus. Connected through an external resistor, 240 Ω (1 %), to 1.8 V
DDR32SDMC_IO_PHY_PWR_VDDA_2_5		-	-	ASC8848 M2: DDR-II/III PHY analog power supply (2.5 V).
DDR32SDMC_1_IO_DQ[0]	W16	I/O	-	DDR-II/III SDRAM 1 read/write data bus.
DDR32SDMC_1_IO_DQ[1]	AA16	I/O	-	-
DDR32SDMC_1_IO_DQ[2]	AB16	I/O	-	-
DDR32SDMC_1_IO_DQ[3]	W15	I/O	-	-
DDR32SDMC_1_IO_DQ[4]	AA15	I/O	-	-
DDR32SDMC_1_IO_DQ[5]	Y15	I/O	-	-
DDR32SDMC_1_IO_DQ[6]	AA14	I/O	-	-
DDR32SDMC_1_IO_DQ[7]	Y14	I/O	-	-
DDR32SDMC_1_IO_DQ[8]	AA19	I/O	-	-
DDR32SDMC_1_IO_DQ[9]	Y18	I/O	-	-
DDR32SDMC_1_IO_DQ[10]	Y19	I/O	-	-
DDR32SDMC_1_IO_DQ[11]	W18	I/O	-	-
DDR32SDMC_1_IO_DQ[12]	AB17	I/O	-	-
DDR32SDMC_1_IO_DQ[13]	AA18	I/O	-	-
DDR32SDMC_1_IO_DQ[14]	AA17	I/O	-	-
DDR32SDMC_1_IO_DQ[15]	Y17	I/O	-	-

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
DDR32SDMC_1_IO_DQS[0]	AB15	I/O	-	DDR-II/III SDRAM 1 data strobe signals. It is edge-aligned with write data and centered in read data. It must be connected on the board to a pull-down resistor, 430~560? (?15%). The resistor must be placed on the board within 0.3 inches of the SoC. DQS[0]: for DQ[7:0] DQS[1]: for DQ[15:8]-
DDR32SDMC_1_IO_DQS[1]	AB19	I/O	-	
DDR32SDMC_1_IO_nDQS[0]	AB14	I/O	-	DDR-II/III SDRAM 1 complementary data strobe signals. It is edge-aligned with write data and centered in read data. It must be connected on the board to a pull-down resistor, 430~560? (?15%). The resistor must be placed on the board within 0.3 inches of the SoC. nDQS[0]: for DQ[7:0] nDQS[1]: for DQ[15:8]-
DDR32SDMC_1_IO_nDQS[1]	AB18	I/O	-	
DDR32SDMC_1_O_DM[0]	Y16	O	-	DDR-II/III SDRAM 1 output data mask signals. DM[0]: for DQ[7:0] DM[1]: for DQ[15:8].
DDR32SDMC_1_O_DM[1]	W19	O	-	
DDR32SDMC_1_O_CKE	AB13	O	-	DDR-II/III SDRAM 1 clock enable signal.
DDR32SDMC_1_O_nCS	AA13	O	-	Active-low DDR-II/III 1 SDRAM chip select signal.
DDR32SDMC_1_O_ODT	AB12	O	-	DDR-II/III SDRAM 1 on-die termination signal.
GPIO interface				
GPIOC_IO_DATA[0]	AB22	I/O	SMT, I8P, PUDP, PDDP, OEEP	General-purpose I/O data signals. Upon reset, GPIOC_IO_DATA[7:0] is set output mode and drives low; GPIOC_IO_DATA[19:8] is set input mode.
GPIOC_IO_DATA[1]	AB21	I/O	-	
GPIOC_IO_DATA[2]	AA21	I/O	-	
GPIOC_IO_DATA[3]	AA20	I/O	-	
GPIOC_IO_DATA[4]	Y20	I/O	-	
GPIOC_IO_DATA[5]	Y21	I/O	-	-
GPIOC_IO_DATA[6]	R16	I/O	-	-
GPIOC_IO_DATA[7]	R17	I/O	-	-
GPIOC_IO_DATA[8]	T17	I/O	SMT, I8P, PUDP, PDDP, OEDP	-
GPIOC_IO_DATA[9]	T16	I/O	-	-
GPIOC_IO_DATA[10]	T18	I/O	-	-
GPIOC_IO_DATA[11]	R18	I/O	-	-
GPIOC_IO_DATA[12]	E22	I/O	-	-

Table 8. ASC8848 SoC signal descriptions *...continued*

Pin Name	BGA Ball	Type	Function	Description
GPIOC_IO_DATA[13]	E21	I/O	-	-
GPIOC_IO_DATA[14]	E20	I/O	-	-
GPIOC_IO_DATA[15]	E19	I/O	-	-
GPIOC_IO_DATA[16]	F19	I/O	-	-
GPIOC_IO_DATA[17]	E18	I/O	-	-
GPIOC_IO_DATA[18]	F18	I/O	-	-
GPIOC_IO_DATA[19]	E17	I/O	-	-
JTAG interface (ARM926EJ)				
HOSTC_I_DBG_nTRST	H18	I	SMT, PUEP	Active low reset for internal synchronizer.
HOSTC_I_DBG_TCK	K18	I	SMT, IEEP, PUEP	JTAG clock input.
HOSTC_I_DBG_TMS	G17	I	SMT, PUEP	JTAG mode selection input signal.
HOSTC_I_DBG_TDI	L18	I	-	JTAG data input signal.
HOSTC_O_DBG_RTCK	M18	O	OEEP, PDEP, I4P	JTAG output clock signal.
HOSTC_O_DBG_TDO	J18	O	OEDP, PUEP, I4P	JTAG data output signal.
IrDA interface				
IRDAC_I_SDA	T3	I	-	IrDA input.
I2S interface				
I2SSC_0_I_BCLK	J1	I	IEEP, SMT	I^{2}S serial clock.
I2SSC_0_I_RXD	K3	I	-	I^{2}S receive data input signal.
I2SSC_0_I_WS	J2	I	-	I^{2}S frame synchronization signal.
I2SSC_0_O_TXD	J3	O	OEEP, I4P	I^{2}S transmit data output signal.
I2SSC_O_TX_MCLK	L1	O	-	I^{2}S master clock output.
10/100 Ethernet MAC interface				
GMAC_I_RX_CLK	A5	I	-	Receive clock signal.
GMAC_I_TX_CLK	A7	I	-	Input transmit clock signal.
GMAC_I_RXDV	D8	I	-	Receive data valid signal. RGMII: Receive control signal.
GMAC_I_RXER	D9	I	-	Receive error signal.
GMAC_I_RXD[0]	B7	I	-	Receive data bus.
GMAC_I_RXD[1]	C7	I	-	-
GMAC_I_RXD[2]	A6	I	-	-
GMAC_I_RXD[3]	B6	I	-	-
GMAC_I_CRS	C5	I	-	Carrier sense signal.
GMAC_I_COL	D5	I	-	Collision detected signal.
GMAC_IO_MD	D6	I/O	OEDP, FSRP	Management data.

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
GMAC_O_TX_CLK	A9	O	FSRP	GMII/RGMII output transmit clock signal. This clock is used only when TX clock is an input signal to the PHY.
GMAC_O_MDC	D7	O	OEEP, FSRP	Management data clock signal.
GMAC_O_TXEN	D11	O	-	Transmit data enable signal.
GMAC_O_TXER	D10	O	-	Transmit error signal.
GMAC_O_TXD[0]	A10	O	-	Transmit data bus.
GMAC_O_TXD[1]	B10	O	-	-
GMAC_O_TXD[2]	C10	O	-	-
GMAC_O_TXD[3]	B9	O	-	-
Synchronous serial interface				
SSIC_I_RXD	R1	I	-	SSI receive data signal.
SSIC_O_BCLK	R2	O	OEEP, I4P	SSI serial clock output.
SSIC_O_TXD	T2	O	OEDP, I4P	SSI transmit data signal.
SSIC_O_nSEL[0]	T1	O	OEEP, I4P, PUEP	SSI slave selection signal.
Mobile storage host control interface				
MSHC_0_I_nDETECT	B18	I	PUEP	Card detect signal.
MSHC_0_I_RX_CCLK	D17	I	IEEP	Card input sampling clock.
MSHC_0_I_WRITE_PROTECT	D16	I	PUEP	Card write protect signal.
MSHC_0_IO_CMD	C17	I/O	OEDP, SMT, PUEP, I8P	Card command signal.
MSHC_0_IO_DATA[0]	A17	I/O		Card data signals.
MSHC_0_IO_DATA[1]	B17	I/O	-	-
MSHC_0_IO_DATA[2]	A16	I/O	-	-
MSHC_0_IO_DATA[3]	B16	I/O	-	-
MSHC_0_O_TX_CCLK	C16	O	OEEP, I8P	Card clock.
NAND FLASH interface				
NFC_I_nRB	C19	I	SMT, PUEP	NAND FLASH read/busy signal.
NFC_IO_DATA[0]	D22	I/O	OEDP, SMT, PUEP	NAND FLASH data signals.
NFC_IO_DATA[1]	D21	I/O	-	-
NFC_IO_DATA[2]	D20	I/O	-	-
NFC_IO_DATA[3]	C22	I/O	-	-
NFC_IO_DATA[4]	C21	I/O	-	-
NFC_IO_DATA[5]	C20	I/O	-	-
NFC_IO_DATA[6]	B22	I/O	-	-
NFC_IO_DATA[7]	B21	I/O	-	-

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
NFC_O_ALE	A22	O	OEEP, I4P	NAND FLASH address latch enable signal.
NFC_O_CLE	D18	O	-	NAND FLASH command latch enable signal.
NFC_O_nCE[0]	A21	O	OEEP, PUEP, I4P	NAND FLASH chip enable signals.
NFC_O_nRE	B20	O	-	NAND FLASH read enable signal.
NFC_O_nWE	B19	O	-	NAND FLASH write enable signal.
NFC_O_nWP[0]	D19	O	-	NAND FLASH write protect signals.
UART (modem control) interface				
UARTC_0_I_SDA	A1	I	-	Serial data input for UART0.
UARTC_0_I_nCTS	B3	I	-	Clear to send signal for UART0.
UARTC_0_I_nDSR	C3	I	-	Data set ready signal for UART0.
UARTC_0_I_nRI	C2	I	-	Ring indicator signal for UART0.
UARTC_0_I_nDCD	B2	I	-	Data carrier detect signal for UART0.
UARTC_0_IO_nRTS	C4	I/O	OEDP, SMT, I8P	Request to send signal for UART0.
UARTC_0_IO_nDTR	A3	I/O	OEDP, SMT, I8P	Data terminal ready signal for UART0.
UARTC_0_O_SDA	A2	O	OEDP, PUEP, I8P	Serial data output for UART0.
UARTC_1_I_nDCD	D3	I	-	Data carrier detect signal for UART1.
UARTC_1_O_SDA	E3	O	OEDP, PUEP, I8P	Serial data output for UART1.
Video input interface				
VIC_I_DEV_0_PCLK	K22	I	IEEP, SMT	Device 0 pixel clock input.
VIC_I_DEV_0_HSYNC	L22	I	SMT	Device 0 horizontal synchronization (line valid) signal.
VIC_I_DEV_0_VSYNC	K21	I	-	Device 0 vertical synchronization (frame valid) signal.
VIC_I_DEV_0_FSYNC	M22	I	-	Device 0 field signal.

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
VIC_I_DEV_0_DATA[0]	L21	I	-	Device 0 video input data bus.
VIC_I_DEV_0_DATA[1]	L20	I	-	
VIC_I_DEV_0_DATA[2]	L19	I	-	
VIC_I_DEV_0_DATA[3]	K20	I	-	
VIC_I_DEV_0_DATA[4]	K19	I	-	
VIC_I_DEV_0_DATA[5]	J22	I	-	
VIC_I_DEV_0_DATA[6]	J21	I	-	
VIC_I_DEV_0_DATA[7]	J20	I	-	
VIC_I_DEV_0_DATA[8]	H21	I	-	
VIC_I_DEV_0_DATA[9]	H20	I	-	
VIC_I_DEV_0_DATA[10]	J19	I		
VIC_I_DEV_0_DATA[11]	H19	I		
Video output interface				
VOC_O_PCLK	T22	O	OEEP, FSRP, I8P	Pixel clock output.
VSSIO_2_5_3_3	N17	-	-	ASC8848 M1 version: I/O ground supply
VOC_I_CLK		-	-	ASC8848 M2 optional: alternate clock source for VOC PLL
VOC_O_VSYNC	W22	O	-	Vertical synchronization (frame valid) signal.
VOC_O_HSYNC	W21	O	-	Horizontal synchronization (line valid) signal.
VOC_O_BLANK	V20	O	-	Blanking signal or data enable (DE) signal.
VOC_O_DATA[0]	V22	O	-	Video output data bus
VOC_O_DATA[1]	V21	O	-	-
VOC_O_DATA[2]	U22	O	-	-
VOC_O_DATA[3]	U21	O	-	-
VOC_O_DATA[4]	U20	O	-	-
VOC_O_DATA[5]	U19	O	-	-
VOC_O_DATA[6]	T21	O	-	-
VOC_O_DATA[7]	T20	O	-	-
Universal Serial Bus (USB) interface				
USBC_I_PHY_ID	H3	I	-	USB mini-receptacle identifier. The ID detection circuitry can differentiate the following conditions: ID pin floating (>100 KΩ) ID pin shorted to ground (<10 Ω)
USBC_IO_PHY_DP	G1	I/O	5VT	USB differential data signal, D+.
USBC_IO_PHY_DM	F1	I/O	5VT	USB differential data signal, D-.
USBC_IO_PHY_REXT_RKELVIN	J4	I/O	-	USB external resistor 43.2 Ω (1 %) connection to ground for bias current in USB 2.0 PHY.
USBC_IO_PHY_VBUS	H2	I/O	5VT	USB 5 V power supply pin.

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Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
USBC_IO_PHY_ATEST	G2	I/O	-	Analog test point for internal analog voltage level measurement.
USBC_O_DRV_VBUS	G3	O	OEEP, I4P	Control off-chip charge pump. 0: Do not drive VBUS 1: Drive VBUSPCI Express x1 Interface
PCI Express x1 interface				
PCIEC_I_PHY_REFCLK_M	B13	I	-	Differential reference clock input, 100 MHz.
PCIEC_I_PHY_REFCLK_P	A13	I	-	Differential reference clock input, 100 MHz.
PCIEC_I_PHY_RX_M	D12	I	-	High-speed differential receive pair.
PCIEC_I_PHY_RX_P	C12	I	-	High-speed differential receive pair.
PCIEC_O_PHY_TX_M	B12	O	-	High-speed differential transmit pair.
PCIEC_O_PHY_TX_P	A12	O	-	High-speed differential transmit pair.
PCIEC_O_PHY_RESREF	C13	O	-	Reference resistor connection, 191 Ω (1 %) to ground.
Power / ground				
DDR32SDMC_IO_PHY_PWR_VDDA_2_5	U13	P	-	DDR-II/III PHY PLL power supply (2.5 V).
DDR32SDMC_IO_PHY_PWR_VDDC_1_0	R7	P	-	ASC8848 M1 version: DDR-II/III PHY core power supply (1.0 V).
VDDC_1_0		P	-	ASC8848 M2: Core power supply(1.0 V)
DDR32SDMC_IO_PHY_PWR_VSSA_2_5	T13	G	-	DDR-II/III PHY PLL ground supply.
DDR32SDMC_IO_PHY_PWR_VSSC_1_0	T7	G	-	ASC8848 M1 version: DDR-II/III PHY core ground supply.
DDR32SDMC_IO_PHY_PWR_VSSA_2_5		G	-	ASC8848 M2: DDR-II/III PHY analog ground supply.
DDR32SDMC_IO_PWR_VDDIO_1_8	U7,U8, U9, U10, U11, U12, V2 , V3, V4, V7, V8, V9, V10, V12, V13, V16 , V17, V18	P	-	DDR-II/III SDRAM I/O power supply (1.8/1.5 V).
DDR32SDMC_IO_PWR_VREF_0_9	V5, V6, V14, V15	P	-	DDR-II/III SDRAM reference power supply (0.9 V).

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
DDR32SDMC_IO_PWR_VSSIO_1_8	R6, T4 , T5, T6, T8 ,T9, T10, T11, T12, T14, T15, U2,U3, U4, U5, U14 , U15, U16, U17, U18, V1, V19, W2, W4, W5, W20, Y1,Y2, Y3, Y4 Y5, AA1 , AA2, AA3, AA4, AA5, AA6, AB1,AB2, AB3, AB4, AB5, AB6, AB20	G	-	DDR-II/III SDRAM I/O ground supply.
DDR2SDMC_I_DATA_0_CALI	W3	I	-	ASC8848 M1 version: PVT calibration for DDR-II SDRAM 0 data bus. Connected through an external resistor, 240 Ω (1 %), to 1.8 V
DDR32SDMC_I_CALI		I	-	ASC8848 M2: PVT Calibration for DDR-II/III data and command. Connected through an external resistor, 240 Ω (1 %) to Gnd
PCIEC_I_PHY_PWR_VDDA_1_0	F13	P	-	PCI Express PHY low-voltage power supply (1.0 V).
PCIEC_I_PHY_PWR_VDDA_2_5	F12	P	-	PCI Express PHY high-voltage power supply (2.5 V).
PCIEC_I_PHY_PWR_VSSA_1_0_2_5	E12, E13, G12, G13	G	-	PCI Express PHY ground supply.
PLLC_I_PLL_0_PWR_VDDA_2_5	F17	P	-	PLL0 analog power supply (2.5 V).
PLLC_I_PLL_0_PWR_VSSA_2_5	F16	G	-	PLL0 analog ground supply.
PLLC_I_PLL_1_PWR_VDDA_2_5	E14	P	-	PLL1 analog power supply (2.5 V).
PLLC_I_PLL_1_PWR_VSSA_2_5	F14	G	-	PLL1 analog ground supply.
PLLC_I_PLL_2_PWR_VDDA_2_5	G7	P	-	PLL2 analog power supply (2.5 V).
PLLC_I_PLL_2_PWR_VSSA_2_5	F7	G	-	PLL2 analog ground supply.
PLLC_I_PLL_3_PWR_VDDA_2_5	P18	P	-	PLL3 analog power supply (2.5 V).
PLLC_I_PLL_3_PWR_VSSA_2_5	P17	G	-	PLL3 analog ground supply.
USBC_IO_PHY_PWR_VDDC_1_0	H5	P	-	USBPHY digital power supply (1.0 V).
USBC_IO_PHY_PWR_VSSC_1_0	H6	G	-	ASC8848 M1 version: USBPHY digital ground supply.
USBC_IO_PHY_PWR_VSSA_2_5_3_3		G		ASC8848 M2: USBPHY analog ground supply.
USBC_IO_PHY_PWR_VDDA_2_5	J5	P	-	USBPHY analog power supply (2.5 V).
USBC_IO_PHY_PWR_VDDA_3_3	G5	P	-	USBPHY analog power supply (3.3 V).
USBC_IO_PHY_PWR_VSSA_2_5_3_3	G6	G	-	USBPHY analog ground supply.

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
USBC_IO_PHY_PWR_VSSA_2_5_3_3	J6	-	-	ASC8848 M1 version: USBPHY analog ground supply.
USBC_IO_PHY_PWR_VSSC_1_0		-	-	ASC8848 M2: USBPHY digital ground supply.
VDDC_1_0	H8, H9, H10, H11, H12, H13, H14, H15, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R8 to R15	P	-	Core power supply (1.0 V).
VSSC_1_0	J9 , J10, J11, J12, J13, J14, K9 , K10, K11, K12, K13, K14, L9 , L10, L11, L12, L13, L14, M9 , M10, M11, M12, M13, M14, N9 , N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14	G	-	Core ground supply.
VDDIO_2_5_3_3	E6, E7, E8, E9, E10	P	-	MII I/O power supply. Should be connected to 3.3V.
VDDIO_3_3	E5, E11, E15, E16, F5, F11, F15, G8, H7, J17, K7, K17, L7, L17, M7, M17, N7, N18	P	-	I/O power supply (3.3 V)
VDDIO_3_3	H17	-	-	ASC8848 M1 version: I/O power supply (3.3 V)
VDDIO_SENSOR		-	-	ASC8848 M2: Sensor power supply if the level-shifters between sensor and this chip are removed
VSSIO_2_5_3_3	A11, D2, E1, E2, F6, F8 , F9, F10, G4, G9,G10, G11, G14 , G15, G16, G18 H1, H16, J7, J16, K1, K2, K16, L2, L3, L16, M2, M3, M16, N4, N16, P6, P7, P16	G	-	I/O ground supply.

Table 8. ASC8848 SoC signal descriptions *…continued*

Pin Name	BGA Ball	Type	Function	Description
Reserved	A14, A15, A20, A4, A8, B14, B15, B4, B5, B8, C14, C15, C18, C6, C8, C9, D1, D13, D14, D3, D4, E4, F2, F20, F21, F22, F4, G19,G20, G21, G22, , H22, H4, , K5, K6, L5, L6, M1, M6, M19 , M20, M21, N1, N2, N19 to N22, N3, N5, N6, P1,P2, P3, P5, P19 , P20, P21, R5, T19, V1, V20, W1, W21, Y6, AB7 to AB9	-	-	Left floating for normal operation
SYS_O_MON_CLK[1]	B11	O	-	ASC8848 M1 version: Monitor clock 1. Connect to MSHC_1_I_RX_CCLK if MSHC 1 interface is enabled or use 90 rotated GMAC_O_TX_CLK
		-	-	ASC8848 M2: Monitor clock 1. Connect to MSHC_1_I_RX_CCLK
Reserved	R4	-	-	ASC8848 M1 version: Left floating for normal operation
DDR32SDMC_IO_PWR_VSSIO_1_8		-	-	ASC8848 M2: DDR-II/III SDRAM I/O ground supply.

Table 9 shows the reference voltages for each I/O. Those signals not listed below all reference VDDIO_3_3 (3.3 V).

Table 9. Reference voltage for I/O

Special I/O	1.0V1	1.8 V	Video In I/O
USBC_I_PHY_ID	SYS_I_OSC_0_CLK	DDR32SDMC_O_CLK	VIC_I_PCLK
USBC_IO_PHY_DP	SYS_I_OSC_1_CLK	DDR32SDMC_O_nCLK	VIC_I_HSYNC
USBC_IO_PHY_DM	SYS_I_OSC_2_CLK	DDR32SDMC_O_nRAS	VIC_I_VSYNC
USBC_IO_PHY_REXT_RKELVIN		DDR32SDMC_O_nCAS	VIC_I_FSYNC
USBC_IO_PHY_VBUS		DDR32SDMC_O_nWE	VIC_I_DATA[0]
USBC_IO_PHY_ATEST		DDR32SDMC_O_ADDR[14:0]	VIC_I_DATA[1]
PCIEC_I_PHY_REFCLK_M		DDR32SDMC_O_BA[2:0]	VIC_I_DATA[2]
PCIEC_I_PHY_REFCLK_P		DDR32SDMC_O_PHY_ATEST	VIC_I_DATA[3]
PCIEC_I_PHY_RX_M		DDR32SDMC_I_CALI	VIC_I_DATA[4]
PCIEC_I_PHY_RX_P		DDR32SDMC_IO_DQ[15:0]	VIC_I_DATA[5]
PCIEC_O_PHY_TX_M		DDR32SDMC_IO_DQS[1:0]	VIC_I_DATA[6]
PCIEC_O_PHY_TX_P		DDR32SDMC_IO_nDQS[1:0]	VIC_I_DATA[7]
PCIEC_O_PHY_RESREF		DDR32SDMC_O_DM[1:0]	VIC_I_DATA[8]
		DDR32SDMC_O_CKE	VIC_I_DATA[9]
		DDR32SDMC_O_nCS	VIC_I_DATA[10]
		DDR32SDMC_O_ODT	VIC_I_DATA[11]

6. Functional description

Memory map: ASC8848/49/50/51 SoC has a 32-bit address bus and is capable of addressing up to 4 Gb address space. Table 10 shows the memory mapped address and its size for each device on AMBA AHB bus. Table 11 shows the memory mapped address and its size for each device on AMBA APB 2.0 bus. Table 12 shows the memory mapped address and its size for each device on AMBA APB 3.0 bus.

The start address and size are power-on default values and users could configure the memory space based on their own requirements. The overlapping of memory space is forbidden and must be taken care of. Figure 10 illustrates the whole memory map.

6.1 Function selection

Table 10. Memory mapped address on AMBA AHB bus.

Start Address	Size (MB)	Description
0x00000000	256	Internal boot ROM / external DDR-II/III SDRAM 0
0x10000000	256	External DDR-II/III SDRAM 1
0x40000000	256	APB 2.0 Devices
0x50000000	256	APB 3.0 Devices
0x60000000	256	PCIe devices
0x80000000	1	USB 2.0 Host Controller (USBC)
0x84000000	1	PCIe Dual Mode Controller (PCIEC)
0x90000000	1	Mobile Storage Controller 0 (MSHC)
0x94000000	1	Mobile Storage Controller 1 (MSHC)
0x98000000	1	Giga-bit Ethernet MAC (GMAC)
0xA0000000	1	NAND Flash Controller (NFC)
0xC0000000	1	AMBA AHB Controller 0 (AHBC)
0xC1000000	1	AMBA AHB Controller 1 (AHBC)
0xC2000000	1	AMBA AHB Controller 2 (AHBC)
0xC4000000	1	DDR-II/III SDRAM Memory Controller 0 (DDR32SDMC)
0xC5000000	1	DDR-II/III SDRAM Memory Controller 1 (DDR32SDMC)
0xC7000000	1	Interrupt Controller (INTC)
0xC8000000	1	AHB-to-APB Bridge (APBC)
0xC9000000	1	Direct Memory Access Controller (DMAC)
0xCA000000	1	Video Input Controller (VIC)
0xCC000000	1	Video Output Controller (VOC)
0xD0000000	1	Data Crypto Engine (DCE)
0xD1000000	1	Deinterlacing Engine (DIE)
0xD2000000	1	Image Back-End Processing Engine (IBPE)
0xD3000000	1	Resize Engine (IRE)
0xD7000000	1	MPEG-4 Encoder Audio Engine (MEAE)
0xD8000000	1	JPEG Encoder Engine (JEBE)
0xDC000000	1	H.264/MPEG-4 Encoder Engine (H4EE)

Table 11. Memory Mapped Address on AMBA APB 2.0 Bus

Start Address	Size (MB)	Description
0x40800000	8	Synchronous Serial Interface Controller (SSIC)
0x41800000	8	Inter-IC Sound Controller 0 (I2SC)
0x42000000	8	Inter-IC Sound Controller 1 (I2SC)
0x42800000	8	Inter-IC Sound Controller 2 (I2SC)
0x43000000	8	Inter-IC Sound Controller 3 (I2SC)
0x43800000	8	Inter-IC Sound Controller 4 (I2SC)
0x47000000	8	USB 2.0 Host Controller (USBSSC)
0x47800000	8	PCIe Dual Mode Controller (PCIESSC)
0x48000000	8	Timer Controller (TMRC)
0x48800000	8	Watchdog Timer (WDT)
0x49000000	8	General Purpose Input/Output Controller (GPIOC)
0x49800000	8	Advanced General Purpose Output Controller (AGPOC)
0x4A000000	8	Universal Asynchronous Receiver/Transmitter Controller 0 (UARTC)
0x4A800000	8	Universal Asynchronous Receiver/Transmitter Controller 1 (UARTC)
0x4B000000	8	Universal Asynchronous Receiver/Transmitter Controller 2 (UARTC)
0x4B800000	8	Universal Asynchronous Receiver/Transmitter Controller 3 (UARTC)
0x4C000000	8	IrDA Controller (IRDAC)
0x4F000000	8	PLL Controller (PLLC)
0x4F800000	8	System Controller (SYSC)

Table 12. Memory Mapped Address on AMBA APB 3.0 Bus (for ASC8848/49/50 M1 version)

Start Address	Size (MB)	Description
0x50000000	1	DDR-II I/O Data Bus 0 Impedance Control Block
0x50100000	1	DDR-II I/O Data Bus 1 Impedance Control Block
0x50800000	1	DDR-II I/O Command Bus Impedance Control Block
0x51000000	1	DDR-II Data Bus 0 Lane 0 Configuration
0x51100000	1	DDR-II Data Bus 0 Lane 1 Configuration
0x51200000	1	DDR-II Data Bus 1 Lane 0 Configuration
0x51300000	1	DDR-II Data Bus 1 Lane 1 Configuration
0x51800000	1	DDR-II Command Bus Configuration

Table 13. Memory Mapped Address on AMBA APB 3.0 Bus for ASC8848/49/50 M2 Version and ASC8851

Start Address	Size (MB)	Description
0x50000000	1M	DDR-II/III PUB Configuration Block

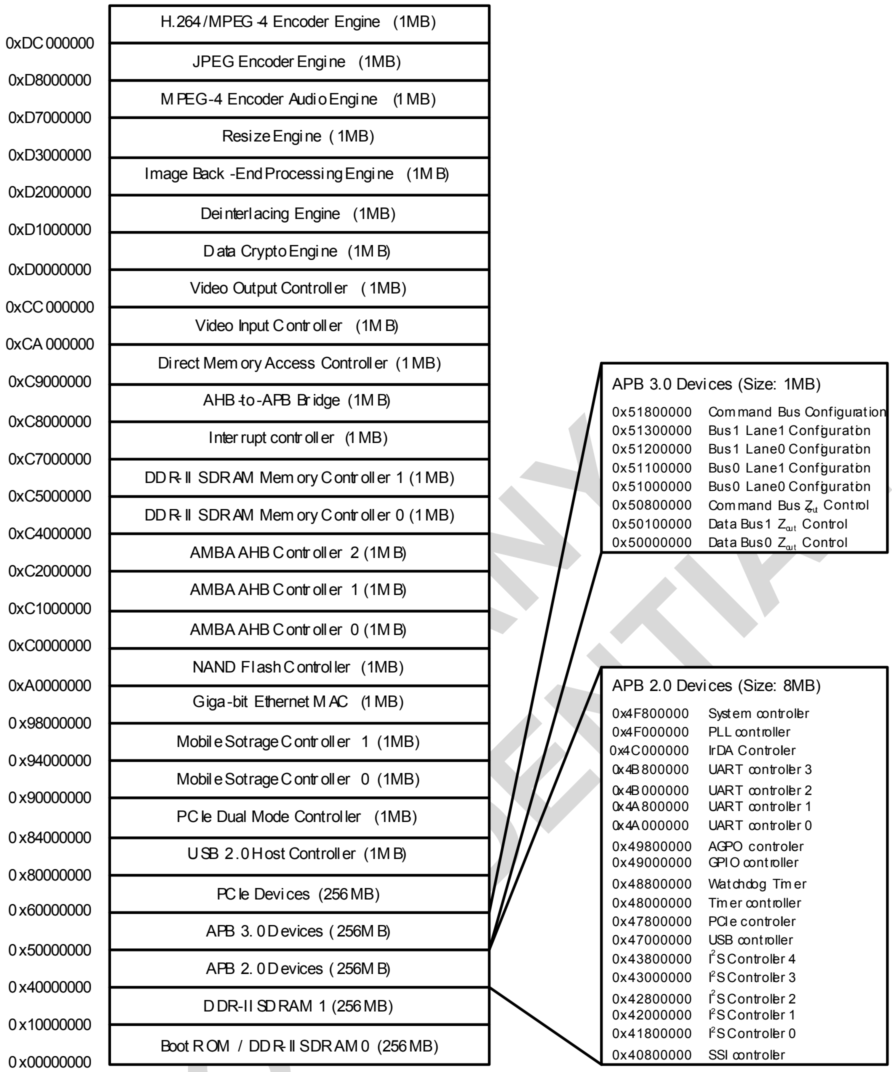

H.264/MPEG-4 Encoder Engine (1MB)
0xDC000000
JPEG Encoder Engine (1MB)
0xD8000000
MPEG-4 Encoder Audio Engine (1MB)
0xD7000000
Resize Engine (1MB)
0xD3000000
Image Back-End Processing Engine (1MB)
0xD2000000
Deinterlacing Engine (1MB)
0xD1000000
Data Crypto Engine (1MB)
0xD0000000
Video Output Controller (1MB)
0xCC000000
Video Input Controller (1MB)
0xCA000000
Direct Memory Access Controller (1MB)
0xC9000000
AHB-to-APB Bridge (1MB)
0xC8000000
Interrupt controller (1MB)
0xC7000000
DDR-II SDRAM Memory Controller 1 (1MB)
0xC5000000
DDR-II SDRAM Memory Controller 0 (1MB)
0xC4000000
AMBA AHB Controller 2 (1MB)
0xC2000000
AMBA AHB Controller 1 (1MB)
0xC1000000
AMBA AHB Controller 0 (1MB)
0xC0000000
NAND Flash Controller (1MB)
0xA0000000
Giga-bit Ethernet MAC (1MB)
0x98000000
Mobile Sotrage Controller 1 (1MB)
0x94000000
Mobile Sotrage Controller 0 (1MB)
0x90000000
PCIe Dual Mode Controller (1MB)
0x84000000
USB 2.0 Host Controller (1MB)
0x80000000
PCIe Devices (256MB)
0x60000000
APB 3.0 Devices (256MB)
0x50000000
APB 2.0 Devices (256MB)
0x40000000
DDR-II SDRAM 1 (256MB)
0x10000000
Boot ROM / DDR-II SDRAM 0 (256MB)
0x00000000
APB 3.0 Devices (Size: 1MB)
0x51800000 Command Bus Configuration
0x51300000 Bus1 Lane1 Configuration
0x51200000 Bus1 Lane0 Configuration
0x51100000 Bus0 Lane1 Configuration
0x51000000 Bus0 Lane0 Configuration
0x50800000 Command Bus Z_{out} Control
0x50100000 Data Bus1 Z_{out} Control
0x50000000 Data Bus0 Z_{out} Control
APB 2.0 Devices (Size: 8MB)
0x4F800000 System controler
0x4F000000 PLL controller
0x4C000000 IrDA Controler
0x4B800000 UART controler 3
0x4B000000 UART controler 2
0x4A800000 UART controler 1
0x4A000000 UART controler 0
0x49800000 AGPO controler
0x49000000 GPIO controller
0x48800000 Watchdog Timer
0x48000000 Timer controller
0x47800000 PCIe controler
0x47000000 USB controller
0x43800000 I^2S Controler 4
0x43000000 I^2S Controler 3
0x42800000 I^2S Controler 2
0x42000000 I^2S Controler 1
0x41800000 I^2S Controler 0
0x40800000 SSI controler

Fig 10. Illustration of Memory Map in ASC8848/49/50 M1 version SoC

6.2 Boot modes

If the SD/SDHC memory card is present, the system will always boot from the memory card. If the SD card boot flow fails or the SD memory card is not present. The boot modes are decided by SYS_I_BOOT_MODE_SEL [1:0]. Therefore pull-up and pull-down resistors or jumpers should be placed on the system board in order to select the desired mode. These pins must be maintained in the same states after power-on. The different boot modes are described as follows.

Table 14. Boot modes

BOOT_MODE[1:0]	Descriptions
0x0	Boot from serial FLASH through SPI interface 0.

Table 14. Boot modes

BOOT_MODE[1:0]	Descriptions
0x1	Reserved.
0x2	Boot from NAND FLASH interface 0 with 4 address cycles.
0x3	Boot from NAND FLASH interface 0 with 5 address cycles.

6.3 Boot flow

6.3.1 SD card boot flow

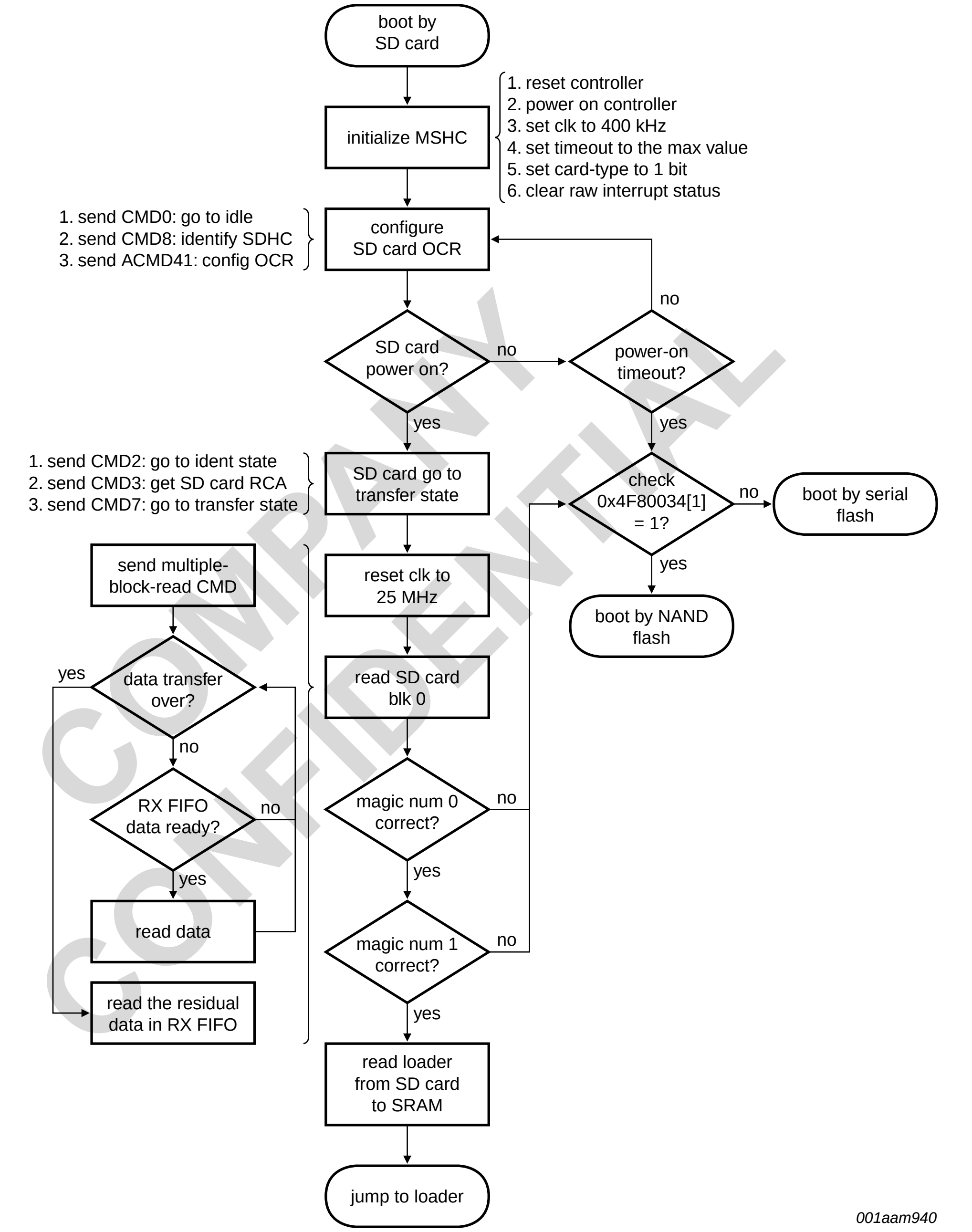


Fig 11. SD card boot flow

6.3.2 Serial flash boot flow

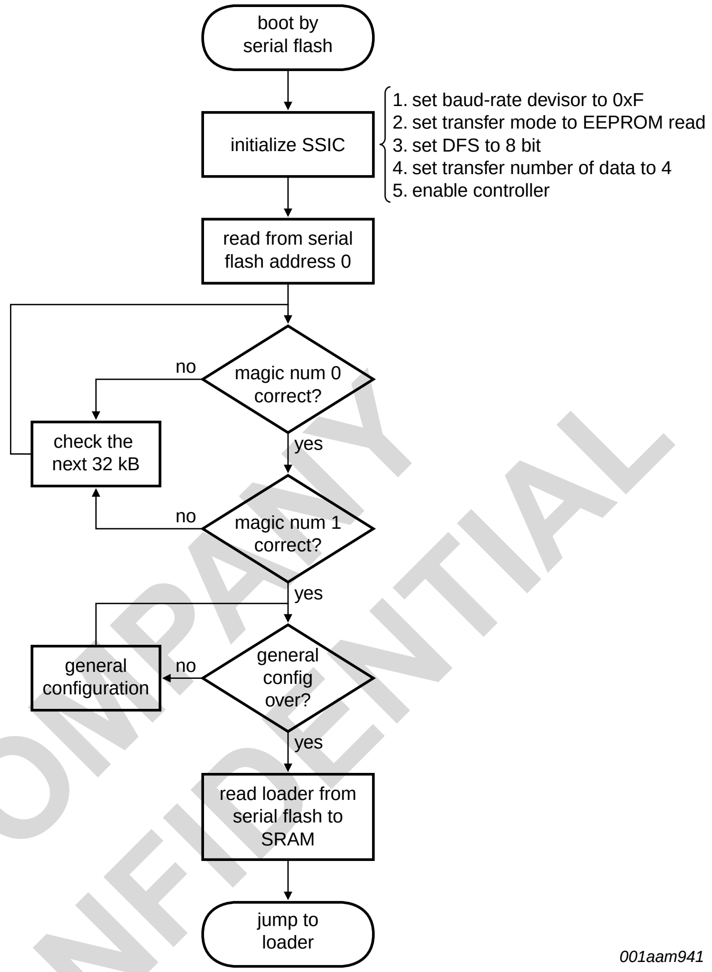


Fig 12. Serial flash boot flow

6.3.3 NAND flash boot flow

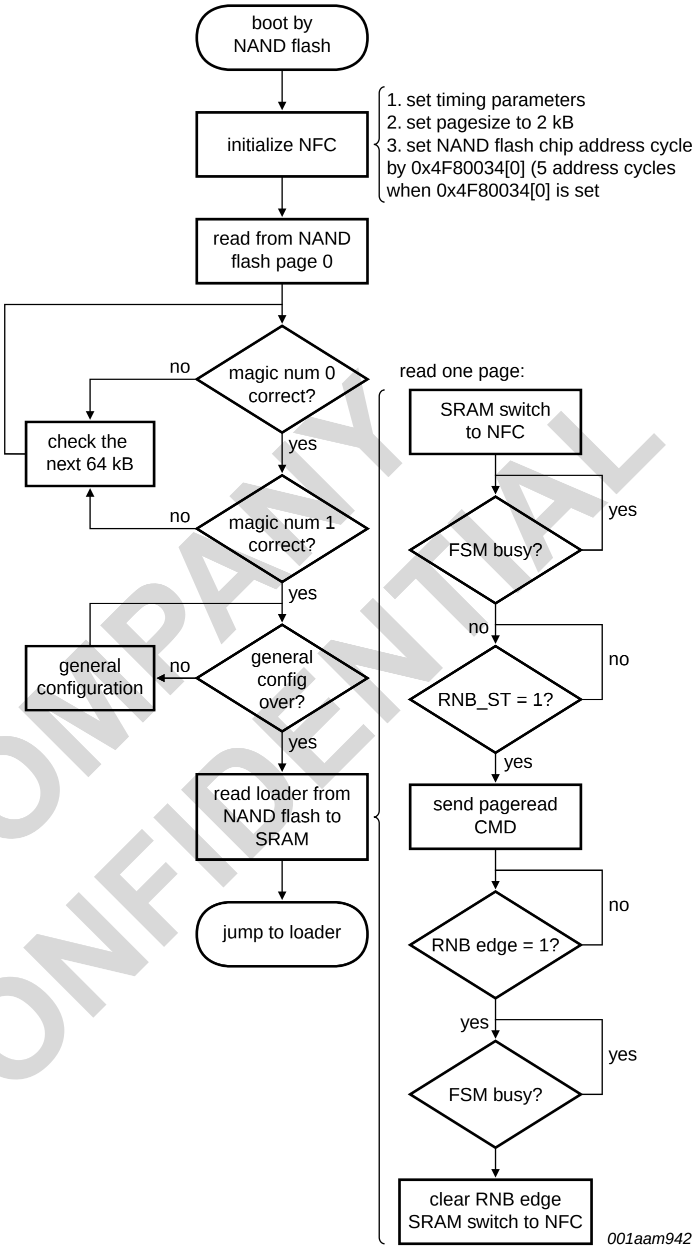


Fig 13. NAND flash boot flow

6.4 Boot image

Boot image for boot ROM code contains boot parameters, and loader code. Boot parameters are read by boot ROM code to check magic numbers and get loader information. Magic number#0 and magic number#1 are "0x82451282" and "0x28791166" for all three boot device images. If magic numbers are both correct, loader code would be transferred to SRAM. When loader is transferred over, programming counter is set to the base address of loader in SRAM and starts to execute loader.

6.4.1 SD card boot image

Magic numbers, loader address, loader size are SD card boot parameters. They have to be placed on the first block of the SD card. Magic number#0 should be written on address 0x0. Magic number#1, loader address, and loader size are at address 0x4, 0x8 and 0xC respectively.

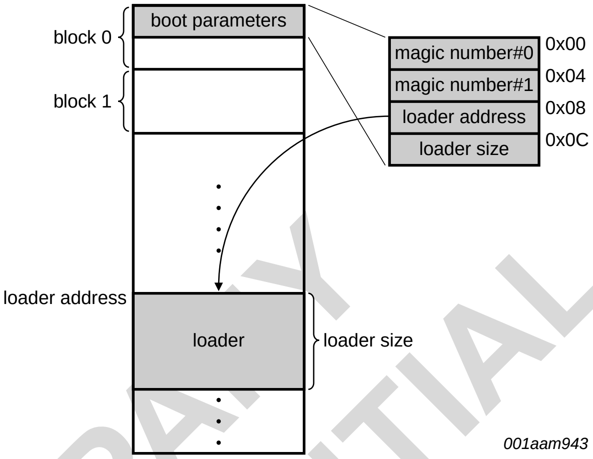


Fig 14. SD card boot image format

6.4.2 Serial flash boot image

Magic numbers, loader address header (pointer of loader address value), loader size header (pointer of loader size value), and general configuration header (pointer of general configuration section) are serial flash boot parameters. They should be placed on the same sector. Sector that contains boot parameters is the boot parameter sector.

Magic number#0 should be written on the base address of boot parameter sector. Magic number#1 should be written on boot parameter sector base address + 0x4. Loader address header should be written on boot parameter sector base address + 0x8. General configuration header should be written on boot parameter sector base address + 0xC. Loader size header should be written on boot parameter sector base address + 0x10.

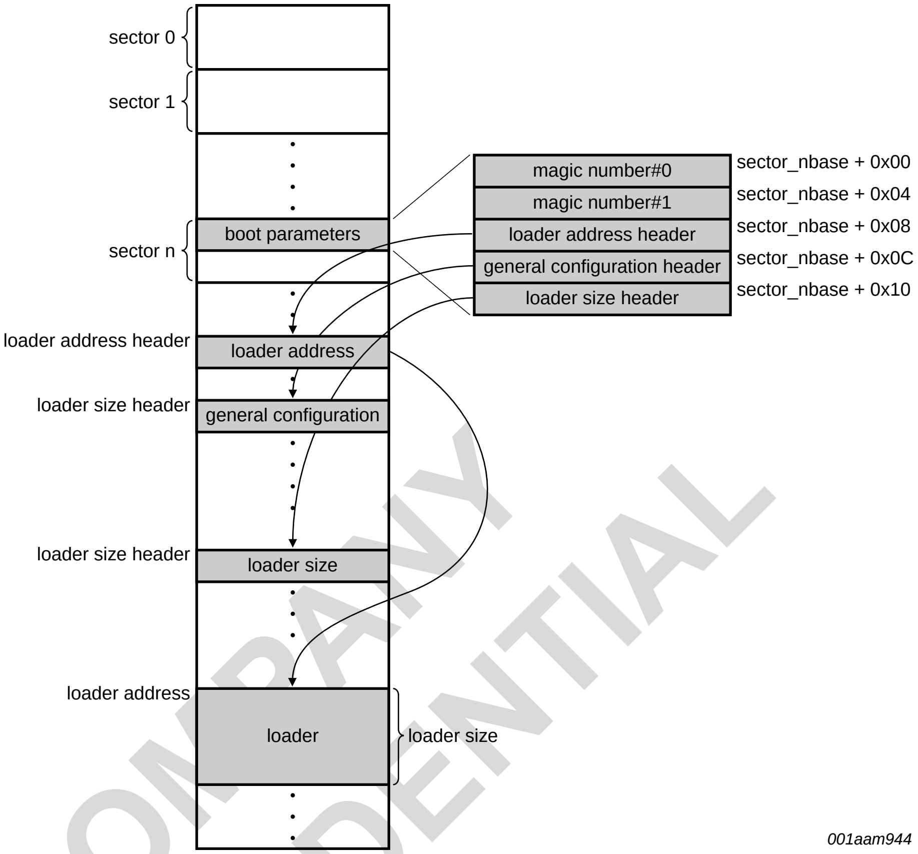


Fig 15. Serial flash boot image

6.4.3 NAND flash boot image

Magic numbers, loader address header (pointer of loader address value), and general configuration header (pointer of general configuration section) are NAND flash boot parameters. They should be placed on the same block. Block that contains boot parameters is the boot parameter block. Magic number#0 should be written on the base address of boot parameter block. Magic number#1 should be written on boot parameter block base address + 0x4. Loader address header should be written on boot parameter block base address + 0x8. General configuration header should be written on boot parameter block base address + 0xC. Loader size is fixed to be 2 kB.

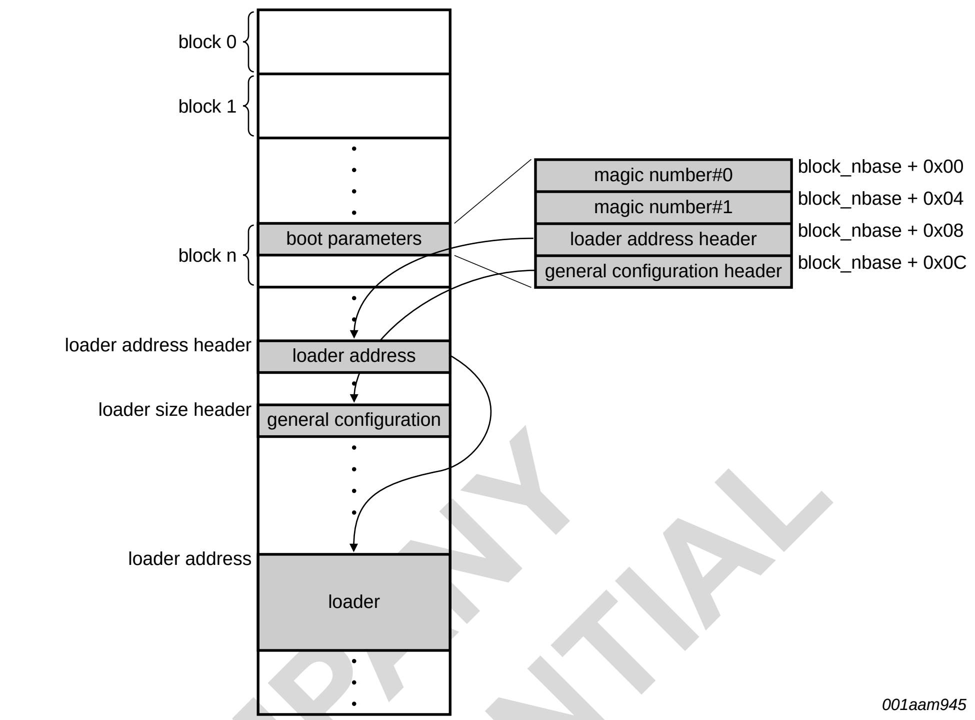


Fig 16. Nand flash boot image

6.5 Limitations

6.5.1 SD card boot code

1. SD / SDHC cards are both compatible with this boot ROM code. Because command parameter register in MSHC is 32 bit width, the maximum size of supported SD memory card should be 32 Gb. If loader is written at the address higher than 32 Gb in SD memory card, it couldn't be correctly accessed by boot ROM code.
2. SD card OCR configuration has a time-out mechanism. After 1000 times failure to check power-on, SD card boot terminates and serial flash boot or NAND flash boot is displaced.
3. Boot parameters have to be written into the first block in SD card. If the magic numbers are incorrect in the first block, SD card boot terminates and serial flash boot or NAND flash boot is displaced.
4. SD card loader is transferred by block. If loader starts from block#2 and ends to block#4, block#2-block#4 are all transferred into SRAM. Base address of loader is allowed to be unaligned to 512B (block size). Though there is an offset from SRAM base address to loader base address, it would be skipped when the program starts to execute loader in SRAM. The maximum loader size is the size of SRAM, 4608 B (equal to 9 blocks).

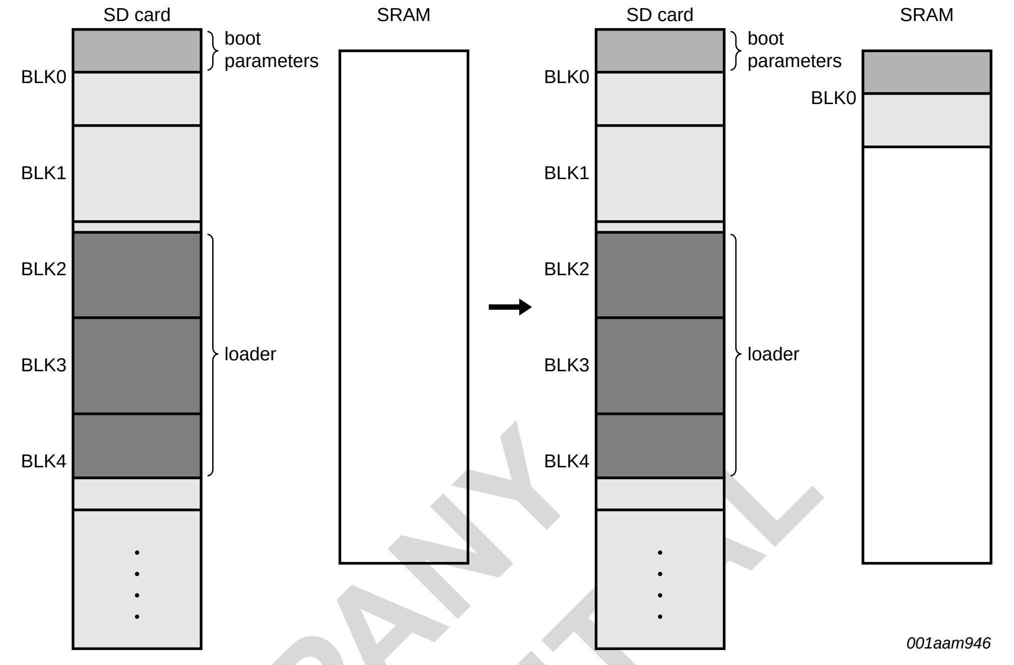


Fig 17. Read boot parameter block

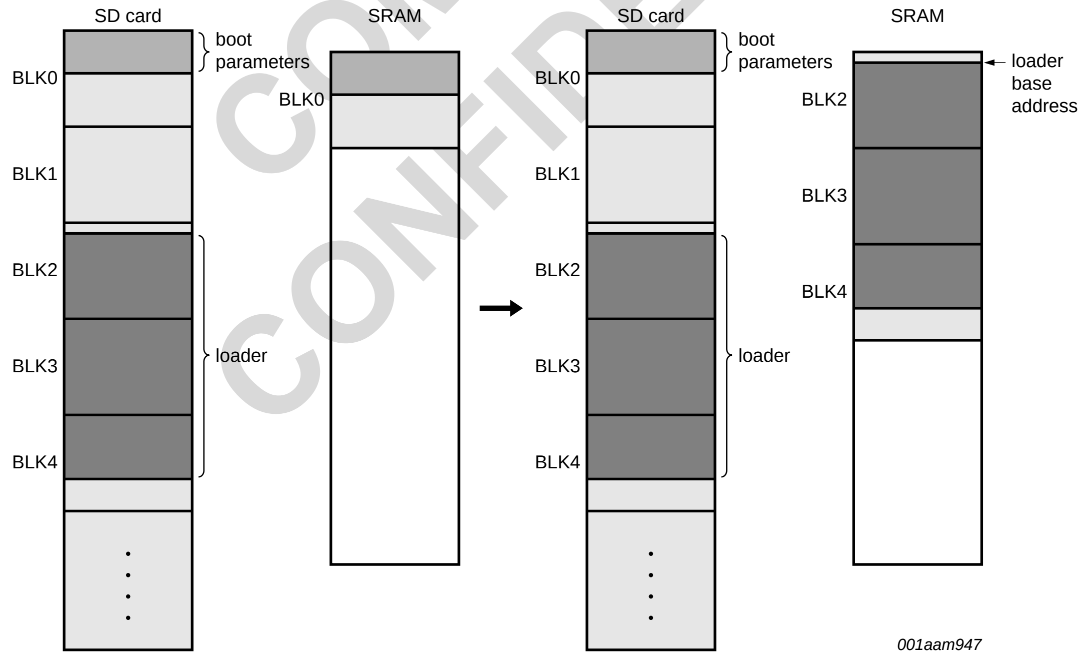


Fig 18. Read loader

6.5.2 Serial flash boot code

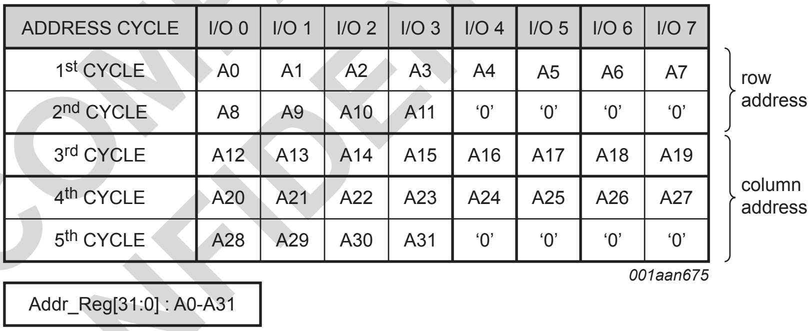
Because there are 3 address cycles sent to serial flash, supported serial flash chip has a size limit of 16 MB. If boot parameters or loader is programmed to address higher than 16 MB in serial flash, it couldn't be correctly accessed by boot ROM code.

Boot parameters can be programmed at any sector of serial flash which has a size smaller than 16 MB. Serial flash is infinitely scanned by 32 kB until magic numbers are hit.

Serial flash loader has a size limit of 4068 B (size of SRAM).

6.5.3 NAND flash boot code

Address of NAND flash chips is defined to be a 32 bits data in this boot ROM code. A relationship between NAND flash address bytes and the 32 bits data is shown in Figure 19 (Nand flash byte address). Because there are 20 bits of column address, maximum page number of NAND flash chip is 1048576. Therefore, the maximum size of NAND flash chip is 16 Gb or 32 Gb according to the page size (2 kB page size or 4 kB page size) of NAND flash chips. If boot parameters or loader code is programmed at address higher than the size limit, it cannot be correctly accessed. For the row address has only 12 bits, spare area could not be accessed in 4 kB page. Loader base address shouldn't be at the spare area in 4 kB page or it cannot be correctly accessed.



ADDRESS CYCLE	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st CYCLE	A0	A1	A2	A3	A4	A5	A6	A7	row address
2nd CYCLE	A8	A9	A10	A11	‘0’	‘0’	‘0’	‘0’	
3rd CYCLE	A12	A13	A14	A15	A16	A17	A18	A19	column address
4th CYCLE	A20	A21	A22	A23	A24	A25	A26	A27	
5th CYCLE	A28	A29	A30	A31	‘0’	‘0’	‘0’	‘0’	

Fig 19. Address codes

Page read operation is only executed once when transferring loader from NAND flash to SRAM, hence NAND flash loader cannot be programmed across pages and size cannot be greater than (2 k+64) bytes on 2 kB page size chips or (4 k+128) bytes on 4 kB page size chips.

Boot parameters can be programmed at any page of NAND flash. NAND flash is infinitely scanned by 64 kB until magic numbers are correct.

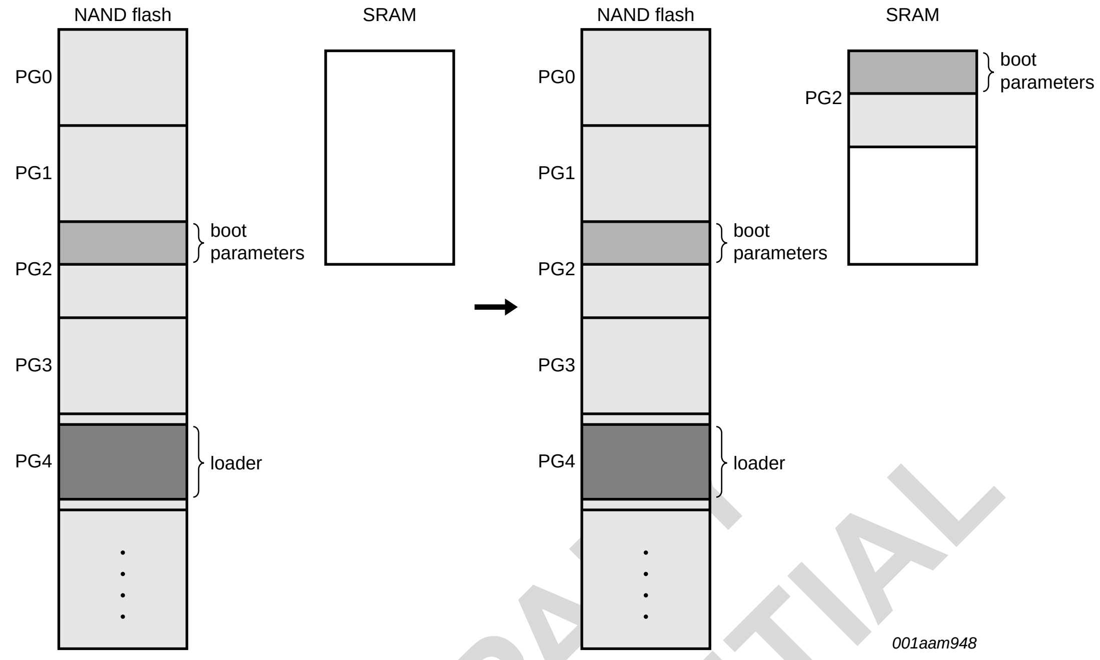


Fig 20. NAND Flash Boot Procedure: Read Boot Parameter Page

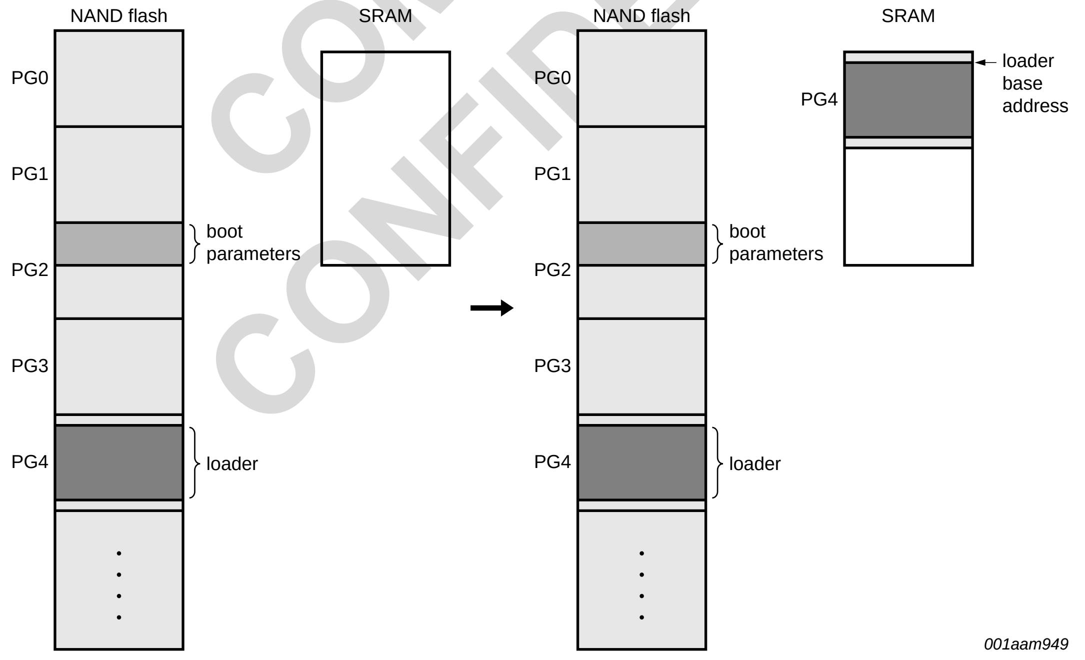


Fig 21. NAND Flash Boot Procedure: Read Loader

7. System controller, resets and clocks

This chapter describes the detailed functions of ASC8848/49/50/51 SoC system controller. The system controller provides an interface to configure the system level parameters through memory map register settings. It is also used to generate some system level clocks and reset signals. In the end of this chapter, the ASC8848/49/50/51 SoC clock and reset schemes are also described.

7.1 Features

7.1.1 Clock generation

The system controller generates clock signals for all IP modules used in ASC8848/49/50/51 project from the internal PLLs and the external clock signals. It also provides gated-clock control over individual modules.

7.1.2 Reset signal generation

The system controller also generates reset signals for all IP modules used in ASC8848/49/50/51 project from the external reset signal.

7.1.3 I/O pad control

The system controller can control output pad driving capability and input pad pull-up of ASC8848/49/50/51 chip

7.2 Memory map register

7.2.1 SYSC_VERSION (0x00000000)

Table 15. SYSC_VERSION

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x08	R	Major version number.
MINOR_VERSION	23 - 16	0x01	R	Minor version number.
BUILD_VERSION	15 - 08	0x00	R	ASC8848/49/50 M1 : Build version number.
		0x0C		ASC8848/49/50/51 M2 : Build version
REVISION	07 - 00	0x02	R	Revision number.

7.2.2 Reserved (0X00000004)

7.2.3 SYSC_CHIP_ID_0 (0x00000008)

Table 16. Chip ID information register 0

Name	Bit	Default	R/W	Description
CHIP_ID_0	31 - 00	0x415A4F4D	R	Chip ID 0.

7.2.4 SYSC_CHIP_ID_1 (0x0000000C)

Table 17. Chip ID information register 1.

Name	Bit	Default	R/W	Description
CHIP_ID_1	31 - 00	0x00005452	R	Chip ID 1.

7.2.5 SYSC_CHIP_ID_2 (0x00000010)

Table 18. Chip ID information register 1.

Name	Bit	Default	R/W	Description
CHIP_ID_2	31 - 00	0x00000000	R	Chip ID 2.

7.2.6 SYSC_CHIP_VERSION (0x00000014)

Chip version information register.

Table 19. Chip version information register

Name	Bit	Default	R/W	Description
CHIP_VERSION	31 - 00	0x01000000	R	ASC8848/49/50 M1 : Chip version
CHIP_VERSION	31 - 00	0x01000000	R	ASC8848/49/50/51 M2: Chip version

7.2.7 SYSC_CNT_CTRL (0x00000018)

Table 20. Embedded 64-bit counter control register.

Name	Bit	Default	R/W	Description
CNT_CLEAR	31 - 31	N/A	W	Write only embedded 64-bit counter clear control. 1’b0: Do nothing. 1’b1: Clear 64-bit embedded counter.
	30 - 28	0x0	R	Reserved.
CNT_DIV	27 - 00	0x0	R/W	64-bit counter clock frequency divider or precision multiplier. This value is used to determine the period per tick. Period per tick in the 64-bit counter = APB clock period x (CNT_DIV+1)

7.2.8 SYSC_CNT_LOW (0x0000001C)

Embedded 64-bit counter low 32-bit value register.

Table 21. Embedded 64-bit counter low 32-bit value register

Name	Bit	Default	R/W	Description
CNT_LOW	31 - 00	0x0	R	Low 32-bit value of the embedded 64-bit counter.

7.2.9 SYSC_CNT_HIGH (0x00000020)

Embedded 64-bit counter high 32-bit value register.

Table 22. Embedded 64-bit counter high 32-bit value register.

Name	Bit	Default	R/W	Description
CNT_HIGH	31 - 00	0x0	R	High 32-bit value of the embedded 64-bit counter.

7.2.10 SYSC_CLK_EN_CTRL_0 (0x00000024)

Internal module clock enable control register 0. For reserved fields, write the default value.

Table 23. Internal module clock enable control register 0

Name	Bit	Default	R/W	Description
SSIC_CLK_EN	31-31	0x1	R/W	SSIC module clock enable control. 1'b0: Disable APB clock for SSIC module. 1'b1: Enable APB clock for SSIC module.
PLLC_CLK_EN	30 - 30	0x1	R/W	PLLC module clock enable control. 1'b0: Disable APB clock for PLLC module. 1'b1: Enable APB clock for PLLC module.
PCIEC_CLK_EN	29 - 29	0x1	R/W	PCIEC module clock enable control. 1'b0: Disable AHB and PCIEC clocks for PCIEC module. 1'b1: Enable AHB and PCIEC clocks for PCIEC module.
NFC_CLK_EN	28 - 28	0x1	R/W	NFC module clock enable control. 1'b0: Disable AHB clock for NFC module. 1'b1: Enable AHB clock for NFC module.
MSHC_1_CLK_EN	27 - 27	0x1	R/W	MSHC 1 module clock enable control. 1'b0: Disable AHB and MSHC clocks for MSHC 1 module. 1'b1: Enable AHB and MSHC clocks for MSHC 1 module.
MSHC_0_CLK_EN	26 - 26	0x1	R/W	MSHC 0 module clock enable control. 1'b0: Disable AHB and MSHC clocks for MSHC 0 module. 1'b1: Enable AHB and MSHC clocks for MSHC 0 module.
MEAE_CLK_EN	25 - 25	0x1	R/W	MEAE module clock enable control. 1'b0: Disable AHB clock for MEAE module. 1'b1: Enable AHB clock for MEAE module.
JEBE_CLK_EN	24 - 24	0x1	R/W	JEBE module clock enable control. 1'b0: Disable AHB clock for JEBE module. 1'b1: Enable AHB clock for JEBE module.
IRE_CLK_EN	23 - 23	0x1	R/W	IRE module clock enable control. 1'b0: Disable AHB clock for IRE module. 1'b1: Enable AHB clock for IRE module.

Table 23. Internal module clock enable control register 0

Name	Bit	Default	R/W	Description
IRDAC_CLK_EN	22 - 22	0x1	R/W	IRDAC module clock enable control. 1'b0: Disable APB clock for IRDAC module. 1'b1: Enable APB clock for IRDAC module.
INTC_CLK_EN	21 - 21	0x1	R/W	INTC module clock enable control. 1'b0: Disable AHB clock for INTC module. 1'b1: Enable AHB clock for INTC module.
IBPE_CLK_EN	20 - 20	0x1	R/W	IBPE module clock enable control. 1'b0: Disable AHB clock for IBPE module. 1'b1: Enable AHB clock for IBPE module.
I2SSC_4_CLK_EN	19 - 19	0x1	R/W	I2SSC 4 module clock enable control. 1'b0: Disable APB and I2SSC clocks for I2SSC 4 module. 1'b1: Enable APB and I2SSC clocks for I2SSC 4 module.
I2SSC_3_CLK_EN	18 - 18	0x1	R/W	I2SSC 3 module clock enable control. 1'b0: Disable APB and I2SSC clocks for I2SSC 3 module. 1'b1: Enable APB and I2SSC clocks for I2SSC 3 module.
I2SSC_2_CLK_EN	17 - 17	0x1	R/W	I2SSC 2 module clock enable control. 1'b0: Disable APB and I2SSC clocks for I2SSC 2 module. 1'b1: Enable APB and I2SSC clocks for I2SSC 2 module.
I2SSC_1_CLK_EN	16 - 16	0x1	R/W	I2SSC 1 module clock enable control. 1'b0: Disable APB and I2SSC clocks for I2SSC 1 module. 1'b1: Enable APB and I2SSC clocks for I2SSC 1 module.
I2SSC_0_CLK_EN	15 - 15	0x1	R/W	I2SSC 0 module clock enable control. 1'b0: Disable APB and I2SSC clocks for I2SSC 0 module. 1'b1: Enable APB and I2SSC clocks for I2SSC 0 module.
	14 - 14	0x1	R/W	Reserved.
H4EE_CLK_EN	13 - 13	0x1	R/W	H4EE module clock enable control. 1'b0: Disable AHB and H4EE clocks for H4EE module. 1'b1: Enable AHB and H4EE clocks for H4EE module.
GPIOC_CLK_EN	12 - 12	0x1	R/W	GPIOC module clock enable control. 1'b0: Disable APB clock for GPIOC module. 1'b1: Enable APB clock for GPIOC module.

Table 23. Internal module clock enable control register 0

Name	Bit	Default	R/W	Description
GMAC_CLK_EN	11 - 11	0x1	R/W	GMAC module clock enable control. 1’b0: Disable AHB and GMAC clocks for GMAC module. 1’b1: Enable AHB and GMAC clocks for GMAC module.
DMAC_CLK_EN	10 - 10	0x1	R/W	DMAC module clock enable control. 1’b0: Disable AHB clock for DMAC module. 1’b1: Enable AHB clock for DMAC module.
DIE_CLK_EN	09 - 09	0x1	R/W	DIE module clock enable control. 1’b0: Disable AHB clock for DIE module. 1’b1: Enable AHB clock for DIE module.
	08 - 08	0x1	R/W	Reserved.
DCE_CLK_EN	07 - 07	0x1	R/W	DCE module clock enable control. 1’b0: Disable AHB clock for DCE module. 1’b1: Enable AHB clock for DCE module.
BRC_CLK_EN	06 - 06	0x1	R/W	BRC module clock enable control. 1’b0: Disable AHB clock for BRC module. 1’b1: Enable AHB clock for BRC module.
	05 - 05	0x1	R/W	Reserved.
APB3C_CLK_EN	04 - 04	0x1	R/W	APB3C module clock enable control. 1’b0: Disable AHB clock for APB3C module. 1’b1: Enable AHB clock for APB3C module.
	03 - 01	0x7	R/W	Reserved.
AGPOC_CLK_EN	00 - 00	0x1	R/W	AGPOC module clock enable control. 1’b0: Disable APB clock for AGPOC module. 1’b1: Enable APB clock for AGPOC module.

7.2.11 SYSC_CLK_EN_CTRL_1 (0x00000028)

Internal module clock enable control register 1. For reserved fields, write the default value.

Table 24. Internal module clock enable control register 1

Name	Bit	Default	R/W	Description
	31 - 13	0x0	R	Reserved.
I2SSC_RX_CLK_EN	12 - 12	0x1	R/W	I2SSC_O_RX_MCLK output enable control. 1’b0: Disable clock output on I2SSC_O_RX_MCLK pad. 1’b1: Enable clock output on I2SSC_O_RX_MCLK pad.
I2SSC_TX_CLK_EN	11 - 11	0x1	R/W	I2SSC_O_TX_MCLK output enable control. 1’b0: Disable clock output on I2SSC_O_TX_MCLK pad. 1’b1: Enable clock output on I2SSC_O_TX_MCLK pad.
WDTC_CLK_EN	10 - 10	0x1	R/W	WDTC module clock enable control. 1’b0: Disable APB clock for WDTC module. 1’b1: Enable APB clock for WDTC module.
VOC_CLK_EN	09 - 09	0x1	R/W	VOC module clock enable control. 1’b0: Disable AHB and VOC clocks for VOC module. 1’b1: Enable AHB and VOC clocks for VOC module.
VIC_ CLK_EN	08 - 07	0x3	R/W	VIC module clock enable control. 2’b00: Disable AHB and VIC clocks for VIC module. 2’b01: Enable AHB and VIC device 0 clocks and disable VIC device 1 clock for VIC module. 2’b10: Enable AHB and VIC device 1 clocks and disable VIC device 0 clock for VIC module. 2’b11: Enable AHB and VIC clocks for VIC module.
USBC_CLK_EN	06 - 06	0x1	R/W	USBC module clock enable control. 1’b0: Disable AHB and USBC clocks for USBC module. 1’b1: Enable AHB and USBC clocks for USBC module.
UARTC_3_CLK_EN	05 - 05	0x1	R/W	UARTC 3 module clock enable control. 1’b0: Disable APB and UARTC clocks for UARTC 3 module. 1’b1: Enable APB and UARTC clocks for UARTC 3 module.
UARTC_2_CLK_EN	04 - 04	0x1	R/W	UARTC 2 module clock enable control. 1’b0: Disable APB and UARTC clocks for UARTC 2 module. 1’b1: Enable APB and UARTC clocks for UARTC 2 module.
UARTC_1_CLK_EN	03 - 03	0x1	R/W	UARTC 1 module clock enable control. 1’b0: Disable APB and UARTC clocks for UARTC 1 module. 1’b1: Enable APB and UARTC clocks for UARTC 1 module.

Table 24. Internal module clock enable control register 1 *…continued*

Name	Bit	Default	R/W	Description
UARTC_0_CLK_EN	02 - 02	0x1	R/W	UARTC 0 module clock enable control. 1’b0: Disable APB and UARTC clocks for UARTC 0 module. 1’b1: Enable APB and UARTC clocks for UARTC 0 module.
TMRC_CLK_EN	01 - 01	0x1	R/W	TMRC module clock enable control. 1’b0: Disable APB clock for TMRC module. 1’b1: Enable APB clock for TMRC module.
	00 - 00	0x1	R/W	

7.2.12 SYSC_CLK_GEN_CFG (0x0000002C)

Internal clock speed control register.

Table 25. Internal clock speed control register

Name	Bit	Default	R/W	Description
GMAC_TX_CLK_CFG	31 - 30	0x0	R/W	GMAC TX clock speed selection. 2’b00: 125MHz (RGMII). 2’b01: 125MHz (GMII). 2’b10: 25MHz. 2’b11: 2.5MHz.
MSHC_1_CLK_CFG	29 - 29	0x0	R/W	MSHC 1 clock speed selection. 1’b0: 25MHz. 1’b1: 19.23MHz.
MSHC_0_CLK_CFG	28 - 28	0x0	R/W	MSHC 0 clock speed selection. 1’b0: 25MHz (for SD/SDIO). 1’b1: 19.23MHz (for MMC).
VIC_DEV_1_CLK_CFG	27 - 26	0x0	R/W	VIC device 1 clock speed selection. 2’b00: Full speed. 2’b01: Half speed. 2’b10: Quarter speed.
VIC_DEV_0_CLK_CFG	25 - 24	0x0	R/W	VIC device 0 clock speed selection. 2’b00: Full speed. 2’b01: Half speed. 2’b10: Quarter speed.
GMAC_REDUCED_MODE _EN	23-23	0x0	R	ASC8848/49/50 M1 - Reserved ASC8848/49/50/51 M2 - GMAC reduced mode enable selection. It controls the output GMAC TX phase. 1'b0: Shift 180 degrees. 1'b1: Shift 90 degrees
VOC_PLL_REF_SEL	22 - 22	0x0	R	ASC8848/49/50 M1 - Reserved ASC8848/49/50/51 M2 - VOC PLL reference clock selection. 1'b0: 24MHz crystal input (SYS_I_OSC_2_CLK). 1'b1: 27MHz oscillator input (VOC_I_CLK)

Table 25. Internal clock speed control register *...continued*

Name	Bit	Default	R/W	Description
VOC_CLK_DIV	21 - 16	0x02	R/W	VOC pixel clock divider. VOC pixel clock frequency = PLL 3 clock frequency/VOC_CLK_DIV
I2SSC_RX_MCLK_DIV	15 - 08	0x10	R/W	I^{2}SSC RX device master clock divider. I^{2}SSC RX master clock frequency = 270.336MHz/I2SSC_RX_MCLK_DIV
I2SSC_TX_MCLK_DIV	07 - 00	0x10	R/W	I^{2}SSC TX device master clock divider. I^{2}SSC TX master clock frequency = 270.336MHz/I2SSC_TX_MCLK_DIV

7.2.13 SYSC_MON_CLK_SEL (0x00000030)

Monitor clock selection register.

Table 26. Monitor clock selection register

Name	Bit	Default	R/W	Description
	31 - 14	0x0	R	Reserved.
MON_CLK_1_SEL	13 - 08	0x15	R/W	Monitor clock 1 selection control. 6’h00: AHB clock. 6’h01: APB clock. 6’h02: GMAC TX positive clock. 6’h03: GMAC TX negative clock. 6’h04: GMAC RX positive clock. 6’h05: GMAC RX negative clock. 6’h06: H4EE clock. 6’h07: HOSTC clock. 6’h08: I2SSC 0 positive bit clock. 6’h09: I2SSC 0 negative bit clock. 6’h0A: I2SSC 1 positive bit clock. 6’h0B: I2SSC 1 negative bit clock. 6’h0C: I2SSC 2 positive bit clock. 6’h0D: I2SSC 2 negative bit clock. 6’h0E: I2SSC 3 positive bit clock. 6’h0F: I2SSC 3 negative bit clock. 6’h10: I2SSC 4 positive bit clock. 6’h11: I2SSC 4 negative bit clock.
MON_CLK_1_SEL	13 - 08	0x15	R/W	6’h1A: USBC core clock. 6’h1B: USBC PHY clock. 6’h1C: VIC device 0 pixel clock. 6’h1D: VIC device 0 divided pixel clock. 6’h1E: VIC device 1 pixel clock. 6’h1F: VIC device 1 divided pixel clock. 6’h20: VOC pixel clock. 6’h21-6’h3F: 1’b0.

Table 26. Monitor clock selection register *…continued*

Name	Bit	Default	R/W	Description
	07 - 06	0x0	R	Reserved.
MON_CLK_0_SEL	05 - 00	0x12	R/W	Monitor clock 1 selection control. 6'h00: AHB clock. 6'h01: APB clock. 6'h02: GMAC TX positive clock. 6'h03: GMAC TX negative clock. 6'h04: GMAC RX positive clock. 6'h05: GMAC RX negative clock. 6'h06: H4EE clock. 6'h07: HOSTC clock. 6'h08: I2SSC 0 positive bit clock. 6'h09: I2SSC 0 negative bit clock. 6'h0A: I2SSC 1 positive bit clock. 6'h0B: I2SSC 1 negative bit clock. 6'h0C: I2SSC 2 positive bit clock. 6'h0D: I2SSC 2 negative bit clock. 6'h0E: I2SSC 3 positive bit clock. 6'h0F: I2SSC 3 negative bit clock.
MON_CLK_0_SEL	05 - 00	0x12	R/W	6'h10: I2SSC 4 positive bit clock. 6'h11: I2SSC 4 negative bit clock. 6'h12: MSHC 0 positive card clock. 6'h13: MSHC 0 negative card clock. 6'h14: MSHC 0 RX card clock. 6'h15: MSHC 1 positive card clock. 6'h16: MSHC 1 negative card clock. 6'h17: MSHC 1 RX card clock. 6'h18: PCIEC core clock. 6'h19: UARTC clock. 6'h1A: USBC core clock. 6'h1B: USBC PHY clock. 6'h1C: VIC device 0 pixel clock. 6'h1D: VIC device 0 divided pixel clock. 6'h1E: VIC device 1 pixel clock. 6'h1F: VIC device 1 divided pixel clock. 6'h20: VOC pixel clock. 6'h21-6'h3F: 1'b0.

7.2.14 SYSC_SYS_INFO (0x00000034)

System information register.

Table 27. System information register

Name	Bit	Default	R/W	Description
	31 - 06	0x0	R	Reserved.
GMAC_TX_DIR	05 - 05	0x0	R	GMAC TX clock direction information. 1’b0: Internal generated clock. 1’b1: External clock source.
GMAC_SPEED_INFO	04 - 03	0x0	R	GMAC speed information. 2’b0X: 1000Mbps. 2’b10: 10Mbps. 2’b11: 100Mbps.
GMAC_IO_INFO	02 - 02	0x0	R	GMAC interface voltage information. 1’b0: GMII/MII interface, 3.3V. 1’b1: RGMII interface, 2.5V.
BOOT_MODE_INFO	01 - 00	0x0	R	Boot mode information. 2’b00: Boot from serial FLASH through SPI interface 0. 2’b01: Reserved. 2’b10: Boot from NAND FLASH interface 0 with 4 address cycles. 2’b11: Boot from NAND FLASH interface 0 with 5 address cycles.

7.2.15 Reserved (0x00000038~0x00000040)

7.2.16 SYSC_PAD_EN_CTRL (0x00000044)

Pad enable control register.

Table 28. Pad enable control register

Name	Bit	Default	R/W	Description
	31 - 28	0x0	R	Reserved.
WDTC_PAD_EN	27	0x1	R/W	WDTC interface pad enable control.
VOC_PAD_EN	26 - 24	0x7	R/W	VOC interface pad enable control. Bit 0: Byte 0 output pad enable control. Bit 1: Byte 1 output pad enable control. Bit 2: Byte 2 output pad enable control.
	23 - 21	0x0	R	Reserved.
VIC_DEV_1_PAD_EN	20	0x1	R/W	VIC device 1 interface pad enable control.
VIC_DEV_0_PAD_EN	19	0x1	R/W	VIC device 0 interface pad enable control.
USBC_PAD_EN	18	0x1	R/W	USBC interface pad enable control.
UARTC_3_PAD_EN	17	0x1	R/W	UARTC 3 interface pad enable control.
UARTC_2_PAD_EN	16	0x1	R/W	UARTC 2 interface pad enable control.
UARTC_1_PAD_EN	15	0x0	R/W	UARTC 1 interface pad enable control.
UARTC_0_PAD_EN	14	0x0	R/W	UARTC 0 interface pad enable control.
SSIC_PAD_EN	13	0x1	R/W	SSIC interface pad enable control.

Table 28. Pad enable control register *…continued*

Name	Bit	Default	R/W	Description
NFC_PAD_EN	12	0x1	R/W	NFC interface pad enable control.
MSHC_1_PAD_EN	11	0x1	R/W	MSHC 1 interface pad enable control.
MSHC_0_PAD_EN	10	0x1	R/W	MSHC 0 interface pad enable control.
I2SSC_4_PAD_EN	09	0x1	R/W	I2SSC 4 interface pad enable control.
I2SSC_3_PAD_EN	08	0x1	R/W	I2SSC 3 interface pad enable control.
I2SSC_2_PAD_EN	07	0x1	R/W	I2SSC 2 interface pad enable control.
I2SSC_1_PAD_EN	06	0x1	R/W	I2SSC 1 interface pad enable control.
I2SSC_0_PAD_EN	05	0x1	R/W	I2SSC 0 interface pad enable control.
HOSTC_PAD_EN	04	0x1	R/W	HOSTC interface pad enable control.
	03	0x0	R	Reserved.
GMAC_PAD_EN	02	0x1	R/W	GMAC interface pad enable control.
	01 - 00	0x0	R	Reserved.

7.2.17 SYSC_IF_CTRL (0x00000048)

Table 29. Interface control register

Name	Bit	Default	R/W	Description
	31-04	0x1042020	R	Reserved
VIC_IF_PWR_LEVEL	03-03	0x0	R/W	ASC8848/49/50 M1 - Reserved
				ASC8848/49/50/51 M2 - VIC IO pad voltage level selection. 1'b0: 2.5~3.3V. 1'b1: 1.8V.
GMAC_IF_PWR_LEVEL	02-02	0x0	R/W	ASC8848/49/50 M1 -Reserved
				ASC8848/49/50/51 M2 - GMAC IO pad voltage level selection. 1'b0: 3.3V. 1'b1: 2.5V.
GMAC_TX_CLK_DIR	01-01	0x0	R/W	ASC8848/49/50 M1 - Reserved
				ASC8848/49/50/51 M2 - GMAC Tx clock direction selection. 1'b0: Internal Tx clock source (PLL 1). 1'b1: External Ethernet PHY Tx clock source
	00 - 00	0x0		Reserved

7.2.18 SYSC_SLEW_CTRL (0x0000004C)

Output pads slew rate control register.

Table 30. Output pads slew rate control register

Name	Bit	Default	R/W	Description
	31 - 02	0x0	R	Reserved.
VOC_SLEW_RATE_CTRL	01	0x1	R/W	VOC output pads slew rate control. 1’b0: Slow. 1’b1: Fast.
GMAC_SLEW_RATE_CTRL	00	0x1	R/W	GMAC output pads slew rate control. 1’b0: Slow. 1’b1: Fast.

7.2.19 SYSC_PULL_CTRL (0x00000050)

Output and bidirectional pads pull up and pull down control register.

Table 31. Output and bidirectional pads pull up and pull down control register

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	R	Reserved.
WDTC_CMD_PUP_EN	15	0x1	R/W	WDTC_O_nRST pad pull up enable control.
UARTC_3_SDA_PUP_EN	14	0x1	R/W	UARTC_3_O_SDA pad pull up enable control.
UARTC_2_SDA_PUP_EN	13	0x1	R/W	UARTC_2_O_SDA pad pull up enable control.
UARTC_1_SDA_PUP_EN	12	0x1	R/W	UARTC_1_O_SDA pad pull up enable control.
UARTC_0_SDA_PUP_EN	11	0x1	R/W	UARTC_0_O_SDA pad pull up enable control.
SSIC_SEL_PUP_EN	10	0x1	R/W	SSIC_O_nSEL pads pull up enable control.
NFC_DATA_PUP_EN	09	0x1	R/W	NFC_IO_DATA pads pull up enable control.
NFC_BUSY_PUP_EN	08	0x1	R/W	NFC_I_nRB pad pull up enable control.
NFC_COM_PUP_EN	07	0x1	R/W	NFC common pads pull up enable control.
MSHC_1_DATA_PUP_EN	06	0x1	R/W	MSHC_1_IO_DATA pads pull up enable control.
MSHC_1_CMD_PUP_EN	05	0x1	R/W	MSHC_1_IO_CMD pad pull up enable control.
MSHC_1_COM_PUP_EN	04	0x1	R/W	MSHC 1 common pads pull up enable control.
MSHC_0_DATA_PUP_EN	03	0x1	R/W	MSHC_0_IO_DATA pads pull up enable control.
MSHC_0_CMD_PUP_EN	02	0x1	R/W	MSHC_0_IO_CMD pad pull up enable control.
MSHC_0_COM_PUP_EN	01	0x1	R/W	MSHC 0 common pads pull up enable control.
HOSTC_COM_PUP_PDN_EN	00	0x1	R/W	HOSTC common pads pull up and pull down enable control.

7.2.20 SYSC_DRV_STRENGTH_CTRL_0 (0x00000054)

Output and bidirectional pads driving strength control register 0.

Table 32. Output and bidirectional pads driving strength control register 0

Name	Bit	Default	R/W	Description
-	31 - 20	0x0	R	Reserved.
AGPOC_GPIOC_DRV_STR	19 - 00	0x0	R/W	AGPOC/GPIOC interface output driving strength control bit 0, which are combined with AGPOC_GPIOC_DRV_STR_1. 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

7.2.21 SYSC_DRV_STRENGTH_CTRL_1 (0x00000058)

Output and bidirectional pads driving strength control register 1.

Table 33. Output and bidirectional pads driving strength control register 1

Name	Bit	Default	R/W	Description
-	31 - 20	0x0	R	Reserved.
AGPOC_GPIOC_DRV_STR	19 - 00	0xFFFFF	R/W	AGPOC/GPIOC interface output driving strength control bit 1.

7.2.22 SYSC_DRV_STRENGTH_CTRL_2 (0x0000005C)

Output and bidirectional pads driving strength control register 2.

Table 34. Output and bidirectional pads driving strength control register 2

Name	Bit	Default	R/W	Description
-	31 - 28	0x0	R	Reserved.
SYSC_DRV_STR	27 - 26	0x0	R/W	SYSC interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
WDTC_DRV_STR	25 - 24	0x1	R/W	WDTC interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
VOC_DRV_STR	23 - 22	0x2	R/W	VOC interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
USBC_DRV_STR	21 - 20	0x1	R/W	USBC interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA

Table 34. Output and bidirectional pads driving strength control register 2 *…continued*

Name	Bit	Default	R/W	Description
UARTC_3_DRV_STR	19 - 18	0x2	R/W	UARTC 3 interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
UARTC_2_DRV_STR	17 - 16	0x2	R/W	UARTC 2 interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
UARTC_1_DRV_STR	15 - 14	0x2	R/W	UARTC 1 interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
UARTC_0_DRV_STR	13 - 12	0x2	R/W	UARTC 0 interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
SSIC_DRV_STR	11 - 10	0x1	R/W	SSIC interface output strength control. 2’b00: 2mA. 2’b01: 4mA. 2’b10: 8mA. 2’b11: 12mA.
NFC_DRV_STR	09 - 08	0x1	R/W	NFC interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
MSHC_1_DRV_STR	07 - 06	0x2	R/W	MSHC 1 interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
MSHC_0_DRV_STR	05 - 04	0x2	R/W	MSHC 0 interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
I2SSC_DRV_STR	03 - 02	0x1	R/W	I2SSC interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA
HSOTC_DRV_STR	01 - 00	0x1	R/W	HOSTC interface output strength control. 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 12mA

7.3 Clock Signal Distributions

7.3.1 System Clocks

The host processor, AHB and APB clocks are generated by PLL 0 and the clock ratio is 6:2:1. The PLL ratio is not configurable. Refer to Section 13.3 for the PLL ratio of ASC8848/49/50/51.

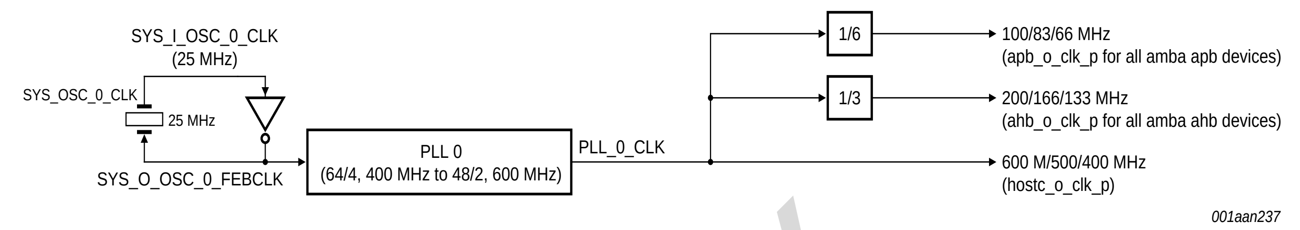


Fig 22. System clock scheme

7.3.2 Giga-Bit Ethernet MAC

For the Giga-bit Ethernet applications, there are two kinds of the transmitter clock (TX_CLK), TX_CLK from PHY and TX_CLK from MAC. MMR_I_GMAC_TX_CLK_DIR from MMR (SYS_I_GMAC_TX_CLK_DIR for ASC8848/49/50 M1 version) is used to control the TX_CLK direction. MMR_I_GMAC_TX_CLK_CFG[1:0] from MMR is used to select the speed mode if TX_CLK is generated by MAC. 2.5/25/125MHz clocks are generated from PLL 1. The PLL ratio is not configurable because the clock rates for 10/100/1000 are well defined. To support RGMII in ASC8849/50 M2 version and ASC8851, the output TX_CLK could be 90 degrees phase shift on-chip to maximize the PHY sampling window through MMR_I_GMAC_REDUCED_MODE_EN."

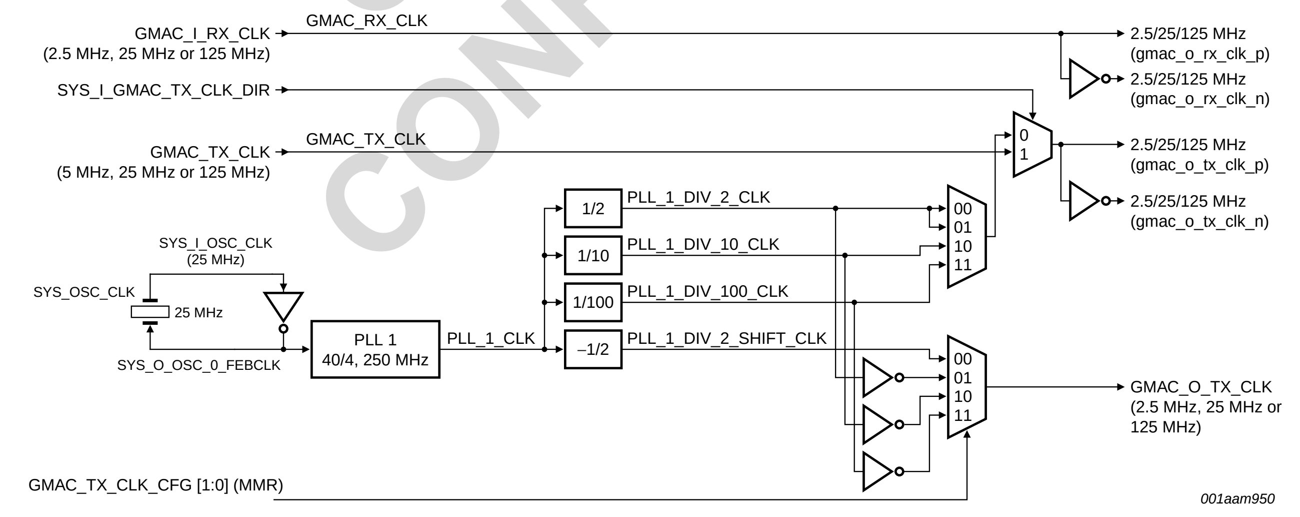


Fig 23. Gigabit Ethernet Clock Scheme (for ASC8850/49/48 M1)

7.3.3 Mobile Storage Controller

There are two clocks for the mobile storage controller. They are generated from PLL 1. The 19.23 MHz clock is for MMC cards while 25 MHz clock is for SD or SDIO cards. The clock rate is chose by MSHC_0_CLK_CFG and MSHC_1_CLK_CFG from MMR.

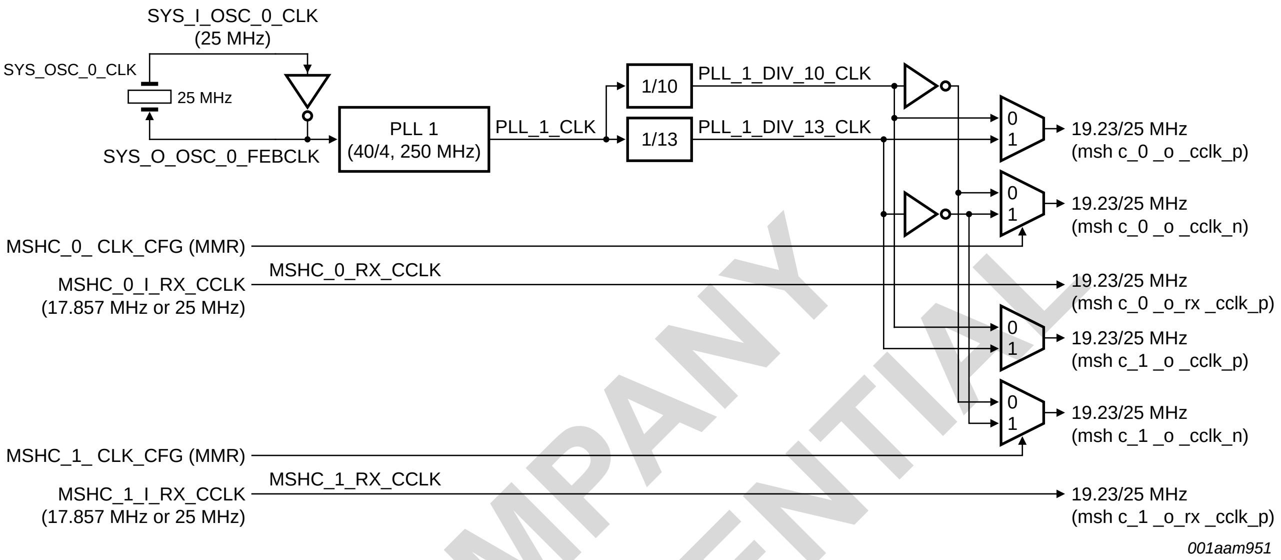


Fig 24. Mobile Storage Controller Clock Scheme

7.3.4 I^{2}S and UART

The 18.432 MHz system clock (SYS_I_OSC_1_CLK) is directly used for I^{2}S and UART. The default settings of PLL 2 and a divide-by-3 divider will generate 270.336 MHz clock I^{2}S master clock is generated by dividing this clock by I2SSC_RX_MCLK_DIV and I2SSC_TX_MCLK_DIV. Since we have five I^{2}S controllers, four for RX-only and one for RX and TX, we could set different master clocks for RX-only and full-duplex I^{2}S controllers respectively. To configure the PLL for other settings, please refer to Chapter 10.

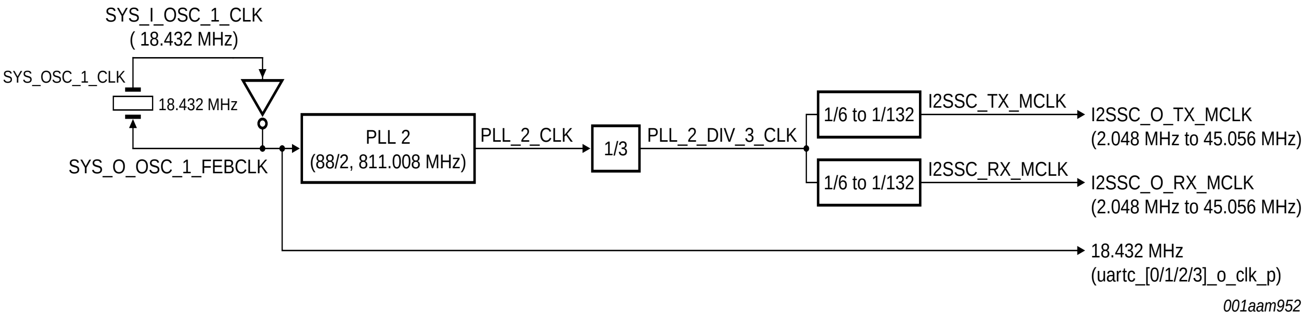


Fig 25. I^{2}S and UART Clock Scheme

The relationship between the master clock and the audio sample rate is either 256 fs or 384 fs depending on the settings on the audio codec chips.

Table 35. Relationship between master clock and audio sample

Sample Rate (kHz)	256 fs		384 fs	
	Master Clock (MHz)	MCLK_DIV	Master Clock (MHz)	MCLK_DIV
8	2.048	132	3.072	88
16	4.096	66	6.144	44
32	8.192	33	12.288	22
44	11.264	24	16.896	16
48	12.288	22	18.432	N/A

7.3.5 Video Output Controller

PLL 3 is dedicated for the video display pixel clock generation. The default setting of PLL 3 and the divider will generate 27MHz clock for TV applications. It could be configured up to 180MHz for LCD panel output or 148.5MHz BT.1120p (in case of ASC8848/49/50 M1 version it is limited to 125 MHz). To configure the PLL for other settings, please refer to Chapter 10. The reference clock is selectable from VOC_I_CLK or SYS_I_OSC_2_CLK through MMR_I_VOC_PLL_SRC_SEL (SYSC_CLK_GEN_CFG[22]) for ASC8848/49/50 M2 version and ASC8851.

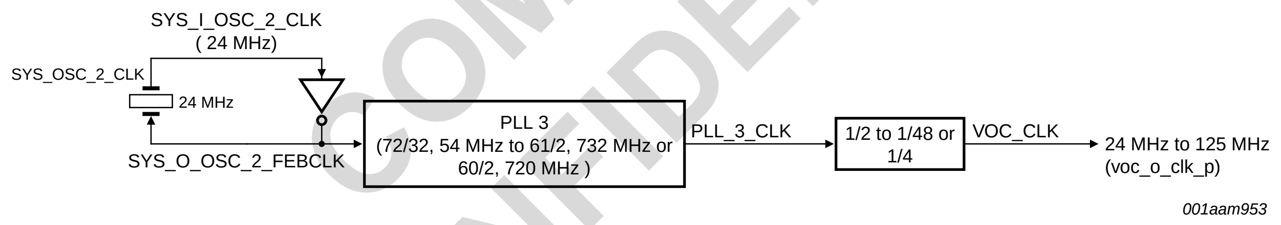


Fig 26. Video Output Controller Clock Scheme

7.3.6 USB

If USB function is required, SYS_I_OSC_2_CLK must be fed with 24MHz clock. PLL inside USB PHY will generate 30 MHz clock for internal UTMI bus and 480MHz clock for USB bus communication.

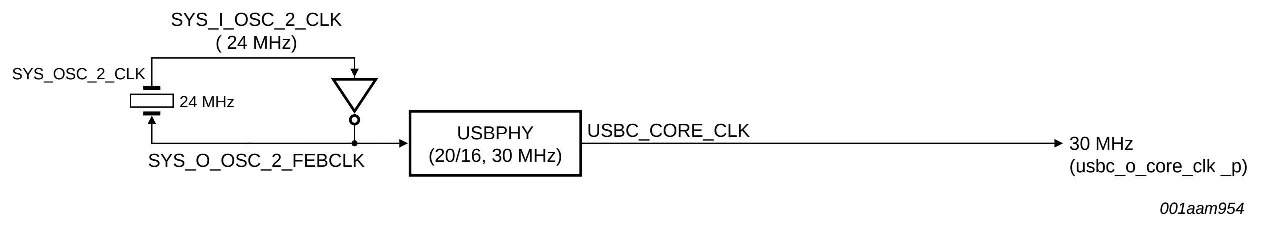


Fig 27. USB clock scheme

7.3.7 Video Input Controller

There are two physical capture devices in ASC8848/49/50/51 SoC. Each one needs two clocks, PCLK and DIV_PCLK. If the video source is a multi-channel video decoder, which means video channels are time-division-multiplexed into one video stream, DIV_PCLK must be set to 27 MHz through VIC_DEV_0_CLK_CFG and VIC_DEV_1_CLK_CFG. If the video source is a single-channel video decoder or a CMOS sensor, PCLK and DIV_PCLK must be the same.

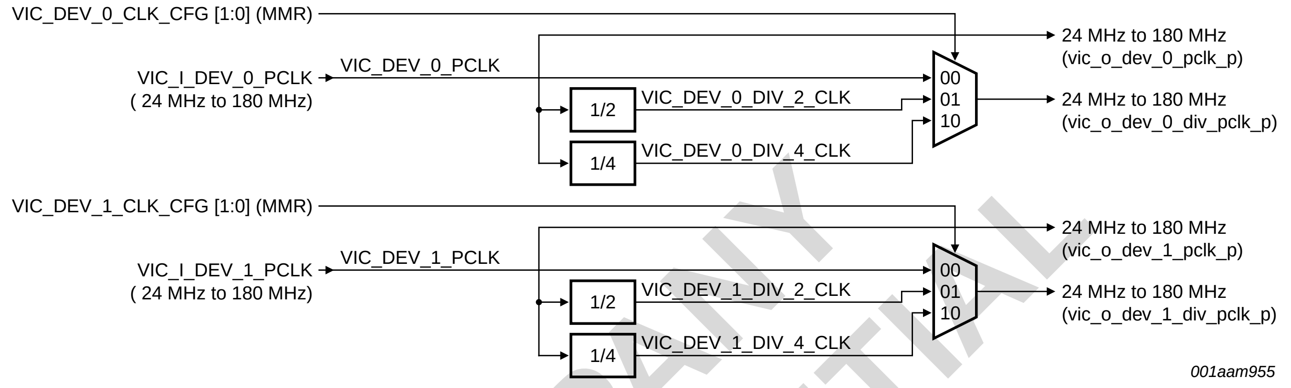


Fig 28. Video Input Controller Clock Scheme

7.3.8 PCI Express

The PCI Express controller needs a differential 100 MHz clock on board fed into PCIEC_I_REFCLK_P and PCIEC_I_REFCLK_M. Through the internal PLL in PCIe PHY, 125 MHz clock is generated for the PCI Express controller.

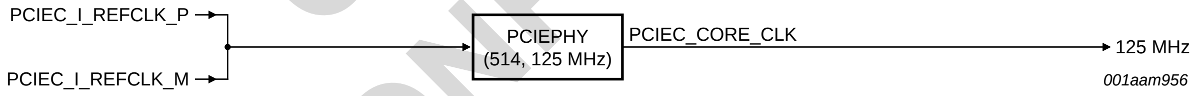


Fig 29. PCI express clock scheme

7.4 Reset signal generation

ASC8848/49/50/51 SoC use low active reset signal in the input system reset signal, SYS_I_nRST. Figure 30 shows the reset signal generation in ASC8848/49/50/51 SoC. Usually an external reset IC is used on board to generate the power-on reset for the whole system. In addition, the reset IC could also receive the external trigger to assert the system reset. If the system is not responding within a specific period, the watchdog timer inside ASC8848/49/50/51 SoC will trigger WDTC_O_nRST (active-low) and the external reset IC will reboot the whole system to make the system back to alive.

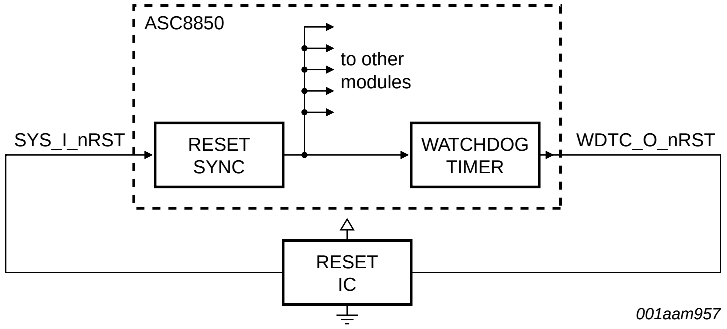


Fig 30. Reset signal generation

8. Boot ROM

8.1 General description

The boot ROM contains the boot codes to perform the boot sequence and load the boot program from different devices, such as SD card, serial Flash memory or NAND Flash memory. There is a SRAM inside the boot ROM controller for the system applications.

8.2 Features

8.2.1 Read Only Memory (ROM)

Support 2048 byte read only memory for boot codes.

8.2.2 Static Random Access Memory (SRAM)

Support 4608 byte static random access memory for the system applications. This memory is shared with the internal buffer of the NAND Flash controller.

8.3 Memory map register

8.3.1 ROM block (0x00000000~0x000007FF)

8.3.2 RAM block (0x00001000~0x000021FF)

8.3.3 BRC_VERSION (0x00004000)

Version information register.

Table 36. Version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x03	R	Major version number.
MINOR_VERSION	23 - 16	0x02	R	Minor version number.
BUILD_VERSION	15 - 08	0x00	R	Build version number.
REVISION	07 - 00	0x09	R	Revision number.

8.3.4 BRC_CTRL (0x00004004)

Control register.

Table 37. Control register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved.
DATA_DIR	00	0x0	R/W	Internal SRAM buffer access direction. 1'b0: Access through AHB (from the host processor). 1'b1: Access through external SRAM interface (from the NAND Flash controller).

9. DDR-II SDRAM controller (For ASC8848/49/50 M1 version only)[2]

9.1 Features

There are two DDR-II SDRAM controllers (DDR2SDMC) inASC8848/49/50M1 version SoC. Each one provides an interface between AMBA AHB bus and external DDR-II SDRAM. They can receive AMBA AHB requests, encode them into DDR-II SDRAM standard commands and then send them to external DDR-II SDRAM. It also has an 8-entry write queue to fulfill zero-wait-state AMBA AHB write access.

9.1.1 Data width

Supports 16-bit data width on external DDR-II SDRAM interface.

9.1.2 External bank

Supports only 1 external bank number.

9.1.3 Memory size

Supports 32 MB, 64 MB, 128 MB, 256 MB, 512 MB and 1 GB external memory sizes.

9.1.4 Data type

Supports 8-bit, 16-bit, 32-bit, and 64-bit data access on AMBA AHB bus.

9.1.5 Page number

Supports 8192, 16384, or 32768 page numbers.

9.1.6 Bank number

Supports 4 or 8 internal banks.

[2] **Remark:** For ASC8848/49/50 M2 version and ASC8851 SDRAM Controller, refer to chapter 10

9.1.7 Burst type

For data writing, the controller can support zero-wait-state random data write crossing at least two different pages. For data reading, any kind of burst type is supported without any latency after the first data is ready.

9.2 Memory map register

All timing parameters are in DRAM clcock cycles. Calculate them based on DRAM databook.

9.2.1 DDR2SDMC_VERSION (0x00000000)

Version information register.

Table 38. Version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x08	R	Major version number.
MINOR_VERSION	23 - 16	0x00	R	Minor version number.
BUILD_VERSION	15 - 08	0x00	R	Build version number.
REVISION	07 - 00	0x02	R	Revision number.

9.2.2 DDR2SDMC_CTRL (0x00000004)

Main control register.

Table 39. Main control register

Name	Bit	Default	R/W	Description
-	31 - 10	0x0	-	Reserved.
DYNAMIC_ODT_CTRL	09 - 09	0x1	R/W	Dynamic ODT control. 1’b0: Disable dynamic ODT control. 1’b1: Enable dynamic ODT control.
PLL_TEST_SEL	08 - 07	0x0	R/W	PHY PLL test signal selection. 2’b00: Disable PHY PLL test signal output. 2’b10: Select PHYAC digital output. 2’b11: Select PHYDATX8 digital output.
PHY_UPDATE_EN	06 - 06	0x0	R/W	PHY PVT auto-update indicator. 1’b0: Disable PHY PVT auto-update mechanism. 1’b1: Enable PHY PVT auto-update mechanism.
PAD_ UPDATE_CTRL	05 - 04	0x0	R/W	PAD PVT auto-update control. 2’b00: Disable all PAD PVT auto-update. 2’b01: Enable PAD PVT auto-update mechanism in data lanes. 2’b10: Enable PAD PVT auto-update mechanism in command lane. 2’b11: Enable all PAD PVT auto-update mechanism
FAST_SETTING_EN	03 - 03	0x0	R/W	Fast setting indicator for mode registers. 1’b0: All fields in mode registers are programmable. 1’b1: Only some specific fields in mode registers are programmable.

Table 39. Main control register *…continued*

Name	Bit	Default	R/W	Description
PWR_ON	02 - 02	0x0	R	Once the DDR2SDMC is enabled by setting DDR2SDMC_CTRL bit 0 to 1, the DDR2SDMC can't issue any command until this bit is 1. 1'b0: DDR2SDMC is not ready to issue command and in the power on state. 1'b1: DDR2SDMC is ready to issue command
FAST_PWR_CTRL	01 - 01	0x0	R/W	Fast power on control. 1'b0: Normal power on sequence. 1'b1: Fast power on sequence, the SSTL I/O calibration status will be ignored. For simulation only.
EN	00 - 00	0x0	R/W	0: Disable DDR2SDMC. 1: Enable DDR2SDMC.

9.2.3 Reserved (0x00000008)

9.2.4 DDR2SDMC_SIZE_CFG (0x0000000C)

Size configuration register.

Table 40. Size configuration register

Name	Bit	Default	R/W	Description
BASE_ADDR	31 - 24	0x0	R/W	DDR-II SDRAM base address (AMBA AHB slave address 31 to 24).
	23 - 10	0x0		Reserved.
BANK_NUM	09 - 08	0x0	R/W	DDR-II SDRAM internal bank number. 2'b01: 4 internal banks. 2'b10: 8 internal banks.
ROW_ADDR_BIT_WIDTH	07 - 04	0x0	R/W	DDR-II SDRAM row address bit width (13~15).
COL_ADDR_BIT_WIDTH	03 - 00	0x0	R/W	DDR-II SDRAM column address bit width (9~11).

9.2.5 DDR2SDMC_LOAD_MODE_0_1_CFG (0x00000010)

Load mode register 0 and 1 configuration register.

Table 41. Load mode register 0 and 1 configuration register

Name	Bit	Default	R/W	Description
-	31	0x0	-	Reserved.
EXT_MODE_REG_DATA	30 - 16	0x0	R/W	DDR-II SDRAM extended mode register data.
-	15	0x0	-	Reserved.
MODE_REG_DATA	14 - 00	0x0	R/W	DDR-II SDRAM mode register data.

9.2.6 DDR2SDMC_LOAD_MODE_2_3_CFG (0x00000014)

Load mode register 2 and 3 configuration register.

Table 42. Load mode register 2 and 3 configuration register

Name	Bit	Default	R/W	Description
-	31	0x0	-	Reserved.
EXT_MODE_REG_3_DATA	30 - 16	0x0	R/W	DDR-II SDRAM extended mode register 3 data.
-	15	0x0	-	Reserved.
EXT_MODE_REG_2_DATA	14 - 00	0x0	R/W	DDR-II SDRAM extended mode register 2 data.

9.2.7 DDR2SDMC_TIMING_CFG_0 (0x00000018)

Timing configuration register 0. Unit: AHB cycle.

Table 43. Timing configuration register

Name	Bit	Default	R/W	Description
-	31 - 24	0x0	-	Reserved.
T_WTR	23 - 20	0x0	R/W	Minimum internal WRITE-to-READ command delay.
T_RTP	19 - 16	0x0	R/W	Minimum internal READ-to-PRECHARGE command delay.
T_RCD	15 - 12	0x0	R/W	Minimum ACTIVE-to-READ or WRITE delay.
T_RRD	11 - 08	0x0	R/W	Minimum ACTIVE-to-ACTIVE command at different bank interval.
T_MRD	07 - 04	0x0	R/W	Minimum LOAD MODE command cycle time.
T_RP	03 - 00	0x0	R/W	Minimum PRECHARGE command period.

9.2.8 DDR2SDMC_TIMING_CFG_1 (0x0000001C)

Timing configuration register 1. Unit: AHB cycle.

Table 44. Timing configuration register 1

Name	Bit	Default	R/W	Description
T_RFC	31 - 24	0x0	R/W	Minimum REFRESH-to-ACTIVE or REFRESH-to-REFRESH command interval.
T_FAW	23 - 16	0x0	R/W	Minimum 4-bank activate period.
T_RC	15 - 08	0x0	R/W	Minimum ACTIVE-to-ACTIVE command at the same bank interval.
T_RAS	07 - 00	0x0	R/W	Minimum ACTIVE-to-PRECHARGE command interval.

9.2.9 DDR2SDMC_TIMING_CFG_2 (0x00000020)

Timing configuration register 2. Unit: AHB cycle.

Table 45. Timing configuration register 2

Name	Bit	Default	R/W	Description
T_IDLE	31 - 16	0x0	R/W	Minimum clock cycles between the first NOP command and the PRECHARGE command.
T_REF	15 - 00	0x0	R/W	Maximum periodic refresh interval.

9.2.10 DDR2SDMC_TIMING_CFG_3 (0x00000024)

Timing configuration register 3. Unit: AHB cycle.

Table 46. Timing configuration register 3

Name	Bit	Default	R/W	Description
T_DLLRST	31 - 20	0x0	R/W	Minimum clock cycles for DDR-II SDRAM internal DLL reset to stable
T_PWRON	19 - 00	0x0	R/W	Minimum clock cycles for DDR-II SDRAM power-up.

10. DDR-II/III SDRAM controller (for ASC8848/49/50 M2 version and ASC8851)

10.1 Features

There are two DDR-II/III SDRAM controllers (DDR32SDMC) in ASC88xx SoC. It provides an interface between AMBA AHB bus and external DDR-II/III SDRAM. It can receive AMBA AHB requests, encode them into DDR-II/III SDRAM standard commands, and then send them to external DDR-II/III SDRAM. It also has an 8-entry write queue to fulfill zero-wait-state AMBA AHB write access.

10.1.1 Data width

Supports 16-bit data width on external DDR-II/III SDRAM interface.

10.1.2 External Bank

Supports only 1 external bank number

10.1.3 Memory Size

DDR-II: Supports 256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb

DDR-III: Supports 512 Mb, 1 Gb, 2 Gb, 4 Gb or 8 Gb

10.1.4 Data Type

Supports 8-bit, 16-bit, 32-bit, and 64-bit data access on AMBA AHB bus

10.1.5 Page Number

DDR-II: Supports 32768, 65536, 131072 or 262144 page number

DDR-III: Supports 32768, 65536, 131072, 262144 or 524288 page numbers

10.1.6 Bank Number

DDR-II: Supports 4 or 8 internal banks

DDR-III: Supports 8 internal banks

10.1.7 Column Latency

DDR-II: Supports CL=4~7

DDR-III: Supports CL=5~11

10.1.8 Burst Type

DDR-II: Supports burst length 4

DDR-III: Supports fixed burst length 8 and on-the-fly burst

10.2 Memory Map Register

All timing parameters are in DRAM clock cycles. Calculate them based on DRAM databook.

10.2.1 DDR32SDMC_VERSION (0x00000000)

Version information register

Table 47. Version control register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x0C	R	Major version number
MINOR_VERSION	23 - 16	0x00	R	Minor version number
BUILD_VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x03	R	Revision number

10.2.1.1 DDR32SDMC_CTRL (0x00000004)

Main control register

Table 48. Main control register

Name	Bit	Default	R/W	Description
FIXED_WRITE_AS_BL8	19-19	0x0	R/W	Fixed write operation as burst length 8 in on-the-fly mode. 1'b0: Write operation is on-the-fly mode 1'b1: Write operation is burst-length 8 mode
FIXED_READ_AS_BL8	18-18	0x0	R/W	Fixed read operation as burst length 8 in on-the-fly mode. 1'b0: Read operation is on-the-fly mode 1'b1: Read operation is burst-length 8 mode
SLAVE_CORE_SYNC_EN	17-17	0x0	R/W	Slave core synchronization enable 1'b0: Disable slave core synchronization 1'b1: Enable slave core synchronization
MCI_IOPHY_UPDATE_ACK_EN	16-16	0x0	R/W	MCI-initiate VT update acknowledge enable control. 1'b0: Ignore PHY acknowledge signal 1'b1: Wait PHY acknowledge signal
MCI_IOPHY_UPDATE_PERIOD	15-12	0x0	R/W	MCI-initiate VT update period 4'b0000: 1 cycle. … 4'b1111: 16 cycles
BPSS_PUB_EN	11-11	0x0	R/W	Bypass PUB enable 1'b0: Controller access PHY through PUB with DFI 1'b1: Controller access PHY directly
DDR_MODE	10-10	0x0	R/W	DDR-II/III mode selection 1'b0: DDR-II mode 1'b1: DDR-III mode
DYNAMIC_ODT_EN	09-09	0x1	R/W	Dynamic ODT control enable. 1'b0: Disable dynamic ODT control. 1'b1: Enable dynamic ODT control
PHY_PLL_DTO_EN	08-08	0x0	R/W	PHY PLL digital test signal output enables. 1'b0: Disable PHY PLL digital test signal output 1'b1: Enable PHY PLL digital test signal output
	07-07	0x0		Reserved

Table 48. Main control register

Name	Bit	Default	R/W	Description
MCI_IOPHY_UPDATE_EN	06-06	0x0	R/W	PHY VT update control selection. 1'b0: PHY-initiate VT update mechanism. 1'b1: MCI-initiate VT update mechanism
	05-04	0x0		Reserved
FAST_SETTING_EN	03-03	0x0	R/W	Fast setting for mode registers 1'b0: All fields in mode registers are programmable. 1'b1: Only some specific fields in mode registers are programmable
PWR_ON	02-02	0x0	R	Power-on status bit. Once the DDR32SDMC is enabled by setting DDR32SDMC_CTRL bit 0 to 1, the DDR32SDMC can't issue any command until this bit is 1. 1'b0: DDR32SDMC is not ready to issue command and in the power on state. 1'b1: DDR32SDMC is ready to issue command
	01-01	0x0		Reserved
EN	00-00	0x0	R/W	DDR-II/III SDRAM controller enable 1'b0: Disable DDR32SDMC. 1'b1: Enable DDR32SDMC

10.2.2 Reserved (0x00000008)

10.2.3 DDR32SDMC_SIZE_CFG (0x0000000C)

Size configuration register

Table 49. Size configuration register

Name	Bit	Default	R/W	Description
BASE_ADDR	31-24	0x0	R/W	DDR-II/III SDRAM base address (AMBA AHB slave address 31 to 24).
	23-10	0x0		Reserved
BANK_NUM	09-08	0x0	R/W	DDR-II/III SDRAM internal bank number. 2'b01: 4 internal banks. 2'b10: 8 internal banks
ROW_ADDR_BIT_WIDTH	07-04	0x0	R/W	DDR-II/III SDRAM row address bit width (13 ≈15)
COL_ADDR_BIT_WIDTH	03-00	0x0	R/W	DDR-II/III SDRAM column address bit width (9 ≈11)

10.2.4 DDR32SDMC_LOAD_MODE_0_1_CFG (0x00000010)

Load mode register 0 and 1 configuration register

Table 50. Load mode register 0 and 1 configuration register

Name	Bit	Default	R/W	Description
	31-31	0x0		Reserved
EXT_MODE_REG_DATA	30-16	0x0	R/W	DDR-II/III SDRAM extended mode register data.
	15-15	0x0		Reserved
MODE_REG_DATA	14-00	0x0	R/W	DDR-II/III SDRAM mode register data.

10.2.5 DDR32SDMC_LOAD_MODE_2_3_CFG (0x00000014)

Load mode register 2 and 3 configuration register.

Table 51. Load mode register 2 and 3 configuration register

Name	Bit	Default	R/W	Description
	31-31	0x0		Reserved
EXT_MODE_REG_3_DATA	30-16	0x0	R/W	DDR-II/III SDRAM extended mode register data.
	15-15	0x0		Reserved
EXT_MODE_REG_2_DATA	14-00	0x0	R/W	DDR-II/III SDRAM mode register data.

10.2.6 DDR32SDMC_TIMING_CFG_0 (0x00000018)

Timing configuration register 0

Table 52. Timing configuration register 0

Name	Bit	Default	R/W	Description
T_MOD	27-24	0x0	R/W	Minimum MRS update time. (DDR-III only)
T_WTR	23-20	0x0	R/W	Minimum internal WRITE-to-READ command delay.
T_RTP	19-16	0x0	R/W	Minimum internal READ-to-PRECHARGE command delay.
T_RCD	15-12	0x0	R/W	Minimum ACTIVE-to-READ or WRITE delay.
T_RRD	11-08	0x0	R/W	Minimum ACTIVE-to-ACTIVE command at different bank interval.
T_MRD	07-04	0x0	R/W	Minimum LOAD MODE command cycle time.
T_RP	03-00	0x0	R/W	Minimum PRECHARGE command period.

10.2.7 DDR32SDMC_TIMING_CFG_1 (0x0000001C)

Timing configuration register 1

Table 53. Timing configuration register 1

Name	Bit	Default	R/W	Description
T_RFC	31-24	0x0	R/W	Minimum REFRESH-to-ACTIVE or REFRESH-to-REFRESH command interval.
T_FAW	23-16	0x0	R/W	Minimum 4-bank activate period.
T_RC	15-08	0x0	R/W	Minimum ACTIVE-to-ACTIVE command at the same bank interval.
T_RAS	07-00	0x0	R/W	Minimum ACTIVE-to-PRECHARGE command interval.

10.2.8 DDR32SDMC_TIMING_CFG_2 (0x00000020)

Timing configuration register 2

Table 54. Timing configuration register 2

Name	Bit	Default	R/W	Description
T_IDLE	31-16	0x0	R/W	DDR-II:Minimum clock cycles between the first NOP command and the PRECHARGE command. DDR-III: Minimum clock cycles between the first NOP command and the EMR2 command
T_REF	15-00	0x0	R/W	Maximum periodic refresh interval.

10.2.9 DDR32SDMC_TIMING_CFG_3 (0x00000024)

Timing configuration register 3

Table 55. Timing configuration register 3

Name	Bit	Default	R/W	Description
T_DLLRST	31-20	0x0	R/W	DDR-II: Minimum clock cycles for DDR-II SDRAM internal DLL reset to stable DDR-III: Minimum clock cycles for DDR-III SDRAM (tRST2CKE >> 8).
T_PWRON	19-00	0x0	R/W	DDR-II:Minimum clock cycles for DDR-II/III SDRAM power-up. DDR-III: Minimum clock cycles for DDR-III SDRAM reset time

10.2.10 DDR32SDMC_ZQ_CTRL (0x00000028)

Output impedance control configuration register

Table 56. Output impedance control configuration

Name	Bit	Default	R/W	Description
	31-28	0x0		Reserved
ZQCL_INTERVAL	27-20	0x0	R/W	Issue ZQCL command every (256*ZQCL_INTERVAL)
ZQCS_INTERVAL	19-08	0x0	R/W	Issue ZQCS command every (16*ZQCS_INTERVAL)
	07-05	0x0		Reserved
T_ZQ_EXTEND_EN	04-04	0x0	R/W	Extend tZQinit, tZQoper and tZQCS two cycles more. 1'b0: Disable. 1'b1: Enable
	03-03	0x0		Reserved
ZQC_FORCE_EN	02-02	0x0	R/W	ZQCS/ZQCL command execution control. 1'b0: Drop ZQCL/ZQCS command if there are other pending DRAM commands. 1'b1: Always execute ZQCL/ZQCS command
ZQCL_EN	01-01	0x0	R/W	ZQCL command enable control. 1'b0: Disable 1'b1: Enable
ZQCS_EN	00-00	0x0	R/W	ZQCS command enable control. 1'b0: Disable 1'b1: Enable

10.2.11 DDR32SDMC_POWR_DOWN_MODE_CTRL (0x0000002C)

Power down mode control register

Table 57. Power down mode control register

Name	Bit	Default	R/W	Description
PRECHARGED_DLL_OFF_PD_CYCLE	31:24:00	0x0	R/W	Auto-refresh count before entry pre-charged power down mode with DLL off.
PRECHARGED_DLL_ON_PD_CYCLE	23:16	0x0	R/W	Auto-refresh count before entry pre-charged power down mode with DLL on.
ACTIVE_PD_CYCLE	15-08	0x0	R/W	Cycle count before entry active power down mode.
	07-03	0x0		Reserved
PRECHARGED_DLL_OFF_PD_EN	02-02	0x0	R/W	Pre-charged power down mode with DLL off enable. 1'b0: Disable 1'b1: Enable
PRECHARGED_DLL_ON_PD_EN	01-01	0x0	R/W	Pre-charged power down mode with DLL on enable 1'b0: Disable 1'b1: Enable
ACTIVE_PD_EN	00-00	0x0	R/W	Active power down enable 1'b0: Disable. 1'b1: Enable

10.2.12 DDR32SDMC_SELF_REFRESH_MODE_CTRL (0x00000030)

Self refresh mode control configuration register

Table 58. Generic table (5col)

Name	Bit	Default	R/W	Description
DLL_OFF_SRF_CYCLE	31:24	0x0	R/W	Auto-refresh count before entry self refresh mode with DLL off.
DLL_ON_SRF_CYCLE	23:16	0x0	R/W	Auto-refresh count before entry self refresh mode with DLL on.
	15-03	0x0		Reserved
DLL_OFF_SRF_EN	13-03	0x0	R/W	Self refresh mode with DLL off enable.
DLL_ON_SRF_EN	01-01	0x0	R/W	Self refresh mode with DLL on enable.
	00-00	0x0		Reserved

10.2.13 7.2.4.DDR32SDMC_POWR_DOWN_AND_SELF_REFRESH_MODE_TIMING (0x00000034)

Power down and self refresh mode timing register

Table 59. Power down and self refresh mode timing register

Name	Bit	Default	R/W	Description
	31-29	0x0		Reserved
T_XPDLL	28-24	0x0	R/W	Exit pre-charge power down with DLL frozen to commands requiring a locked DLL.
T_DLLK_EXTEND	23-23	0x0	R/W	Extend tDLLK and tXSDLL two cycles more 1'b0: Disable. 1'b1: Enable
T_XP	22-20	0x0	R/W	Exit power down with DLL on to any valid command; Exit per-charge power down with DLL frozen to commands not requiring a locked DLL.
T_PD	18-16	0x0	R/W	Power down entry to exit timing.
T_XS	15:08	0x0	R/W	Exit self refresh to commands not requiring a locked DLL.
	07-07	0x0		Reserved
T_CKSREX	06-04	0x0	R/W	Valid clock requirement after self refresh entry (SRE) or power down entry (PDE) Valid clock requirement before self refresh exit (SRX) or power down exit (PDX) or reset exit
T_CKESR	02-00	0x0	R/W	Minimum CKE low width for self refresh entry to exit timing.

10.2.14 DDR32SDMC_IO_DYNAMIC_CTRL (0x00000038)

IO dynamic control register

Table 60. IO dynamic control register

Name	Bit	Default	R/W	Description
	31-09	0x0		Reserved
DYNAMIC_DQ_DQS_RCV_EN	08-08	0x0	R/W	DM[3:0], DQ[15:0] and DQS[3:0] IO receiving dynamic power down control 1'b0: Disable 1'b1: Enable
DYNAMIC_DM_DQ_DQS_DRV_EN	07-07	0x0	R/W	DM[3:0], DQ[15:0] and DQS[3:0] IO driving dynamic power down control 1'b0: Disable. 1'b1: Enable
DYNAMIC_ADDR_DRV_EN	06-06	0x0	R/W	ADDR[15:0] IO driving dynamic power down control 1'b0: Disable. 1'b1: Enable
DYNAMIC_CMD_DRV_EN	05-05	0x0	R/W	nRAS, nCAS, nWE and BA[2:0] IO driving dynamic power down control 1'b0: Disable. 1'b1: Enable
DYNAMIC_CLK_DRV_EN	04-04	0x0	R/W	CLK IO driving dynamic power down control 1'b0: Disable. 1'b1: Enable
NOP_AC_OE_DISABLE	03-03	0x0	R/W	AC output disable control in NOP 1'b0: Disable. 1'b1: Enable
DYNAMIC_ADDR_OE_EN	02-02	0x0	R/W	ADDR[15:0] IO output enable dynamic control.
DYNAMIC_CMD_OE_EN	01-01	0x0	R/W	nRAS, nCAS, nWE and BA[2:0] IO output enable dynamic control 1'b0: Disable. 1'b1: Enable
DYNAMIC_CLK_OE_EN	00-00	0x0	R/W	CLK IO output enable dynamic control.

10.2.15 DDR32SDMC_IO_BIT_ENABLE (0x0000003C)

IO bit enable register

Table 61. IO bit enable register

Name	Bit	Default	R/W	Description
	31-19	0x0		Reserved
CKE_BIT_EN	18-18	0x1	R/W	CKE output enable control 1'b0: Disable 1'b1: Enable

Table 61. IO bit enable register

Name	Bit	Default	R/W	Description
ODT_BIT_EN	17-17	0x1	R/W	ODT output enable control 1'b0: Disable 1'b1: Enable
CS_N_BIT_EN	16-16	0x1	R/W	nCS output enable control 1'b0: Disable 1'b1: Enable
ADDR_BIT_EN	15-00	0xFFFF	R/W	ADDR[15:0] output enable control 1'b0: Disable 1'b1: Enable

10.2.16 DDR32SDMC_DFI_CTRL (0x00000040)

DFI control register

Table 62. DFI control register

Name	Bit	Default	R/W	Description
	31-12	0x0		Reserved
DFI_LP_WAKEUP	11-08	0x0	R/W	DFI low power wake up time. (Please check PUB databook for details)
	07-07	0x0		Reserved
DFI_LP_ACK	06-06	0x0	R	DFI low power acknowledge.
DFI_LP_REQ	05-05	0x0	R/W	DFI low power request.
DFI_INIT_COMPLETE	04-04	0x0	R	DFI initialization complete.
DFI_DRAM_CLK_DISABLE	03-03	0x0	R/W	DFI disable DRAM clock.
DFI_DATA_HALFWORDLANE_DISABLE	02-01	0x0	R/W	DFI data half word lane disable.
DFI_INIT_START	00-00	0x0	R/W	DFI initialization start.

10.2.17 DDR32SDMC_LOAD_MODE_CTRL (0x00000044)

Load mode control register

Table 63. Load mode control register

Name	Bit	Default	R/W	Description
	31-06	0x0		Reserved
LODE_MODE_IDX	05-04	0x0	R/W	LMR command ID. 2'b00: MR0 2'b01: MR1 2'b10: MR2 2'b11: MR3
	03-01	0x0		Reserved
LOAD_MODE_OP_EN	00-00	0x0	R/W	Launch LMR command.

11. Interrupt Controller

11.1 General description

ASC8848/49/50/51 SoC interrupt controller supports 64 interrupt sources but only 44 of them are connected internally. It provides one output to the host processor. The interrupt sources could be configured as edge-triggered or level-triggered with positive polarity.

11.2 Features

11.2.1 Interrupt Number

Supports 44 independent interrupt signals.

11.2.2 Interrupt Source

Provides both edge and level-triggered interrupt sources with positive polarity.

11.2.3 Interrupt Map

The interrupt controller will interrupt host processor whenever one of the 44 interrupt sources is asserted. The host processor will read the status of the interrupt controller and decide which interrupt source is to be serviced first. This procedure will not stop until all interrupts are serviced. Refer to Table 64 for the interrupt number assignment.

Table 64. Interrupt number assignment

Number	Source	Type	Descriptions
0	TMRC 0	Edge	Timer 0
1	APBC	Level	APB DMA controller
2	VIC	Level	Video Input Controller
3	VOC	Level	Video Output Controller
4	DMAC	Level	DMA Controller
5	GMAC	Level	Giga-bit Ethernet MAC
6	MSHC 0	Level	Mobile Storage Controller 0
7	MSHC 1	Level	Mobile Storage Controller 1
8	USBC	Level	USB 2.0 OTG Controller
9	PCIE_LVL	Level	PCIe Controller Level Interrupt
10	NFC	Level	NAND Flash Controller
11	DCE	Level	Data Crypto Engine
12	H4EE	Level	H.264 Encoder Engine
13	JEBE	Level	JPEG Encoder Engine
14	IBPE	Level	Image Back-End Processing Engine
15	DIE	Level	Deinterlacing Engine
16	IRE	Level	Resize Engine
17	MEAE	Level	MPEG-4 Audio Engine
18	SSIC	Level	Synchronous serial interface
19	I2SSC 0	Level	I2S slave controller 0
20	I2SSC 1	Level	I2S slave controller 1

Table 64. Interrupt number assignment *…continued*

Number	Source	Type	Descriptions
21	I2SSC 2	Level	I2S slave controller 2
22	I2SSC 3	Level	I2S slave controller 3
23	I2SSC 4	Level	I2S slave controller 4
24	WDTC	Edge	Watchdog
25	UARTC 0	Level	UART device 0
26	UARTC 1	Level	UART device 1
27	UARTC 2	Level	UART device 2
28	UARTC 3	Level	UART device 3
29	AGPOC	Level	Advanced general purpose output
30	GPIOC	Level	General purpose I/O
31	IRDAC	Level	IrDA controller
32	TMRC 1	Edge	Timer 1
33	TMRC 2	Edge	Timer 2
34	TMRC 3	Edge	Timer 3
35	PCIE_EDGE	Edge	PCIe controller edge interrupt
36	PCIE MSI 7	Edge	PCIe MSI 7 interrupt for ASC8848/49/50 M1 Version
	VIC Dev 0	Edge	VIC device 0 VSYNC signal for ASC8848/49/50 M2 Version and ASC8851
37	PCIE MSI 6	Edge	PCIe MSI 6 interrupt for ASC8848/49/50 M1 Version
	VIC Dev 1	Edge	VIC device 1 VSYNC signal for ASC8848/49/50 M2 Version and ASC8851
38	PCIE MSI 5	Edge	PCIe MSI 5 interrupt for ASC8848/49/50 M1 Version
	-	-	Reserved for ASC8848/49/50 M2 Version and ASC8851
39	PCIE MSI 4	Edge	PCIe MSI 4 interrupt for ASC8848/49/50 M1 Version
	-	-	Reserved for ASC8848/49/50 M2 Version and ASC8851
40	PCIE Dev 4	Edge	PCIe device 4 MSI
41	PCIE Dev 5	Edge	PCIe device 5 MSI
42	PCIE Dev 6	Edge	PCIe device 6 MSI
43	PCIE Dev 7	Edge	PCIe device 7 MSI

11.3 Memory map register

11.3.1 INTC_VERSION (0x00000000)

Version information register.

Table 65. Version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x01	R	Major version number.
MINOR_VERSION	23 - 16	0x01	R	Minor version number.
BUILD_VERSION	15 - 08	0x00	R	Build version number.
REVISION	07 - 00	0x00	R	Revision number.

11.3.2 INTC_SRC_LO (0x00000004)

Low 32-bit IRQ source register.

Table 66. Low 32-bit IRQ source register

Name	Bit	Default	R/W	Description
SRC_LO	31 - 00	0x0	R	IRQ source bit 0~31.

11.3.3 INTC_SRC_HI (0x00000008)

High 32-bit IRQ source register.

Table 67. High 32-bit IRQ source register

Name	Bit	Default	R/W	Description
SRC_HI	31 - 00	0x0	R	IRQ source bit 32~63.

11.3.4 INTC_STAT_LO (0x0000000C)

Low 32-bit masked IRQ source register.

Table 68. Low 32-bit masked IRQ source register

Name	Bit	Default	R/W	Description
STAT_LO	31 - 00	0x0	R	IRQ masked source bit 0~31.

11.3.5 INTC_STAT_HI (0x00000010)

High 32-bit masked IRQ source register.

Table 69. High 32-bit masked IRQ source register

Name	Bit	Default	R/W	Description
STAT_HI	31 - 00	0x0	R	IRQ masked source bit 32~63.

11.3.6 INTC_MASK_LO (0x00000014)

Low 32-bit mask register.

Table 70. Low 32-bit mask register

Name	Bit	Default	R/W	Description
MASK_LO	31 - 00	0x0	R/W	Mask control bit 0~31. 1’b0: IRQ masked. 1’b1: IRQ enabled.

11.3.7 INTC_MASK_HI (0x00000018)

High 32-bit mask register.

Table 71. High 32-bit mask register

Name	Bit	Default	R/W	Description
MASK_HI	31 - 00	0x0	R/W	Mask control bit 32~63. 1'b0: IRQ masked. 1'b1: IRQ enabled.

11.3.8 INTC_CLEAR_LO (0x0000001C)

Low 32-bit status clear register.

Table 72. Low 32-bit status clear register

Name	Bit	Default	R/W	Description
CLEAR_LO	31 - 00	0x0	W	Status clear control bit 0~31. This register is self cleared. 1'b0: Do nothing. 1'b1: Clear IRQ.

11.3.9 INTC_CLEAR_HI (0x00000020)

High 32-bit status clear register.

Table 73. High 32-bit status clear register

Name	Bit	Default	R/W	Description
CLEAR_HI	31 - 00	0x0	W	Status clear control bit 32~63. This register is self cleared. 1'b0: Do nothing. 1'b1: Clear IRQ.

11.3.10 INTC_TRIGGER_MODE_LO (0x00000024)

Low 32-bit IRQ trigger mode register.

Table 74. Low 32-bit IRQ trigger mode register

Name	Bit	Default	R/W	Description
TRIGGER_MODE_LO	31 - 00	0x0	R/W	Trigger mode control bit 0~31. 1'b0: Level triggered. 1'b1: Edge triggered.

11.3.11 INTC_TRIGGER_MODE_HI (0x00000028)

High 32-bit IRQ trigger mode register.

Table 75. High 32-bit IRQ trigger mode register

Name	Bit	Default	R/W	Description
TRIGGER_MODE_HI	31 - 00	0x0	R/W	Trigger mode control bit 32~63. 1'b0: Level triggered. 1'b1: Edge triggered.

11.3.12 INTC_SET_LO (0x0000002C)

Low 32-bit IRQ software set register.

Table 76. Low 32-bit IRQ software set register

Name	Bit	Default	R/W	Description
TRIGGER_MODE_LO	31 - 00	0x0	W	Software set control bit 0~31. This register is self cleared. 1’b0: Do nothing. 1’b1: Set IRQ.

11.3.13 INTC_SET_HI (0x00000030)

High 32-bit IRQ software set register.

Table 77. High 32-bit IRQ software set register

Name	Bit	Default	R/W	Description
TRIGGER_MODE_HI	31 - 00	0x0	W	Software set control bit 32~63. This register is self cleared. 1’b0: Do nothing. 1’b1: Set IRQ.

12. Timer Controller

12.1 General description

ASC8848/49/50/51 SoC provides four independent sets of 32-bit timers. APB clock is used to clock each timer. Each timer could be configured to increment or decrement its value at each clock rising edge. There is one match register for each timer. When the value of the timer is equal to the match register, an interrupt is asserted. Auto-reload register is incorporated to generate regular ticks for software scheduling.

12.2 Features

12.2.1 Interrupt mode

Each timer has a match register. When the value of match register is equal to the timer, the interrupt is triggered immediately.

Furthermore, the interrupt can be asserted when the timer is overflowed or underflowed. Users can disable the interrupt by TM(0~3)_OF_EN and TM(0~3)_MATCH_EN bits in timer control resister.

12.2.2 Counting direction

Each timer can increment or decrement its value. Users can customize the counting direction of each timer by TM(0~3)_CNT_DIR bit in the control register.

12.2.3 Auto-reload value

No matter TM(0~3)_OF_EN bit in the timer control register is enabled or disabled, TM(0~3)_LOAD value will be automatically loaded into the counter register when the counter overflows or underflows. Users can use TM(0~3)_LOAD to set the period between two counter overflows.

12.2.4 Memory map register

12.2.4.1 TMRC_VERSION (0x00000000)

Version information register.

Table 78. Version Information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x03	R	Major version number.
MINOR_VERSION	23 - 16	0x00	R	Minor version number.
BUILD_VERSION	15 - 08	0x00	R	Build version number.
REVISION	07 - 00	0x03	R	Revision number.

12.2.4.2 TMRC_CTRL (0x00000004)

Control register of four independent timers.

Table 79. Control register of four independent timers

Name	Bit	Default	R/W	Description
-	31 - 16	-	-	Reserved
TM3_ CNT_DIR	15	0x0	R/W	Timer3 counting direction 0: incrementing 1: decrementing
TM3_MATCH_EN	14	0x0	R/W	Timer3 match interrupt enable bit 0: disable 1: enable
TM3_OF_EN	13	0x0	R/W	Timer3 overflow/underflow interrupt enable bit 0: disable 1: enable
TM3_EN	12	0x0	R/W	Timer3 enable bit 0: disable 1:enable
TM2_ CNT_DIR	11	0x0	R/W	Timer2 counting direction 0: incrementing 1: decrementing
TM2_MATCH_EN	10	0x0	R/W	Timer2 match interrupt enable bit 0: disable 1: enable
TM2_OF_EN	09	0x0	R/W	Timer2 overflow/underflow interrupt enable bit 0: disable 1: enable
TM2_EN	08	0x0	R/W	Timer2 enable bit 0: disable 1:enable

Table 79. Control register of four independent timers *…continued*

Name	Bit	Default	R/W	Description
TM1_ CNT_DIR	07	0x0	R/W	Timer1 counting direction 0: incrementing 1: decrementing
TM1_MATCH_EN	06	0x0	R/W	Timer1 match interrupt enable bit 0: disable 1: enable
TM1_OF_EN	05	0x0	R/W	Timer1 overflow/underflow interrupt enable bit 0: disable 1: enable
TM1_EN	04	0x0	R/W	Timer1 enable bit 0: disable 1:enable
TM0_ CNT_DIR	03	0x0	R/W	Timer0 counting direction 0: incrementing 1: decrementing
TM0_MATCH_EN	02	0x0	R/W	Timer0 match interrupt enable bit 0: disable 1: enable
TM0_OF_EN	01	0x0	R/W	Timer0 overflow/underflow interrupt enable bit 0: disable 1: enable
TM0_EN	00	0x0	R/W	Timer0 enable bit 0: disable 1:enable

12.2.4.3 Reserved (0x00000008)

12.2.4.4 TMRC_TIMER0_COUNTER (0x0000000C)

Timer0 counter register.

Table 80. Timer0 counter register

Name	Bit	Default	R/W	Description

TM0_CNT	31 - 00	0x0	R/W	Timer0 counter. The R/W status is as follows.
				TM0_EN=1’b0: R/W
				TM0_EN=1’b1: RO

12.2.4.5 TMRC_TIMER0_AUTO_RELOAD_VALUE (0x00000010)

Timer0 auto-reload register.

Table 81. Timer0 auto-reload register

Name	Bit	Default	R/W	Description
TM0_LOAD	31 - 00	0x0	R/W	Timer0 auto reload value

12.2.4.6 TMRC_TIMER0_MATCH_VALUE (0x00000014)

Timer0 match value register.

Table 82. Timer0 match value register

Name	Bit	Default	R/W	Description
TM0_MATCH_VAL	31 - 00	0x0	R/W	Timer0 match value

12.2.4.7 TMRC_TIMER1_COUNTER (0x00000018)

Timer1 counter register.

Table 83. Timer1 counter register

Name	Bit	Default	R/W	Description

TM1_CNT	31 - 00	0x0	R/W	Timer1 counter. The R/W status is as follows.
				TM1_EN=1'b0: R/W
				TM1_EN=1'b1: RO

12.2.4.8 TMRC_TIMER1_AUTO_RELOAD_VALUE (0x0000001C)

Timer1 auto-reload register.

Table 84. Timer1 auto-reload register

Name	Bit	Default	R/W	Description
TM1_LOAD	31 - 00	0x0	R/W	Timer1 auto reload value

12.2.4.9 TMRC_TIMER1_MATCH_VALUE (0x00000020)

Timer1 match value register.

Table 85. Timer1 match value register

Name	Bit	Default	R/W	Description
TM1_MATCH_VAL	31 - 00	0x0	R/W	Timer1 match value

12.2.4.10 TMRC_TIMER2_COUNTER (0x00000024)

Timer2 counter register.

Table 86. Timer2 counter register

Name	Bit	Default	R/W	Description

TM2_CNT	31 - 00	0x0	R/W	Timer2 counter. The R/W status is as follows.
				TM2_EN=1'b0: R/W
				TM2_EN=1'b1: RO

12.2.4.11 TMRC_TIMER2_AUTO_RELOAD_VALUE (0x00000028)

Timer2 auto-reload register.

Table 87. Timer2 auto-reload register

Name	Bit	Default	R/W	Description
TM2_LOAD	31 - 00	0x0	R/W	Timer2 auto reload value

12.2.4.12 TMRC_TIMER2_MATCH_VALUE (0x0000002C)

Timer2 match value register.

Table 88. Timer2 match value register

Name	Bit	Default	R/W	Description
TM2_MATCH_VAL	31 - 00	0x0	R/W	Timer2 match value

12.2.4.13 TMRC_TIMER3_COUNTER (0x00000030)

Timer3 counter register.

Table 89. Timer3 counter register

Name	Bit	Default	R/W	Description

TM3_CNT	31 - 00	0x0	R/W	Timer3 counter. The R/W status is as follows.
				TM3_EN=1’b0: R/W
				TM3_EN=1’b1: RO

12.2.4.14 TMRC_TIMER3_AUTO_RELOAD_VALUE (0x00000034)

Timer3 auto-reload register.

Table 90. Timer3 auto-reload register

Name	Bit	Default	R/W	Description
TM3_LOAD	31 - 00	0x0	R/W	Timer3 auto reload value

12.2.4.15 TMRC_TIMER3_MATCH_VALUE (0x00000038)

Timer3 match value register.

Table 91. Timer3 match value registers

Name	Bit	Default	R/W	Description
TM3_MATCH_VAL	31 - 00	0x0	R/W	Timer3 match value

13. Phase Lock Loop Controller

13.1 General description

ASC8848/49/50/51 SoC provides four PLLs to generate all clocks. PLL. PLL 0 is for system use including AHB/APB/DRAM clocks; PLL 1 is for Giga-bit Ethernet MAC; PLL 2 is for I^2S master clock generation; PLL 3 is for the video display pixel clock generation. Only PLL 2 and PLL 3 could be configured depending on the desired sample rate and the output resolution.

13.2 Features

The ASC8848/49/50/51 supports:

- Four PLLs, which are built-in for various applications
- Two PLLs, which are programmable through the register settings

13.3 Memory Map Register

13.3.1 PLLC_VERSION (0X00000000)

Version information register.

Table 92. Version Information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x03	R	Major version number.
MINOR_VERSION	23 - 16	0x00	R	Minor version number.
BUILD_VERSION	15 - 08	0x00	R	Build version number.
REVISION	07 - 00	0x04	R	Revision number.

13.3.2 PLLC_CTRL_0 (0x00000004)

Control register 0. Do not disable this PLL.

Table 93. Control register 0

Name	Bit	Default	R/W	Description
-	31 - 03	0x0	-	Reserved.
PLL_LOCK	02	0x0	R	PLL lock indicator.
PLL_CLK_EN	01	0x1	R/W	PLL function clock output enable. 1'b0: Disable 1'b1: Enable
PLL_PWR_ON	00	0x1	R/W	PLL power on control. 1'b0: PLL power down 1'b1: PLL power on

13.3.3 PLLC_RATIO_0 (0x00000008)

Ratio register 0. This register value depends on different models.

Table 94. Ratio register 0

Name		Bit	Default	R/W	Description
-	-	31 - 27	0x0	-	Reserved.
FILTER_RANGE		26 - 24	0x2	R	This sets the PLL loop filter to work with the post-reference divider frequency. Choose the highest valid range for best jitter performance. 3'b000: Reserved. 3'b001: 10 MHz to 16 MHz 3'b010: 16 MHz to 26 MHz 3'b011: 26 MHz to 42 MHz 3'b100: 42 MHz to 65 MHz 3'b101: 65 MHz to 104 MHz 3'b110: 104 MHz to 166 MHz 3'b111: 166 MHz to 200 MHz
		23 - 19	0x0		Reserved.
DIV_OUT	ASC8851 ASC8850 ASC8849 ASC8848	18 - 16	0x1 0x1 0x2 0x2	R R R	Output divider value
		15 - 14	0x0		Reserved.
DIV_REF		13 - 08	0x0	R	Reference divider value
DIV_FB	ASC8851 ASC8850 ASC8849 ASC8848	07 - 00	0x2F 0x2F 0x47 0x3F	R R	 Feedback divider value

13.3.4 PLLC_CTRL_1(0x0000000C)

Control register 1.

Table 95. Control register 1

Name	Bit	Default	R/W	Description
-	31 - 03	0x0	-	Reserved.
PLL_LOCK	02	0x0	R	PLL lock indicator.
PLL_CLK_EN	01	0x1	R/W	PLL function clock output enable. 1'b0: Disable 1'b1: Enable
PLL_PWR_ON	00	0x1	R/W	PLL power on control. 1'b0: PLL power down 1'b1: PLL power on

13.3.5 PLLC_RATIO_1 (0x00000010)

Ratio register 1.

Table 96. Ratio register 1

Name	Bit	Default	R/W	Description
-	31 - 27	0x0	-	Reserved.
FILTER_RANGE	26 - 24	0x2	R	This sets the PLL loop filter to work with the post-reference divider frequency. Choose the highest valid range for best jitter performance. 3'b000: Reserved. 3'b001: 10 to 16MHz 3'b010: 16 to 26MHz 3'b011: 26 to 42MHz 3'b100: 42 to 65MHz 3'b101: 65 to 104MHz 3'b110: 104 to 166MHz 3'b111: 166 to 200MHz
-	23 - 19	0x0	-	Reserved.
DIV_OUT	18 - 16	0x1	R	Output divider value.
-	15 - 14	0x0	-	Reserved.
DIV_REF	13 - 08	0x0	R	Reference divider value.
DIV_FB	07 - 00	0x27	R	Feedback divider value.

13.3.6 PLLC_CTRL_2 (0x00000014)

Control register 2.

Table 97. Control-register 2

Name	Bit	Default	R/W	Description
-	31 - 04	0x0	-	Reserved.
PLL_ADJUST_EN	03	0x0	R/W	PLL adjustment control. 1'b0: Disable 1'b1: Enable
PLL_LOCK	02	0x0	R	PLL lock indicator.
PLL_CLK_EN	01	0x1	R/W	PLL function clock output enable. 1'b0: Disable 1'b1: Enable
PLL_PWR_ON	00	0x1	R/W	PLL power on control. 1'b0: PLL power down 1'b1: PLL power on

13.3.7 PLLC_RATIO_2 (0x00000018)

Ratio register 2.

Table 98. Ratio register 2

Name	Bit	Default	R/W	Description
	31 - 27	0x0		Reserved.
FILTER_RANGE	26 - 24	0x2	R/W	This sets the PLL loop filter to work with the post-reference divider frequency. Choose the highest valid range for best jitter performance. 3'b000: Reserved. 3'b001: 10 to 16MHz 3'b010: 16 to 26MHz 3'b011: 26 to 42MHz 3'b100: 42 to 65MHz 3'b101: 65 to 104MHz 3'b110: 104 to 166MHz 3'b111: 166 to 200MHz
	23 - 19	0x0		Reserved.
DIV_OUT	18 - 16	0x1	R/W	Output divider value.
	15 - 14	0x0		Reserved.
DIV_REF	13 - 08	0x0	R/W	Reference divider value.
DIV_FB	07 - 00	0x57	R/W	Feedback divider value.

13.3.8 PLLC_CTRL_3 (0x0000001C)

Control register 3.

Table 99. Control register 3

Name	Bit	Default	R/W	Description
	31 - 04	0x0		Reserved.
PLL_ADJUST_EN	03	0x0	R/W	PLL adjustment control. 1'b0: Disable 1'b1: Enable
PLL_LOCK	02	0x0	R	PLL lock indicator.
PLL_CLK_EN	01	0x1	R/W	PLL function clock output enable. 1'b0: Disable 1'b1: Enable
PLL_PWR_ON	00	0x1	R/W	PLL power on control. 1'b0: PLL power down 1'b1: PLL power on

13.3.9 PLLC_RATIO_3 (0x00000020)

Ratio register 3.

Table 100. Ratio Register 3

Name	Bit	Default	R/W	Description
-	31 - 27	0x0	-	Reserved.
FILTER_RANGE	26 - 24	0x2	R/W	This sets the PLL loop filter to work with the post-reference divider frequency. Choose the highest valid range for best jitter performance. 3'b000: Reserved. 3'b001: 10 MHz to 16 MHz 3'b010: 16 MHz to 26 MHz 3'b011: 26 MHz to 42 MHz 3'b100: 42 MHz to 65 MHz 3'b101: 65 MHz to 104 MHz 3'b110: 104 MHz to 166 MHz 3'b111: 166 MHz to 200 MHz
-	23 - 19	0x0	-	Reserved.
DIV_OUT	18 - 16	0x5	R/W	Output divider value.
-	15 - 14	0x0	-	Reserved.
DIV_REF	13 - 08	0x0	R/W	Reference divider value.
DIV_FB	07 - 00	0x47	R/W	Feedback divider value.

13.4 Block Diagram

Figure 31 shows the block diagram of the PLL. M is (DIV_FB+1); N is (DIV_REF+1); DIV is 2^{DIV_OUT}. The formula is: $PLLOUT_{Freq} = F_{REFq}$ X M/N X 1/DIV.

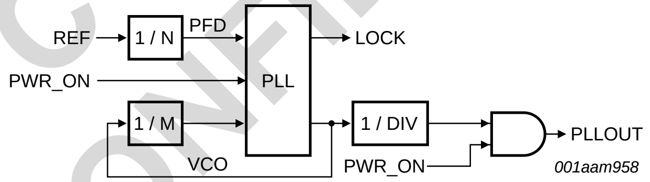


Fig 31. The Block Diagram of PLL

The operation limits of the PLL are listed below. DIV_OUT, DIV_REF, DIV_FB, and FILTER_RANGE must be within the operation limits.

Table 101. Operation Limits of PLL

Symbol	Description	Conditions	Min.	Type.	Max.	Units
$f_{i(ref)}$	input reference frequency	-	10	-	800	MHz
$f_{ref(PD)}$	reference frequency.	post-divide	10	-	200	MHz
$_1$	output frequency	for divided outputs.	10	-	1000	MHz
$f_{ref(VCO)}$)	VCO reference frequency.	-	1000	-	2000	MHz
δ_o	output duty cycle	for divided outputs.	45	-	55	%
$E_{\varphi(stat)}$	static phase error.	-	–50	+/-25	50	ps
LTJ	maximum long term jitter	for post-divide reference period.	+/-1 %	-	-	
CCJ	maximum cycle-to-cycle jitter	for the output period.	+/-1 %	-	-	

13.5 Programming

To change the PLL 2/3 output frequency, perform the following steps:

1. Set PWR_ON and PLL_CLK_EN to 1’b0 and PLL_ADJUST_EN to 1’b1.
2. Change DIV_OUT, DIV_REF, DIV_FB, and FILTER_RANGE corresponding to the desired frequency.
3. Set PWR_ON to 1’b1 and PLL_ADJUST_EN to 1’b0.
4. Wait until PLL_LOCK to become 1’b1 and then set PLL_CLK_EN to 1’b1.

14. Video Input Controller

14.1 Features

14.1.1 Input formats

- Support 1-channel 16-bit YCbCr 4:2:2 format with separate or embedded SYNC signals.
- Support 1-channel Bayer pattern (Bayer RGB or CMYG) raw data format up to 16-bit.
- Support 2-channel standard CCIR-656 8-bit YCbCr 4:2:2 progressive or interlace format.
- Support 2-channel 8-bit YCbCr 4:2:2 format with separate SYNC signals.
- Support 2-channel 2-to-1 time-multiplexed CCIR-656 8-bit YCbCr 4:2:2 progressive or interlace format.
- Support 2-channel 4-to-1 time-multiplexed CCIR-656 8-bit YCbCr 4:2:2 progressive or interlace format.
- Capture up to 8-channel video data simultaneously.

14.1.2 Image cropping

Specify the region of interest to be captured. Four parameters are required, the starting coordinate and the width and height of the cropped image.

14.1.3 Image adjustment

Support saturation, brightness and contrast adjustment. The advanced contrast enhancement that can improve the image quality in high contrast environment.

14.1.4 Photometric lens distortion correction

Photometric lens distortion correction can calibrate the photometric distortion which causes the dark corners.

14.1.5 Image front-end processing

Support CFA, 3A statistics, color correction, gamma correction.

14.1.6 Wide Dynamic Range (WDR)

Support tone mapping that can provide wide dynamic range image quality.

14.1.7 Output modes

- Mirror (reverse the horizontal order)
- Flip (reverse the vertical order)
- Field mode (save two fields in an interleaved frame or two separate fields)

14.1.8 Output Formats

Support YCbCr 4:2:2 and YCbCr 4:2:0 formats.

14.1.9 Horizontal Blanking Interval

The horizontal blanking interval should be at least 2.5us.

14.2 Memory Map Register

The memory mapped registers of VIC can be accessed via AMBA AHB slave interface. Note that registers with * are only updated at each frame end, the others are updated at once. The hierarchy of the register map is as follows. For those registers without n, m postfix, they are global registers or dedicated for the Bayer format.

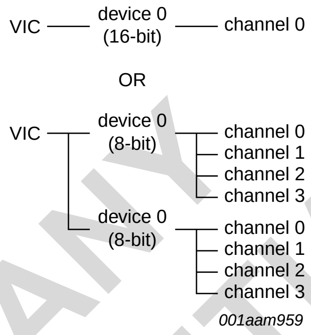


Fig 32. The Hierarchy of the Register Map

VIC could be configured as one 16-bit device or two 8-bit devices. When configured as one 16-bit device, it could accept the Bayer format up to 16-bit data, BT.1120 and 16-bit YCbCr 4:2:2 with separate SYNC signals. Always use channel 0 for the 16-bit device. When configured as two 8-bit devices, the supported formats and channels for each device are listed in Table 102. The two 8-bit devices should have the same input format, like BT.656 or time-multiplexed BT.656 or 8-bit YCbCr 4:2:2 with separate SYNC signals. Be careful not to let AF/AE windows exceed the input frame/field.

Table 102. Configuration for a 8-bit device

Edge type	Channel number	PCLK (MHz)	DIV_PCLK (MHz)	Support	Channel MMR		Table notes
					w/o CHID	w/ CHID	
Single Edge	1	24 - 180	24 - 180	Yes	0	0	[1]
	2	54	27	Partial	N/A	0,2	[2]
	4	108	27	Yes	0,1,2,3	CHID	[3]
Double Edge	1	N/A	N/A	N/A	N/A	N/A	N/A
	2	27	27	Yes	0,2	0,2	[4]
	4	54	27	No	N/A	N/A	[5]

[1] 1. A 27 MHz 1-channel BT.656 or an 8 b video stream w/ SYNC signals.
2. Always use channel 0 with or without CHID.

[2] 1. 54MHz 2-channel time-multiplexed BT.656.
2. w/ CHID: Always use CHID 0 and 2 for two video streams.
3. w/ CHID: Channels are dispatched according to CHID

[3] 1. 108MHz 4-channel time-multiplexed BT.656.
2. w/o CHID: Dispatch video streams to channel 0,1,2,3 depending on the order of the SYNC codes of the individual channel in the video stream detected.
3. w/ CHID: Channels are dispatched according to CHID.

[4] 1. 27 MHz 2-channel time-multiplexed BT.656.
2. w/o CHID: CH0 is the video stream at the rising edge; CH1 is the video stream at the falling.
3. w/ CHID: Always use CHID 0 and 2 for two video streams.
4. w/ CHID: Channels are dispatched according to CHID

[5] 1. 54 MHz 4-channel time-multiplexed BT.656.

14.2.1 VIC_VERSION (0x00000000)

Version information register.

Table 103. Version Information Register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x08	R	Major version number.
MINOR_VERSION	23 - 16	0x00	R	Minor version number.
BUILD_VERSION	15 - 08	0x00	R	Build version number.
REVISION	07 - 00	0x0D	R	Revision number.

14.2.2 VIC_CTRL (0x00000004)

The global control register.

Table 104. Global control register

Name	Bit	Default	R/W	Description
CLEAR	31	0x0	R/W	Write 1’b1 to clear maximum request-to-grant interval. Hardware will automatically clear this bit.
CLOCK_RATE	30 - 08	0x0	R/W	Number of AHB cycles for one tick.
-	07 - 06	0x0	-	Reserved.
HEADER_REF	05	0x0	R/W	Sync code detection scheme for BT.1120 mode 1’b0: The chroma channel uses the sync codes in itself. 1’b1: The chroma channel uses the sync codes from the luma channel.
IN_FORMAT*	04 - 02	0x0	R/W	Input formats. 3’b000: 8-bits input data with separate SYNC signals. 3’b001: 16-bits input data separate SYNC signals. 3’b010: 8-bit input data with sync codes (BT.656 input) 3’b011: 16-bit input data with sync codes (BT. 1120 input) 3’b100: Bayer data input.
-	01	0x0	-	Reserved.
VIC_EN	00	0x0	R/W	VIC enable control. 1’b0: Disable the VIC module. 1’b1: Enable the VIC module.

14.2.3 VIC_CTRL_DEVICE_n (0x00000008+n*4)

Control register for device n (n=0,1).

Table 105. Control register for device n

Name	Bit	Default	R/W	Description
-	31 - 09	0x0	-	Reserved.
CCIR656_CHID_TYPE_n	08 - 07	0x0	R/W	Select the Channel ID format for time-multiplexed output. 2'b00: No channel ID. 2'b01: CHID with the specific ITU-R BT.656 sync code. 2'b10: CHID with the specific horizontal blanking code. 2'b11: CHID with both the specific ITU-R BT.656 sync and horizontal blanking code.
CCIR656_MUX_n	06 - 05	0x0	R/W	Number of channels of BT.656 data in VIC device_n. 2'b00: 1 channel. 2'b01: 2 channels. 2'b10: 4 channels. 2'b11: 0 channel (disable this device).
CCIR656_EDGE_n	04	0x0	R/W	Specify the type of clock edge used to sample the BT.656 data in VIC device_n 1'b0: Single edge. 1'b1: Double edge (both rising edge and falling edge).
-	03	0x0	-	Reserved.
RAW_FIELD_MODE_EN_n*	02	0x0	R/W	Using separate SYNC signals, the field pin control. 1'b0: Disable the field pin. 1'b1: Enable the field pin to determine the input field.
HSYNC_TRG_n*	01	0x0	R/W	VIC_I_HSYNC_n trigger 1'b0: Rising edge. 1'b1: Falling edge.
VSYNC_TRG_n*	00	0x0	R/W	VIC_I_VSYNC_n trigger 1'b0: Rising edge. 1'b1: Falling edge.

14.2.4 VIC_CTRL_ CHANNEL_n_m (0x00000010+(n*4+m)*4)

Video input controller control register for channel_n_m (n=0,1; m=0,1,2,3). The maximum number of channel supported in ASC8851 / 8850 / 8849 / 8848 is 8 / 6 / 4 / 3 respectively.

Table 106. Video input controller control register

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
INT_REM_LINE_n_m*	28 - 24	0x0	R/W	Generate interrupt when the remaining number of lines is equal to INT_REM_LINE_n_m.
-	23 - 19	0x0	-	Reserved.
FIELD_INVERT_n_m*	18	0x0	R/W	Field bit control. 1'b0: Field bit 0 is top field. 1'b1: Field bit 1 is top field.

Table 106. Video input controller control register *...continued*

Name	Bit	Default	R/W	Description
FIELD_MODE_n_m*	17	0x0	R/W	Output field mode control. 1'b0: Write two single fields in SDRAM. 1'b1: Write one interleaved field in SDRAM.
OUT_FORMAT_n_m*	16	0x0	R/W	Output image format. 1'b0: YCb Cr 4: 2: 2 1'b1: YCb Cr 4: 2:0.
ECCFVH_n*	15	0x0	R/W	Error detection using FVH field. 1'b1: Enable FVH error detection. 1'b0: Disable FVH error detection.
MIRROR_n_m*	14	0x0	R/W	Mirror frame before writing to SDRAM 1'b0: Don't mirror. 1'b1: Mirror.
FLIP_n_m*	13	0x0	R/W	Flip frame before writing to SDRAM 1'b0: Don't flip. 1'b1: Flip.
CCIR656_P_n_m*	12	0x0	R/W	Progressive BT.656 input 1'b0: Interlaced BT.656 input. 1'b1: Progressive BT.656 input.
	11	0x0		Reserved.
NOSIG_CLEAR_n_m	10	0x0	R/W	No-signal counter enable control. 1'b0: Disable and clear no-signal counter. 1'b1: Enable no-signal counter.
UPDATE_MMR_n_m	09	0x0	R/W	Force update MMR immediately when set to 1. This bit will clear itself after updating MMR. This bit is used for the first time when VIC is initialized. Registers with * are updated through this bit.
OUT_EN_n_m*	08	0x0	R/W	Enable data write to SDRAM when set to 1
INT_EN_n_m	07	0x0	R/W	Interrupt generation control. 1'b0: Disable. 1'b1: Enable.
FIFO_FULL_OUT_EN_n_m	06	0x0	R/W	FIFO full output enable control. 1'b0: Disable data write out when FIFO full occurs.1'b1: Enable data write out when FIFO full occurs. This bit must be set to 1'b1 for ASC8848/49/50 M1 version
NOSIG_ERR_ACK_EN_n_m	05	0x0	R/W	NOSIG_ERR_ACK_n_m enable control. 1'b0: Disable. 1'b1: Enable.
FIFO_FULL_ACK_EN_n_m	04	0x0	R/W	FIFO_FULL_ACK_n_m enable control. 1'b0: Disable. 1'b1: Enable.

Table 106. Video input controller control register *…continued*

Name	Bit	Default	R/W	Description
OP_CMPT_ACK_EN_n_m	03	0x0	R/W	OP_CMPT_ACK_n_m enable control. 1’b0: Disable. 1’b1: Enable.
NOSIG_ERR_ACK_n_m	02	0x0	R/W	Set when no-signal error occurs and NOSIG_ERR_ACK_EN_n_m is 1’b1. 1’b0: No no-signal error occurs. 1’b1: No-Signal error occurs.
FIFO_FULL_ACK_n_m	01	0x0	R/W	Set when FIFO full occurs and FIFO_FULL_ACK_n_m is 1’b1. 1’b0: No FIFO full occurs. 1’b1: FIFO full occurs.
OP_CMPT_ACK_n_m	00	0x0	R/W	Set when VIC operation is complete and OP_CMPT_ACK_EN_n_m is 1’b1. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.

14.2.5 VIC_STAT_0 (0x00000030)

Video input controller status register for channel_0_m (m = 0,1,2,3)

Table 107. Video input controller status register

Name	Bit	Default	R/W	Description
-	31 - 30	0x0	-	Reserved.
BUF_0_3	29	0x0	R	The buffer which is being written (occupied) by the channel. 1’b0: Buffer0 is being used by VIC. 1’b1: Buffer1 is being used by VIC.
FERR_0_3	28	0x0	R	Frame error status. 1’b1: Error found when capturing. 1’b0: No error occurred.
FIELD_0_3	27	0x0	R	Field information. 1’b0: Top field. 1’b1: Bottom field.
NOSIG_ERR_0_3	26	0x0	R	Set when no-signal error occurs. 1’b0: No no-signal error occurs. 1’b1: No-Signal error occurs.
FIFO_FULL_0_3	25	0x0	R	Set when FIFO full occurs. 1’b0: No FIFO full occurs. 1’b1: FIFO full occurs.
OP_CMPT_0_3	24	0x0	R	Set when VIC operation is complete. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.
-	23 - 22	0x0	-	Reserved.

Table 107. Video input controller status register *…continued*

Name	Bit	Default	R/W	Description
BUF_0_2	21	0x0	R	The buffer which is being written (occupied) by the channel. 1’b0: Buffer0 is being used by VIC. 1’b1: Buffer1 is being used by VIC.
FERR_0_2	20	0x0	R	Frame status. 1’b1: Error found when capturing. 1’b0: No error occurred.
FIELD_0_2	19	0x0	R	Field status. 1’b0: Top field. 1’b1: Bottom field.
NOSIG_ERR_0_2	18	0x0	R	Set when no-signal error occurs. 1’b0: No no-signal error occurs. 1’b1: No-Signal error occurs.
FIFO_FULL_0_2	17	0x0	R	Set when FIFO full occurs. 1’b0: No FIFO full occurs. 1’b1: FIFO full occurs.
OP_CMPT_0_2	16	0x0	R	Set when VIC operation is complete. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.
-	15 - 14	0x0	-	Reserved.
BUF_0_1	13	0x0	R	The buffer which is being written (occupied) by the channel. 1’b0: Buffer0 is being used by VIC. 1’b1: Buffer1 is being used by VIC.
FERR_0_1	12	0x0	R	Frame status. 1’b1: Error found when capturing. 1’b0: No error occurred.
FIELD_0_1	11	0x0	R	Field status. 1’b0: Top field. 1’b1: Bottom field.
NOSIG_ERR_0_1	10	0x0	R	Set when no-signal error occurs. 1’b0: No no-signal error occurs. 1’b1: No-Signal error occurs.
FIFO_FULL_0_1	09	0x0	R	Set when FIFO full occurs. 1’b0: No FIFO full occurs. 1’b1: FIFO full occurs.
OP_CMPT_0_1	08	0x0	R	Set when VIC operation is complete. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.
-	07	0x1	-	Reserved.
LOAD_CMPT_0_0	06	0x0	R	Set when VIC completes loading gamma table. 1’b0: VIC gamma table loading is not complete. 1’b1: VIC gamma table loading is complete.

Table 107. Video input controller status register *…continued*

Name	Bit	Default	R/W	Description
BUF_0_0	05	0x0	R	The buffer which is being written (occupied) by the channel. 1'b0: Buffer0 is being used by VIC. 1'b1: Buffer1 is being used by VIC.
FERR_0_0	04	0x0	R	Frame status. 1'b1: Error found when capturing. 1'b0: No error occurred.
FIELD_0_0	03	0x0	R	Field status. 1'b0: Top field. 1'b1: Bottom field.
NOSIG_ERR_0_0	02	0x0	R	Set when no-signal error occurs. 1'b0: No no-signal error occurs. 1'b1: No-Signal error occurs.
FIFO_FULL_0_0	01	0x0	R	Set when FIFO full occurs. 1'b0: No FIFO full occurs. 1'b1: FIFO full occurs.
OP_CMPT_0_0	00	0x0	R	Set when VIC operation is complete. 1'b0: VIC operation is not complete. 1'b1: VIC operation is complete.

14.2.6 VIC_STAT_1 (0x00000034)

Video input controller status register for channel_n_m (n=0,1; m=0,1,2,3).

Table 108. Video input controller status register for channel_n_m

Name	Bit	Default	R/W	Description
	31 - 24	-	-	Reserved.
BUF_1_3	23	0x0	R	The buffer which is being written (occupied) by the channel. 1'b0: Buffer0 is being used by VIC. 1'b1: Buffer1 is being used by VIC.
FERR_1_3	22	0x0	R	Frame error status. 1'b1: Error found when capturing. 1'b0: No error occurred.
FIELD_1_3	21	0x0	R	Field information. 1'b0: Top field. 1'b1: Bottom field.
NOSIG_ERR_1_3	20	0x0	R	Set when no-signal error occurs. 1'b0: No no-signal error occurs. 1'b1: No-Signal error occurs.
FIFO_FULL_1_3	19	0x0	R	Set when FIFO full occurs. 1'b0: No FIFO full occurs. 1'b1: FIFO full occurs.

Table 108. Video input controller status register for channel_n_m *…continued*

Name	Bit	Default	R/W	Description
OP_CMPT_1_3	18	0x0	R	Set when VIC operation is complete. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.
BUF_1_2	17	0x0	R	The buffer which is being written (occupied) by the channel. 1’b0: Buffer0 is being used by VIC. 1’b1: Buffer1 is being used by VIC.
FERR_1_2	16	0x0	R	Frame status. 1’b1: Error found when capturing. 1’b0: No error occurred.
FIELD_1_2	15	0x0	R	Field status. 1’b0: Top field. 1’b1: Bottom field.
NOSIG_ERR_1_2	14	0x0	R	Set when no-signal error occurs. 1’b0: No no-signal error occurs. 1’b1: No-Signal error occurs.
FIFO_FULL_1_2	13	0x0	R	Set when FIFO full occurs. 1’b0: No FIFO full occurs. 1’b1: FIFO full occurs.
OP_CMPT_1_2	12	0x0	R	Set when VIC operation is complete. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.
BUF_1_1	11	0x0	R	The buffer which is being written (occupied) by the channel. 1’b0: Buffer0 is being used by VIC. 1’b1: Buffer1 is being used by VIC.
FERR_1_1	10	0x0	R	Frame status. 1’b1: Error found when capturing. 1’b0: No error occurred.
FIELD_1_1	09	0x0	R	Field status. 1’b0: Top field. 1’b1: Bottom field.
NOSIG_ERR_1_1	08	0x0	R	Set when no-signal error occurs. 1’b0: No no-signal error occurs. 1’b1: No-Signal error occurs.
FIFO_FULL_1_1	07	0x0	R	Set when FIFO full occurs. 1’b0: No FIFO full occurs. 1’b1: FIFO full occurs.
OP_CMPT_1_1	06	0x0	R	Set when VIC operation is complete. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.

Table 108. Video input controller status register for channel_n_m *…continued*

Name	Bit	Default	R/W	Description
BUF_1_0	05	0x0	R	The buffer which is being written (occupied) by the channel. 1’b0: Buffer0 is being used by VIC. 1’b1: Buffer1 is being used by VIC.
FERR_1_0	04	0x0	R	Frame status. 1’b1: Error found when capturing. 1’b0: No error occurred.
FIELD_1_0	03	0x0	R	Field status. 1’b0: Top field. 1’b1: Bottom field.
NOSIG_ERR_1_0	02	0x0	R	Set when no-signal error occurs. 1’b0: No no-signal error occurs. 1’b1: No-Signal error occurs.
FIFO_FULL_1_0	01	0x0	R	Set when FIFO full occurs. 1’b0: No FIFO full occurs. 1’b1: FIFO full occurs.
OP_CMPT_1_0	00	0x0	R	Set when VIC operation is complete. 1’b0: VIC operation is not complete. 1’b1: VIC operation is complete.

14.2.7 VIC_SYNC_DELAY_n (0x00000038+n*4)

This register provides the VIC module to accept shifted HSYNC signal for device_n (n = 0,1). Supports up to 4096 pixel clocks delay.

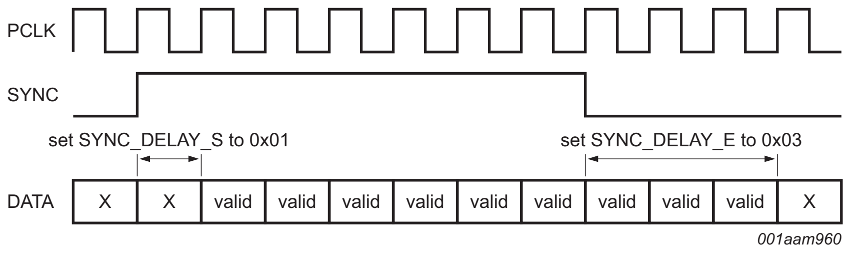


Fig 33. VIC Sync delay

Table 109. VIC sync delay

Name	Bit	Default	R/W	Description
SYNC_DELAY_S_n*	31 - 16	0x0	R/W	HSYNC start point delay cycle.
SYNC_DELAY_E_n*	15 - 00	0x0	R/W	HSYNC end point delay cycle.

14.2.8 VIC_MILLI_SECOND_n_m (0x00000040+n*0xE0+M*0x38)

This register contains the tick information.

Table 110. VIC milli second

Name	Bit	Default	R/W	Description
MILLI_SECOND	31 - 00	0x0	R	The number of ticks after VIC initialized. This could be used as the hardware timestamp for one captured frame. It could represent 1ms or 1us depending on CLOCK_RATE register in VIC_CTRL.

14.2.9 VIC_ADDR Group1 (0x00000044+n*0xE0+m80x38~0x0000004C+n*0xE0+m*0x38)

These registers specify the 1st output buffer addresses for channel_n_m (n = 0,1; m = 0, 1, 2, 3).

Table 111. VIC_ADDR Group1

Name	Bit	Default	R/W	Description
Y_ADDR_BUF0_n_m* (0x00000044 + n*0xE0 + m*0x38)	31 - 00	0x0	R/W	Starting address of the first buffer of Y-component.
CB_ADDR_BUF0_n_m* (0x00000048 + n*0xE0 + m*0x38)	31 - 00	0x0	R/W	Starting address of the first buffer of Cb-component.
CR_ADDR_BUF0_n_m* (0x0000004C + n*0xE0 + m*0x38)	31 - 00	0x0	R/W	Starting address of the first buffer of Cr-component.

14.2.10 VIC_ADDR Group2 (0x00000050+n*0xE0+m*038~0x00000058 +n*0xE0+m*0x38)

These registers specify the 2nd output buffer addresses for channel_n_m (n=0,1; m=0,1,2,3).

Table 112. VIC_ADDR group2

Name	Bit	Default	R/W	Description
Y_ADDR_BUF1_n_m* (0x00000050+ n*0xE0+m*0x38)	31-00	0x0	R/W	Starting address of the second buffer of Y component.
CB_ADDR_BUF1_n_m* (0x00000054+ n*0xE0+m*0x38)	31-00	0x0	R/W	Starting address of the second buffer of Cb component.
CR_ADDR_BUF1_n_m* (0x00000058+ n*0xE0+m*0x38)	31-00	0x0	R/W	Starting address of the second buffer of Cr component.

14.2.11 VIC_IN_SIZE_n_m (0x0000005C+ n*0xE0+m*0x38)

This register specifies the input frame/field width and height for channel_n_m (n = 0,1; m = 0, 1, 2, 3).

The number of pixels per line supported in ASC8848/49/50/51 is 2560/2560/4096/4096 respectively.

Table 113. VIC input size n_m

Name	Bit	Default	R/W	Description
HEIGHT_n_m*	31 - 16	0x0	R/W	Input frame/field height.
WIDTH_n_m*	15 - 00	0x0	R/W	Input frame/field height

14.2.12 VIC_CAP_H_n_m (0x00000060+n*0xE0+m*0x38)

This register specifies the horizontal capturing parameters for channel_n_m (n=0,1; m=0,1,2,3). Support up to 4096 pixels per line.

Table 114. Horizontal capturing parameters

Name	Bit	Default	R/W	Description
NPH_n_m*	31-16	0x0	R/W	Number of capturing pixels per line in horizontal direction. This register must be multiple of 16.
SPH_n_m*	15-00	0x0	R/W	Start capturing pixel horizontal. This register must be even.

14.2.13 VIC_CAP_V_n_m (0x00000064+ n*0xE0+m*0x38)

This register specifies the vertical capturing parameters for channel_n_m (n = 0,1; m = 0, 1, 2, 3). Supports up to 4096 lines per frame.

Table 115. Vertical capturing parameters

Name	Bit	Default	R/W	Description
NLV_n_m*	31 - 16	0x0	R/W	Number of capturing lines vertical for one progressive frame or two interlaced fields. This register must be even.
SLV_n_m*	15 - 00	0x0	R/W	Start capturing line vertical for one progressive frame or two interlaced fields. This register must be even.

14.2.14 VIC_STRIDE_n_m (0x00000068+ n*0xE0+m*0x38)

This register specifies the capturing strides for channel_n_m (n = 0,1; m = 0, 1, 2, 3). Supports up to 4096.

Table 116. Capturing strides for channel n_m

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	-	Reserved
STRIDE_n_m*	15 - 00	0x0	R/W	Stride for Y component. The stride for Cb/Cr component is half the value.

14.2.15 VIC_SBC_n_m (0x0000006C+ n*0xE0+m*0x38)

This register specifies saturation, brightness and contrast adjustments for channel_n_m (n = 0,1; m = 0, 1, 2, 3).

Table 117. Saturation, brightness and contrast adjustments for channel n_m

Name	Bit	Default	R/W	Description
-	31 - 25	0x0	-	Reserved
SATURATION_n_m*	24 - 16	0x0	R/W	The saturation control on the output chrominance. (0~511, 128: off)
BRIGHTNESS_n_m*	15 - 08	0x0	R/W	The brightness control on the output luminance. (-128~127, 0: off)
CONTRAST_n_m*	07 - 00	0x0	R/W	The contrast control on the output luminance (-128~127, 0: off)

14.2.16 VIC_CE_CTRL_n_m (0x0000070+n*0xE0+m*0x38)

Contrast enhancement control register.

Table 118. Contrast enhancement control register

Name	Bit	Default	R/W	Description
-	31 - 07	0x0	-	Reserved
CE_LOAD_TBL_CMPT	06	0x0	R/W	Load contrast enhance table complete signal. This register will be set by VIC and cleared by SW.
CE_LOAD_TBL_EN	05	0x0	R/W	Load contrast enhance table enable signal. Write 1’b1 to enable and this register will be cleared by VIC.
CE_BRIGHTNESS	04 - 01	0x0	R/W	Brightness control signal
CE_EN	00	0x0	R/W	Contrast enhancement enable control. 1’b0: Disable. 1’b1: Enable.

14.2.17 VIC_CE_TBL_ADDR_n_m (0x00000074+n*0xE0+m*0X38)

Contrast enhancement table address.

Table 119. Contrast enhancement table address

Name	Bit	Default	R/W	Description
CE_TBL_ADDR_n_m	31 - 00	0x0	R/W	Contrast enhancement

14.2.18 VIC_NO_SIGNAL (0x00000200)

This register specifies the no-signal interrupt generation period of the VIC module.

Table 120. No signal interrupt generation

Name	Bit	Default	R/W	Description
NO_SIGNAL	31 - 00	0x0	R/W	Number of AHB cycles to generate no-signal interrupt. If no SYNC code has been found for NO_SIGNAL cycles, MMR; FERR will be set to high and the interrupt will be asserted.

14.2.19 VIC_CMOS_CTRL (0x00000204)

This register configures the CMOS control register for device 0.

Table 121. Configuration of CMOS control register

Name	Bit	Default	R/W	Description
-	31 - 30	0x0	-	Reserved
CLAMP	29 - 22	0x0	R/W	Black clamp value in signed-magnitude format. If the MSB is 0, this value is for subtraction. If the MSB is 1, it is for addition.
ADDITIONAL_PAD_EN	21	0x0	R/W	Support two additional padding rows and columns for CMYG or Bilinear interpolation. 1’b0: Disable. 1’b1: Enable.
BAYER_BITWIDTH	20 - 16	0xA	R/W	The bit width of the Bayer pattern.
BLANK	15 - 04	0x0	R/W	Internal horizontal blanking when input external HSYNC is not present. It is recommended to set the same as the input external HSYNC. (unit: pixel clock)
LOAD_TBL_EN	03	0x0	R/W	Write 1’b1 to this register to start loading the gamma table. This register will clear itself.
DENOISE_EN*	02	0x0	R/W	The de-impulse noise removal enable control (Only for PCCI CFA method). 1’b0: Disable. 1’b1: Enable
CFA_MODE*	01 - 00	0x0	R/W	The CFA method. 2’b00: Bilinear interpolation (Bayer format). 2’b01: Primary consistent color interpolation (Bayer format). 2’b10: CyMgYeG interpolation. 2’b11: Reserved.

14.2.20 VIC_RGB2YCBCR_COEFF_0 (0x00000208)

RGB to YCbCr conversion matrix:

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} COEFF0 & COEFF1 & COEFF2 \\ -COEFF3 & -COEFF4 & COEFF5 \\ COEFF6 & -COEFF7 & -COEFF8 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \Big/ 256 + \begin{bmatrix} OFFSET \\ 128 \\ 128 \end{bmatrix}$$

This register configures the coefficients for RGB to YCbCr conversion matrix.

Table 122. RGB to YCbCr conversion matrix

Name	Bit	Default	R/W	Description
COEFF3	31 - 24	0x2C	R/W	RGB2YCbCr coefficient 3.
COEFF2	23 - 16	0x1D	R/W	RGB2YCbCr coefficient 2.
COEFF1	15 - 08	0x96	R/W	RGB2YCbCr coefficient 1.
COEFF0	07 - 00	0x4D	R/W	RGB2YCbCr coefficient 0.

14.2.21 VIC_RGB2YCBCR_COEFF_1 (0x0000020C)

This register configures the coefficients for RGB to YCbCr conversion matrix.

Table 123. RGB to YCbCr conversion matrix

Name	Bit	Default	R/W	Description
COEFF7	31 - 24	0x6E	R/W	RGB2YCbCr coefficient 7.
COEFF6	23 - 16	0x83	R/W	RGB2YCbCr coefficient 6.
COEFF5	15 - 08	0x83	R/W	RGB2YCbCr coefficient 5.
COEFF4	07 - 00	0x57	R/W	RGB2YCbCr coefficient 5.

14.2.22 VIC_RGB2YCBCR_COEFF_2 (0x00000210)

This register configures the coefficients for RGB to YCbCr conversion matrix and the Y killer function.

Table 124. RGB to YCbCr conversion matrix

Name	Bit	Default	R/W	Description
-	31 - 21	0x0	-	Reserved.
Y_KILLER	20 - 13	0xFF	R/W	Cb/Cr is set to zero if Y is larger than Y_KILLER.
OFFSET	12 - 08	0x0	R/W	RGB2YCbCr offset for Y.
COEFF8	07 - 00	0x15	R/W	RGB2YCbCr coefficient 8.

14.2.23 VIC_DENOISE_THRESHOLD (0x00000214)

This register configures the threshold for impulse noise removal.

Table 125. Impulse noise removal

Name	Bit	Default	R/W	Description
ROAD_THR	31 - 16	0x0	R/W	ROAD threshold. 0xFA is recommended.
NEIGHBOR_THR	15 - 00	0x0	R/W	Neighbor threshold. 0x28 is recommended.

14.2.24 VIC_AWB_CTRL (0x00000218)

This register configures the configuration for AWB.

Table 126. Configuration for AWB

Name	Bit	Default	R/W	Description
CBCR_MAX	31 - 24	0x0	R/W	Cb and Cr maximum threshold. It indicates the Cb or Cr value is ignored for averaging when it is larger than this threshold value.
CBCR_MIN	23 - 16	0x0	R/W	Cb and Cr minimum threshold. It indicates the Cb or Cr value is ignored for averaging when it is smaller than this threshold value.
-	15 - 14	0x0	-	Reserved.
	13	0x0		ASC8848/49/50 M1 version : Reserved
				ASC8848/49/50 M2 version and ASC8851 : AWB tuning position 1’b0: AWB tuning after CFA. 1’b1: AWB tuning before CFA.
AWB_AFTER_CC*	12	0x0	R/W	AWB measurement control. 1’b0: AWB measurement is before color correction. 1’b1: AWB measurement is after color correction.
MANUAL_WB_EN	11	0x0	R/W	Manual white balance control enable. 1’b0: Enable auto white balance. 1’b1: Enable manual white balance.
MAX_STEP	10 - 07	0x1	R/W	R/B gain adjustment maximum step size.
MIN_STEP	06 - 03	0x1	R/W	R/B gain adjustment minimum step size.
-	02 - 01	0x0	R/W	Reserved.
WB_EN	00	0x0	R/W	WB control enable. 1'b0: Disable WB. 1'b1: Enable WB.

14.2.25 VIC_AWB_ THRESHOLD (0x0000021C)

This register configures the threshold values in AWB.

Table 127. Threshold values in AWB

Name	Bit	Default	R/W	Description
CB_UPPER_BOND	31 - 24	0x0	R/W	Cb upper bond threshold. It indicates the blue or red component of the frame is too deep when it exceeds this threshold value.
CB_LOWER_BOND	23 - 16	0x0	R/W	Cb lower bond threshold. It indicates the blue or red component of the frame is too weak when it doesn’t exceed this threshold value.
CR_UPPER_BOND	15 - 08	0x0	R/W	Cr upper bond threshold. It indicates the blue or red component of the frame is too deep when it exceeds this threshold value.
CR_LOWER_BOND	07 - 00	0x0	R/W	Cr lower bond threshold. It indicates the blue or red component of the frame is too weak when it doesn’t exceed this threshold value.

14.2.26 VIC_AE_SRC_SEL (0x00000220)

Table 128. Generic

Name	Bit	Default	R/W	Description
	31-01	0x0		Reserved
AE_SRC_SEL	00-00	0x0		ASC8848/49/50 M1 version : Reserved
			R/W	ASC8848/49/50 M2 version and ASC8851 : AE luminance source selection 1’b0: After gamma correction. 1’b1: Before gamma correction.

14.2.27 Reserved (0x00000224~0x0000022C)

14.2.28 VIC_AWB_MANUAL_GAIN (0x00000230)

User defined R/B gain when manual WB is enabled.

Table 129. User defined R/B gain

Name	Bit	Default	R/W	Description
GAIN_UPPER_BOND	31 - 24	0x0	R/W	AWB gain upper bond.
GAIN_LOWER_BOND	23 - 16	0x0	R/W	AWB gain lower bond.
MANUAL_R_GAIN	15 - 08	0x0	R/W	User defined R gain (MANUAL_R_GAIN/64) when manual WB is enabled.
				Internal R gain when auto WB is enabled for ASC8848/49/50 M2 version and ASC8851 only
MANUAL_B_GAIN	07 - 00	0x0	R/W	User defined B gain (MANUAL_B_GAIN/64) when manual WB is enabled.
				Internal B gain when auto WB is enabled for ASC8848/49/50 M2 version and ASC8851 only

14.2.29 VIC_COLORCRT_COEFF_R (0x00000234)

Color correction matrix:

$$\begin{bmatrix} R_{out} \\ G_{out} \\ B_{out} \end{bmatrix} = \begin{bmatrix} COEFF\_RR & COEFF\_GR & COEFF\_BR \\ COEFF\_RG & COEFF\_GG & COEFF\_BG \\ COEFF\_RB & COEFF\_GB & COEFF\_BB \end{bmatrix} \begin{bmatrix} R_{in} \\ G_{in} \\ B_{in} \end{bmatrix} \Big/ 128 - \begin{bmatrix} R_{offset} \\ G_{offset} \\ B_{offset} \end{bmatrix}$$

This register configures the coefficients for color correction matrix.

Table 130. Coefficients for color correction

Name	Bit	Default	R/W	Description
COEFF_R_OFFSET	31 - 28	0x0	-	Reserved for ASC8848/49/50 M1 version
			R/W	Coefficient R offset, in range 0~15 for ASC8848/49/50 M2 version and ASC8851
COEFF_RR	27 - 18	0x0	R/W	Coefficient RR, in range -511~511. (First bit means sign-bit)
COEFF_GR	17 - 09	0x0	R/W	Coefficient GR, in range -255~255. (First bit means sign-bit)
COEFF_BR	08 - 00	0x0	R/W	Coefficient BR, in range -255~255. (First bit means sign-bit)

14.2.30 VIC_COLORCRT_COEFF_G (0x00000238)

This register configures the coefficients for color correction matrix.

Table 131. Coefficients for color correction matrix

Name	Bit	Default	R/W	Description
COEFF_G_OFFSET	31 - 28	0x0	-	Reserved for ASC8848/49/50 M1 version
			R/W	Coefficient Goffset, in range 0~15.
COEFF_RG	27 - 19	0x0	R/W	Coefficient RG, in range -255~255. (First bit means sign-bit)
COEFF_GG	18 - 09	0x0	R/W	Coefficient GG, in range -511~511. (First bit means sign-bit)
COEFF_BG	08 - 00	0x0	R/W	Coefficient BG, in range -255~255. (First bit means sign-bit)

14.2.31 VIC_COLORCRT_COEFF_B (0x0000023C)

This register configures the coefficients for color correction matrix.

Table 132. Color correction matrix

Name	Bit	Default	R/W	Description
COEFF_B_OFFSET	31 - 28	0x0	-	Reserved for ASC8848/49/50 M1 version
			R/W	Coefficient Boffset, in range 0~15 for ASC8848/49/50 M2 version and ASC8851
COEFF_RB	27 - 19	0x0	R/W	Coefficient RB, in range -255~255. (First bit means sign-bit)
COEFF_GB	18 - 10	0x0	R/W	Coefficient GB, in range -255~255. (First bit means sign-bit)
COEFF_BB	09 - 00	0x0	R/W	Coefficient BB, in range -511~511. (First bit means sign-bit)

14.2.32 VIC_GAMMA_TBL_ADDR (0x00000240)

This register specifies the gamma table address.

Table 133. Gamma table address

Name	Bit	Default	R/W	Function
GAMMA_TBL_ADDR	31 - 00	0x0	R/W	Gamma table address.

14.2.33 VIC_AF_CTRL0 (0x00000244)

This register specifies the control register 0 for AF.

Table 134. Control register 0 for AF

Name	Bit	Default	R/W	Description
-	31 - 24	0x0	R/W	Reserved
AF_EN	23	0x0	R/W	Enable auto-focus statistics output. 1’b0: Disable, 1’b1: Enable
-	27 - 00	0x0	R/W	Reserved

14.2.34 VIC_AF_WINDOW_START_POSITION (0x00000248)

This register specified the starting position of AF window.

Table 135. Starting position of AF window

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AF_WINDOW_START_POS_X	28 - 16	0x0	R/W	The X coordinate of AF window upper-left corner.
-	15 - 13	0x0	-	Reserved.
AF_WINDOW_START_POS_Y	12 - 00	0x0	R/W	The Y coordinate of AF window upper-left corner.

14.2.35 VIC_AF_WINDOW_SIZE (0x0000024C)

This register specifies the size of AF window.

Table 136. AF window size

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AF_WINDOW_WIDTH	28 - 16	0x0	R/W	AF window width.
-	15 - 13	0x0	-	Reserved.
AF_WINDOW_HEIGHT	12 - 00	0x0	R/W	AF window height.

14.2.36 VIC_AF_FOCUS_VALUE_HIGH (0x00000250)

This register records the focus value of AF.

Table 137. AF high focus value

Name	Bit	Default	R/W	Description
-	31 - 15	0x0	-	Reserved.
AF_FOCUS_VALUE_HIGH	14 - 00	0x0	R	Focus value higher 15 bits.

14.2.37 VIC_AF_FOCUS_VALUE_LOW (0x00000254)

This register records the focus value of AF.

Table 138. Low focus value of AF

Name	Bit	Default	R/W	Description
AF_FOCUS_VALUE_LOW	31 - 00	0x0	R	Focus value lower 32 bits.

14.2.38 VIC_AE_WINDOW0_START (0x0000025C)

This register specified the starting position of AE window 0.

Table 139. Starting position of AE window

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AE_WIN0_VER_START	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner.
-	15 - 13	0x0	-	Reserved.
AE_WIN0_HOR_START	12 - 00	0x0	R/W	The X coordinate of AE window upper-left corner.

14.2.39 VIC_AE_WINDOW0_RANGE (0x00000260)

This register specified the size of AE window 0.

Table 140. Size of AE window

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AE_WIN0_HEIGHT	28 - 16	0x0	R/W	AE window height.
-	15 - 13	0x0	-	Reserved.
AE_WIN0_WIDTH	12 - 00	0x0	R/W	AE window width.

14.2.40 VIC_AE_WINDOW1_START (0x00000264)

This register specified the starting position of AE window 1.

Table 141. Starting position of AE window

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AE_WIN1_VER_START	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner.
-	15 - 13	0x0	-	Reserved.
AE_WIN1_HOR_START	12 - 00	0x0	R/W	The X coordinate of AE window upper-left corner.

14.2.41 VIC_AE_WINDOW1_RANGE (0x00000268)

This register specified the size of AE window 1. The window width is up to 4096 pixels.

Table 142. AE window1 range

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AE_WIN1_HEIGHT	28 - 16	0x0	R/W	AE window height.
-	15 - 13	0x0	-	Reserved.
AE_WIN1_WIDTH	12 - 00	0x0	R/W	AE window width.

14.2.42 VIC_AE_WINDOW2_START (0x0000026C)

This register specified the starting position of AE window 2.

Table 143. Starting position of AE window2

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AE_WIN2_VER_START	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner.
-	15 - 13	0x0	-	Reserved.
AE_WIN2_HOR_START	12 - 00	0x0	R/W	The X coordinate of AE window upper-left corner.

14.2.43 VIC_AE_WINDOW2_RANGE (0x00000270)

This register specified the size of AE window 2. The window width is up to 4096 pixels.

Table 144. AE window2 range

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved.
AE_WIN2_HEIGHT	28 - 16	0x0	R/W	AE window height.
-	15 - 13	0x0	-	Reserved.
AE_WIN2_WIDTH	12 - 00	0x0	R/W	AE window width.

14.2.44 VIC_AE_WINDOW3_START (0x00000274)

This register specified the starting position of AE window 3.

Table 145. Starting position of AE window 3

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN3_VER_START	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner
-	15 - 13	0x0	-	Reserved
AE_WIN3_HOR_START	12 - 00	0x0	R/W	The X co-ordinate of AE window upper-left corner

14.2.45 VIC_AE_WINDOW3_RANGE (0x00000278)

This register specified the size of AE window 3. The window width is up to 4096 pixels.

Table 146. AE Window3 Range

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN3_HEIGHT	28 - 16	0x0	R/W	AE window height
-	15 - 13	0x0	-	Reserved
AE_WIN3_WIDTH	12 - 00	0x0	R/W	AE window width

14.2.46 VIC_AE_WINDOW4_START (0x0000027C)

This register specified the starting position of AE window 4.

Table 147. Starting position of AE

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN4_VER_START	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner
-	15 - 13	0x0	-	Reserved
AE_WIN4_HOR_START	12 - 00	0x0	R/W	The X coordinate of AE window upper-left corner

14.2.47 VIC_AE_WINDOW4_RANGE (0x00000280)

This register specified the size of AE window 4.

Table 148. Size of AE window4

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN4_HEIGHT	28 - 16	0x0	R/W	AE window height
-	15 - 13	0x0	-	Reserved
AE_WIN4_WIDTH	12 - 00	0x0	R/W	AE window width

14.2.48 VIC_AE_WINDOW5_START (0x00000284)

This register specified the starting position of AE window 5.

Table 149. Starting position of AE window

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN5_VER_START	28 - 16	0x0	R/W	The Y co-ordinate of AE window upper-left corner
-	15 - 13	0x0	-	Reserved
AE_WIN5_HOR_START	12 - 00	0x0	R/W	The X coordinate of AE window upper left corner

14.2.49 VIC_AE_WINDOW5_RANGE (0x00000288)

This register specified the size of AE window 5.

Table 150. Size of AE window 5

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN5_HEIGHT	28 - 16	0x0	R/W	AE window height
-	15 - 13	0x0	-	Reserved
AE_WIN5_WIDTH	12 - 00	0x0	R/W	AE window width

14.2.50 VIC_AE_WINDOW6_START (0x0000028C)

This register specified the starting position of AE window 6.

Table 151. Starting position of AE window 6

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN6_VER_START	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner
-	15 - 13	0x0	-	Reserved
AE_WIN6_HOR_START	12 - 00	0x0	r/w	The X coordinate of AE window upper-left corner

14.2.51 VIC_AE_WINDOW6_RANGE (0x00000290)

This register specified the size of AE window 6. The window width is up to 4096 pixels.

Table 152. Size of AE window6

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN6_HEIGHT	28 - 16	0x0	R/W	AE window height
-	15 - 13	0x0	-	Reserved
AE_WIN6_WIDTH	12 - 00	0x0	R/W	AE window width

14.2.52 VIC_AE_WINDOW7_START (0x00000294)

This register specified the starting position of AE window 7.

Table 153. Starting position of AE window 7

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN7_VER_STAT	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner
-	15 - 13	0x0	-	Reserved
AE_WIN7_HOR_START	12 - 00	0x0	R/W	The X coordinate of AE window upper left corner

14.2.53 VIC_AE_WINDOW7_RANGE (0x00000298)

This register specified the size of AE window 7. The window width is up to 4096 pixels.

Table 154. AE Window7 range

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN7_HEIGHT	28 - 16	0x0	R/W	AE window height
-	15 - 13	0x0	-	Reserved
AE_WIN7_WIDTH	12 - 00	0x0	R/W	AE window width

14.2.54 VIC_AE_WINDOW8_START (0x0000029C)

This register specified the starting position of AE window 8.

Table 155. Starting position of AE window8

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN8_VER_START	28 - 16	0x0	R/W	The Y coordinate of AE window upper-left corner
-	15 - 13	0x0	-	Reserved
AE_WIN8_HOR_START	12 - 00	0x0	R/W	The X coordinate of AE window upper-left corner

14.2.55 VIC_AE_WINDOW8_RANGE (0x000002A0)

This register specified the size of AE window 8. The window width is up to 4096 pixels.

Table 156. Size of AE window8

Name	Bit	Default	R/W	Description
-	31 - 29	0x0	-	Reserved
AE_WIN8_HEIGHT	28 - 16	0x0	R/W	AE window height
-	15 - 13	0x0	-	Reserved
AE_WIN8_WIDTH	12 - 00	0x0	R/W	AE window width

14.2.56 VIC_AE_WINDOW0_LUMINANCE (0x000002A4)

Window 0 luminance value measured by AE.

Table 157. Luminance value measurement

Name	Bit	Default	R/W	Description
AE_WIN0_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.57 VIC_AE_WINDOW1_LUMINANCE (0x000002A8)

Window 1 luminance value measured by AE.

Table 158. Window1 luminance value

Name	Bit	Default	R/W	Description
AE_WIN1_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.58 VIC_AE_WINDOW2_LUMINANCE (0x000002AC)

Window 2 luminance value measured by AE.

Table 159. Window 2 luminance measurement

Name	Bit	Default	R/W	Description
AE_WIN1_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.59 VIC_AE_WINDOW3_LUMINANCE (0x000002B0)

Window 3 luminance value measured by AE.

Table 160. Window 3 luminance measurement

Name	Bit	Default	R/W	Description
AE_WIN3_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.60 VIC_YCBCR_CLIP (0x000002B4)

Clip value for YCbCr.

Table 161. Clip value for YCbCr

Name	Bit	Default	R/W	Description
CLIP_Y_UPPER	31 - 24	0xFF	R/W	Upper bound for Y
CLIP_Y_LOWER	23 - 16	0x0	R/W	Lower bound for Y
CLIP_CBCR_UPPER	15 - 08	0xFF	R/W	Upper bound for Cb/Cr
CLIP_CBCR_LOWER	07 - 00	0x0	R/W	Lower bound for Cb/Cr

14.2.61 VIC_CMYG_CTRL0 (0x000002B8)

Configuration for CMYG sensors. Using PATTERN_VSHIFT and PATTER_HSHIFT to make the Bayer RGB or CMYG pattern like below to be correctly CFA-interpolated.

G	R	G	R
B	G	B	G
G	R	G	R
B	G	B	G

Cy	Ye	Cy	Ye
G	Mg	G	Mg
Cy	Ye	Cy	Ye
Mg	G	Mg	G

Table 162. Configuration for CMYG sensors

Name	Bit	Default	R/W	Description
IS_EDGE_THRD	31 - 22	0x0	R/W	Sobel gradient threshold for distinguishing if the operation pixel has an edge
-	21 - 04	0x0	-	Reserved
PATTERN_VSHIFT	03 - 02	0x0	R/W	Pattern vertical shifting number (For Bayer RGB and CMYG sensor)
PATTERN_HSHIFT	01 - 00	0x0	R/W	Pattern horizontal shifting number (For Bayer RGB and CMYG sensor)

14.2.62 VIC_CMYG_CTRL1 (0x000002BC)

Configuration for CMYG sensors.

Table 163. CMYG_CTRL1

Name	Bit	Default	R/W	Description
-	31 - 29	-	-	Reserved
ATTENUATE_MET HOD	28 - 26	0x0	R/W	3’b000: 1/2 3’b001: 1/4 3’b010: Left pixel 3’b011: Set 0 3’b100: Set 4095 Others: Reserved
DIR_EDGE_DIF_THRD	25 - 16	0x0	R/W	Threshold for distinguishing if the operating pixel has a strong edge
CHROMA_DIF_THRD	15 - 00	0x0	R/W	Threshold for attenuating chroma signals

14.2.63 VIC_AE_WINDOW4_LUMINANCE (0x000002C0)

Window 4 luminance value measured by AE.

Table 164. Window4 luminance

Name	Bit	Default	R/W	Description
AE_WIN4_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.64 VIC_AE_WINDOW5_LUMINANCE (0x000002C4)

Window 5 luminance value measured by AE.

Table 165. Window 5 luminance

Name	Bit	Default	R/W	Description
AE_WIN5_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.65 VIC_AE_WINDOW6_LUMINANCE (0x000002C8)

Window 6 luminance value measured by AE.

Table 166. Window 6 luminance

Name	Bit	Default	R/W	Description
AE_WIN6_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.66 VIC_AE_WINDOW7_LUMINANCE (0x000002CC)

Window 7 luminance value measured by AE.

Table 167. Window 7 luminance

Name	Bit	Default	R/W	Description
AE_WIN7_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.67 VIC_TM_CTRL (0x000002D0)

Tone Mapping control signals

Table 168. Tone mapping control signals

Name	Bit	Default	R/W	Description
GAMMA_OVERFLOW _SLOPE	31-28	0x0		Reserved for ASC8848/49/50 M1 version.
			R/W	Slope for R/G/B greater than 256 to do gamma mapping for ASC8848/49/50 M2 version and ASC8851 0: clip to 255 1:01 2:02 3:03 4:04 5:16 6:32 7.64 8.128

Table 168. Tone mapping control signals

Name	Bit	Default	R/W	Description
	27-04	0x0		Reserved
TM_BLEND_VALUE	03 - 01	0x0	R/W	The blending value of alpha=0.7 and alpha=1.
TM_EN	00 - 00	0x0	R/W	Enable signal for tone mapping function 1’b0: Disable 1’b1: Enable

14.2.68 VIC_AWB_EXCLUDE_HORI_WINDOW (0x000002D4)

AWB exclude horizontal window.

Table 169. AWB exclude horizontal window

Name	Bit	Default	R/W	Description
AWB_EXCLUDE_X_START	31 - 16	0x0	R/W	The X coordinate of the exclusive AWB window upper-left corner
AWB_EXCLUDE_X_END	15 - 00	0x0	R/W	The X coordinate of the exclusive AWB window lower-right corner

14.2.69 VIC_AWB_EXCLUDE_VERT_WINDOW (0x000002D8)

AWB exclude horizontal window.

Table 170. AWB exclude vertical window

Name	Bit	Default	R/W	Description
AWB_EXCLUDE_Y_START	31-16	0x0	R/W	The Y coordinate of the exclusive AWB window upper-left corner
AWB_EXCLUDE_Y_END	15-00	0x0	R/W	The Y coordinates of the exclusive AWB window lower-right corner

14.2.70 VIC_AWB_CB_SUM (0x000002DC)

AWB statistics: Sum of Cb component.

Table 171. Sum of Cb component

Name	Bit	Default	R/W	Description
AWB_CB_SUM	31 - 00	0x0	R	Sum of Cb components of the whole frame except the exclusive AWB window

14.2.71 VIC_AWB_CR_SUM (0x000002E0)

AWB statistics: Sum of Cr component.

Table 172. Sum of Cr components

Name	Bit	Default	R/W	Description
AWB_CR_SUM	31 - 00	0x0	R	Sum of Cr components of the whole frame except the exclusive AWB window

14.2.72 VIC_AE_WINDOW8_LUMINANCE (0x000002E4)

Window 8 luminance value measured by AE.

Table 173. Window 8 luminance value measurement

Name	Bit	Default	R/W	Description
AE_WIN8_LUM	31 - 00	0x0	R	Total luminance in AE window

14.2.73 VIC_AE_WINDOWS_MSB_LUMINANCE (0x000002E8)

This register specifies the control signals for AE.

Table 174. Windows MSB luminance

Name	Bit	Default	R/W	Description
-	31 - 18	0x0	-	Reserved
AE_WIN8_MSB_LUM	17 - 16	0x0	R	MSB 2bits of the total luminance in AE widow 8
AE_WIN7_MSB_LUM	15 - 14	0x0	R	MSB 2bits of the total luminance in AE widow 7
AE_WIN6_MSB_LUM	13 - 12	0x0	R	MSB 2bits of the total luminance in AE widow 6
AE_WIN5_MSB_LUM	11 - 10	0x0	R	MSB 2bits of the total luminance in AE widow 5
AE_WIN4_MSB_LUM	09 - 08	0x0	R	MSB 2bits of the total luminance in AE widow 4
AE_WIN3_MSB_LUM	07 - 06	0x0	R	MSB 2bits of the total luminance in AE widow 3
AE_WIN2_MSB_LUM	05 - 04	0x0	R	MSB 2bits of the total luminance in AE widow 2
AE_WIN1_MSB_LUM	03 - 02	0x0	R	MSB 2bits of the total luminance in AE widow 1
AE_WIN0_MSB_LUM	01 - 00	0x0	R	MSB 2bits of the total luminance in AE widow 0

14.2.74 VIC_AF_CTRL1 (0x000002EC)

This register specifies the control register 1 for AF.

Table 175. Windows MSB luminance

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
AF_FRAME_INTV	07 - 00	0x0	R/W	Calculate the focus value every AF_FRAME_INTV frame

14.2.75 VIC_PHOTO_LDC_CTRL (0x000002F0)

Photometric lens distortion correction control register.

Table 176. Photometric lens distortion correction control register

Name	Bit	Default	R/W	Description
-	31 - 03	0x0	-	Reserved
PHOTO_LDC_LOAD_TBL_CMPT	02	0x0	R/W	Photometric lens distortion correction table loading complete indication. This bit is set by VIC and cleared by SW. 1’b0 still loading 1’b1: Loading complete
PHOTO_LDC_FIRST_LOAD_TBL_EN	01	0x0	R/W	Enable signal of the first time table loading for photometric lens distortion correction function. This bit should be sent to 1’b1 at the initialization of VIC and then be cleared to 0 by VIC. 1’b0: Disable 1’b1: Enable
PHOTO_LDC_EN*	00	0x0	R/W	Enable signal for photometric lens distortion correction function 1’b0: Disable 1’b1:Enable

14.2.76 VIC_PHOTO_LDC_TBL_ADDR (0x000002F4)

Photometric lens distortion correction table address.

Table 177. Photometric lens distortion correction table address

Name	Bit	Default	R/W	Description
PHOTO_LDC_TBL_ADDR	31 - 00	0x0	R/W	Photometric lens distortion correction table address

14.2.77 VIC_AWB_RED_SUM (0x000002F8)

AWB statistics: Sum of R component.

Table 178. Sum of R component

Name	Bit	Default	R/W	Description
AWB_RED_SUM	31 - 00	0x0	R	Sum of R components of the whole frame except the exclusive AWB window

14.2.78 VIC_AWB_GREEN_SUM (0x000002FC)

AWB statistics: Sum of G component.

Table 179. Sum of G component

Name	Bit	Default	R/W	Description
AWB_GREEN_SUM	31 - 00	0x0	R	Sum of G components of the whole frame except the exclusive AWB window.

14.2.79 VIC_AWB_BLUE_SUM (0x00000300)

AWB statistics: Sum of B component.

Table 180. Sum of B component

Name	Bit	Default	R/W	Description
AWB_BLUE_SUM	31 - 00	0x0	R	Sum of B components of the whole frame except the exclusive AWB window

14.2.80 VIC_CMOS_HOR_PENALTY_THR (0x00000304)

Horizontal penalty threshold for CFA PCCI edge detector. It makes CFA PCCI more easily to use vertical interpolation.

Table 181. Horizontal penalty threshold for CFA PCCI edge detector

Name	Bit	Default	R/W	Description
-	31 - 18	0x0	-	Reserved
CFA_PCCI_HOR_PEN_THR	17 - 00	0x0	R/W	Horizontal penalty threshold for CFA PCCI edge detector

14.2.81 VIC_CMOS_VER_PENALTY_THR (0x00000308)

Vertical penalty threshold for CFA PCCI edge detector. It makes CFA PCCI more easily to use horizontal interpolation.

Table 182. Vertical penalty threshold

Name	Bit	Default	R/W	Description
-	31 - 18	0x0	-	Reserved
CFA_PCCI_VER_PEN_THR	17 - 00	0x0	R/W	Vertical penalty threshold for CFA PCCI edge detector

14.3 Block Diagram

The IC can be configured either as one 16-bit device or as two 8-bit devices.

14.3.1 16-Bit Device

When it is configured as a 16-bit device, the VIC accepts Bayer RGB, CMYG or BT.1120 input formats. In this configuration, the pixel clock is up to 180MHz.

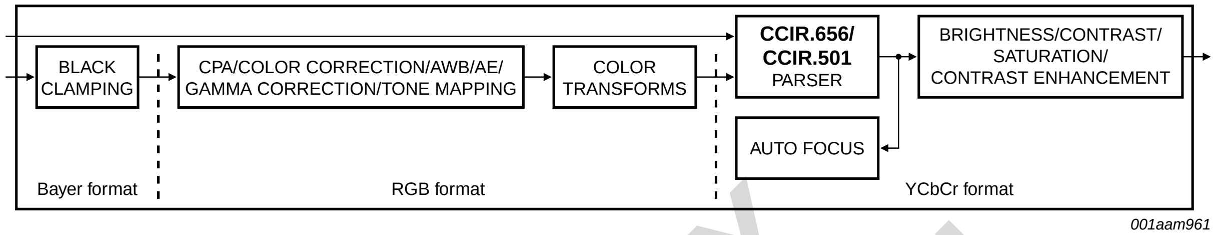

BLACK CLAMPING
CPA/COLOR CORRECTION/AWB/AE/ GAMMA CORRECTION/TONE MAPPING
COLOR TRANSFORMS
CCIR.656/ CCIR.501 PARSER
BRIGHTNESS/CONTRAST/ SATURATION/ CONTRAST ENHANCEMENT
AUTO FOCUS
Bayer format
RGB format
YCbCr format
001aam961

Fig 34. Block Diagram of a 16-Bit Device

14.3.2 8-Bit Device

When VIC is configured as two 8-bit devices, it can accept single-channel video stream, two-channel time-multiplexed video stream, or four-channel time-multiplexed video stream. The supported clock frequency is specified in Table 103.

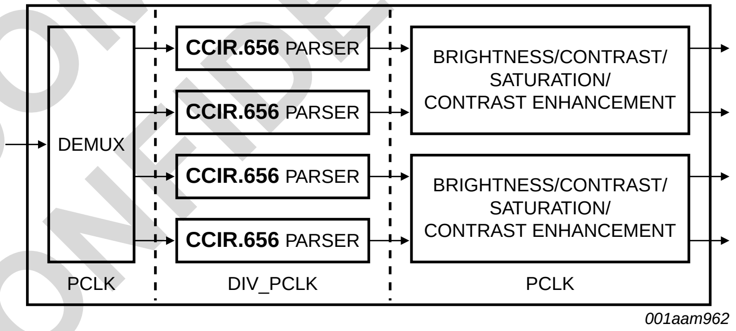

DEMUX
CCIR.656 PARSER
CCIR.656 PARSER
CCIR.656 PARSER
CCIR.656 PARSER
BRIGHTNESS/CONTRAST/ SATURATION/ CONTRAST ENHANCEMENT
BRIGHTNESS/CONTRAST/ SATURATION/ CONTRAST ENHANCEMENT
PCLK
DIV_PCLK
PCLK
001aam962

Fig 35. Block Diagram of an 8-bit Device

14.4 Input Formats

There are various kinds of video stream formats supported in the VIC. To support SD/HD video decoders or CMOS sensors, BT.656, BT.1120, 8-/16-bit YCbCr 4:2:2 with separate SYNC signals is to be used. To support multiple channel applications, the time-division-multiplexed BT.656 video stream is used.

14.4.1 16-Bit Device

14.4.1.1 Bayer RGB and CMYG

In Bayer/CMYG format, the VSYNC blanking must be at least 3 line periods. For ASC8848/49/50 M1 version additional requirements are
* VSYNC must be asserted before the first active video of HSYNC at least one pixel clock.

* If HSYNC will be toggling in VSYNC blanking, the de-assertion of HSYNC must be prior to VSYNC assertion at least one pixel clock..

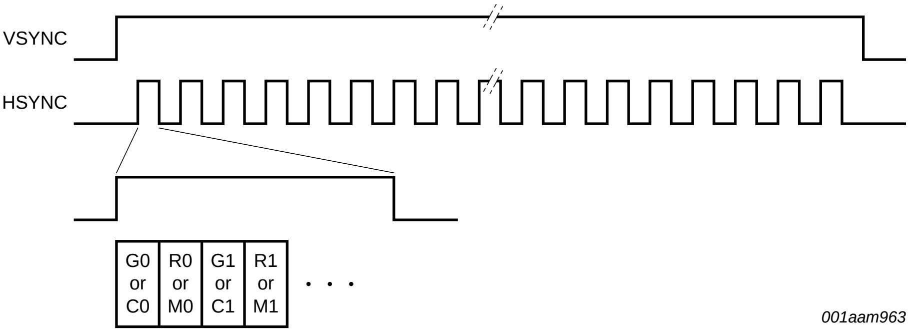


Fig 36. Timing diagram of Bayer RGB and CMYG format

14.4.1.2 YCbCr

There are two kinds of video streams supported in this configuration, BT.1120 and YCbCr 4:2:2 with seperate SYNC signals. BT.1120 format has embedded SYNC codes in the data pins. The high byte of the 16-bit data is Cb/Cr component while the low byte is the Y component. The video format timing is up to 1080p60@148.5MHz.

Figure 37 provides a typical timing diagram for BT.1120.

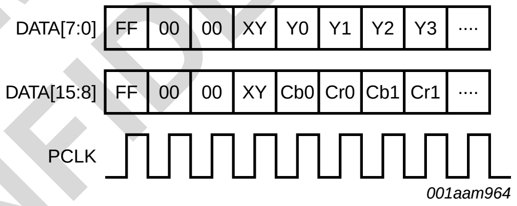


Fig 37. Timing diagram of BT1120

Figure 38 shows the typical timing of 16-bit YCbCr supported by most HDMI receivers.

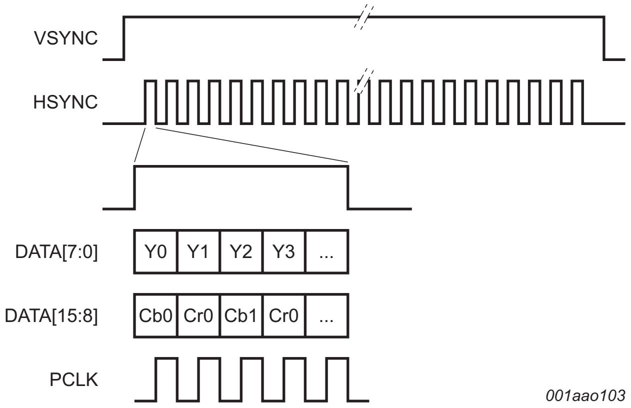


Fig 38. Timing diagram of 16-bit YCbCr with seperate SYNC signals

14.4.2 8-Bit Device

14.4.2.1 Single-Channel Video Stream

There are two kinds of video streams supported in this configuration, BT.656 and YCbCr 4:2:2 with separate SYNC signals. Figure 39 is a typical timing diagram of video decoders.

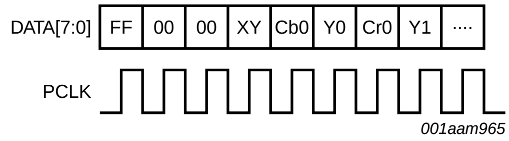


Fig 39. Timing Diagram of Single-Channel BT656 Video Stream

Figure 40 shows the typical timing diagram of CMOS smart sensors.

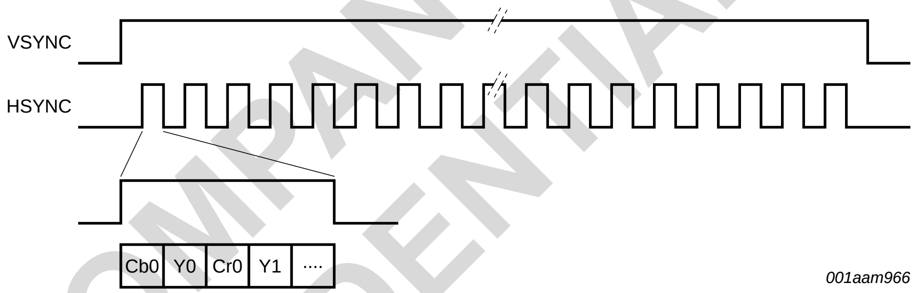


Fig 40. Timing Diagram of Single-Channel Video Stream with Separate SYNC signals.

14.4.2.2 2-Channel Video Stream with Single-Edge Clocking

The 2-channel time-multiplexed video stream must be specified with the channel ID (CHID) either in the SYNC codes or the horizontal blanking code. CHID[1:0] must be 2’b00 and 2’b10. The video stream will be de-multiplexed in VIC into CH0 and CH2 according to the channel ID.

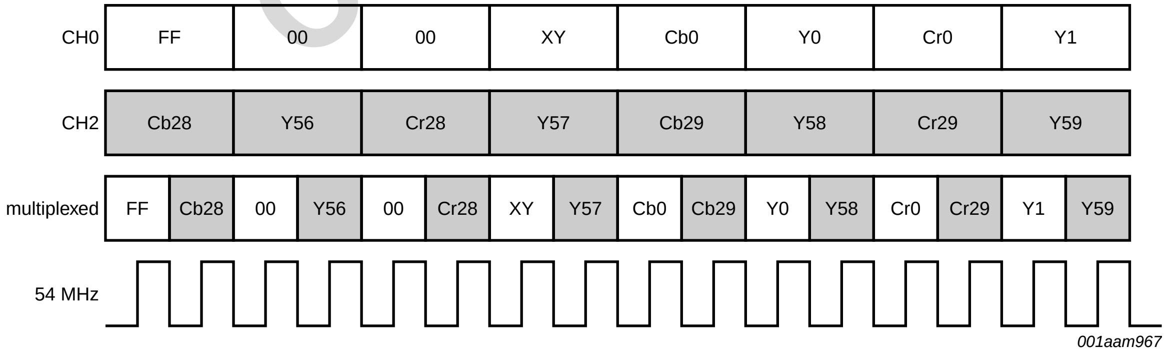


Fig 41. Timing Diagram of Two-Channel Video Stream with Single-Edge Clocking

14.4.2.3 2-Channel Video Stream with Double-Edge Clocking

The 2-channel time-multiplexed video stream will be de-multiplexed in VIC into CH0 (rising edge) and CH2 (falling edge) if no CHID is specified. If the channel ID is added, CHID[1:0] must be 2’b00 and 2’b10 and then the video stream will be de-multiplexed in VIC into CH0 and CH2 according to the channel ID.

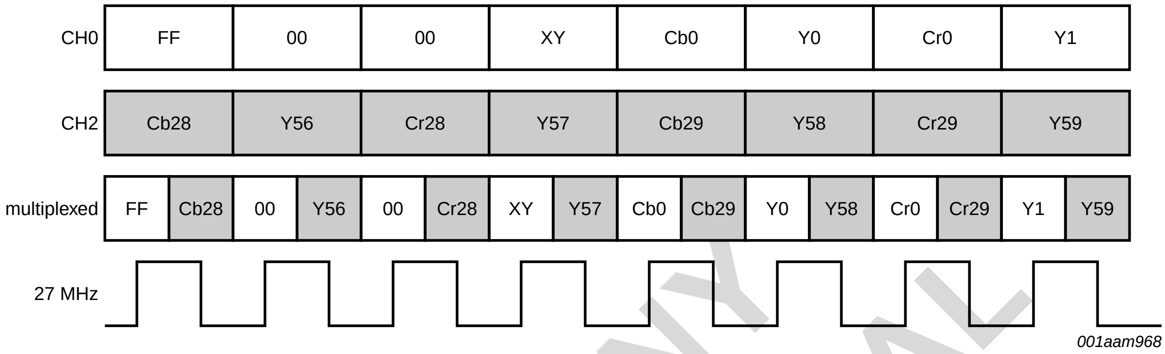


Fig 42. Timing Diagram of Two-Channel Video Stream with Double-Edge Clocking

14.4.2.4 4-Channel Video Stream with Single-Edge Clocking

The 4-channel time-multiplexed video stream will be de-multiplexed in VIC into CH0, CH1, CH2, and CH3 depending on the order of the SYNC codes of the individual channel in the video stream detected if no CHID is specified. If the channel ID is added, CHID[1:0] must be 2’b00, 2’b01, 2’b10, and 2’b11 and then the video stream will be de-multiplexed in VIC into CH0, CH1, CH2, and CH3 according to the channel ID.

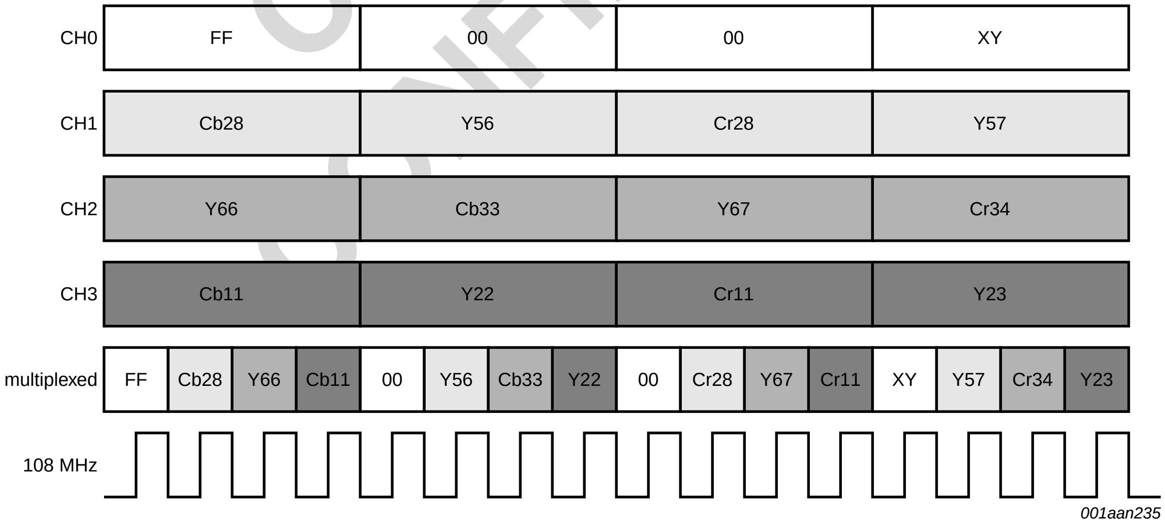


Fig 43. Timing Diagram of Four-Channel Video Stream with Single-Edge Clocking

14.4.2.5 Channel ID Format

There are two kinds of channel ID formats supported in VIC to identify the individual channel in the time-multiplexed video stream. First, the channel ID is inserted in the SYNC codes as shown in Table 183.

Table 183. Channel ID format for 4-channel Time-Multiplexed Video Stream (SYNC Codes)

BT.656 Timing Reference Signal							Description
First	Second	Third	Fourth				
			CH0	CH1	CH2	CH3	
FF	00	00	80	81	82	83	Field 1, active, SAV
FF	00	00	90	91	92	93	Field 1, active, EAV
FF	00	00	A0	A1	A2	A3	Field 1, blanking, SAV
FF	00	00	B0	B1	B2	B3	Field 1, blanking, EAV
FF	00	00	C0	C1	C2	C3	Field 2, active, SAV
FF	00	00	D0	D1	D2	D3	Field 2, active EAV
FF	00	00	E0	D1	D2	D3	Field 2, blanking, SAV
FF	00	00	F0	F1	F2	F3	Field 2, blanking, EAV

Second, the channel ID is inserted in the horizontal blanking code as shown in Table 184

Table 184. Channel ID Format for 4-channel Time-Multiplexed Video Stream (Horizontal Blanking Code)

	CH0	CH1	CH2	CH3
Y	10	11	12	13
Cb/Cr	80	81	82	83

14.4.3 Interrupt Generation

VIC supports up to 8 channels and all channels share one common interrupt. This sections shows how to distinguish which device issues the interrupts and how the interrupt is generated. Each channel has its own STAT and CTRL MMR.

Table 185 shows all conditions possibly encountered during the video capture. OP_CMPT_ACK_EN, FIFO_FULL_ACK_EN and NOSIG_ERR_ACK_EN decides which kind of interrupt will be asserted.

Table 185. Video Capture Status Descriptions

Condition	Associate knowledge and status signals	
	STAT	CTRL

Frame capture without errors:
1.OP_CMPT_ACK_EN = 1.
2.Frame header found (BT.656).
3.INT_REM_LINE meet
	OP_CMPT = 1
	FERR = 0
		OP_CMPT_ACK = 1

Input parsing error: 1.OP_CMPT_ACK_EN = 1 2.Parsing error due to invalid frame header (BT.656) or input width mismatch.	FERR = 1	OP_CMPT_ACK = 1

FIFO full error:
1.FIFO_FULL_ ACK_EN = 1
2.Output FIFO is full and the pixels are dropped.
	FIFO_FULL = 1
	FERR = 1
		FIFO_FULL_ACK = 1

No signal error:
1.NOSIG_ERR_ACK_EN = 1
2.Next frame header or frame sync is not detected after a given period.
	NOSIG_ERR = 1
	FERR = 1
		NOSIG_ERR_ACK = 1

Since all interrupts are ORed together, after the host receives the interrupt signal, it should check the STAT for FERR, OP_CMPT, FIFO_FULL, and NOSIG_ERR of all channels to know which channel asserts the interrupt and what type of conditions occurred. Remember to clear the corresponding ACK bits in CTRL MMR in order to de-assert the interrupt.

15. General Purpose I/O

15.1 General description

ASC8848/49/50/51 SoC provides 20 general-purpose I/O (GPIO). Each GPIO can be configured as input or output independently. Some of the GPIO signals are shared with other signals. See Table 186 for details. For multi-function pins, make sure only one function is enabled at one time. GPIO must be to set input direction to disable it so as not to interfere with the advanced general purpose output function.

Table 186. GPIO Signals

Name	Description
GPIO[19:8]	Dedicated for GPIO.
GPIO[7:0]	1. GPIO[7:0]. AGPO[7:0] must be disabled first (enabled by default and disabled by setting AGPOC_DFT_DATA_OE_N to 32'h000000FF). 2. AGPO[7:0] controlled by the advanced general purpose output controller.

15.2 Features

15.2.1 I/O pins

Up to 20 independent bi-directional I/O pins.

15.2.2 Pull Mode

Each pin can be configured pull-high or pull-low independently.

15.2.3 Interrupt Mode

Each pin can be configured to high-level, low-level, positive-edge, negative-edge, or both-edge trigger mode separately to trigger the GPIO interrupt signal. The GPIO interrupt signal is level-triggered to the interrupt controller. When one GPIO is level-triggered, the application needs to clear the external interrupt source to make the GPIO interrupt signal de-asserted. When one GPIO is edge-triggered, the application needs to clear the GPIO interrupt signal through GPIOC_INTR_CLEAER register.

15.2.4 De-Bounce Mode

When the de-bounce mode is enabled, each pin can be de-bounced to filter out the unexpected noise from the data input pin if the noise period is less than the de-bouncing period.

15.3 Memory Map Registers

15.3.1 GPIOC_VERSION (0x00000000)

Version information register.

Table 187. Version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x03	R	Major version number
MINOR_VERSION	23 - 16	0x00	R	Minor version number
BUILD_VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x08	R	Revision number

15.3.2 GPIOC_DATA_OUT (0x00000004)

Output data register.

Table 188. Output data register

Name	Bit	Default	R/W	Description
DATA_OUT	19 - 00	0x0	R/W	If the direction is output, write this register to control the output logic level.

15.3.3 GPIOC_DATA_IN (0x00000008)

Input data register.

Table 189. Input data register

Name	Bit	Default	R/W	Description
DATA_IN	19-00	0x0	R	This register shows the logic level on the GPIO

15.3.4 GPIOC_PIN_DIR (0x0000000C)

Pin direction register.

Table 190. Pin direction register

Name	Bit	Default	R/W	Description
PIN_DIR	19-00	0x0	R/W	1’b0: Input 1’b1:Output

15.3.5 Reserved (0x00000010)

15.3.6 GPIOC_DATA_SET (0x00000014)

Output data set register.

Table 191. Output data set register

Name	Bit	Default	R/W	Description
DATA_SET	19-00	0x0	W	When writing 1’b1 to some bits in this register, the corresponding bits on the GPIO will be set to 1’b1. This register is self cleared.

15.3.7 GPIOC_DATA_CLEAR (0x00000018)

Output data clear register.

Table 192. Output data clear register

Name	Bit	Default	R/W	Description
DATA_CLR	19 - 00	0x0	W	When writing 1’b1 to some bits in this register, the correspondent bits on the GPIO will be set to 1’b0. This register is self cleared.

15.3.8 GPIOC_PIN_PULL_ENABLE (0x0000001C)

Pull mode enable register.

Table 193. Pull mode enable register

Name	Bit	Default	R/W	Description
PIN_PULL_EN	19 - 00	0x0	R/W	Control the pull-up or pull-down function of the GPIO 1’b0: Disable 1’b1: Enable

15.3.9 GPIOC_PIN_PULL_TYPE (0x00000020)

Pull type register.

15.3.10 GPIOC_INTR_ENABLE (0x00000024)

Interrupt enable register.

Table 194. Interrupt enable register

Name	Bit	Default	R/W	Description
INTR_EN	19 - 00	0x0	R/W	It is a mask of interrupt detection logic. When the pin direction is set to input and the interrupt detection is enabled, the interrupt detection logic can accept interrupt from the output port of the bidirectional I/O pad.

15.3.11 GPIOC_INTR_RAW_STATE (0x00000028)

Interrupt raw state register.

Table 195. Interrupt raw state register

Name	Bit	Default	R/W	Description
INTR_RAW_STATE	19 - 00	0x0	R	When the corresponding INTR_EN bit is HIGH, this register shows the state of the external interrupt sources.

15.3.12 GPOIC_INTR_MASK_STATE (0x0000002C)

Masked interrupt state register.

Table 196. Masked interrupt state register

Name	Bit	Default	R/W	Description
INTR_MASK_STATE	19 - 00	0x0	R	When the corresponding INTR_EN bit is HIGH, this register shows masked external interrupt sources. GPIOC’s interrupt pin will be asserted once this register is not zero.

15.3.13 GPIOC_INTR_MASK (0x00000030)

Interrupt mask register.

Table 197. Interrupt mask register

Name	Bit	Default	R/W	Description
INTR_MASK	19 - 00	0x0	R/W	Interrupt mask control bits. 1’b0: External interrupt is enabled 1’b1: External interrupt is masked.

15.3.14 GPIOC_INTR_CLEAR (0x00000034)

Interrupt state clear register.

Table 198. Interrupt state clear register

Name	Bit	Default	R/W	Description
INTR_CLR	19 - 00	0x0	W	When writing 1’b1 to this register, the correspondent bit of the interrupt state register is cleared. This register is self cleared.

15.3.15 GPIOC_INTR_TRIGGER_TYPE (0x00000038)

Interrupt triggered method register.

Table 199. Interrupt triggered method register

Name	Bit	Default	R/W	Description
INTR_TRIG_TYPE	19 - 00	0x0	R/W	1’b0: Edge-triggered type 1’b1: Level-triggered type

15.3.16 GPIOC_INTR_BOTH (0x0000003C)

Edge triggered mode register.

Table 200. Edge triggered mode register

Name	Bit	Default	R/W	Description
INTR_BOTH	19 - 00	0x0	R/W	This register is only meaningful if the interrupt type is set to edge trigger type.

15.3.17 GPIOC_INTR_DIR (0x00000040)

Interrupt direction register.

Table 201. Interrupt direction register

Name	Bit	Default	R/W	Description
INTR_DIR	19 - 00	0x0	R/W	1’b0: Positive edge or high level trigger 1’b1: Negative edge or low level trigger

15.3.18 GPIOC_DEBOUNCE_ENABLE (0x00000044)

De-bounce enable register.

Table 202. De-bounce enable register

Name	Bit	Default	R/W	Description
DEBOUNCE_EN	19 - 00	0x0	R/W	1’b’0: Disable de-bounce capability 1’b1: Enable de-bounce capability

15.3.19 GPIOC_DEBOUNCE_PERIOD (0x00000048)

De-bounce cycle register.

Table 203. De-bounce cycle register

Name	Bit	Default	R/W	Description
-	31 - 24	-	-	Reserved
DEBOUNCE_PERIOD	23 - 00	0x0	R/W	Minimum de-bounce period in APB clock cycle.

16. USB 2.0

16.1 General description

There is a one-port USB2.0 in ASC8848/49/50/51 SoC. It is compliant with USB specification 2.0 and OTG supplement to the USB 2.0 specification revision 1.0a. It also supports session request protocol (SRP) and host negotiation protocol (HNP). USB 2.0 test modes are implemented to facilitate the compliance testing.

Acting as a host controller, 5 V VBUS could be removed if it is not required.

16.2 Features

The USB 2.0 provides the following features.

- Supports 480 Mbps high-speed, 12 Mbps full-speed, and 1.5 Mbps low-speed (Host mode only) data transmission rates
- Supports a generic root hub
- Implements a 4KB FIFO and dynamic FIFO sizing
- Includes a DMA controller to support TX and RX transfers
- Supports off-chip charge pump regulator to generate 5 V for VBUS
- Supports Session Request Protocol (SRP)
- Supports Host Negotiation Protocol (HNP)

17. Inter-IC Sound Slave Controller

17.1 General description

The Inter-IC Sound (I2S) Bus is a simple three-wire serial bus protocol developed by Philips to transfer stereo audio data. The bus only handles the transfer of audio data; hence control and subcoding signals need to be transferred separately using a different bus protocol (such as I2C). The I2S controller in ASC8848/49/50/51 SoC only supports slave mode which means the bit-clock (BCLK) and word select (WS) must be provided by the external audio codec. The master clock (MCLK) which might be 256fs or 384fs could be provided by ASC8848/49/50/51 SoC through the system controller (Section 7.2.12 and Table 25).

17.2 Features

- Supports I2S slave mode
- Full duplex communication due to the independence of transmitter and receiver
- Audio data resolutions up to 32 bits
- Programmable thresholds of RX and TX FIFOs
- Support external DMA interface to request APBC to move data from/to I2SSC
- Independent RX and TX FIFOs
- Independent 8-entry left and right FIFOs for RX and TX FIFOs
- Four RX-only and one full-duplex I2SSC controllers

17.3 Memory Map Register

17.3.1 IER (0x00000000)

This register acts as a global enable/disable control for I2SSC.

Table 204. IER

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
IEN	00 - 00	0x0	R/W	I2SSC enable control 1’b0: Disable 1’b1: Enable

17.3.2 IRER (0x00000004)

This register acts as an enable/disable for the I2SSC receiver block.

Table 205. IRER

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
RXEN	00 - 00	0x0	R/W	Received block enable control 1’b0: Disable 1’b1: Enable

17.3.3 ITER (0x00000008)

This register acts as an enable/disable for the I2SSC transmitter block.

Table 206. ITER

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
TXEN	00 - 00	0x0	R/W	Transmitter block enable control 1’b0: Disable 1’b1: Enable

17.3.4 CER (0x0000000C)

This register acts as an enable/disable for the I2SSC clock generation block.

Table 207. CER

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
CLKEN	00 - 00	0X0	R/W	Clock generation block enable control 1’b0: Disable 1’b1: Enable

17.3.5 Reserved (0x00000010)

17.3.6 RXFFR (0x00000014)

Receiver block FIFO reset register.

Table 208. Receiver block FIFI reset register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
RXFFR	00 - 00	0x0	W	Receiver FIFO Reset. Writing a 1 to this register flushes all the RX FIFOs (this is a self clearing bit). The receiver block must be disabled prior to writing this bit.

17.3.7 TXFFR (0x00000018)

Transmitter block FIFO reset register.

Table 209. Transmitted block FIFO reset register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
TXFFR	00 - 00	0x0	W	Transmitter FIFO Reset. Writing a 1 to this register flushes all the TX FIFOs (this is a self clearing bit). The transmitter block must be disabled prior to writing this bit.

17.3.8 LRBR (0x00000020)

Left receive buffer register.

Table 210. Left receive buffer register

Name	Bit	Default	R/W	Description
LRBR	31 - 00	0x0	R	The left stereo data received serially from the receiver channel input is read through this register. If the RX FIFO is full and the two-stage read operation (for instance, a read from LRBR followed by a read from RRBR) is not performed before the start of the next stereo pair, then the new data is lost and an overrun interrupt occurs. (Data already in the RX FIFO is preserved)

17.3.9 LTHR (0x00000020)

Left transmit holding register.

Table 211. LTHR

Name	Bit	Default	R/W	Description
LTHR	31 - 00	0x0	W	The left stereo data to be transmitted serially through the transmit channel output is written through this register. Writing is a two-stage process.(1) A write to this register passes the left stereo sample to the transmitter (2) This MUST be followed by writing the right stereo sample to the RTHR register. Data should only be written to the FIFO when it is not full. Any attempt to write to a full FIFO results in that data being lost and an overrun interrupt being generated.

17.3.10 RRBR (0x00000024)

Right receive buffer register.

Table 212. Right receive buffer register

Name	Bit	Default	R/W	Description
RRBR	31 - 00	0x0	R	The right stereo data received serially from the receive channel input is read through this register. If the RX FIFO is full and the two-stage read operation (for instance, read from LRBR followed by a read from RRBR) is not performed before the start of the next stereo pair, then the new data is lost and an overrun interrupt occurs. (Data already in the RX FIFO is preserved)

17.3.11 RTHR (0x00000024)

Right transmit holding register.

Table 213. Right transmit holding register

Name	Bit	Default	R/W	Description
RTHR	31 - 00	0x0	W	The right stereo data to be transmitted serially through the transmit channel output is written through this register. Writing is a two stage process. (1) A left stereo sample MUST first be written to the LTHR register. (2) A write to this register passes the right stereo sample to the transmitter.MUST first be written to the LTHR register. (2) A write to this register passes the right stereo sample to the transmitter. Data should only be written to the FIFO when it is not full. Any attempt to write to a full FIFO results in that data being lost and an overrun interrupt being generated.

17.3.12 RER (0x00000028)

Receive enable register.

Table 214. Receive enable register

Name	Bit	Default	R/W	Description
-	31 - 00	0x0	-	Reserved
RXCHEN	00 - 00	0x1	R/W	Receive channel enable. This bit enables/disables a receive channel. On enable, the channel begins receiving on the next left stereo cycle. A global disable of I2S (IER[0] = 0) or the Receiver block (IRER[0] = 0) overrides this value. 1’b1: Enable.receiving on the next left stereo cycle. A global disable of I2S (IER[0] = 0) or the Receiver block (IRER[0] = 0) overrides this value. 1’b1: Enable. 1’b0: Disable.

17.3.13 TER (0x0000002C)

Transmit enable register.

Table 215. Transmit enable register

Name	Bit	Default	R/W	Description
-	31 - 00	0x0	-	Reserved
TXCHEN	00 - 00	0x1	R/W	Transmit channel enable. This bit enables/ disables a transmit channel. On enable, the channel begins transmitting on the next left stereo cycle. A global disable of I2S (IER[0] = 0) or Transmitter block (ITER[0] = 0) overrides this value. 1’b0: Disable. 1’b1: Enable.

17.3.14 RCR (0x00000030)

Receive configuration register.

Table 216. Receive configuration register

Name	Bit	Default	R/W	Description
-	31 - 03	0x0	-	Reserved
WLEN	02 - 00	0x5	R/W	These bits are used to program the desired data resolution of the receiver and enables the LSB of the incoming left (or right) word to be placed in the LSB of the LRBR (or RRBR) register. 3'b000: Ignore word length. 3'b001: 12 bit resolution. 3'b010: 16 bit resolution. 3'b011: 20 bit resolution. 3'b100: 24 bit resolution. 3'b101: 32 bit resolution. The channel must be disabled prior to any changes in this value (RER[0] = 0)

17.3.15 TCR (0x00000034)

Transmit configuration register.

Table 217. Transmit configuration register

Name	Bit	Default	R/W	Description
-	31 - 03	0x0	-	Reserved
WLEN	02 - 00	0x5	R/W	These bits are used to program the data resolution of the transmitter and ensures the MSB of the data is transmitted first. 3'b000: Ignore word length. 3'b001: 12 bit resolution. 3'b010: 16 bit resolution. 3'b011: 20 bit resolution. 3'b100: 24 bit resolution. 3'b101: 32 bit resolution. The channel must be disabled prior to any changes in this value (TER[0] = 0).

17.3.16 ISR (0x00000038)

Interrupt status register.

Table 218. Interrupt status register

Name	Bit	Default	R/W	Description
-	31 - 06	0x0	-	Reserved
TXFO	05	0x0	R	Status of Data Overrun interrupt for the TX channel. Attempt to write to full TX FIFO. 1’b0: TX FIFO write valid. 1’b1: TX FIFO write overrun.
TXFE	04	0x1	R	Status of Transmit Empty Trigger interrupt. TX FIFO is empty. 1’b1: trigger level reached. 1’b0: trigger level not reached.
	03 - 02	0X0		Reserved
RXFO	01	0x0	R	Status of Data Overrun interrupt for the RX channel. Incoming data lost due to a full RX FIFO. 1’b0: RX FIFO write valid. 1’b1: RX FIFO write overrun.
RXDA	00	0x0	R	Status of Receive Data Available interrupt. RX FIFO data available. 1’b1: trigger level reached. 1’b0: trigger level not reached.

17.3.17 IMR (0x0000003C)

Interrupt mask register.

Table 219. Interrupt mask register

Name	Bit	Default	R/W	Description
	31 - 06	0x0		Reserved
TXFOM	05	0x1	R/W	Masks TX FIFO Overrun interrupt. 1’b1: masks interrupt. 1’b0: unmasks interrupt.
TXFEM	04	0x1	R/W	Masks TX FIFO Empty interrupt. 1’b1: masks interrupt. 1’b0: unmasks interrupt.
	03 - 02	0x0		Reserved
RXFOM	01	0x1	R/W	Masks RX FIFO Overrun interrupt. 1’b1: masks interrupt. 1’b0: unmasks interrupt.
RXDAM	00	0x1	R/W	Masks RX FIFO Data Available interrupt. 1’b1: masks interrupt. 1’b0: unmasks interrupt.

17.3.18 ROR (0x00000040)

Receive overrun register.

Table 220. Receive overrun register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
RXCHO	00 - 00	0x0	R	Read this bit to clear he RX FIFO Data Overrun interrupt. 1’b0: RX FIFO write valid. 1’b1: RX FIFO write overrun.

17.3.19 TOR (0x00000044)

Transmit overrun register.

Table 221. Transmit overrun register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
TXCHO	00 - 00	0x0	R	Read this bit to clear the TX FIFO Data Overrun interrupt. 1’b0: TX FIFO write valid. 1’b1: TX FIFO write overrun.

17.3.20 RFCR (0x00000048)

Receive FIFO configuration register.

Table 222. Receive FIFO configuration register

Name	Bit	Default	R/W	Description
-	31 - 04	0x0	-	Reserved
RXCHDT	03 - 00	0x1	R/W	These bits program the trigger level in the RX FIFO at which the Received Data Available interrupt is generated. Trigger Level = Programmed Value + 1 The channel must be disabled prior to any changes in this value (that is, RER[0] = 0).

17.3.21 TFCR (0x0000004C)

Transmit FIFO configuration register.

Table 223. Transmit FIFO configuration register

Name	Bit	Default	R/W	Description
-	31 - 04	0x0	-	Reserved
TXCHET	03 - 00	0x1	R/W	Transmit Channel Empty Trigger. These bits program the trigger level in the TX FIFO at which the Empty Threshold Reached Interrupt is generated. Trigger Level = TXCHET The channel must be disabled prior to any changes in this value (that is, TER[0] = 0)

17.3.22 RFF (0x00000050)

Receive FIFO flush register.

Table 224. Receive FIFO flush register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
RXCHFR	00	0x0	W	Receive Channel FIFO Reset. Writing a 1 to this register flushes an individual RX FIFO. (This is a self clearing bit.) RX channel or block must be disabled prior to writing to this bit.

17.3.23 TFF (0x00000054)

Transmit FIFO Flush Register.

Table 225. Transmit FIFO flush register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
TXCHFR	00	0x0	W	Transmit Channel FIFO Reset. Writing a 1 to this register flushes channel's TX FIFO. (This is a self clearing bit.) TX channel or block must be disabled prior to writing to this bit.

17.3.24 RXDMA (0x000001C0)

Receiver block DMA register. The RXDMA register allows access to enabled receive channel via a single point rather than through the LRBR and RRBR registers. The receive channels takes two reads to read stereo data pairs. The order of returned data is left data first and then right data.

Table 226. RXDMA

Name	Bit	Default	R/W	Description
RXDMA	31 - 00	0x0	R	Receiver Block DMA Register. Used to cycle repeatedly through the enabled receive channel, reading stereo data pairs.

17.3.25 RRXDMA (0x000001C4)

Reset receiver block DMA register.

Table 227. Reset receiver block DMA register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
RRXDMA[1]	00	0x0	W	Reset Receiver Block DMA Register. Writing a 1 to this self-clearing register resets the RXDMA register.

[1] Writing to this register has no effect if the component is performing a stereo pair read (such as, when left stereo data has been read but not right stereo data).

17.3.26 TXDMA (0x000001C8)

Transmitter block DMA register. The TXDMA register functions similar to the RXDMA register and allows write accesses via a single point rather than through the LTHR and RTHR registers.

Table 228. TXDMA

Name	Bit	Default	R/W	Description
TXDMA[1]	31 - 00	0x0	W	Transmitter Block DMA Register.

[1] Used to cycle repeatedly through the enabled transmit channel, writing stereo data pairs.

17.3.27 RTXDMA (0x000001CC)

Reset receiver block DMA register.

Table 229. RTXDMA

Name	Bit	Default	R/W	Description
-	31 - 01	0x00	-	Reserved
RTXDMA[1]	00	0x00	W	Reset Transmitter Block DMA Register. Writing a 1 to this self-clearing register resets the TXDMA register.

[1] This register has no effect in the middle of a stereo pair write (such as, when left stereo data has been written but not right stereo data).

18. Ethernet MAC Controller

18.1 General Description

The Ethernet MAC 10/100/1000 controller in ASC8848/49/50/51 SoC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports Gigabit Media Independent Interface (GMII) / Media Independent Interface (MII) defined in the IEEE 802.3 specifications. It also supports the industry standard, Reduced Gigabit Media Independent Interface (RGMII).

18.2 Features

The Ethernet MAC 10/100/1000 controller provides the following features.

- Supports IEEE 802.3-2002 for Ethernet MAC and GMII
- Supports RGMII specification from HP/Marvell for RGMII
- Checksum of load engine to ease the system loading (Not for Jumbo Ethernet frames)
- Independent TX and RX FIFO for the internal DMA engine
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- 64-bit Hash filter for multicast addresses
- Supports only full-duplex operation

19. Synchronous Serial Interface Controller

19.1 Features

The synchronous serial interface (SSI) controller has the following features.

- Programmable signal polarity
- Programmable serial bit clock phase and frequency
- Programmable serial bit data sequence
- Programmable threshold interrupt of RX and TX FIFOs
- Programmable interrupt enable/disable
- Support external DMA interface to request APBC to move data from/to SSIC
- Independent 32-entry RX and TX FIFOs

19.2 Memory Map Register

19.2.1 CTRLR0 (0x00000000)

This register controls the serial data transfer.

Table 230. CTRLR0

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	-	Reserved
CFS	15 - 12	0x0	R/W	Selects the length of the control word for the Microwire frame format. 0000: 1-bit control word 0001: 2-bit control word 0010: 3-bit control word 0011: 4-bit control word 0100: 5-bit control word 0101: 6-bit control word 0110: 7-bit control word 0111: 8-bit control word 1000: 9-bit control word 1001: 10-bit control word 1010: 11-bit control word 1011: 12-bit control word 1100: 13-bit control word 1101: 14-bit control word 1110: 15-bit control word 1111: 16-bit control word
SRL[1]	11	0x0	R/W	Used for testing purposes only. 0: Normal Mode Operation 1: Test Mode Operation
-	10	0x0	-	Reserved

Table 230. CTRLR0 *…continued*

Name	Bit	Default	R/W	Description
TMOD[2]	09-08	0X0	R/W	Selects the mode of transfer for serial communication. 00: Transmit & Receive 01: Transmit Only 10: Receive Only 11: EEPROM Read
SCPOL[3]	07	0x0	R/W	0: Inactive state of serial clock is low 1: Inactive state of serial clock is high
SCPH[4]	06	0x0	R/W	0: Serial clock toggles in middle of first data bit 1: Serial clock toggles at start of first data bit
FRF	05 - 04	0x0	R/W	Selects which serial protocol transfers the data: 00 — Motorola SPI 01 — Texas Instruments SSP 10 — National Semiconductors Microwire 11 — Reserve

[1] When internally active, connects the transmit shift register output to the receive shift register input:

[2] This field does not affect the transfer duplicity. Only indicates whether the receive or transmit data are valid. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. In eeprom-read mode, receive data is not valid while control data is being transmitted. When all control data is sent to the EEPROM, receive data becomes valid and transmit data becomes invalid. All data in the transmit FIFO is considered control data in this mode.

[3] Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the SSI master is not actively transferring data on the serial bus.

[4] Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH =1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock.

19.2.2 CTRLR1 (0x00000004)

This register controls the end of serial transfers when in receive-only mode. It is impossible to write to this register when the SSI controller is enabled. The SSI controller is enabled and disabled by writing to the SSIENR register.

Table 231. CTRLR1

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	-	Reserved
NDF[1]	15 - 00	0x0	R/W	Number of data frames.

[1] When TMOD = 10 or TMOD = 11, this register field sets the number of data frames to be continuously received by the SSI controller. The SSI controller continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer.

19.2.3 SSIENR (0x00000008)

This register enables and disables the SSI controller.

Table 232. SSIENR

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
SSI_EN[1]	00	0x0	R/W	Enables and disables all SSI operations.

[1] When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when the device is disabled. It is impossible to program some of the SSI control registers when enabled.

19.2.4 MWCR (0x0000000C)

This register controls the direction of the data word for the half-duplex Microwire serial protocol.

Table 233. MWCR

Name	Bit	Default	R/W	Description
-	31 - 03	0x0	-	Reserved
MHS[1]	02	0x0	R/W	Used to enable and disable the “busy/ready” handshaking interface for the Microwire protocol. 0: handshaking interface is disabled 1: handshaking interface is enabled
MDD[2]	01	0x0	R/W	Defines the direction of the data word when the Microwire serial protocol is used.
MWMOD[3]	00	0x0	R/W	Defines whether the Microwire transfer is sequential or non-sequential. 0: non-sequential transfer 1: sequential transfer

[1] When enabled, the SSI controller checks for a ready status from the target slave, after the transfer of the last data/control bit, before clearing the BUSY status in the SR register:

[2] When this bit is set to 0, the data word is received by the SSI MacroCell from the external serial device. When this bit is set to 1, the data word is transmitted from the SSI MacroCell to the external serial device.

[3] When sequential mode is used, only one control word is needed to transmit or receive a block of data words. When non-sequential mode is used, there must be a control word for each data word that is transmitted or received.

19.2.5 SER (0x00000010)

The register enables the individual slave select output lines. Up to 2 slave-select output signals are available on the SSI controller. You cannot write to this register when the SSI controller is busy.

Table 234. Save-select output signals

Name	Bit	Default	R/W	Description
-	31 - 02	0x0	-	Reserved
SER[1]	01 - 00	0x0	R/W	Each bit in this register corresponds to a slave select line (ss_x_n]) from the SSI master. 1: Selected 0: Not Selected

[1] When a bit in this register is set (1), the corresponding slave select line from the master is activated when a serial transfer begins. It should be noted that setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, you should enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set.

19.2.6 BAUDR (0x00000014)

The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the serial clock divider value. It is impossible to write to this register when the SSI controller is enabled.

Table 235. BAUDR

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	-	Reserved
SCKDV[1]	15 - 00	0x0	R/W	Serial clock divider

[1] The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation.

$$F_{sclk\_out} = \frac{FAPB\_CLK}{SCKDV} \tag{1}$$

where SCKDV is any even value between 2 and 65534. For example, If FAPB_CLK = 100 MHz and SCKDV = 4, then:

$$F_{sclk\_out} = \frac{100}{4} = 25\text{ MHz} \tag{2}$$

19.2.7 TXFTLR (0x00000018)

This register controls the threshold value for the transmit FIFO memory. It is impossible to write to this register when the SSI controller is enabled.

Table 236. TXFTLR

Name	Bit	Default	R/W	Description
-	31 - 05	0x0	-	Reserved
TFT[1]	04 - 00	0x0	R/W	0000_0000: ssi_txe_intr is asserted when 0 data entries are present in transmit FIFO 0000_0001: ssi_txe_intr is asserted when 1 or less data entry is present in transmit FIFO 0000_0010: ssi_txe_intr is asserted when 2 or less data entries are present in transmit FIFO 0000_0011: ssi_txe_intr is asserted when 3 or less data entries are present in transmit FIFO … 1111_1100: ssi_txe_intr is asserted when 252 or less data entries are present in transmit FIFO 1111_1101: ssi_txe_intr is asserted when 253 or less data entries are present in transmit FIFO 1111_1110: ssi_txe_intr is asserted when 254 or less data entries are present in transmit FIFO 1111_1111: ssi_txe_intr is asserted when 255 or less data entries are present in transmit FIFO

[1] Controls the level of entries (or below) at which the transmit FIFO controller triggers an interrupt. The FIFO depth is 32. If you attempt to set this value greater than or equal to the depth of the FIFO, this field is not written and retains its current value. When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

19.2.8 RXFTLR (0x0000001C)

This register controls the threshold value for the receive FIFO memory. It is impossible to write to this register when the SSI controller is enabled.

Table 237. RXFTLR

Name	Bit	Default	R/W	Description
-	31 - 05	0x0	-	Reserved
RFT[1]	04 - 00	0x0	R/W	0000_0000: ssi_rxf_intr is asserted when 1 or more data entry is present in receive FIFO 0000_0001: ssi_rxf_intr is asserted when 2 or more data entries are present in receive FIFO 0000_0010: ssi_rxf_intr is asserted when 3 or more data entries are present in receive FIFO 0000_0011: ssi_rxf_intr is asserted when 4 or more data entries are present in receive FIFO … 1111_1100: ssi_rxf_intr is asserted when 253 or more data entries are present in receive FIFO 1111_1101: ssi_rxf_intr is asserted when 254 or more data entries are present in receive FIFO 1111_1110: ssi_rxf_intr is asserted when 255 or more data entries are present in receive FIFO 1111_1111: ssi_rxf_intr is asserted when 256 data entries are present in receive FIFO

[1] Controls the level of entries (or above) at which the receive FIFO controller triggers an interrupt. The FIFO depth is configurable in the range 32. If you attempt to set this value greater than the depth of the FIFO, this field is not written and retains its current value. When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

19.2.9 TXFLR (0x00000020)

Transmit FIFO level register.

Table 238. Transmit FIFO level register

Name	Bit	Default	R/W	Description
-	31 - 06	0x0	-	Reserved
TXTFT	05 - 00	0x0	R	contains the number of valid data entries in the transmit FIFO

19.2.10 RXFLR (0x00000024)

Receive FIFO level register.

Table 239. RXFLR

Name	Bit	Default	R/W	Description
-	31 - 06	0x0	-	Reserved
RXTFT	05 - 00	0x0	R	Contains the number of valid data entries in the receive FIFO.

19.2.11 SR(0x00000028)

This is a read-only register used to indicate the current transfer status, FIFO status, and any transmission/reception errors that may have occurred. The status register may be read at any time. None of the bits in this register request an interrupt.

Table 240. SR

Name	Bit	Default	R/W	Description
-	31 - 07	0x0	-	Reserved
DCOL[1]	06	0x0	RSR	0: No error 1: Transmit data collision error
TXE[2]	05	0x0	R	0: No error 1: Transmission error
RFF[3]	04	0x0	R	0: Receive FIFO is not full 1: Receive FIFO is full

[1] This bit is set if the SSI master is actively transmitting when another master selects this device as a slave. This informs the processor that the last data transfer was halted before completion:

[2] Set if the transmit FIFO is empty when a transfer is started. This bit can be set only when the SSI controller is configured as a slave device. Data from the previous transmission is resent on the txe line:

[3] When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared:

19.2.12 IMR (0x0000002C)

Interrupt mask register.

Table 241. Interrupt mask register

Name	Bit	Default	R/W	Description
-	31 - 06	0x0	-	Reserved
MSTIM	05	0x1	R/W	0: ssi_mst_intr interrupt is masked 1: ssi_mst_intr interrupt is not masked
RXFIM	04	0x1	R/W	0: ssi_rxf_intr interrupt is masked 1: ssi_rxf_intr interrupt is not masked
RXOIM	03	0X1	R/W	0: ssi_rxo_intr interrupt is masked 1: ssi_rxo_intr interrupt is not masked

19.2.13 ISR (0x00000030)

Interrupt status register.

19.2.14 RISR (0x00000034)

Raw interrupt status register.

Table 242. Raw interrupt

Name	Bit	Default	R/W	Description
-	31 - 06	0x0	-	Reserved
MSTIR	05	0x0	R	0: ssi_mst_intr interrupt is not active prior to masking 1: ssi_mst_intr interrupt is active prior masking
RXFIR	04	0x0	R	0:ssi_rxf_intr interrupt is not active prior to masking 1: ssi_rxf_intr interrupt is active prior to masking

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Table 242. Raw interrupt *…continued*

Name	Bit	Default	R/W	Description
RXOIR	03	0x0	R	0: ssi_rxo_intr interrupt is not active prior to masking 1: ssi_rxo_intr interrupt is active prior masking
RXUIR	02	0x0	R	0:ssi_rxu_intr interrupt is not active prior to masking 1: ssi_rxu_intr interrupt is active prior to masking
TXOIR	01	0x0	R	0: ssi_txo_intr interrupt is not active prior to masking 1: ssi_txo_intr interrupt is active prior masking
TXEIR	00	0x0	R	0: ssi_txe_intr interrupt is not active prior to masking 1: ssi_txe_intr interrupt is active prior masking

19.2.15 TXOICR (0x00000038)

Transmit FIFO Overflow Interrupt Clear Register.

Table 243. Transmit FIFO overflow interrupt clear register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
TXOICR[1]	00	0x0	R	This register reflects the status of the interrupt.

[1] A read from this register clears the ssi_txo_intr interrupt; writing has no effect.

19.2.16 RXOICR (0x0000003C)

Receive FIFO overflow interrupt clear register.

Table 244. Receive FIFO overflow interrupt clear register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
RXOICR[1]	00	0x0	R	This register reflects the status of the interrupt.

[1] A read from this register clears the ssi_rxo_intr interrupt; writing has no effect.

19.2.17 RXUICR (0x00000040)

Receive FIFO underflow interrupt clear register.

Table 245. Receive FIFO underflow interrupt clear register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
RXOICR[1]	00	0x0	R	This register reflects the status of the interrupt.

[1] A read from this register clears the ssi_rxu_intr interrupt; writing has no effect.

19.2.18 MSTICR (0x00000044)

Multi-master interrupt clear register.

Table 246. Multi-master interrupt clear register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
MSTICR[1]	00	0x0	R	This register reflects the status of the interrupt.

[1] A read from this register clears the ssi_mst_intr interrupt; writing has no effect.

19.2.19 ICR (0x00000048)

Interrupt clear register.

Table 247. Interrupt clear register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
ICR[1]	00	0x0	R	This register is set if any of the interrupts below are active.

[1] A read clears the ssi_txo_intr, ssi_rxu_intr, ssi_rxo_intr, and the ssi_mst_intr interrupts. Writing to this register has no effect.

19.2.20 DMACR (0x0000004C)

DMA control register.

Table 248. DMA control register

Name	Bit	Default	R/W	Description
-	31 - 02	0x0	-	Reserved
TDMAE	01	0x0	R/W	This bit enables/disables the transmit FIFO DMA channel: 0: Transmit DMA disabled 1: Transmit DMA enabled
RDMAE	00	0x0	R/W	This bit enables/disables the receive FIFO DMA channel: 0: Receive DMA disabled 1: Receive DMA enabled

19.2.21 DMATDLR (0x00000050)

DMA transmit data level register.

Table 249. DMA transmit data level register

Name	Bit	Default	R/W	Description
-	31 - 05	0x0	-	Reserved
TDMAE[1]	04 - 00	0x0	R/W	0000_0000: dma_tx_req is asserted when 0 data entries are present in the receive FIFO 0000_0001: dma_tx_req is asserted when 1 or less data entry is present in the receive FIFO 0000_0010: dma_tx_req is asserted when 2 or less data entries are present in the receive FIFO 0000_0011: dma_tx_req is asserted when 3 or less data entries are present in the receive FIFO … 1111_1100: dma_tx_req is asserted when 252 or less data entries are present in the receive FIFO 1111_1101: dma_tx_req is asserted when 253 or less data entries are present in the receive FIFO 1111_1110: dma_tx_req is asserted when 254 or less data entries are present in the receive FIFO 1111_1111: dma_tx_req is asserted when 255 or less data entries are present in the receive FIFO

[1] This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

19.2.22 DMARDLR (0x00000054)

DMA receive data level register.

Table 250. DMA receive data level register

Name	Bit	Default	R/W	Description
-	31 - 05	0x0	-	Reserved
RDMAE[1]	04 - 00	0x0	R/W	0000_0000: dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO 0000_0001: dma_rx_req is asserted when 2 or more data entries are present in the receive FIFO 0000_0010: dma_rx_req is asserted when 3 or more data entries are present in the receive FIFO 0000_0011: dma_rx_req is asserted when 4 or more valid data entries are present in the receive FIFO … 1111_1100: dma_rx_req is asserted when 253 or more data entries are present in the receive FIFO 1111_1101: dma_rx_req is asserted when 254 or more data entries are present in the receive FIFO 1111_1110: dma_rx_req is asserted when 255 or more data entries are present in the receive FIFO 1111_1111: dma_rx_req is asserted when 256 data entries are present in the receive FIFO

[1] This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and RDMAE=1.

19.2.23 Reserved (0x00000058~0x0000005C)

19.2.24 DR (0x00000060 to 0x0000009C)

The SSI data register is a 16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SSI_EN = 1. FIFOs are reset when SSI_EN = 0.

Table 251. Data register

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	-	Reserved
DR	15 - 00	0x0	R/W	When writing to this register, the data must be right-justified. Read data is automatically right-justified. Read: Receive FIFO buffer Write: Transmit FIFO buffer

19.3 I/O Timing

Table 252. I/O Timing

Signal	Symbol	MIN	MAX	Unit
SSIC_I_RXD	T_{Setup}	-	-	ns
SSIC_I_RXD	T_{Hold}	-	-	ns

20. Advanced General Purpose Output

The advanced general purpose output controller provides a 128-bit pattern buffer per port to output a series of user-defined bits for any protocol such as I2C, SPI. There are up to 8 output ports which are shared with GPIO[7:0]. Please refer to Table 186.

20.1 Features

To be defined.

20.1.1 Port Control Type

There are two port control types, data control and data output enable control. It needs external pull-up or pull-down resistors when using data output enable control type.

20.1.2 Pattern Repeat

The pattern repeat function is used to send the same pattern with a specific number of times up to 409 times. This could ease the host processor loading.

20.1.3 Non-stop Pattern

To output non-stop pattern, configure the repeat time to 0xFFF and the data pattern will be output continuously until it is disabled.

20.2 Memory Map Register

20.2.1 AGPOC_VERSION (0x00000000)

Version information register.

Table 253. Version Information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x01	R	Major version number
MINOR_VERSION	23 - 16	0x00	R	Minor version number
BUILD_VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x05	R	Revision number

20.2.2 AGPOC_CTRL(0x00000004)

Control register.

Table 254. Control register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
ENABLE	07 - 00	0x0	R/W	1’b0: Disable and clear status register. 1’b1: Start to output the data pattern.

20.2.3 AGPOC_STATUS(0x00000008)

Status register.

Table 255. Status register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
OP_COMPT	07 - 00	0x0	R/W	Operation complete status. Write ENABLE register with 1’b0 to clear this register.

20.2.4 AGPOC_INTR_MASK (0x0000000C)

Interrupt mask register.

Table 256. Interrupt mask register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
INTR_MASK	07 - 00	0x0	R/W	Interrupt mask control bit. 1’b0: Enable interrupt 1’b1: Disable interrupt

20.2.5 AGPOC_DFT_DATA_OE_N (0x00000010)

Default data output enable_n port register.

Table 257. Default data output enable_n port register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
DFT_DATA_OE_N	07 - 00	0x0	R/W	Default value for data output enable_n port. 1’b0: Enable output 1’b1: Disable output

20.2.6 AGPOC_DFT_DATA (0x00000014)

Default data port value register.

Table 258. Default data port value register.

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
DFT_DATA	07 - 00	0x0	R/W	Default value for data port

20.2.7 AGPOC_CTRL_PORT_SEL (0x00000018)

Control port selection register.

Table 259. Control port selection register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
CTRL_PORT_SEL	07 - 00	0x0	R/W	Control port selection

20.2.8 AGPOC_BIT_n_PATTERN _0 (0x0000001C + n*28)

Port n pattern 0 register, n = 0~7.

Table 260. Port n pattern 0 register

Name	Bit	Default	R/W	Description
PATTERN_0	31 - 00	0x0	R/W	Data pattern [31:0]

20.2.9 AGPOC_BIT_n_PATTERN _1 (0x00000020 + n*28)

Port n pattern 1 register, n = 0~7.

Table 261. Port n pattern 1 register

Name	Bit	Default	R/W	Description
PATTERN_1	31 - 00	0x0	R/W	Data pattern [63:32]

20.2.10 AGPOC_BIT_n_PATTERN_2 (0x00000024 + n*28)

Port n pattern 2 register, n = 0~7.

Table 262. Port n pattern 2 register

Name	Bit	Default	R/W	Description
PATTERN_2	31 - 00	0x0	R/W	Data pattern [95:64]

20.2.11 AGPOC_BIT_n_ PATTERN _3 (0x00000028 + n*28)

Port n pattern 3 register, n = 0~7.

Table 263. Port n pattern 3 register

Name	Bit	Default	R/W	Description
PATTERN_3	31 - 00	0x0	R/W	Data pattern [127:96]

20.2.12 AGPOC_BIT_n_PERIOD (0x0000002C +n*28)

Port n period register, n = 0~7.

Table 264. Port n period register

Name	Bit	Default	R/W	Description
PERIOD	31 - 00	0x0	R/W	Output data period. Unit APB cycles.

20.2.13 AGPOC_BIT_n_LENGTH (0x00000030)

Port n length register, n = 0~7.

Table 265. Port n length register

Name	Bit	Default	R/W	Description
-	31 - 07	0x0	-	Reserved
LENGTH	06 - 00	0x0	R/W	Output (LENGTH+1) bits in the 128-bit pattern register

20.2.14 AGPOC_BIT_n_INTVREPEAT (0x00000034 + n*28)

Port n repeat and interval register, n = 0~7.

Table 266. Port n repeat and interval register

Name	Bit	Default	R/W	Description
REPEAT	31 - 20	0x0	R/W	Repeat times for the same data pattern. (REPEAT+1) times will be executed in one operation. When this value is set to 0xFFF, the repeat time will be infinite.
INTERVAL	19 - 00	0x0	R/W	The interval for one complete data pattern. Unit: bit time. Must be larger or equal to LENGTH register.

20.2.15 Port Control Type

There are two types of port control mechanism depicted below. It needs external pull-up or pull-down resistors when CTRL_PORT_SEL is 1’b1.

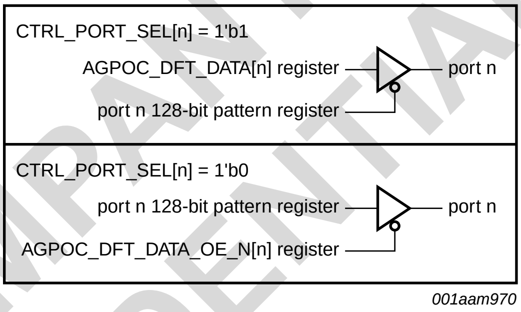

CTRL_PORT_SEL[n] = 1'b1
AGPOC_DFT_DATA[n] register
port n
port n 128-bit pattern register
CTRL_PORT_SEL[n] = 1'b0
port n 128-bit pattern register
port n
AGPOC_DFT_DATA_OE_N[n] register
001aam970

Fig 44. Illustration of the port control types

20.3 Programming

Figure 45 shows the timing representation of each parameter such as period, length, interval, repeat registers. The repeat function is used to send a pattern repeatedly in a single operation. After (LENGTH+1) bits are sent, the output will be kept in the default state, DFT_DATA or DFT_DATA_OE_N depending on the CTRL_PORT_SEL until next operation or repeat previous operation again if REPEAT is not zero.

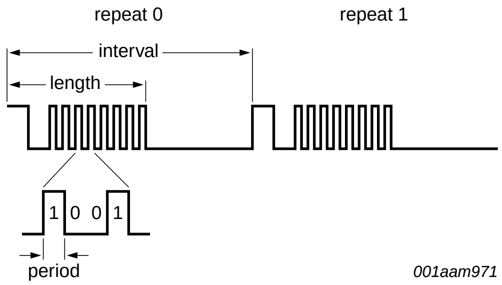
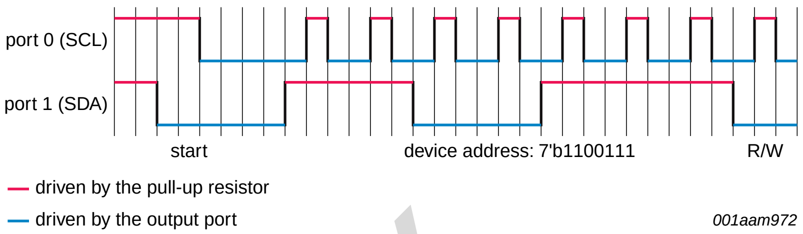


Fig 45. Timing representation of each parameter

Use I^{2}C protocol as an example. The pattern register is shifted out from LSB to MSB. This example shows only 32-bit pattern registers. It is a read operation to the device address 7’b1100111. Since there is ACK or NACK from the device, it had better to make the output tri-state at those cycles. But it is unable to know if ACK or NACK is received because APGOC does not handle the input data. After finishing the register settings, write 1’b1 to the ENABLE bit of the related ports and the operation is started. The interrupt could be used to notify the host processor when the operation is completed. To de-assert the interrupt, the host processor needs to write 1’b0 to the ENABLE bit of the related ports to clear the interrupt.


port 0 (SCL)
port 1 (SDA)
start
device address: 7'b1100111
R/W
driven by the pull-up resistor
driven by the output port
001aam972

Port 0: Used as SCL

Pattern register 0 = 0100_1001_0010_0100_1001_0010_0000_1111

CTRL_PORT_SEL = 1’B1

AGPOC_DFT_DATA = 1’b0

A pull-up resistor is placed at the output port 0.

Port 1: Used as SDA

Pattern register 0 = 0001_1111_1111_0000_0011_1111_0000_0011

CTRL_PORT_SEL = 1’b1

AGPOC_DFT_DATA = 1’b0

A pull-up resistor is placed at the output port 1.

Fig 46. Example of the I^{2}C Protocol

21. IrDA

21.1 General description

The IrDA controller is designed for receiving IrDA commands from the consumer remote controller. It receives the signal from the external IrDA demodulator and the decoded data is sent to the application through APB interface. A variety of remote control protocols are supported such as NEC, Toshiba, Matsushita, Philips RC5, Sharp and Sony SIRC protocols.

21.2 Features

The IrDA controller supports the following:

- bi-phase modulation, pulse distance modulation, and pulse width modulation.
- de-bounce function for the input IrDA signal.

21.2.1 Modulation type

Supports bi-phase modulation, pulse distance modulation and pulse width modulation

21.2.2 De-bounce

Supports be-bounce function for the input IrDA signal.

21.3 Memory Map Register

21.3.1 IRDAC VERSION (0x00000000)

Version information register.

Table 267. Version Information register

Name	Bit	Default	R/W	Description
MAJOR REVISION	31 - 24	0x04	R	Major version number
MINOR_REVISION	23 - 16	0x01	R	Minor version number
BUILD VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x04	R	Revision number

21.3.2 IRDAC_CTRL (0x00000004)

Control register.

Table 268. Control register

Name	Bit	Default	R/W	Description
-	31 - 22	0x0	-	Reserved
DATA_NUM	21 - 16	0x0	R/W	Data number, number of bits in one data real data number = DATA_NUM + 1
-	15 - 12	0x0	-	Reserved

21.3.3 IRDAC_STAT (0x00000008)

Status register.

Table 269. Status register

Name	Bit	Default	R/W	Description
-	31 - 12	0x0	-	Reserved
ERR_BIT	11 - 07	0x0	R	The bit number of the a command sequence where a error occurs (or does not correspond to a specific protocol)
ERR_STATE	06 - 04	0x0	R	The state where a error occurs (or does not correspond to a specific protocol) 3'b000: No error 3'b001: Reserved 3'b010: Error occurs in BURST_LEN 3'b011: Error occurs in SILEN_LEN 3'b100: Error occurs in REPEAT_LEN 3'b101: Error occurs in MODU_LEN 3'b110: Error occurs in LOGIC_LEN 3'b111: Reserved
REPEAT	03	0x0	R	Repeat flag
FIFO_FULL	02	0x0	R	IFO full flag 1'b0: FIFO is not full 1'b1: FIFO is full
FIFO_NOT_EMPTY	01	0x0	R	FIFO not empty flag 1'b0: FIFO is empty 1'b1: FIFO is not empty
OP_CMPT	00	0x0	R	Set when IRDAC operation is complete. 1'b0: IRDAC is busy or idle. 1'b1: IRDAC operation is complete.

21.3.4 IRDAC_RBR_LO (0x0000000C)

Lower bits of the received data.

Table 270. Lower bits of received data

Name	Bit	Default	R/W	Description
RBR_LO[1]	31 - 00	0x0	R	Read port of FIFO.

[1] Users can read this register to get low 32-bit data latched in the FIFO.

21.3.5 IRDAC_RBR_HI (0x00000010)

Higher bits of the received data.

Table 271. Higher bits of the received data

Name	Bit	Default	R/W	Description
RBR_HI[1]	31 - 00	0x0	R	Read port of FIFO.

[1] Users can read this register to get high 32-bit data latched in the FIFO.

21.3.6 IRDAC_TIMING (0x00000014)

Timing register.

Table 272. Timing register

Name	Bit	Default	R/W	Description
-	31 - 24	0x00	-	Reserved
MODU_LEN	23 - 16	0x00	R/W	Modulation length. Time of modulation = (MODU_LEN ´ IR sampling time)
ZERO_LEN	15 - 08	0x00	R/W	Logic zero length. Time of logic zero = (ZERO_LEN ´ IR sampling time)
ONE_LEN	07 - 00	0x00	R/W	Logic one length. Time of logic one = (ONE_LEN ´ IR sampling time)

21.3.7 IRDAC_TIMING_EXT(0x00000018)

Extended timing register.

Table 273. Extended timing register

Name	Bit	Default	R/W	Description
-	31 - 28	0x0	-	Reserved
DEBOUNCE	27 - 24	0x0	R/W	De-bounce length. Time of repeat = (DEBOUNCE´IR sampling time)
REPEAT_LEN	23 - 16	0x00	R/W	Repeat length. Time of repeat = (REPEAT_LEN´IR sampling time)
SILEN_LEN	15 - 08	0x00	R/W	Silence length. Time of silence = (SILEN_LEN´IR sampling time´2)
BURST_LEN	07 - 00	0x00	R/W	Burst length. Time of start = (BURST_LEN ´ IR sampling time ´ 4)

21.3.8 IRDAC_INTERVAL_FREQ_DIV (0x0000001C)

Frequency divisor and the repeat code interval.

Table 274. Frequency divisor and repeat code interval

Name	Bit	Default	R/W	Description
FREQ_DIV	31 - 16	0x0000	R/W	the frequency divisor that generates the IR sampling frequency.
REPEAT_INTERVAL	15 - 00	0x0000	R/W	defined as the interval from the last bit of the previous command and the first bit of the next repeated command interval of two consecutive data package.

[1] Frequency = frequency of APB_CLK / (FREQ_DIV+1).

[2] Interval = (REPEAT_INTERVAL ´ IR sampling time)

21.4 Programming

The sampling clock of IrDA signal is derived from the input APB clock. The frequency of sampling clock, which is denoted as fs, is equal to the frequency of fAPB_CLK/(FREQ_DIV+1). The sampling time Ts is defined by 1/ fs.

Figure 47 illustrates the timing definition of data bits in three kinds of modulation. In all types of modulation, the field MODU_LEN, which means the length of modulation time, must be filled. MODU_LEN is defined by TD/Ts, where TD is time of modulation shown in Figure 47. Note that the definition of modulation time is different in three modulations. TD is the interval of “mark” part (low level) in pulse distance modulation, whereas TD is the interval of “space” part (high level) in pulse width modulation. In bi-phase modulation, TD is half of the bit time. Since the logical one and zero are defined by the phase of the signal in the bi-phase modulation, it does not need to define the logical one/zero length.

On the other hand, the time of logical one TO and logical zero TZ should be defined in the other two modulations. Similar to definition of MODU_LEN, ONE_LEN is defined by TO/Ts, and ZERO_LEN is defined by TZ/Ts. Also note that the definitions of the interval of logical one/zero are different in pulse distance modulation and pulse width modulation. See Figure 47 for details.

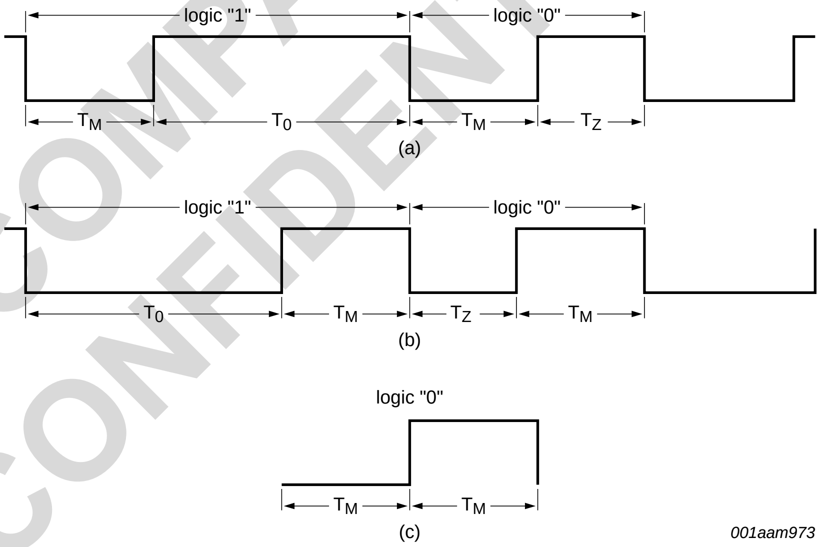


Fig 47. Timing Definition of Data Bits in three kinds of modulation (a) Pulse Distance Modulation (b) Pulse Width Modulation (c) Bi-Phase Modulation.

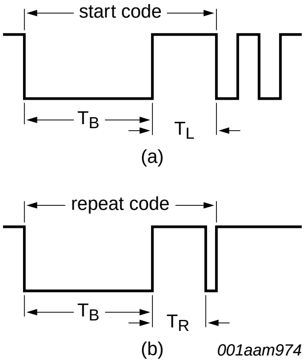


Fig 48. Timing Definition of Start and Repeat Code

In NEC and Sony SIRC protocol, there is the start code, and BURST_MODE_EN should be enabled. Once BURST_MODE_EN is enabled, the IrDA controller will be idle until the start code with correct timing comes. For the start code, it has two parts: one is burst part and one is silent part. The burst part is low level at the receiver side and BURST_LEN is defined by TB/4Ts, where TB is the burst time. (9ms for NEC protocol and 2.4ms for Sony SIRC protocol) The silent part, which follows the burst part, is high level and SILEN_LEN is defined by TL/2Ts, where TL is the silent time. (4.5ms for NEC protocol and 600ms for Sony SIRC protocol) Figure 48 shows the timing definition of start code.

In NEC protocol, the repeat code is transmitted for as long as the key remains down. Let the time of silent part of the repeat code be TR, then REPEAT_LEN is defined by TR/2Ts. the timing definition of repeat code is illustrated in Figure 49. In addition, REPEAT_INTERVAL can be set for the interval of two consecutive commands when the key on the remote control is held down. As long as the interval of two consecutive commands meets the repeat interval, or repeat code occurs, the repeat flag in register IRDAC_STAT will be 1.

22. Mobile Storage Host Controller

22.1 General Description

The mobile storage host controller (MSHC) is a secure digital multimedia card controller, which simultaneously supports Secure Digital memory (SD Mem), Secure Digital I/O (SDIO), and Multimedia Cards (MMC).

22.2 Features

- Supports Secure Digital memory version 2.0 protocol commands
- Supports Secure Digital I/O version 2.0 protocol commands
- Supports Multimedia Card version 4.3 protocol commands
- Supports half-duplex internal DMA block with descriptor-based linked list
- Supports combined 16-entry TX/RX FIFO

22.3 Memory Map Register

22.3.1 CTRL (0x00000000)

Control Register.

Table 275. Control register

Name	Bit	Default	R/W	Description
-	31 - 26	-	-	Reserved
USE_INTERNAL_DMAC	25	0x0	R/W	Use internal DMA engine. 1’b0: The host performs data transfers through the slave interface. 1’b1: Internal DMAC used for data transfer.
ENABLE_OD_PULLUP	24	0x1	R/W	External CMD open-drain pull-up 1’b0: Disable. 1’b1: Enable.
-	23 - 12	-	-	Reserved
CEATA_DEVICE_INTERRUPT_STATUS[1]	11	0x0	R/W	1'b0: Interrupts not enabled in CE-ATA device (nIEN = 1 in ATA control register). 1'b1: Interrupts are enabled in CE-ATA device (nIEN = 0 in ATA control register).
SEND_AUTO_STOP_CCSD[2]	10	0x0	R/W	1'b0: Clear bit if MSHC does not reset the bit. 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device.
SEND_CCSD[3]	09	0x0	R/W	1'b0: Clear bit if MSHC does not reset the bit. 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device.
ABORT_READ_DATA[4]	08	0x0	R/W	1'b0: No change. 1'b1: Abort read
SEND_IRQ_RESPONSE[5]	07	0x0	R/W	1'b0: No change. 1'b1: Send auto IRQ response.

Table 275. Control register *…continued*

Name	Bit	Default	R/W	Description
READ_WAIT	06	0x0	R/W	1'b0: Clear read wait. 1'b1: Assert read wait. For sending read-wait to SDIO cards.
DMA_ENABLE[6]	05	0x0	R/W	1'b0: Disable DMA transfer mode. 1'b1: Enable DMA transfer mode.
INT_ENABLE[7]	04	0x0	R/W	Global interrupt enable/disable bit: 1'b0: Disable interrupts. 1'b1: Enable interrupts.
	03	0x0	R/W	Reserved
DMA_RESET[8]	02	0x0	R/W	1'b0: No change. 1'b1: Reset internal DMA interface control logic
FIFO_RESET[9]	01	0x0	R/W	1'b0: No change. 1'b1: Reset to data FIFO to reset FIFO pointers
CONTROLLER_RESET[10]	00	0x0	R/W	1'b0: No change. 1'b1: Reset MSHC.

[1] Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled (nIEN = 1). If the host enables CE-ATA device interrupt, then software should set this bit

[2] NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together; send_auto_stop_ccsd should not be set independent of send_ccsd. When set, MSHC automatically sends internally generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, MSHC automatically clears send_auto_stop_ccsd bit.

[3] When set, MSHC sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, MSHC automatically clears send_ccsd bit. It also sets Command Done (CD) bit in RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. Note that once the send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.

[4] After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.

[5] Bit automatically clears once response is sent. To wait for MMC card interrupts, host issues CMD40, and MSHC waits for interrupt response from MMC card(s). In meantime, if host wants MSHC to exit waiting for interrupt state, it can set this bit, at which time MSHC command state-machine sends CMD40 response on bus and returns to idle state.

[6] Valid only if MSHC configured for External DMA interface. Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside MSHC to prioritize simultaneous host/DMA access.

[7] The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.

[8] To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.

[9] To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.

[10] To reset controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles.
This resets: * Card interface state machines
* ABORT_READ_DATA, SEND_IRQ_RESPONSE, and READ_WAIT bits of CTRL register
* START_CMD bit of CMD register
Does not affect any registers or DMA interface, or FIFO or host interrupts

22.3.2 Reserved (0x00000004)

This register is reserved.

22.3.3 CLKDIV (0x00000008)

Clock Divider Register.

Table 276. Clock divider register

Name	Bit	Default	R/W	Description
-	31 - 08	-	-	Reserved
CLK_DIVIDER[1]	07 - 00	0x0	R/W	Clock divider value.

[1] Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, value of “ff” means divide by 2*255 = 510, and so on.

22.3.4 Reserved (0x0000000C)

This register is reset to 0x0 and should not be altered.

22.3.5 CLKENA (0x00000010)

Clock Enable Register

Table 277. Clock Enable Register

Name	Bit	Default	R/W	Description
-	31 - 17	-	-	Reserved
CCLK_LOW_POWER	16	0x0	R/W	Low-power control for SD card clock and MMC card clock. 1'b0: Non-low-power mode 1'b1: Low-power mode[1]
	15 - 01	0x0		Reserved
CCLK_ENABLE[2]	00	0x0	R/W	Clock-enable control. 1'b0: Clock disabled 1'b1: Clock enabled

[1] Stops clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).

[2] Up to 16 SD card clocks and one MMC card clock supported.

22.3.6 TMOUT (0x00000014)

Timeout Register.

Table 278. Timeout register

Name	Bit	Default	R/W	Description
DATA_TIMEOUT[1]	31 - 08	0xFFFFFF	R/W	Value for card Data Read Timeout.
RESPONSE_TIMEOUT[2]	07 - 00	0x40	R/W	Response timeout value.

[1] The same value also used for Data Starvation by Host timeout. Value is in number of card output clocks.

[2] Value is in number of card output clocks.

22.3.7 CTYPE (0x00000018)

Card Type Register.

Table 279. Card type register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
CARD_WIDTH	00	0x0	R/W	Indicates if card is 1-bit or 4-bit: 1'b0: 1-bit mode. 1'b1: 4-bit mode

22.3.8 BLKSIZ (0x0000001C)

Block Size Register

Table 280. Block size register

Name	Bit	Default	R/W	Description
-	31 - 16	-	-	Reserved
BLOCK_SIZE	15 - 00	0x200	R/W	Block size

22.3.9 BYTCNT (0x00000020)

Byte Count Register.

Table 281. Byte count register

Name	Bit	Default	R/W	Description
BYTE_COUNT[1]	31 - 00	0x200	R/W	Number of bytes to be transferred.

[1] Integer multiple of Block Size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.

22.3.10 INTMASK (0x00000024)

Interrupt Mask Register.

Table 282. Interrupt mask register

Name	Bit	Default	R/W	Description
-	31 - 17	-	-	Reserved
SDIO_INT_MASK	16	0x0	R/W	Mask SDIO interrupts When masked, SDIO interrupt detection for that card is disabled. 1'b0: mask the interrupt. 1'b1: enable the interrupt.
INT_MASK	15 - 00	0x0	R/W	Bits used to mask unwanted interrupts. 1'b0: mask the interrupt. 1'b1: enable the interrupt. bit 15 – End-bit error (read)/Write no CRC (EBE) bit 14 – Auto command done (ACD) bit 13 – Start-bit error (SBE) bit 12 – Hardware locked write error (HLE) bit 11 – FIFO underrun/overrun error (FRUN) bit 10 – Data starvation-by-host timeout (HTO) bit 9 – Data read timeout (DRTO) bit 8 – Response timeout (RTO) bit 7 – Data CRC error (DCRC) bit 6 – Response CRC error (RCRC) bit 5 – Receive FIFO data request (RXDR) bit 4 – Transmit FIFO data request (TXDR) bit 3 – Data transfer over (DTO) bit 2 – Command done (CD) bit 1 – Response error (RE) bit 0 – Card detect (CD)

22.3.11 CMDARG (0x00000028)

Command Argument Register.

Table 283. Command argument register

Name	Bit	Default	R/W	Description
CMD_ARG	31 - 00	0x0	R/W	Value indicates command argument to be passed to card

22.3.12 CMD (0x0000002C)

Command Register.

Table 284. Command register

Name	Bit	Default	R/W	Description
START_CMD[1]	31	0x0	R/W	Start command.
	30 - 28	-	-	Reserved
BOOT_MODE	27	0x0	R/W	Boot Mode 1'b0: Mandatory Boot operation 1'b1: Alternate Boot operation
DISABLE_BOOT[2]	26	0x0	R/W	Disable Boot.
EXPECT_BOOT_ACK[3]	25	0x0	R/W	Expect Boot Acknowledge.
ENABLE_BOOT[4]	24	0x0	R/W	Enable Boot
CCS_EXPECTED[5]	23	0x0	R/W	1'b0: Interrupts are not enabled in CE-ATA device (nIEN = 1 in ATA control register), or command does not expect CCS from device 1'b1: Interrupts are enabled in CE-ATA device (nIEN = 0), and RW_BLK command expects command completion signal from CE-ATA device
READ_CEATA_DEVICE[6]	22	0x0	R/W	1'b0: Host is not performing read access (RW_REG or RW_BLK) towards CE-ATA device 1'b1: Host is performing read access (RW_REG or RW_BLK) towards CE-ATA device
UPDATE_CLOCK_REGISTERS_ONLY[7]	21	0x0	R/W	1'b0: Normal command sequence. 1'b1: Do not send commands, just update clock register value into card clock domain.
CARD_NUMBER	20 - 16	0x0	R/W	Must be 0x0
SEND_INITIALIZATION[8]	15	0x0	R/W	1'b0: Do not send initialization sequence (80 clocks of 1) before sending this command. 1'b1: Send initialization sequence before sending this command.
STOP_ABORT_CMD	14	0x0	R/W	1'b0: Neither stop nor abort command.[9] 1'b1: Stop or abort command intended to stop current data transfer in progress.[10]
WAIT_PRVDATA_COMPLETE[11]	13	0x0	R/W	The WAIT_PRVDATA_COMPLETE = 0 option
SEND_AUTO_STOP[12]	12	0x0	R/W	1'b0: No stop command sent at end of data transfer. 1'b1: Send stop command at end of data transfer.
TRANSFER_MODE	11	0x0	R/W	1'b0: Block data transfer command 1'b1: Stream data transfer command Don't care if no data expected.
READ/WRITE	10	0x0	R/W	1'b0: Read from card 1'b1: Write to card Don't care if no data expected from card.
DATA_EXPECTED	09	0x0	R/W	1'b0: No data transfer expected (read/write). 1'b1: Data transfer expected (read/write).
CHECK_RESPONSE_CRC[13]	08	0x0	R/W	1'b0: Do not check response CRC. 1'b1: Check response CRC.

Table 284. Command register *…continued*

Name	Bit	Default	R/W	Description
RESPONSE_LENGTH	07	0x0	R/W	1'b0: Short response expected from card. 1'b1: Long response expected from card.
RESPONSE_EXPECT	06	0x0	R/W	1'b0: No response expected from card. 1'b1: Response expected from card.
CMD_INDEX	05 - 00	0x0	R/W	Command index

[1] Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD_MMC_CEATA cards, Command Done bit is set in raw interrupt register.

[2] When software sets this bit along with START_CMD, CIU terminates the boot operation. Do NOT set DISABLE_BOOT and ENABLE_BOOT together.

[3] When Software sets this bit along with ENABLE_CMD, CIU expects a boot acknowledge start pattern of "0-1-0" from the selected card.

[4] This bit should be set only for mandatory boot mode. When Software sets this bit along with START_CMD, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do NOT set DISABLE_BOOT and ENABLE_BOOT together.

[5] If the command expects Command Completion Signal (CCS) from the CE-ATA device, the software should set this control bit. MSHC sets Data Transfer Over (DTO) bit in RINTSTS register and generates interrupt to host if Data Transfer Over interrupt is not masked.

[6] Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. MSHC should not indicate read data timeout while waiting for data from CE-ATA device

[7] Changes card clocks; provided in order to change clock frequency or stop clock without having to send command to cards. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.

[8] After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).

[9] To stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0.

[10] When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with CMD[26] = DISABLE_BOOT.

[11] This is typically used to query status of card during data transfer or to stop current data transfer; CARD_NUMBER should be same as in previous command.

[12] When set, MSHC sends stop command to SD_MMC_CEATA cards at end of data transfer. Refer to Table 212 Auto-Stop Generation to determine:

* when SEND_AUTO_STOP bit should be set, since some data transfers do not need explicit stop commands

* open-ended transfers that software should explicitly send to stop command

Additionally, when “resume” is sent to resume – suspended memory access of SD-Combo card – bit should be set correctly if suspended data transfer needs SEND_AUTO_STOP. Don't care if no data expected from card

[13] Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.

22.3.13 RESP0 (0x00000030)

Response Register 0.

Table 285. Response register 0

Name	Bit	Default	R/W	Description
RESPONSE_0	31 - 00	0x0	R	Bit[31:0] of response

22.3.14 RESP0 (0x00000030)

Response Register 0.

Table 286. RESPONSE

Name	Bit	Default	R/W	Description
RESPONSE_0	31 - 00	0x0	R	Bit[31:0] of response

22.3.15 RESP1 (0x00000034)

Response Register 1.

Table 287. Response register 1

Name	Bit	Default	R/W	Description
RESPONSE_1[1]	31 - 00	0x0	R	Register represents bit[63:32] of long response.

[1] When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in Response 0 register.

22.3.16 RESP2 (0x00000038)

Response Register 2.

Table 288. Response register 2

Name	Bit	Default	R/W	Description
RESPONSE_2	31 - 00	0x0	R	Bit[95: 65] of long response

22.3.17 RESP3 (0x0000003C)

Response Register 3.

Table 289. Response register 3

Name	Bit	Default	R/W	Description
RESPONSE_3	31 - 00	0x0	R	Bit[127:96] of long response

22.3.18 MINTSTS (0x00000040)

Masked Interrupt Status Register.

Table 290. Masked interrupt status register

Name	Bit	Default	R/W	Description
-	31 - 17	-	-	Reserved
SDIO_INTERRUPT	16	0x0	R	Interrupt from SDIO card. SDIO interrupt for card enabled only if corresponding SDIO_INT_MASK bit is set in Interrupt mask register (mask bit 1 enables interrupt; 0 masks interrupt). 1'b0: No SDIO interrupt from card 1'b1: SDIO interrupt from card In MMC-Ver3.3-only mode, bits always 0.
INT_STATUS	15 - 00	0x0	R	Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15 – End-bit error (read)/write no CRC (EBE) bit 14 – Auto command done (ACD) bit 13 – Start-bit error (SBE) bit 12 – Hardware locked write error (HLE) bit 11 – FIFO underrun/overrun error (FRUN) bit 10 – Data starvation by host timeout (HTO) bit 9 – Data read timeout (DRTO) bit 8 – Response timeout (RTO) bit 7 – Data CRC error (DCRC) bit 6 – Response CRC error (RCRC) bit 5 – Receive FIFO data request (RXDR) bit 4 – Transmit FIFO data request (TXDR) bit 3 – Data transfer over (DTO) bit 2 – Command done (CD) bit 1 – Response error (RE) bit 0 – Card detect (CD)

22.3.19 RINTSTS (0x00000044)

Interrupt status register.

Table 291. Interrupt status register

Name	Bit	Default	R/W	Description
-	31 - 17	-	-	Reserved
SDIO_INTERRUPT	16	0x0	R/W	Interrupt from SDIO card. Writes to these bits clear them. Value of 1 clears bit and 0 leaves bit intact. 1'b0: No SDIO interrupt from card 1'b1: SDIO interrupt from card In MMC-Ver3.3-only mode, bits always 0. Bits are logged regardless of interrupt-mask status.
INT_STATUS	15 - 00	0x0	R/W	Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status. bit 15 – End-bit error (read)/write no CRC (EBE) bit 14 – Auto command done (ACD) bit 13 – Start-bit error (SBE) bit 12 – Hardware locked write error (HLE) bit 11 – FIFO underrun/overrun error (FRUN) bit 10 – Data starvation-by-host timeout (HTO) bit 9 – Data read timeout (DRTO)/Boot Data Start (BDS) bit 8 – Response timeout (RTO)/Boot Ack Received (BAR) bit 7 – Data CRC error (DCRC) bit 6 – Response CRC error (RCRC) bit 5 – Receive FIFO data request (RXDR) bit 4 – Transmit FIFO data request (TXDR) bit 3 – Data transfer over (DTO) bit 2 – Command done (CD) bit 1 – Response error (RE) bit 0 – Card detect (CD)

22.3.20 STATUS (0x00000048)

Status Register.

Table 292. Status register

Name	Bit	Default	R/W	Description
-	31 - 30	-	-	Reserved
FIFO_COUNT	29 - 17	0x0	R	FIFO count – Number of filled locations in FIFO.
RESPONSE_INDEX	16 - 11	0X0	R	Index of previous response, including any auto-stop sent by core.
DATA_STATE_MC_BUSY	10	0x0	R	Data transmit or receive state-machine is busy.
DATA_BUSY	09	-	R	Inverted version of raw selected card_data[0]. 1'b0: card data not busy. 1'b1: card data busy
DATA_3_STATUS	08	-	R	Raw selected card_data[3]; checks whether card is present. 1'b0: card not present. 1'b1: card present.
COMMAND_FSM_STATES[1]	07 - 04	0x0	R	Command FSM states: 4'b0000 – Idle/Wait for CCS/Send CCSD/Boot Mode 4'b0001 – Send init sequence 4'b0010 – Tx cmd start bit 4'b0011 – Tx cmd tx bit 4'b0100 – Tx cmd index + arg 4'b0101 – Tx cmd crc7 4'b0110 – Tx cmd end bit 4'b0111 – Rx resp start bit 4'b1000 – Rx resp IRQ response 4'b1001 – Rx resp tx bit 4'b1010 – Rx resp cmd idx 4'b1011 – Rx resp data 4'b1100 – Rx resp crc7 4'b1101 – Rx resp end bit 4'b1110 – Cmd path wait NCC 4'b1111 – Wait; CMD-to-response turnaround
FIFO_FULL	03	0x0	R	FIFO is full status
FIFO_EMPTY	02	0x0	R	FIFO is empty status
FIFO_TX_WATERMARK	01	0x1	R	FIFO reached Transmit watermark level; not qualified with data transfer
FIFO_RX-WATERMARK	00	0x1	R	FIFO reached Receive watermark level; not qualified with data transfer.

[1] Note there are 19 command FSM states. The STATUS Register (7:4) has 4 bits to represent the command FSM states, so status 0 represents four states.

22.3.21 FIFOTH (0x0000004C)

FIFO Threshold Watermark Register.

Table 293. FIFO threshold watermark register

Name	Bit	Default	R/W	Description
-	31 - 31	-	-	Reserved
DW_DMA_MULTIPLE_ TRANSACTION_SIZE	30 - 28	0x0	R/W	Burst size of multiple transaction. 8 transfers recommended. 3'b000: 1 transfer 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers
RX_WMARK[1]	21 - 16	0xF	R/W	FIFO threshold watermark level when receiving data to card.
-	15 - 12	-	-	Reserved
TX_WMARK[2]	11 - 00	0x0	R/W	FIFO threshold watermark level when transmitting data to card.

[1] In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set.

RX_WMARK<=14, 7 is recommended. Note that in DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout

[2] In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. TX_WMARK >= 1, 8 is recommended.

22.3.22 CDETECT (0x00000050)

Card Detect Register.

Table 294. Card detect register

Name	Bit	Default	R/W	Description
-	31-01	-	-	Reserved
CARD_DETECT_N	00-00	-	R	Value on card_detect_n input ports; read-only bits. 1’b0 represents presence of card

22.3.23 WRTPRT (0x00000054)

Receive FIFO configuration register.

Table 295. Receive FIFO configuration register

Name	Bit	Default	R/W	Description
-	31 - 01	-	-	Reserved
WRITE_PROJECT	00	-	R	Value on card_write_prt input ports; 1'b1 represents write protection.

22.3.24 Reserved (0x00000058)

This register is reserved.

22.3.25 TCBCNT (0x0000005C)

Transferred CIU Card Byte Count Register.

Table 296. Transferred CIU card byte count register

Name	Bit	Default	R/W	Description
TRANS_CARD_BYTE_COUNT	31 - 00	0x0	R	Number of bytes transferred by CIU unit to card.

22.3.26 TBBCNT (0x00000060)

Transferred Host to BIU-FIFO Byte Count Register.

Table 297. Transferred Host

Name	Bit	Default	R/W	Description
TRANS_FIFO_BYTE_COUNT	31 - 00	0x0	R	Number of bytes transferred between Host/DMA memory and BIU FIFO.

22.3.27 DEBNCE (0x00000064)

Transferred Host to BIU-FIFO Byte Count Register.

Table 298. Transferred Host to BIU-FIFO byte count register

Name	Bit	Default	R/W	Description
-	31 - 24	-	-	Reserved
DEBOUNCE_COUNT	23 - 00	0xFFFFFF	R/W	Number of host clocks (AHB clock) used by debounce filter logic; typical debounce time is 5-25 ms.

22.3.28 USRID (0x00000068)

User ID Register.

Table 299. User ID register

Name	Bit	Default	R/W	Description
USRID	31 - 00	0x7967797	R	User identification register, value set by user. Can also be used as scratch pad register by user

22.3.29 VERID (0x0000006C)

Version ID Register.

Table 300. Version ID register

Name	Bit	Default	R/W	Description
VERID	31 - 00	0x5342210A	R	Version identification register

22.3.30 Reserved (0x00000070~0x0000007C)

This register is reserved.

22.3.31 BMOD (0x00000080)

Bus Mode Register.

Table 301. Bus mode register

Name	Bit	Default	R/W	Description
-	31 - 11	-	-	Reserved
PBL[1]	10 - 08	0x0	R	Programmable Burst Length. The encode value is as follows: 3'b000: 1 transfer 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers
DE	07	0x0	R/W	IDMAC Enable. When set, the IDMAC is enabled.
DSL[2]	06 - 02	0x0	R/W	Descriptor Skip Length.
FB[3]	01	0x0	R/W	Fixed Burst.
SWR[4]	00	0x0	R/W	Software Reset.

[1] These bits indicate the maximum number of beats to be performed in one internal DMA controller (IDMAC) transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register.

[2] Specifies the number of 32-bit WORD to skip between two unchained descriptors. This is applicable only for dual buffer structure.

[3] Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.

[4] When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

22.3.32 PLDMND (0x00000084)

Poll Demand Register.

Table 302. Poll demand register

Name	Bit	Default	R/W	Description
PD[1]	31 - 00	-	W	Poll Demand.

[1] If the OWN bit of a descriptor is not set, the FSM goes to the Suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation. This is a write only register.

22.3.33 DBADDR (0x00000088)

Descriptor List Base Address Register.

Table 303. Descriptor list base address register

Name	Bit	Default	R/W	Description
SDL[1]	31 - 00	0x0	R/W	Start of Descriptor List.

[1] Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

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22.3.34 IDSTS (0x0000008C)

Internal DMAC Status Register.

Table 304. Internal DMAC status register

Name	Bit	Default	R/W	Description
-	31 - 17	-	-	Reserved
FSM	16 - 13	0x0	R	DMAC FSM present state. 4'b0000: DMA_IDLE 4'b0001: DMA_SUSPEND 4'b0010: DESC_RD 4'b0011: DESC_CHK 4'b0100: DMA_RD_REQ_WAIT 4'b0101: DMA_WR_REQ_WAIT 4'b0110: DMA_RD 4'b0111: DMA_WR 4'b1000: DESC_CLOSE
EB[1]	12 - 10	0x0	R	Error Bits. 3'b001 – Host Abort received during transmission 3'b010 – Host Abort received during reception Others: Reserved
AIS[2]	09	0x0	R/W	Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2] – Fatal Bus Interrupt IDSTS[4] – DU bit Interrupt IDSTS[5] – Card Error Summary Interrupt Only unmasked bits affect this bit.
NIS[3]	08	0x0	R/W	Normal Interrupt Summary. Logical OR of the following: IDSTS[0] – Transmit Interrupt IDSTS[1] – Receive Interrupt Only unmasked bits affect this bit.
-	07 - 06	-	-	Reserved
CES[4]	05	0x0	R/W	Card Error Summary. Indicates the logical OR of the following bits: EBE – End Bit Error RTO – Response Timeout/Boot Ack Timeout RCRC – Response CRC SBE – Start Bit Error DRTO – Data Read Timeout/BDS timeout DCRC – Data CRC for Receive RE – Response Error
DU[5]	04	0x0	R/W	Descriptor Unavailable Interrupt.
-	03	-	-	Reserved
FBE[6]	02	0x0	R/W	Fatal Bus Error Interrupt.
R1[7]	01	0x0	R/W	Receive Interrupt.
T1[8]	00	0x0	R/W	Transmit Interrupt.

[1] Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt.

[2] This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit

[3] This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.

[4] Indicates the status of the transaction to/from the card; also present in RINTSTS. Writing a 1 clears this bit.

[5] This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.

[6] Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.

[7] Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.

[8] Indicates that data transmission is finished for a descriptor. Writing a ‘1’ clears this bit

22.3.35 IDINTEN (0x00000090)

Internal DMAC Interrupt Enable Register.

Table 305. Internal DMAC interrupt enable register

Name	Bit	Default	R/W	Description
-	31 - 10	-	-	Reserved
AI[1]	09	0x0	R/W	Abnormal Interrupt Summary Enable. This bit enables the following bits: IDINTEN[2] – Fatal Bus Error Interrupt. IDINTEN[4] – DU Interrupt. IDINTEN[5] – Card Error Summary Interrupt.
NI[2]	08	0x0	R/W	Normal Interrupt Summary This bit enables the following bits: IDINTEN[0] – Transmit Interrupt. IDINTEN[1] – Receive Interrupt.
-	07 - 06	-	-	Reserved
CES[3]	05	0x0	R/W	Card Error summary Interrupt Enable.
DU[4]	04	0x0	R/W	Descriptor Unavailable Interrupt.
	03			Reserved
FBE[5]	02	0x0	R/W	Fatal Bus Error Enable.
RI[6]	01	0x0	R/W	Receive Interrupt Enable.
TI[7]	00	0x0	R/W	Transmit Interrupt Enable.

[1] When set, an abnormal interrupt is enabled.

[2] Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled.

[3] When set, it enables the card interrupt summary.

[4] When set along with abnormal interrupt summary enable, the DU interrupt is enabled.

[5] When set with abnormal summary enable, the fatal bus error interrupt is enabled. When reset, fatal bus error enable interrupt is disabled.

[6] When set with normal interrupt summary enable, receive interrupt is enabled. When reset, receive interrupt is disabled.

[7] When set with normal interrupt summary enable, transmit interrupt is enabled. When reset, transmit interrupt is disabled.

22.3.36 DSCADDR (0x00000094)

Current Host Descriptor Address Register.

Table 306. Current host descriptor address register

Name	Bit	Default	R/W	Description
HDA[1]	31 - 00	0x0	R	Host Descriptor Address Pointer.

[1] Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC.

22.3.37 BUFADDR (0x00000098)

Current Buffer Descriptor Address Register.

Table 307. Current buffer descriptor address register

Name	Bit	Default	R/W	Description
HBA[1]	31 - 00	0x0	R	Host Buffer Address Pointer.

[1] Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC.

22.3.38 Reserved (0x0000009C~0x000000FC)

DATA (0x00000100~0x00000140)

Data FIFO read/write.

Table 308. Data FIFO read/write

Name	Bit	Default	R/W	Description
FIFO	31 - 00	-	R/W	If address offset is equal or greater than 0x100, then FIFO is selected

22.4 Auto Stop

The MSHC internally generates a stop command and is loaded in the command path when the SEND_AUTO_STOP bit is set in the Command register. The auto-stop command helps to send an exact number of data bytes using a stream read or write for the MMC, and a multiple-block read or write for SD memory transfer for SD cards. The software should set the send_auto_stop bit according to details listed in Table 212.

Table 309. Auto Stop

Card type	Transfer type	Byte count	SEND_AUTO_STOP bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count = 0 is illegal
MMC	Single-block write	>0	No	Byte count = 0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes[1]	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes[1]	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count = 0 is illegal
SDMEM	Single-block write	>0	No	Byte count = 0 is illegal
SDMEM	Multiple-block read	0	No	Open ended multiple block
SMEM	Multiple-block read	>0	Yes[1]	Auto stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open ended multiple block
SDMEM	Multiple-block write	>0	Yes[1]	Auto stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count = 0 is illegal

[1] The condition under which the transfer mode is set to block transfer and BYTE_COUNT is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If BYTE_COUNT = n*BLOCK_SIZE (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue CMD18/CMD25 commands without setting the SEND_AUTO_STOP bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the SEND_AUTO_STOP bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.

22.5 Descriptors

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure: The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (BMOD @0x80).
- Chain Structure: Each descriptor points to a unique buffer and the next descriptor.

Figure 48 illustrates the IDMAC dual-buffer descriptor structure.

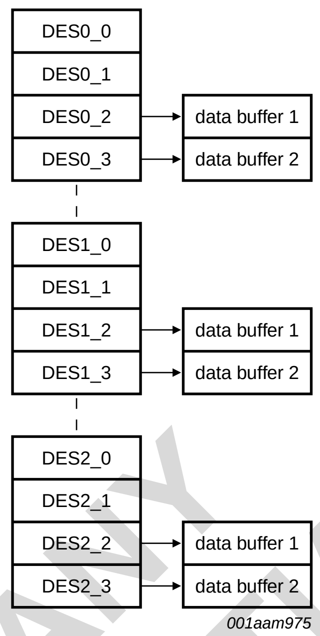

Fig 49. Dual-Buffer Descriptor Structure

Figure 50 illustrates the IDMAC chain descriptor structure.

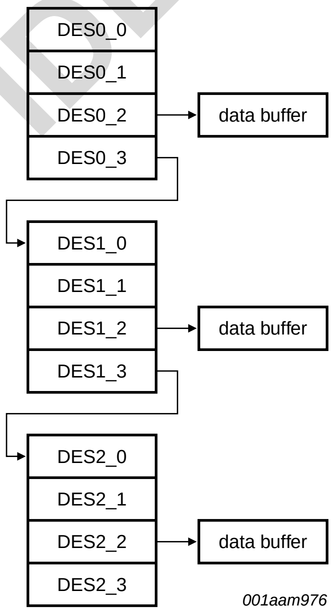

Fig 50. Chain Descriptor Structure

Each descriptor contains 16 bytes of control and status information. DES_0 is a notation used to denote the [31:0] bits, DES_1 to denote [63:32] bits, DES_2 to denote [95:64] bits, and DES_3 to denote [127:96] bits in a descriptor.

The Des0 descriptor in the IDMAC contains control and status information; Table 310 lists the bits in this descriptor.

Table 310. Bits in IDMAC Des0 descriptor

Bits	Name	Description
31[1]	OWN	Owned
30[2]	(CES)	Card Error Summary - Indicates the logical OR of the following bits: • EBE: End Bit Error • RTO: Response Time out • RCRC: Response CRC • SBE: Start Bit Error • DRTO: Data Read Timeout • DCRC: Data CRC for Receive • RE: Response Error
29 - 06	-	Reserved
05[3]	ER	End of Ring
04[4]	CH	Second Address Chained
03[5]	FS	First Descriptor
02[6]	LD	Last Descriptor
01[7]	DIC	Disable Interrupt on Completion
00	-	Reserved

[1] When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data transfer.

[2] These error bits indicate the status of the transaction to or from the card. These bits are also present in RINTSTS.

[3] When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.

[4] When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.

[5] When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.

[6] When set, this bit indicates that the buffers pointed to by this descriptor are the last buffers of the data.

[7] When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.

The Des1 descriptor contains the buffer size; Table 311 lists the bits in this descriptor.

Table 311. Bits in IDMAC Des1 Descriptor

Bits	Name	Descriptor
31 - 26	-	Reserved
25 - 13[1]	BS2	Buffer 2 Size
12 - 00[2]	BS1	Buffer 1 Size

[1] These bits indicate the second data buffer byte size. The buffer size must be a multiple of 4 respectively. In the case where the buffer size is not a multiple of 4, the resulting behavior is undefined. This field is not valid if DES0[4] is set.

[2] Indicates the data buffer byte size, which must be a multiple of 4 bytes. In the case where the buffer size is not a multiple of 4, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next descriptor in case of a chain structure, or to the next buffer in case of a dual-buffer structure.

The Des2 descriptor contains the address pointer to the data buffer; Table 312 lists the bits in this descriptor. IDMAC Des2 Descriptor.

Table 312. Bits in IDMAC Des2 Descriptor

Bits	Name	Descriptor
31 - 00[1]	BAP1	Buffer Address Pointer 1

[1] These bits indicate the physical address of the first data buffer. The IDMAC ignores DES2 [1:0] internally

The Des3 descriptor contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 313. Bits in IDMAC Des3 Descriptor Address (BAP2)

Bits	Name	Description
31 - 00[1]	BAP2	Buffer Address Pointer 2 / Next Descriptor Address

[1] These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned (DES3[1:0] = 0. Internally the LSBs are ignored).

23. NAND FLASH Controller

23.1 General description

There is a NAND FLASH memory controller in ASC8848/49/50/51 SoC which supports two devices. It is designed to interface with NAND FLASH devices that are compliant with ONFI standard 1.0. Some custom commands provided by Samsung, Micron and STM are also implemented. With built-in hardware ECC, MLC NAND FLASH memories could be supported.

23.2 Features

The NAND FLASH memory controller provides the following features.

- Supports Open NAND Flash Interface (ONFI) rev. 1.0 compatible devices
- Programmable page size, 2KB and 4KB
- Hardware BCH ECC (correct up to 8 and detect up to 16 distorted bits every 512 bytes)
- Embedded DMA Engine
- Support 4 or 5 address cycles
- Fully programmable timing parameters
- Common ready/busy signal for each memory
- Supports boot from NAND FLASH by firmware

23.3 Memory Map Register

23.3.1 FLCONF (0x00001300)

Timing parameter configuration register. TAHB is the period of AHB clock.

Table 314. Timing Parameter configuration register

Name	Bit	Default	R/W	Description
-	31 - 30	-	-	Reserved
TWB	29 -23	0x0	R/W	WE# high to R/B# low. t_{WB}=(TWB+1)* T_{AHB}.
TWHR	22 - 17	0x0	R/W	WE# high to RE# low. t_{WHR}=(TWHR+1)* T_{AHB}.
TWP	16 - 11	0x0	R/W	WE# pulse width. t_{WP}=(TWP+2)* T_{AHB}.
TRP[1]	10 - 05	0x0	R/W	RE# pulse width. t_{RP}=(TRP+1)* T_{AHB}.
TWH	04 - 00	0x0	R/W	WE# high hold time. t_{WH}=(TWH+1)* T_{AHB}.

[1] EDO mode is not supported which means t_{RP} must be larger than t_{REA} to ensure the correct operation.

23.3.2 FLCTRL (0x00001304)

Control register.

Table 315. Control register

Name	Bit	Default	R/W	Description
-	31 - 23	-	-	Reserved
WR_PROT	23	0x1	R/W	Active-low write protect bit
-	22 - 19	-	-	Reserved
FLCE	18 - 16	0x00	R/W	Chip enable (0~7).
	15 - 13		R/W	Reserved
BLOCK_SIZE	12	0x0	R/W	Block size. 1’b0: 64 pages 1’b1: 128 pages
PAGE_SIZE	11	0x0	R/W	Page size. 1’b0: 4KB 1’b1: 2KB
SPARE_SIZE	10	0x0	R/W	Spare area size. The first 64B will be used for error correction and could not be modified. 1’b0: 64B for 2KB page; 128B for 4KB page. 1’b1: 112B for 2KB page; 224B for 4KB page.
ECC	09	0x0	R/W	Hardware ECC enable. 1’b0: Disable 1’b1: Enable
INTR_EN	08	0x0	R/W	Global interrupt enable. 1’b0: Disable 1’b1: Enable
ACC_ERR_INTR_EN	07	0x0	R/W	Incorrect FLDATA register access interrupt enable. FLDATA register could not be accessed during NAND Flash read or write transfer. 1’b0: Disable 1’b1: Enable
-	06	0X0	R/W	Reserved
RUB_INTR_EN	05	0x0	R/W	Interrupt on the rising edge of read/busy port. 1’b0: Disable 1’b1: Enable
DMA_ERR_INTR_EN	04	0x0	R/W	AHB error response interrupt enable during DMA transfer. 1’b0: Disable 1’b1: Enable
DMA_TRIGGER	03	0x0	R/W	Automatically complete the DMA read data transfer before NAND Flash write transfer or complete the DMA write data transfer after NAND Flash read transfer. 1’b0: Disable 1’b1: Enable

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Table 315. Control register *…continued*

Name	Bit	Default	R/W	Description
TRANS_CMPT_INTR_EN	02	0x0	R/W	Transfer complete interrupt enable. 1’b0: Disable 1’b1: Enable
RNB_MODE	01	0x0	R/W	Read/busy line mode. 1’b0: Separate ready/busy line for each device 1’b1: Common read/busy line for all devices
ADDR_CYCLE	00	0x0	R/W	Number of address bytes sent to NAND Flash device. 1’b0: 4 address cycles 1’b1: 5 address cycles

23.3.3 FLCOMM (0x00001308)

Command register.

Table 316. Command register

Name	Bit	Default	R/W	Description
-	31 - 16	-	-	Reserved
FLCOMM[1]	15 - 00	0x0	R/W	FLash memory COMMands.

[1] Refer to Table 223 Operations Supported in the NAND Flash Memory Controller for the supported FLASH memory commands.

23.3.4 FLADDR_0_LO (0x0000130C)

Lower bits for Flash address 0 register.

Table 317. Flash address 0 register

Name	Bit	Default	R/W	Description
FLADDR_0_LO	23	0x1	R/W	Low 32 bits for the read FLASH memory address.

23.3.5 FLADDR_1_LO (0x00001310)

Lower bits for Flash address 1 register.

Table 318. Flash address 1 register

Name	Bit	Default	R/W	Description
FLADDR_1_LO	31 - 00	0x0	R/W	Low 32 bits for the write FLASH memory address.

23.3.6 FLDATA (0x00001314)

Data register to read/write the FLASH memory.

Table 319. FLDATA

Name	Bit	Default	R/W	Description
FLDATA[1]	31 - 00	0x0	R/W	Flash memory data.

[1] Read/write the Flash memory one by one through the host processor instead of using the internal buffer to transfer a whole page in a time.

23.3.7 Reserved (0x00001318)

This register is reserved.

23.3.8 FLSTATE (0x0000131C)

Status register.

Table 320. Status register

Name	Bit	Default	R/W	Description
-	31 - 10	-	-	Reserved
TRANS_CMPT_FLAG[1]	09	0x0	R	Transfer complete flag.
DMA_ERR	08	0x0	R	Same as ERR_FLAG in FLDMA_CTRL
DMA_BUSY	07	0x0	R	Same DMA_BUSY in FLDMA_CTRL
FSM[3]	06 - 05	0x0	R	FSM Busy.[3] 2’b00: Controller is in an IDLE state 2’b01: Controller executes command ending up to 16 clock cycles 2’b10/2’b11: Controller executes normal command – long delays.
INTR[4]	04	0x0	R	Interrupt request.
-	03	-	-	Reserved
ACC_ERR[5]	02	0x0	R	Access Error.
RNB_INTR[6]	01	0x0	R	Ready/Busy edge.
RNB_STATE[7]	00	-	R	Ready/Busy state.

[1] Flag is cleared when a new command is written to the FLCOMM register.

[2] This field gives the current state of the controller. When writing to FLCOMM register, FSM will be set to 2’b10 and back to 2’b00 when the command is done.

[3] First code means that controller gives RETRY response, second one gives SPLIT response.

[4] This bit is valid only when INTR_EN in FLCTRL register is enabled. Those interrupts enabled in FLCTRL will trigger this bit. Write 1’b0 to clear it.

[5] This bit is set when an illegal access attempt has been detected. Illegal Access occurs when an executed command implies a transfer while the host tries to make an opposing attempt. Write 1’b0 to clear it.

[6] This bit is set when the rising edge of R/B# has been detected. Write 1’b0 to clear it.

[7] This bit reflects the current state of R/B# input pin

23.3.9 Reserved (0x00001320~0x0000133C)

23.3.10 FLECCSTATUS (0x00001340)

ECC status register.

Table 321. ECC status register

Name	Bit	Default	R/W	Description
-	31 - 24	-	-	Reserved
ERROR_FLAG[1]	23 - 16	0x0	R	Error flag.
-	15 - 08	-	-	Reserved
CORRECT_FLAG[2]	07 - 00	0x0	R	Error correct flag.

[1] Each bit corresponds to the 512 byte subpage of the memory page size. If errors occur during read process in buffered mode, bits corresponding to the subpage where errors were noticed are sets.

[2] Each bit corresponds to the 512 byte subpage of the memory page size. The only valid bits are those for which corresponding ecc error bits are set. If errors for a given subpage were successfully corrected, the appropriate bit is set.

23.3.11 FLADDR_0_HI (0x00001344)

Higher bits for Flash address 0 register.

Table 322. Higher bits for Flash address 0 register

Name	Bit	Default	R/W	Description
-	31 - 04	-	-	Reserved
FLADDR_0_HI	03 - 00	0x1	R/W	Higher bits for the read FLASH memory address.

23.3.12 FLADDR_1_HI (0x00001348)

Higher bits for Flash address 1 register.

Table 323. Higher bits for Flash address 1 register

Name	Bit	Default	R/W	Description
-	31 - 04	-	-	Reserved
FLADDR_1_H1	03 - 00	0x0	R/W	Higher bits for the write FLASH memory address.

23.3.13 Reserved (0x0000134C~0x0000137C)

This register is reserved.

23.3.14 FLDMA_ADDR(0x00001380)

DMA address register.

Table 324. DMA address register

Name	Bit	Default	R/W	Description
FLDMA_ADDR	31 - 00	0x0	R/W	The base address of the DMA buffer.

23.3.15 FLDMA_CTRL (0x00001384)

DMA control register.

Table 325. DMA control register

Name	Bit	Default	R/W	Description
-	31 - 25	-	-	Reserved
START_FLAG[1]	24	0x0	R/W	DMA start flag.
-	23 - 17	-	-	Reserved
DMA_DIR[2]	16	0x0	R/W	DMA transfer direction. 1'b0: Write data from AHB to internal BUFFER 1'b1: Read from internal BUFFER and write to AHB
DMA_SIZE[3]	15 - 14	0X0	R/W	Transfer size. 2'b00: 8-bits transfer size 2'b01: 16-bits transfer size 2'b10: Reserved 2'b11: 32-bits transfer size

Table 325. DMA control register *…continued*

Name	Bit	Default	R/W	Description
DMA_BURST[4]	13 - 11	0x0	R/W	Burst type. 3'b000: Single transfer address decrement 3'b001: Burst of unspecified length address decrement 3'b010: Single transfer address increment 3'b011: Burst of unspecified length address increment 3'b100: 4 beat burst address increment 3'b101: 8 beat burst address increment 3'b110: 16 beat burst address increment 3'b111: Stream burst (address const)
-	10 - 03	-	-	Reserved
DMA_BUSY[5]	02	0x0	R	DMA busy.
ERR_FLAG[6]	01	0x0	R	DMA error flag.
-	00	0X0	-	Reserved

[1] Setting this bit forces the DMA controller to start a block transfer. The flag is cleared automatically by the DMA controller when it gains control of the internal bus.

[2] This flag defines transmission direction.

[3] These bits define the requested transfer size on the AHB bus.

[4] These bits define the main transfer type used by the DMA to precede the requested transfer.

[5] The flag is set when the DMA is transmitting data and a write attempt to sfr register is noticed.

[6] Flag is set when during DMA transfer transmission errors occur. Cleared when writing FLDMA_CTRL register.

23.3.16 FLDMA_CNTR (0x00001388)

DMA counter and the internal buffer start address registers.

Table 326. DMA counter and internal buffer start address registers

Name	Bit	Default	R/W	Description
-	31 - 29	-	-	Reserved
DMA_CNTR[1]	28 - 16	0x0	R/W	DMA counter.
-	15 - 13	-	-	Reserved
BUFF_ADDR[2]	12 - 00	0x0	R/W	Internal buffer address.

[1] This register stores the size to be transferred. This register decrements its value during transfer.

[2] Only valid when writing NAND Flash memory. Specify the address of the internal buffer from which the controller starts moving into NAND Flash memory. When reading NAND Flash memory, it always starts writing at address 0.

23.4 Timing

Timing Parameters

Table 327 shows how to derive the timing parameters defined in ONFI rev. 1.0 from FLCONF register.

Table 327. Timing parameter partnership

Parameter	Formula	Descriptions
tADL	TWHR+1	ALE to data start
tALH	TWH+1	ALE hold time
tALS	TWP+1	ALE setup time
tCH	TWH+1	CE# hold time
tCLH	TWH+1	CLE hold time
tCLS	TWP+1	CLE setup time
tCS	TWP/TRP+1	CE# setup time
tDH	TWH+1	Data hold time
tDS	TWP/TRP+1	Data setup time
tWC	TWH+TWP+2	Write cycle time
tAR	TWHR+1	ALE to RE# delay
tCLR	min 3	CLE to RE# delay
tOH	TWH+1	Data output hold time
tRC	TRP+TWH+2	Read cycle time
tREA	0	RE# access time
tREH	TWH+1	RE# high hold time
tRR	TWP+1	Ready to RE# low

23.4.1 Timing Relationship

The relationship of timing parameters stored in FLCONF is depicted below.

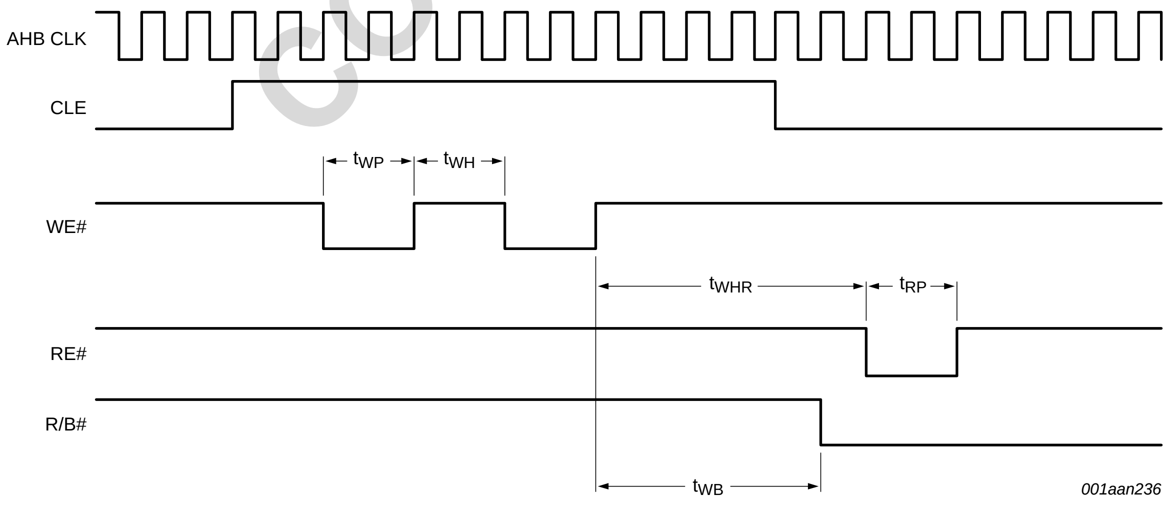

Fig 51. Timing relationship

23.5 Commands

All commands supported in the NAND Flash memory controller is listed Table 328. To use Page Read operation, write 0x0030 to the FLCOMM register and the NAND Flash memory controller will write 0x00 command to the command register in the NAND FLASH memory, then write 4 or 5 ADDRESS cycles (FLADDR_0_HI, FLADDR_0_LO) depending on the ADDR_CYCLE in FLCTRL register and finish with 0x30 command.

Table 328. Operations supported in NAND flash memory controller

Operation	Command	Command		Valid while busy	Descriptions
		First	Second		
Generic commands					
Page Read	0x0030	0x00	0x30	No	Reads full Page automatically and transfers it into the BUFFER
Page Read 1	0x0130	0x00	0x30	No	Sends instructions and address to the flash memory device
Read for internal data move	0x0035	0x00	0x35	No	Sends instructions and address (4 or 5 bytes) to flash memory
Random data read	0x0005	0x05	0xE0	No	Sends instructions and 2 address bytes to flash memory
Read status	0x0070	0x70	-	Yes	Sends instructions to flash memory
Program Page	0x0080	0x80	0x10	No	Automatically writes contents of the BUFFER to the flash memory
Program Page 1	0x0180	0x80	-	No	Sends instruction and address to the flash memory
Program Page cache	0x0580	0x80	0x15	No	Automatically writes contents of the BUFFER to the flash memory
Write Page	0x0010	0x10	-	No	Sends instruction to the flash memory
Write cache	0x0015	0x15	-	No	Sends only instruction to flash memory
Program for internal data move	0x0085	0x85	0x10	No	Writes instruction 0x85h, next address (4 or 5 bytes) and instruction 0x10h
Random data input for program	0x0185	0x85	-	No	Writes instruction and 2 address bytes
Block erase	0x0060	0x60	0xD0	No	Writes instructions address to flash memory
Reset	0x00FF	0xFF	-	Yes	Writes instruction to flash memory
Read ID	0x0090	0x90	-	No	Writes instruction and address
Micron memories					
Page Read Cache Mode Start	0x1031	0x31	-	No	Reads automatically full Page and transfers it into the BUFFER
Page Read Cache Mode Start last	0x103F	0x3F	-	No	Reads automatically full Page and puts it into the BUFFER
Page Read Cache Mode Start 1	0x1131	0x31	-	No	Sends instruction to flash memory
Page Read Cache Mode Start Last 1	0x113F	0x3F	-	No	Sends instruction to flash memory
Program page 2	0x1280	0x80	0x11	No	Automatically writes contents of BUFFER to flash memory.
OTP Program	0x10A0	0xA0	0x10	No	Automatically write whole Page to OTP memory area
OTP Program 1	0x11A0	0xA0	0x10	No	Sends instruction and address only

Table 328. Operations supported in NAND flash memory controller *…continued*

Operation	Command	Command		Valid while busy	Descriptions
		First	Second		
OTP Protect	0x10A5	0xA5	0x10	No	Protects OTP memory area
OTP Read	0x10AF	0xAF	0x30	No	Reads automatically full Page and puts it into BUFFER
OTP Read 1	0x11AF	0xAF	0x30	No	Sends instruction and address bytes only
Plane Page Read	0x1230	0x00	0x30	No	Writes read commands and addresses for first and second planes, next transfers first plane into the BUFFER
Plane Page Read 1	0x1330	0x00	0x30	No	Writes read commands and addresses for first and second planes
Plane Random Data Read	0x1206	0x06	0xE0	No	Switches read to the second plane. After writing command the whole page is read into the BUFFER
Plane Random Data Read 1	0x1306	0x06	0xE0	No	Switches read to the second plane. After writing command the controller goes to the idle read state
Plane Page Program	0x1081	0x81	0x10	No	Automatically writes contents of BUFFER to flash memory
Plane Page Program 1	0x1181	0x81	-	No	Only writes command 0x81h and 4 or 5 address bytes.
Plane Page Read for Internal Data Move	0x1235	0x00	0x35	No	Reads two pages on different planes to internal data buffer
Plane Page Program for Internal Data Move	0x1285	0x85	0x11	No	Writes internal memory data register contents to the new location
Plane Page Eraser	0x1160	0x60	0xD0	Yes	Erases two pages on different planes
Plane Page Read Status	0x1078	0x78	-	Yes	Writes read status command and goes to the idle read state
Write Plane Page	0X1011	0x11	-	No	
STM Memories					
Cache Read	0x2031	0x00	0x31	No	Reads automatically full Page and puts it into BUFFER
Cache Read 1	0x2131	0x00	0x31	No	Sends instruction and address bytes to flash memory
Cache Read 2	0x2231			No	Only reads automatically full page and puts it into BUFFER, no instruction nor address bytes are sen
Exit Cache Read	0x2034	0x34			Sends only an instruction to flash memory
Read Block Lock Status	0x207A	0x7A	-	No	Writes only an instruction
Blocks Unlock	0x2023	0x23	0x24	No	Writes an instruction followed by 2 or 3 address bytes, then again an instruction and 2 or 3 address bytes
Blocks Lock	0x202A	0x2A		No	Writes instruction only
Blocks Lock-Down	0x202C	0x2C	-	No	Writes instruction only
Samsung Memories					
Program Page 2	0x0280	0x80	0x11	No	Automatically writes contents of BUFFER to flash memory
Program Page Cache	0x0580	0x80	0x15	No	Automatically writes contents of BUFFER to flash memory

Table 328. Operations supported in NAND flash memory controller *…continued*

Operation	Command	Command		Valid while busy	Descriptions
		First	Second		
Block Erase 1	0x0160	0x60	0xD0	No	Sends instruction 0x60h, next address (2 or 3 byte), next command 0x60h, address (2 or 3 byte), and command (0xD0h)
Plane Page Program	0x0081	0x81	0x10	No	Automatically writes contents of BUFFER to flash memory
Plane Page Program 1	0x0181	0x81	-	No	Only writes command 0x81h and 4 or 5 address bytes
Read EDC Status	0x007B	0x7B	-	Yes	Writes instruction only
Read Chip 1 Status	0x00F1	0xF1	-	Yes	Writes instruction only
Read Chip 2 Status	0x00F2	0xF2	-	Yes	Writes instruction only
Write Plane Page	0x0011	0x11	-	No	Writes command only

23.6 Address Mapping

Table 329 and Table 330 show the address mapping from the FLADDR0 and FLADDR1 to the address bytes on the I/O lines. Table 329 is for 2KB page size and Table 330 is for 4KB page size. If ADDR_CYCLE in FLCTRL register is 0 (address cycle is 4), the 5th byte is ignored.

Table 329. Address mapping and Address Bytes Relation for 8-Bit Memory Devices – 2KB Page

Address Cycle	I/O[0]	I/O[1]	I/O[2]	I/O[3]	I/O[4]	I/O[5]	I/O[6]	I/O[7]
1st cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd cycle	A8	A9	A10	A11	0	0	0	0
3rd cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th cycle	A28	A29	A30	A31	A32	A33	A34	A35

Table 330. Address mapping and Address Bytes Relation for 8-Bit Memory Devices – 4KB Page

Address Cycle	I/O[0]	I/O[1]	I/O[2]	I/O[3]	I/O[4]	I/O[5]	I/O[6]	I/O[7]
1st cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd cycle	A8	A9	A10	A11	A12	0	0	0
3rd cycle	A13	A14	A15	A16	A17	A18	A19	A20
4th cycle	A21	A22	A23	A24	A25	A26	A27	A28
5th cycle	A29	A30	A31	A32	A33	A34	A33	0

23.7 Programming

There are two kinds of transfers in the NAND Flash memory controller, DMA transfer and NAND Flash memory transfer. DMA transfer moves data from DRAM to the internal buffer or from the internal buffer to DRAM. NAND Flash memory transfer moves data from the internal buffer to the NAND Flash memory or from the NAND Flash memory to the internal buffer. The internal buffer is shared with the boot ROM controller.

23.7.1 NAND Flash Memory Transfer

There are two kinds of NAND Flash memory transfers. One is to transfer whole page from/to internal buffer, like Page Read; the other is to transfer command first and then use the host processor to push or pop data through FLDATA register, like Page Read 1. Use Page Read operation as an example.

1. Switch the internal buffer for the NAND Flash memory controller.
2. Set up FLCONF register according to the NAND Flash memory datasheet.
3. Set up FLCTRL register
    a. Write BLOCK_SIZE, PAGE_SIZE, SPARE_SIZE, and ADDR_CYCLE according to the NAND Flash memory datasheet.
    b. DMA_Trigger = 1’b0, if only NAND Flash memory transfer is required.
    c. RNB_MODE = 1’b0, according to the system configuration
    d. TRANS_CMPT_INTR_EN = 1’b1
    e. RNB_INTR_EN = 1’b0
    f. DMA_ERR_INTR_EN = 1’b1
    g. ACC_ERR_INTR_EN = 1’b1
    h. INTR_EN = 1’b1
    i. ECC = 1’b1, enable error correction mechanism. This bit must be enabled or disabled for both read and write operations.
    j. FLCE = 3’b5, enable NAND Flash memory device 5.
    k. WR_PROT = 1’b1, make NAND Flash memory writable.
4. Write FLADDR_0_LO and FLADDR_0_HI registers to specify the page to read from the NAND Flash memory.
5. Write FLCOMM register with 0x0030 according to Table 328
6. Wait the interrupt or wait FSM in FLSTATE register to be IDLE.

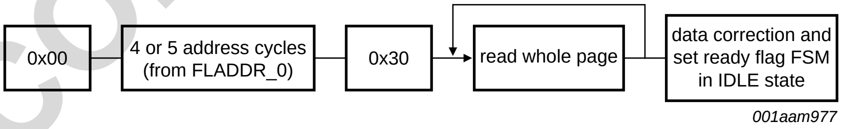
0x00
4 or 5 address cycles (from FLADDR_0)
0x30
read whole page
data correction and set ready flag FSM in IDLE state
001aam977

Fig 52. Page read operation

23.7.2 DMA Transfer

The programming procedure is as follows.

1. Switch the internal buffer for the boot ROM controller.
2. Fill 2048 bytes in the internal buffer by the host processor.
3. Switch the internal buffer for the NAND Flash memory controller.
4. Write FLDMA_ADDR with 0x01000000, move 2048 bytes to address 0x01000000.
5. Write FLDMA_CNTR with 0x08000000.
6. Set up FLDMA_CTRL
    a. DMA_DIR=1’b1, read data from the internal buffer and write to AHB.
    b. DMA_SIZE=2’b11, 32-bit transfer
    c. DMA_BURST=3’b101, 8-beat burst transfer
    d. START_FLAG=1’b1, start DMA transfer.
7. Wait DMA_BUSY in FLSTATE to become 1’b0, then check if the data in address 0x01000000 is correct by the host processor.

23.7.3 Combined Transfer

To make the NAND Flash memory transfer and the DMA transfer to start one by one automatically, set DMA_TRIGGER to 1’b1 with the above configurations and the page data will be first loaded from the NAND Flash memory to the internal buffer, error corrected and then written to the DMA buffer.

24. PCI Express Dual Mode Controller

24.1 General Description

There is a one-lane PCI Express dual mode (DM) controller in ASC8848/49/50/51 SoC. It is compliant with PCIe 1.1 specification and could operate in either Root Complex (RC) mode or Endpoint (EP) mode. PCIe is ubiquitous in all PCs and various applications are adopted quickly for this trend. Built-in with PCIe, SoC could connect with all PCIe devices with less I/O than PCI interface. With PCIe dual mode controller, it is easy to extend the system capability by cascading multiple chips with one acting as RC while the others acting as EPs.

24.2 Features

The PCIe dual mode controller provides the following features.

- Supports 2.5Gbps data transfer rate
- Supports legacy PCI and MSI interrupts (only one INTx interrupt and up to 8 MSI interrupts)
- Includes a DMA controller to support TX and RX transfers
- Supports memory space address translation
- Supports PCIe active state power management (ASPM L0s)
- Supports end-to-end CRC (ECRC) generation and checking
- Not support multi-function devices.

25. UART Interfaces

25.1 General description

Four UART interfaces are provided in ASC8848/49/50/51 SoC. UART provides a serial communication interface with a computer. Only two interfaces support MODEM functions with CTS, RTS, DSR, DTR, RI and DCD. It is possible to use phone line communication through MODEM functions when the wired or wireless network is out of order.

25.2 Features

25.2.1 FIFO

There is a 16-byte FIFO for both TX and RX to reduce the number of interrupts sent to the host processor.

25.2.2 Frame Format

Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data.

25.2.3 Baud Rate

Programmable baud rate generator divides UART clock by DL (divisor latch) and generate the 16x baud rate clock. The UART clock is 18.432MHz.

Table 331. Baud Rate

Baud Rate(bps)	16xBaud Rate	DL	DLL	DLM
300	4,800	3840	0x00	0x0F
1,200	19,200	960	0xC0	0x03
2,400	38,400	480	0xE0	0x01
4,800	76,800	240	0xF0	0x00
9,600	153,600	120	0x78	0x00
19,200	307,200	60	0x3C	0x00
38,400	614,400	30	0x1E	0x00
57,600	921,600	20	0x14	0x00
115,200	1,843,200	10	0x0A	0x00

25.2.4 MODEM Control

Supports MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD).

25.2.5 Data Format

Fully programmable serial interface characteristics.

- 5, 6, 7 or 8-bit characters.
- Even, odd or no-parity bit generation and detection
- 1, 1.5, or 2 stop bits generation

25.3 Memory Map Register

25.3.1 UARTC_VERSION (0x00000000)

Version information register.

Table 332. Version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x02	R	Major version number
MINOR_VERSION	23 - 16	0x00	R	Minor version number
BUILD_VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x17	R	Revision number

25.3.2 UARTC_RBR (0x00000004)

Receive buffer register.

Table 333. Receive buffer register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
RBR	07 - 00	0x0	R	Receive data port

25.3.3 UARTC_THR (0x00000004)

Transmitter holding register.

Table 334. Transmitter holding register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
THR	07 - 00	0x0	W	Transmit data port

25.3.4 UARTC_IER (0x00000008)

Interrupt enable register.

Table 335. Interrupt enable register

Name	Bit	Default	R/W	Description
-	31 - 04	0x0	-	Reserved
Modem status	03	0x0	R/W	1'b0: disable the modem status register interrupt. 1'b1: enable the modem status register interrupt
Receiver line status	02	0x0	R/W	1'b0: disable the receiver line status interrupt. 1'b1: enable the receiver line status interrupt.
THR empty	01	0x0	R/W	1'b0: disable the transmitter empty interrupt. 1'b1: enable the transmitter empty interrupt.
Data Ready	00	0x0	R/W	1'b0: disable the receiver ready interrupt. 1'b1: enable the receiver ready interrupt.

25.3.5 UARTC_IIR (0x0000000C)

Interrupt identification register.

Table 336. Interrupt Identification register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
FIFO enable mode	07 - 06	0x1	R	2’b00: No FIFO. 2’b10: unusable FIFO. 2’b11: FIFO enable.
-	05 - 04	0x0	-	Reserved
FIFI mode only	03	0x0	R	In the FIFO mode this bit is set along with bit 2 when a timeout is pending.
Interrupt identification	02 - 01	0x0	R	These bits identify the highest priority interrupt that is pending. Table 337 describes the different interrupt conditions and their identification code.
Interrupt status	00	0x1	R	1’b0: an interrupt is pending. 1’b1: no interrupt is pending.

Table 337. Interrupt identification register

FIFO mode only	Interrupt identification register			Interrupt set and reset function			
Bit3	Bit2	Bit1	Bit 0	Priority level	Interrupt type	Source description	Interrupt reset method
0	0	0	1	-	None	[1]	None
0	1	1	0	First	Receiver line status	[2]	Read Line Status Register (LSR)
0	1	0	0	Second	Receiver data ready	[3]	Read Receiver Buffer Register (RBR)
1	1	0	0	Second	Character reception timeout	[4]	Read Receiver Buffer Register (RBR)
0	0	1	0	Third	Transmitter holding register empty	[5]	Write transmitter holding register (THR)
0	0	0	0	Fourth	Modem status	[6]	Read Modem Status Register (MSR)

[1] There is no interrupt pending

[2] There is an overrun error, parity error, framing error or break interrupt indication corresponding to the received data on FIFO.

[3] In non-FIFO mode, there is receive available in the RBR register.
In FIFO mode, the number of characters in the RX FIFO is equal to or greater than the trigger level programmed in FCR.

[4] There is least one character in the RX FIFO and during the time corresponding to four characters at the selected baud rate, no new characters has been received and no reading has been executed on the RX FIFO.

[5] In non-FIFO mode, the 1-byte THR is empty. In FIFO mode, the complete 16-byte TX FIFO is empty, so 1to 16 characters can be written to THR.

[6] A change has been detected in the Clear to Send (CTS), Data Set Ready (DSR) or Carrier detect (CD) input lines or a trailing edge in the Ring Indicator (RI) input line.

25.3.6 UARTC_FCR (0x0000000C)

FIFO control register.

Table 338. FIFO control register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
RX FIFO trigger level	07 - 06	0x0	W	2'b00: 1 character. 2'b01: 4 characters. 2'b10: 8 characters. 2'b11: 14 characters.
-	05 - 03	0x0	-	Reserved
TX FIFO reset	02	0x0	W	1'b0: no change. 1'b1: clears the content of the TX FIFO and resets its counter logic to zero. Return to zero after clearing the FIFOs. Do not assert this reset. TX FIFO could possibly be regarded as non-empty temporarily.
RX FIFO reset	01	0x0	W	1'b0: no change. 1'b1: clears the content of the RX FIFO and resets its counter logic to zero. Return to zero after clearing the FIFOs. Do not assert this reset. RX FIFO could possibly be regarded as non-empty temporarily.
FIFO enable	00	0x0	W	1'b0: disable TX and RX FIFOs. 1'b1: enable TX and RX FIFOs

25.3.7 UARTC_LCR (0x00000010)

Line control register.

Table 339. Line control register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
DLAB	07	0x0	R/W	1'b0: RBR, THR and IER accessible. 1'b1: DLL and DLM accessible
Set Break	06	0x0	R/W	1'b0: disable break condition 1'b1: enable break condition, force the serial output to space (logic 0) state
Stick Parity	05	0x0	R/W	1'b0: disable stick parity. 1'b1: If even parity is logic 1, the parity bit forced to logic 0. If even parity is logic 0, the parity bit forced to logic 1
Even Parity	04	0x0	R/W	1'b0: an odd number of logic 1s is transmitted or checked in the data word bits and parity bit. 1'b'1: an even number of logic 1s is transmitted or checked in the data word bits and parity bit.

Table 339. Line control register *…continued*

Name	Bit	Default	R/W	Description
Parity enable	03	0x0	R/W	1’b0: disable parity generation. 1’b1: enable parity generation.
Stop bits	02	0x0	R/W	1’b0: 1 stop bit. 1’b1: 1.5 stop bits (5-bit word) / 2 stop bits (6-,7- or 8-bit word).
Word length	01 - 00	0x0	R/W	2’b00: 5 bits. 2’b01: 6 bits. 2’b10: 7 bits. 2’b11: 8 bits

25.3.8 UARTC_MCR (0x00000014)

MODEM control register.

Table 340. Modem control register

Name	Bit	Default	R/W	Description
-	31 - 05	0x0	-	Reserved
Loop	04	0x0	R/W	1’b0: normal operating mode. 1’b1: enable local loop-back mode.
Out2	03	0x0	R/W	1’b0: force Out2to high. 1’b1: force Out2to low
Out1	02	0x0	R/W	1’b0: force Out1 to high. 1’b1: force Out1 to low.
RTS (request to send)	01	0x0	R/W	1’b0: force RTS to high. 1’b1: force RTS to low. This bit controls the “request to send” active low output
DTR (data terminal ready)	00	0x0	R/W	1’b0: force DTR to high. 1’b1: force DTR to low. This bit controls the “data terminal ready”, active low output.

25.3.9 UARTC_LSR (0x00000018)

Line status register.

Table 341. Line status register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
FIFO data error	07	0X0	R	1’b0: none. 1’b1: at least one parity error, framing error and break indicator is in the FIFO. Cleared by read LSR.
Transmitter empty	06	0x1	R	1’b0: transmit holding or shift registers is full. 1’b1: transmitter hold and shift register are empty.
THR empty	05	0x1	R	1’b0: transmit holding register is full. 1’b1: transmitter hold register is empty.

Table 341. Line status register *…continued*

Name	Bit	Default	R/W	Description
Break interrupt	04	0x0	R	1’b0: no break condition. 1’b1: the receiver’s line input sin is held at zero for a complete character time. Cleared by read LSR.
Framing error	03	0x0	R	1’b0: no framing error. 1’b1: the received character does not have a valid stop bit (a 0 is detected in the stop bit position instead of 1). Cleared by read LSR.
Parity error	02	0x0	R	1’b0: no parity error. 1’b1: the parity of the received character is wrong according to the current setting in LCR. Cleared by read LSR.
Overrun error	01	0x0	R	1’b0: no overrun error. 1’b1: a character has been completely assembled in the receiver shift register without free space to put it in the RX FIFO or holding register. Cleared by read LSR.
Receive data ready	00	0x0	R	1’b0: no data in receiver buffer. 1’b1: data has received in receiver buffer.

25.3.10 UARTC_MSR (0x0000001C)

MODEM status register.

Table 342. MODEM status register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
DCD	07	0x0	R	Data carrier detect, is complement of the DCD input.
RI	06	0X0	R	Ring indicator, is complement of the RI input.
DSR	05	0x0	R	Data set ready, is complement of the DSR input.
CTS	04	0x0	R	Clear to send, is complement of the CTS input.
Delta DCD	03	0x0	R	DCD state change detection. This bit is cleared after MSR is read. 1'b0: no DCD changed state. 1'b1: DCD changed state.
Trailing edge RI	02	0x0	R	RI trailing edge detection. This bit is cleared after MSR is read. 1'b0: no RI changed state. 1'b1: RI changed state.
Delta DSR	01	0x0	R	DSR state change detection. This bit is cleared after MSR is read. 1'b0: no DSR changed state. 1'b1: DSR changed state.
Delta CTS	00	0x0	R	CTS state change detection. This bit is cleared after MSR is read. 1'b0: no CTS changed state. 1'b1: CTS changed state.

25.3.11 UARTC_SPR (0x00000020)

Scratch pad register.

Table 343. Scratch pad register

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
User data	07 - 00	0x0	R/W	8 bits of information can be stored in this register.

25.3.12 UARTC_DLL (0x00000004)

Divisor latch LSB.

Table 344. Divisor latch LSB

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
DLL	07 - 00	0x0	R/W	Baud rate divisor latch least significant byte.

25.3.13 UARTC_DLM (0x00000008)

Divisor latch MSB.

Table 345. Divisor latch MSB

Name	Bit	Default	R/W	Description
-	31 - 08	0x0	-	Reserved
DLM	07 - 00	0x0	R/W	Baud rate divisor latch most significant byte.

26. Watchdog

26.1 General description

There is one watchdog timer in ASC8848/49/50/51 SoC and it is used to monitor the system. The watchdog counter decrements its value at every APB clock. If the system does not reload the counter, the interrupt will be asserted when the counter is equal to the match value. If there is still no response after the interrupt, the system reset will be asserted.

26.2 Features

26.2.1 Key Value

The key value to reload the watchdog counter is a specific 32-bit data, 0x28791166. The watchdog counter will not be reloaded if the written value in the WDTC_RELOAD_CTRL register does not match the key value.

26.2.2 Programmable Reset Length.

Once the watchdog counter reaches zero, the system reset will be asserted. The length of the system reset is programmable using WDTC_RST_LEN register.

26.3 Memory Map Register

26.3.1 WDTC_VERSION (0x00000000)

Version information register.

Table 346. WDTC version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x01	R	Major version number
MINOR_VERSION	23 - 16	0x00	R	Minor version number
BUILD_VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x03	R	Revision number

26.3.2 WDTC_CTRL (0x00000004)

Control register.

Table 347. Control register

Name	Bit	Default	R/W	Description
-	31 - 03	0x0	-	Reserved
OP_EN	02	0x0	R/W	Operation enable control. 1’b0: Disable WDTC. 1’b1: Enable WDTC.
ACK_EN	01	0x0	R/W	Match value match acknowledgement enable control. 1’b0: Disable match acknowledgement (interrupt). 1’b1: Enable match acknowledgement (interrupt).
ACK	00	0x0	R/W	Match value match acknowledgement. This bit is only valid when both OP_EN and ACK_EN bits are HIGH. 1’b0: Value of WDTC counter not equal to match value MMR. 1’b1: Value of WDTC counter equals match value MMR.

26.3.3 WDTC_STAT (0x00000008)

State register.

Table 348. State register

Name	Bit	Default	R/W	Description
-	31 - 01	0x0	-	Reserved
MATCH	00	0x0	R	Match value match status. 1’b0: The value of WDTC counter doesn’t equal to match value MMR. 1’b1: The value of WDTC counter equals to match value MMR.

26.3.4 WDTC_COUNT (0x0000000C)

Counter register.

Table 349. Counter register

Name	Bit	Default	R/W	Description
COUNT	31 - 00	0xFFFFFFFF	R	WDTC counter value.

26.3.5 WDTC_RELOAD_VALUE (0x00000010)

Reload value register.

Table 350. Reload value register

Name	Bit	Default	R/W	Description
RELOAD_VALUE	31 - 00	0xFFFFFFFF	R/W	WDTC reload value. When writing key value to RELOAD_CTRL MMR, the COUNT MMR will load the value in RELOAD_VALUE to it.

26.3.6 WDTC_MATCH_VALUE (0x00000014)

Match value register.

Table 351. Match value register

Name	Bit	Default	R/W	Description
MATCH_VALUE[1]	31 - 00	0x0	R/W	WDTC match value.

[1] When the COUNT value equals to MATCH_VALUE and both OP_EN and ACK_EN are HIGH, the WDTC will send a one-cycle pulse interrupt through its intc_o_intr_p output port.

26.3.7 WDTC_RELOAD_CTRL (0x00000018)

Reload control register.

Table 352. Reload control register

Name	Bit	Default	R/W	Description
RELOAD_CTRL[1]	31 - 00	0x0	W	WDTC reload control.

[1] Writing the key value to this register will make COUNT MMR load RELOAD_VALUE to it. The key value is fixed to 0x28791166.

26.3.8 WDTC_RST_LEN (0x0000001C)

Reset length register.

Table 353. Reset length register

Name	Bit	Default	R/W	Description
RST_LEN	31-00	0x0000FFFF	R/W	WDTC output reset signal length control.

26.4 Operation

Figure 53 shows the operation of the watchdog timer. If the system keeps reloading the watchdog counter, the interrupt and the system reset will never be asserted. Once the interrupt is asserted when the watchdog counter is equal to the match value, there is still a period of time for the system to reload the watchdog counter to prevent the system reset being asserted. The length of the system reset is program able depending on the application’s requirement.

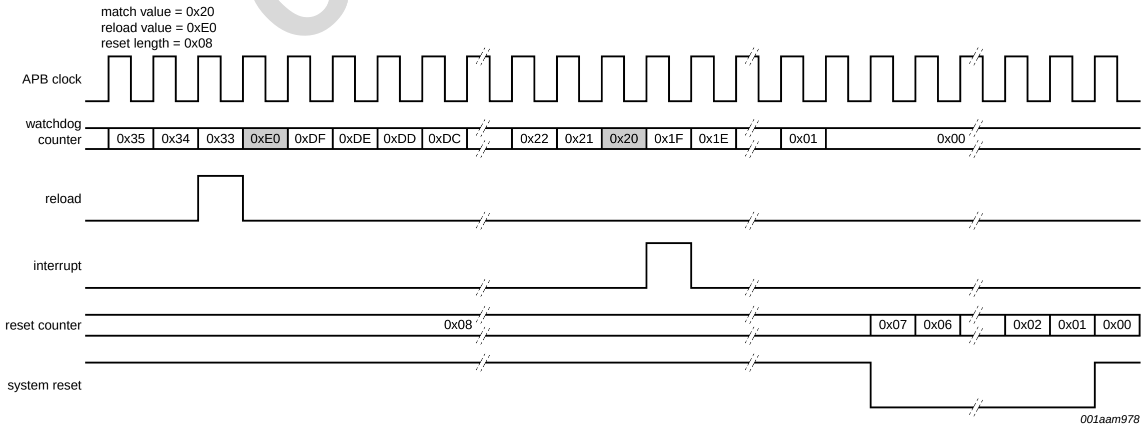

Fig 53. Operation of the Watchdog Timer

27. Video Output Controller

27.1 General description

Video Output Controller (VOC) generates the timing reference signals and transmits digital video content. It can connect to a video encoder, a LCD panel, or an HDMI transmitter. The pixel clock is up to 180MHz..

27.2 Features

27.2.1 Input Video Data Format

Supports YCbCr 4:2:0 and YCbCr 4:2:2 formats

27.2.2 Output Data Format

Support 8-bit YCbCr 4:2:2 progressive or interlace format with separate SYNC signals and BT.656 interface .
Support 16-bit YCbCr 4:2:2 progressive format with separate SYNC signals and BT.1120 interface.

Support RGB24 raw data with separate SYNC signals. Each VSYNC represents one field of the input frame and even (or top) field is output first

27.3 Memory Map Register

27.3.1 VOC_VERSION (0x00000000)

Version information register.

Table 354. VOC version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x01	R	Major version number
MINOR_VERSION	23 - 16	0x03	R	Minor version number
BUILD_VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x0E	R	Revision number

27.3.2 VOC_CTRL (0x00000004)

Control register.

Table 355. VOC control register

Name	Bit	Default	R/W	Description
IN_STRIDE	31 - 16	0x0	R/W	Input video stride
-	15 - 14	0x0	-	Reserved
	13 -13	0x0		Reserved for ASC8848/49/50 M1 version and ASC8848 M2 version. Enable BT.1120 progressive output format for ASC8849/50 M2 version and ASC8851 1’b0: Output format is decided by OUT_FORMAT (VOC_CTRL[6]). 1’b1: BT.1120 progressive output format

Table 355. VOC control register *…continued*

Name	Bit	Default	R/W	Description
OUTPIN_SEL	12 - 11	0x0	R/W	When OUT_FORMAT is BT.656, the 8-bit YCbCr 4:2:2 data could be output through different byte lanes. 2'b00: voc_o_data[7:0]. 2'b01: voc_o_data[15:8]. 2'b1x: voc_o_data[23:16]. When output format is BT.1120 the 16-bit YCbCr 4:2:2 data could be output through different byte lanes. 2'bx0: voc_o_data[0:7] for Y; voc_o_data[8:15] for CbCr 2'bx1: voc_o_data[8:15] for Y; voc_o_data[16:23] for CbCr
FREERUN_EN	10	0x0	R/W	Enable the free-run mode of buffer switching. 1'b0: Disable. 1'b1: Enable.
CBCR_FORMAT	09	0x0	R/W	The chroma components format in YUV420 input image format. 1'b0: One field YCbCr 4:2:2. 1'b1: Two fields YCbCr 4:2:0.
FIELD_MODE	08	0x0	R/W	1'b0: One interleaved field in SDRAM. 1'b1: Two single fields in SDRAM.
IN_FORMAT	07	0x0	R/W	Input image format. 1'b0: YCbCr 4:2:0. 1'b1: YCbCr 4:2:2.
OUT_FORMAT	06	0x0	R/W	Output format. 1'b0:Output RGB data with HSYNC, VSYNC, and BLANK 1'b1: Output BT.656 interlaced parallel data.
BLANK_TRG	05	0x0	R/W	Blank signal polarity. 1'b0: Active high blank signal. 1'b1: Active low blank signal.
CLK_POL	04	0x0	R/W	Output pixel clock polarity. 1'b0: positive edge aligned with data. 1'b 1: negative edge aligned with data.
RST_EN	03	0x0	R/W	Software reset signal. This signal will be cleared automatically once the reset procedure is complete. 1'b0: Do nothing or VOC reset is complete. 1'b1: Start to reset VOC module.
OP_EN	02	0x0	R/W	Set to start VOC operation. 1'b0: Disable VOC operation. 1'b1: Enable VOC operation.
OP_CMPT_ACK_EN	01	0x0	R/W	Mask for VOC operation complete acknowledge. 1'b0: Disable VOC operation complete acknowledge. 1'b1: Enable VOC operation complete acknowledge.
OP_CMPT_ACK	00	0x0	R/W	Set when VOC operation is complete. 1'b0: VOC is busy or idle. 1'b1: VOC operation is complete.

27.3.3 VOC_STAT (0x00000008)

Status register.

Table 356. Status register

Name	Bit	Default	R/W	Description
-	31 - 04	0x0	-	Reserved
FRAME_NUM	03	0x0	R	When this signal is set, the MMRs of address should be updated. 1’b0:. 1’b1:
FIELD	02	0x0	R	Current output field for interlace BT.656 output. 1’b0: Top field. 1’b1: Bottom field.
AMBA_ERR	01	0x0	R	Set when AMBA error occurs.
OP_CMPT	00	0x0	R	Set when VOC operation is complete. 1’b0: VOC is busy or idle. 1’b1: VOC operation is complete.

27.3.4 VOC_ADDR Group (0x0000000C~0x00000020)

These registers specify input video buffer addresses.

27.3.5 VOC_IN_SIZE (0x00000024)

This register specifies the input video/image size.

Table 357. Input video size

Name	Bit	Default	R/W	Description
IN_HEIGHT	31 - 16	0x0	R/W	Input video height.
IN_WIDTH	15 - 00	0x0	R/W	Input video height.

27.3.6 VOC_OUT_SIZE (0x0000028)

This register specifies the output video full size (includes blanking).

Table 358. Output video full size

Name	Bit	Default	R/W	Description
HEIGHT	31 - 16	0x0	R/W	Output video height
WIDTH	15 - 0	0x0	R/W	Output video width

27.3.7 VOC_OUT_SIZE_CTRL (0x0000002C)

This register specifies the output video position configuration parameters for BT.656.

Table 359. Video position configuration parameters

Name	Bit	Default	R/W	Description
-	31 - 24	0x0	-	Reserved
F1_OLAP	23 - 20	0x0	R/W	Overlap of the SAV and EAV code from field 1 to field 0. (PAL:2, NTSC:3)
F0_OLAP	19 - 16	0x0	R/W	Overlap of the SAV and EAV codes from field 0 to field 1. (PAL:2, NTSC:2)
F0_HEIGHT	15 - 00	0x0	R/W	Field 0 height (PAL:312, NTSC:262)

27.3.8 VOC_HSYNC_CTRL (0x00000030)

This register controls the HSYNC output signal behavior.

Table 360. HSYNC output signal behavior

Name	Bit	Default	R/W	Description
POLARITY	31	0x0	R/W	HSYNC polarity. 1’b0: Active high. 1’b1: Active low
-	30 - 24	0x0	-	Reserved
DELAY_END	23 - 12	0x0	R/W	HSYNC end point delay cycle.
DELAY_START	11 - 00	0X0	R/W	HSYNC start point delay cycle.

27.3.9 VOC_VSYNC_CTRL (0x00000034)

This register controls the VSYNC output signal behavior.

Table 361. VSYNC output signal behavior

Name	Bit	Default	R/W	Description
POLARITY	31	0x0	R/W	VSYNC polarity. 1’b0: Active high. 1’b1: Active low
-	30 - 24	0x0	-	Reserved
DELAY_END	23 - 12	0x0	R/W	VSYNC end point delay cycle.
DELAY_START	11 - 00	0X0	R/W	VSYNC start point delay cycle.

27.3.10 VOC_SBC_CTRL (0x00000038)

This register specifies saturation, brightness and contrast adjustments.

Table 362. Saturation, brightness and contrast adjustments

Name	Bit	Default	R/W	Description
-	31 - 25	0x0	-	Reserved
SATURATION	24-16	0x80	R/W	The saturation control on the output chrominance. (0~511, 128: off)
BRIGHTNESS	15-08	0x0	R/W	The brightness control on the output luminance (-128~127, 0:off)
CONTRAST	07-00	0X0	R/W	The contrast control on the output luminance. (-128~127, 0:off)

27.3.11 VOC_YCBCR2RGB_COEFF_0 (0x000003C)

YCbCr to RGB conversion matrix:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} COEFF0 & 0 & COEFF1 \\ COEFF2 & -COEFF3 & -COEFF4 \\ COEFF5 & COEFF6 & 0 \end{bmatrix} \begin{bmatrix} Y - Y\_OFFSET \\ Cb - CB\_OFFSET \\ Cr - CR\_OFFSET \end{bmatrix} \Big/ 256$$

This register configures the coefficients for RGB to YCbCr conversion matrix.

Table 363. YCbCr to RGB conversion matrix

Name	Bit	Default	R/W	Description
-	31	0x0	-	Reserved
COEFF2	29 - 20	0x12A	R/W	Coefficient 2
COEFF1	19 - 10	0x199	R/W	Coefficient 1
COEFF0	09 - 00	0x12A	R/W	Coefficient 0

27.3.12 VOC_YCBCR2RGB_COEFF_1 (0x00000040)

This register configures the coefficients for RGB to YCbCr conversion matrix.

Table 364. RGB to YCbCr conversion

Name	Bit	Default	R/W	Description
-	31 - 30	0x0	-	Reserved
COEFF5	29 - 20	0x12A	R/W	Coefficient 5
COEFF4	19 - 10	0x0D0	R/W	Coefficient 4
COEFF3	09 - 00	0x064	R/W	Coefficient 3

27.3.13 VOC_YCBCR2RGB_COEFF_2 (0x00000044)

This register configures the coefficients for RGB to YCbCr conversion matrix.

Table 365. Configure coefficient for RGB to YCbCr conversion matrix

Name	Bit	Default	R/W	Description
CR_OFFSET	31 - 24	0x80	R/W	Offset for Cr
CB_OFFSET	23 - 16	0x80	R/W	Offset for Cb.
Y_OFFSET	15 - 10	0x10	R/W	Offset for Y
COEFF6	09 - 00	0x204	R/W	Coefficient 6

27.4 Output Format

Figure 54 shows the timing diagram of 8-bit YCbCr 4:2:2 with separate SYNC signals and the BT.656 interface. These two formats will be output at the same time. The 8-bit data port could be output from different byte lanes depending on the register OUTPIN_SEL. Both progressive and interlaced formats are supported. Each VSYNC contains one field when the output is interlaced.

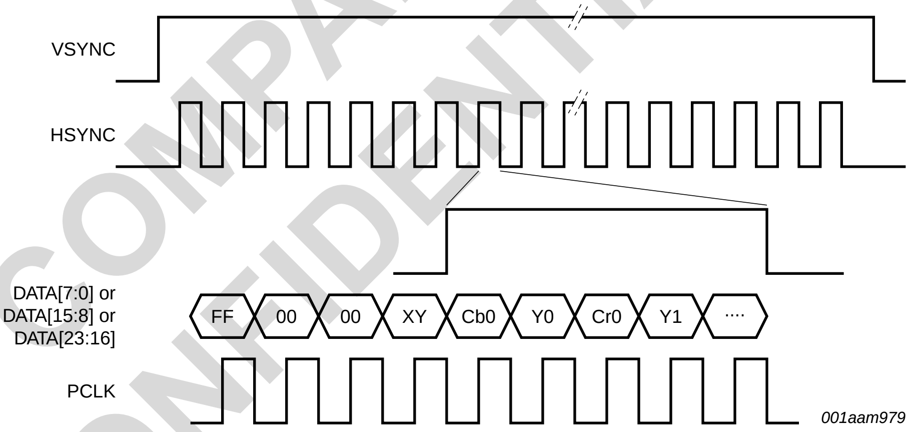

Fig 54. Timing Diagram of 8-bit YCbCr 4.2.2 with separate SYNC signals and BT.656 interface

Figure 55 shows the timing diagram of 16-bit YCbCr 4:2:2 with separate SYNC signals and BT.1120 interface. These two formats will be output at the same time. The 16-bit data port could be output from different byte lanes depending on the register OUTPIN_SEL. Only progressive format is supported

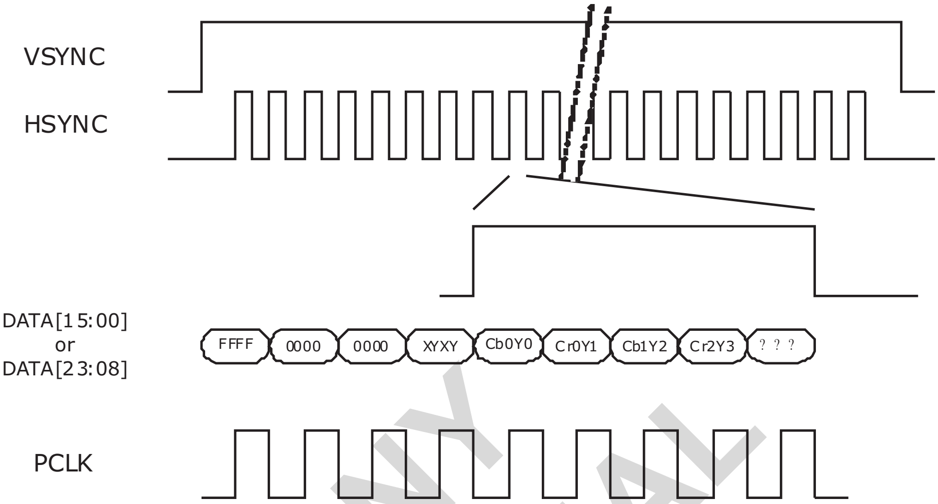

Fig 55. Timing diagram of 16-bit YCbCr 4:2:2 with separate SYNC signals and BT.1120 interface

Figure 56 shows the timing diagram of 24-bit RGB interface. It could be used to connect with the LCD module, HDMI transmitters and DAC for VGA format

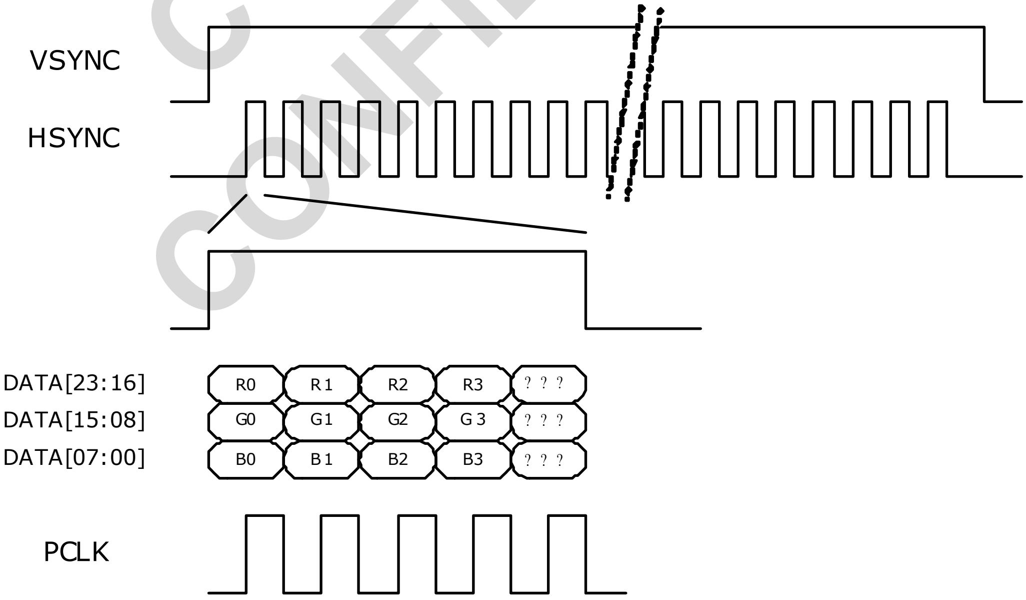

Fig 56. Timing Diagram of 24-bit RGB Parallel Interface.

28. AHB-to-APB Bridge and DMA Controller

28.1 Features

This controller provides an AHB-to-APB bridge and a DMA engine to transfer between AHB and APB buses. The bridge is the only master on the APB bus. The DMA engine is mainly used to transfer data from main memory to a device or vice versa without the host processor's intervention. There is a two-level priority in the DMA arbitration. For DMA operations in the same priority, round-robin arbitration is used. The following list comprises the various features supported:

- up to 16-channel APB DMA operations. Each channel operates independently.
- up to 15 peripheral DMA request/grant ports.
- 4 directions: APB-to-APB, APB-to-AHB, AHB-to-APB, and AHB-to-AHB DMA operations.
- 2D scatter DMA with the linked list. Internal MMR will be updated automatically.
- 8-/16-/32-/64-bit transfers.
- single, burst 4, burst 8 and burst 16 transfers.
- increment and decrement DMA addressing.

28.2 Memory Map Register

28.2.1 APBC_SLAVE_n_BASESIZE (0x00000000+n*4)

Slave configuration register (n=0~31).

Table 366. Slave configuration register

Name	Bit	Default	R/W	Description
BASE_ADDR_n	31 - 20	-	R/W	Slave n base address [31:20].
-	19 - 00	0X0	-	Reserved

28.2.2 APBC_VERSION (0x00000080)

Version information register.

Table 367. Version information register

Name	Bit	Default	R/W	Description
MAJOR_VERSION	31 - 24	0x06	R	Major version number
MINOR_VERSION	23 - 16	0x00	R	Minor version number
BUILD_VERSION	15 - 08	0x00	R	Build version number
REVISION	07 - 00	0x06	R	Revision number

28.2.3 APBC_DMA_PRIORITY (0x00000084)

DMA priority level register.

Table 368. DMA Priority level register

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	-	Reserved
PRIORITY_LEVEL	15 - 00	0x0	R/W	Bits 0 - 15 represent channel 0 - 15 priorities. Round-robin arbitration is used for requests in the same priority. 1’b0: Lower level. 1’b1: Higher level

28.2.4 Reserved (0x00000088)

28.2.5 APBC_DMA_CHN_MONITER(0x0000008c)

DMA channel monitor register.

Table 369. DMA channel mon iter register

Name	Bit	Default	R/W	Description
-	31 - 16	0x0	-	Reserved
CHN_MONITER	15 - 00	0x0	R/W	Bits 0 - 15 represent channel 0 - 15 statuses. It shows the channel which activated the interrupt signal and won’t be set to 0 until the software set it to 0.

28.2.6 APBC_DMA_n_SRC_ADDR (0x00000090+n*16)

Source address for DMA channel n (n = 0~15).

Table 370. Source address for DMA channel n

Name	Bit	Default	R/W	Description
SRC_ADDR_n	31 - 00	0x0	R/W	The source address for the current DMA cycle can be read from this register

28.2.7 APBC_DMA_n_DES_ADDR (0x00000094+n*16)

Destination address for DMA channel n (n = 0~15).

Table 371. Destination address for DMA channel n

Name	Bit	Default	R/W	Description
DES_ADDR_n	31 - 00	0x00	R/W	The destination address of the current DMA cycle can be read from this register.

28.2.8 APBC_DMA_n_LLP (0x00000098+n*16)

Linked list description pointer address (n = 0~15).

Table 372. Linked list description point address

Name	Bit	Default	R/W	Description
ADDR_LLP_n	31 - 00	0x0	R/W	Linked list description pointer address. Scatter DMA require this pointer to locate the command of the subsequent DMA transfer and trigger AHB master to acquire the info. Zero pointer address means no further DMA is requested. Following diagrams illustrates the data structure of linked list description

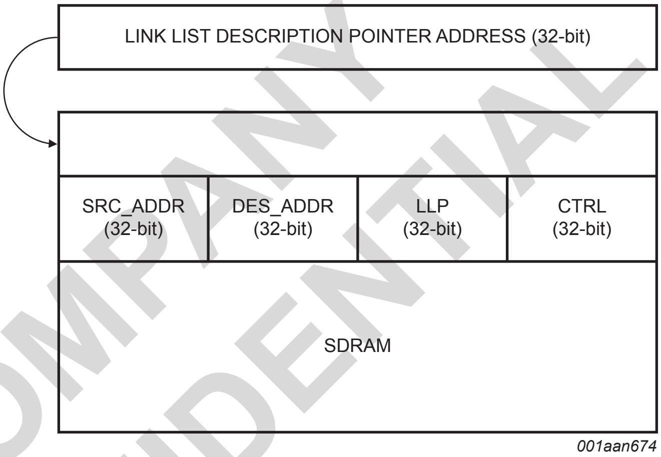

Fig 57. Data structure of linked list description

28.2.9 APBC_DMA_n_CTRL (0x0000009c+n*16)

Basic control register (n = 0~15).

Table 373. Basic control register n

Name	Bit	Default	R/W	Description
CYC_n	31 - 20	0x0	R/W	A DMA cycle consist of 1/4/8/16-beat bus data transfer cycles, depending on BURST_MODE_n in the DMA channel command register.
DATA_SZ_n	19 - 18	0x0	R/W	Data width of transfer. 00: 8-bit, byte. 01: 16-bit, half-word. 10: 32-bit, word. If you use the data size, the burst length could not be set to exceed 8 in one cycle. 11: 64-bit, double-word. If you use the data size, the burst length could not be set to exceed 4 in one cycle.
BYTE_SWAP_OPTION_n	17	0x0	R/W	Byte swap option for 16-bit and 32-bit data widths. 0: NO SWAP. Do not change the byte order of the transferred data. 1: Use SWAP. Swap the byte order of the transferred data

Table 373. Basic control register n *…continued*

<table>
<tr><th>Name</th><th>Bit</th><th>Default</th><th>R/W</th><th colspan="5">Description</th></tr>
<tr><td>REQ_TYPE_n</td><td>16</td><td>0x0</td><td>R/W</td><td colspan="5">DMA transfer type corresponding to one DMA request. When REQ_SEL_n is zero, this parameter would be ignored and proceed DMA as REQ_TYPE_n is assigned zero.
0: cease DMA transfer and assert DMA GRANT signal after the CYC_n is reduced as zero.
1: cease DMA transfer and assert DMA GRANT signal after the CYC_n is reduced by one</td></tr>
<tr><td>REQ_SEL_n</td><td>15 - 12</td><td>0x0</td><td>R/W</td><td colspan="5">Request signal select for DMA mode.
0000: No request / grant signal.
0001~1111 (1~15): request / grant signal multiplexer select.</td></tr>
<tr><td>DES_ADDR_INC_n</td><td>11 - 10</td><td>0x0</td><td>R/W</td><td colspan="5">Destination address incremental style.
00: No increment.
01: Positive increment.
10: Negative increment.
11: Reserved.
Refer SRC_ADDR_INC to understand the actual number of address increment.</td></tr>
<tr><td rowspan="8">SRC_ADDR_INC_n</td><td rowspan="8">09 - 08</td><td rowspan="8">0x0</td><td rowspan="8">R/W</td><td colspan="5">Source address incremental style.
00: No increment.
01: Positive increment.</td></tr>
<tr><td>BURST_MODE</td><td>Byte</td><td>Half-word</td><td>Word</td><td>Double-word</td></tr>
<tr><td>0</td><td>+1</td><td>+2</td><td>+4</td><td>+8</td></tr>
<tr><td>1</td><td>+4</td><td>+8</td><td>+16</td><td>+32</td></tr>
<tr><td>2</td><td>+8</td><td>+16</td><td>+32</td><td>+64</td></tr>
<tr><td>3</td><td>+16</td><td>+32</td><td>+64</td><td>+128</td></tr>
<tr><td colspan="5">10: Negative increment</td></tr>
<tr><td colspan="5">11: Reserved</td></tr>
<tr><td>TRANS_TYPE_n</td><td>07 - 06</td><td>0x0</td><td>R/W</td><td colspan="5">Transfer type.
00: AHB2AHB.
01: AHB2APB.
10: APB2AHB.
11: APB2APB.</td></tr>
<tr><td>BURST_MODE_n</td><td>05 - 04</td><td>0x0</td><td>R/W</td><td colspan="5">Burst mode.
00: SINGLE
01: INCR burst type with length 4
10: INCR burst type with length 8
11: INCR burst type with length 16</td></tr>
<tr><td>INTR_LL_EN_n</td><td>03</td><td>0x0</td><td>R/W</td><td colspan="5">Enable (1) / Disable (0) link-list update interrupt flag. When link-list is updated from AHB SDRAM, 4-clk edge-style interrupt will be asserted. This interrupt can be used to notify individual continuous memory DMA is completed.</td></tr>
</table>

Table 373. Basic control register n *…continued*

Name	Bit	Default	R/W	Description
INTR_CMPT_EN_n	02	0x0	R/W	Enable (1) / Disable (0) DMA completion interrupt flag.
INTR_CMPT_n	01	0x0	R/W	DMA completion interrupt flag. 0: No interrupt occurs. 1: Interrupt occurs, write 0 to clear flag.
OP_EN_n	00	0x0	R/W	Enable / Disable APBC 0: Disable or stop the DMA channel. 1: Enable or start the DMA channel. If the transfer doesn't require DMA request to trigger, the assertion of this bit will start the transfer.

28.3 APB DMA Operation

28.3.1 DMA Port

The DMA port is hard coded and REQ_SEL_n must be filled according to Table 374. There are two type of devices could benefit from the DMA operation, SSIC and I2SSC 0~4. REQ_TYPE_n must be 1 for both devices.REQ_TYPE_n must be 1 for both devices.

Table 374. DMA Port

DMA Port	DMA Operation
0	-
1	-
2	SSIC RX DMA
3	SSIC TX DMA
4	-
5	-
6	I2SSC 0 RX DMA
7	I2SSC 0 TX DMA
8	I2SSC 1 RX DMA
9	-
10	I2SSC 2 RX DMA
11	-
12	I2SSC 3 RX DMA
13	-
14	I2SSC 4 RX DMA
15	-

28.3.2 Programming

1. Prepare the linked list in the main memory. The format is the same as the DMA MMR including SRC_ADDR, DES_ADDR, LLP, and CTRL. If LLP is equal to 0x00000000, it means the end of the linked list. The first entry has to be filled in the MMR directly.
2. For a SSIC TX transfer using DMA channel 0 with 16384 bytes separated in 4 linked list pointers:

   Specify the first LLP in the MMR

   a. 0xC8000090 (SRC_ADDR) = 0x01000000 (physical memory base address for TX data)

   b. 0xC8000094 (DES_ADDR) = 0x40800060 (DR register in SSIC)

   c. 0xC8000098 (LLP) = 0x00100000 (next LLP in the main memory)

   d. 0xC800009C (CTRL) = 0x20073145 (16-bit data width, byte swap enable, DMA port 3 from Table 374, AHB-to-APB, burst length 4, only one interrupt after four LLPs are done)

   Specify the second LLP in the main memory address, 0x00100000

   a. 0x00100000 (SRC_ADDR) = 0x01001000

   b. 0x00100004 (DES_ADDR) = 0x40800060

   c. 0x00100008 (LLP) = 0x00100004

   d. 0x0010000C (CTRL) = 0x20073145

   Specify the third LLP in the main memory address, 0x00100004

   a. 0x00100000 (SRC_ADDR) = 0x01002000

   b. 0x00100004 (DES_ADDR) = 0x40800060

   c. 0x00100008 (LLP) = 0x00100008

   d. 0x0010000C (CTRL) = 0x20073145

   Specify the fourth LLP in the main memory address, 0x00100008

   a. 0x00100000 (SRC_ADDR) = 0x01003000

   b. 0x00100004 (DES_ADDR) = 0x40800060

   c. 0x00100008 (LLP) = 0x00000000 (the last LLP)

   d. 0x0010000C (CTRL) = 0x20073145
3. Configure the peripheral device like SSIC or I2SSC 0~4 to start DMA operations. The DMA operation starts when the hard coded DMA TX or RX request of the peripheral device is asserted.

29. Limiting values

Table 375. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions[7]		Min	Max	Unit
T_{case}	Case temperature	-	[1]	0	85	°C
$V_{DD(C)(1v0)}$	Core power supply	on pin VDDC_1_0	[2] [3]	0.975	1.025	V
$V_{DD(C\_DDR32SDMC\_IO\_PHY)(1v0)}$	DDR-II/III PHY core power supply	on pin DDR32SDMC_IO_PHY_PWR_VDDC_1_0				
$V_{DDA(PCIEC\_I\_PHY)(1v0)}$	PCI Express PHY low-voltage power supply	on pin PCIEC_I_PHY_PWR_VDDA_1_0				
$V_{DD(C\_USBC\_IO\_PHY)(1v0)}$	USBPHY digital power supply	On pin USBC_IO_PHY_PWR_VDDC_1_0				
$V_{DD(IO)(3v3)}$	input/output supply voltage (3.3 V)	on pin VDDIO_3_3		3.135	3.465	V
$V_{DD(IO)(3v3)}$	I/O power supply for GMII	on pin VDDIO_2_5_3_3				
$V_{DDA(USBC\_IO\_PHY)(3v3)}$	USBPHY analog power supply	on pin USBC_IO_PHY_PWR_VDDA_3_3				
$V_{DD(IO)(3v3)}$	I/O power supply for RGMII	on pin VDDIO_2_5_3_3		2.375	2.625	V
$V_{DDA(DDR32SDMC\_IO\_PHY)(2v5)}$	DDR-II/III PHY PLL power supply	on pin DDR32SDMC_IO_PHY_PWR_VDDA_2_5				
$V_{DDA(PCIEC\_I\_PHY)(2v5)}$	PCI Express PHY high-voltage power supply.	on pin PCIEC_I_PHY_PWR_VDDA_2_5				
$V_{DDA(PLLC\_I\_PLL0)(2v5)}$	PLL0 analog power supply	on pin PLLC_I_PLL_0_PWR_VDDA_2_5				
$V_{DDA(PLLC\_I\_PLL1)(2v5)}$	PLL1 analog power supply	on pin PLLC_I_PLL_1_PWR_VDDA_2_5				
$V_{DDA(PLLC\_I\_PLL2)(2v5)}$	PLL2 analog power supply	on pin PLLC_I_PLL_2_PWR_VDDA_2_5				
$V_{DDA(PLLC\_I\_PLL3)(2v5)}$	PLL3 analog power supply	on pin PLLC_I_PLL_3_PWR_VDDA_2_5				
$V_{DDA(USBC\_IO\_PHY)(2v5)}$	USBPHY analog power supply	on pin USBC_IO_PHY_PWR_VDDA_2_5				
$V_{DD(IO\_DDR32SDMC\_IO)(1v8)}$	DDR-II SDRAM I/O power supply (VDDQ).	on pin DDR32SDMC_IO_PWR_VDDIO_1_8		1.71	1.89	V
	DDR-III SDRAM I/O power supply (VDDQ)			1.425	1.575	V
$V_{REF(DDR32SDMC\_IO)(0v9)}$	DDR-II/III SDRAM reference power supply (VREF).	on pin DDR32SDMC_IO_PWR_VREF_0_9		0.49* VDDQ	0.51* VDDQ	V
VTT	External termination voltage			VREF-0.04	VREF +0.04	V

Table 375. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions[7]		Min	Max	Unit
$V_{SS(C)(1v0)}$	Core ground supply	on pin VSSC_1_0		0	0	V
$V_{SS(IO)(3v3)}$	I/O ground supply	on pin VSSIO_2_5_3_3				
$V_{SSA(DDR32SDMC\_IO\_PHY)(2v5)}$	DDR-II/III PHY PLL ground supply	on pin DDR32SDMC_IO_PHY_PWR_VSSA_2_5				
$V_{SS(C\_DDR32SDMC\_IO\_PHY)(1v0)}$	DDR-II/III PHY core ground supply	on pin DDR32SDMC_IO_PHY_PWR_VSSC_1_0				
$V_{SSA(PCIEC\_I\_PHY)(1v0, 2v5)}$	PCI Express PHY ground supply	on pin PCIEC_I_PHY_PWR_VSSA_1_0_2_5				
$V_{SS(C\_USBC\_IO\_PHY)(1v0)}$	USBPHY digital ground supply	on pin USBC_IO_PHY_PWR_VSSC_1_0				
$V_{SSA(USBC\_IO\_PHY)(1v0, 2v5)}$	USBPHY analog ground supply	on pin USBC_IO_PHY_PWR_VSSA_2_5_3_3				
$V_{SSA(PLLC\_I\_PLL0)(2v5)}$	PLL0 analog ground supply.	on pin PLLC_I_PLL_0_PWR_VSSA_2_5				
$V_{SSA(PLLC\_I\_PLL1)(2v5)}$	PLL1 analog ground supply.	on pin PLLC_I_PLL_1_PWR_VSSA_2_5				
$V_{SSA(PLLC\_I\_PLL2)(2v5)}$	PLL2 analog ground supply.	on pin PLLC_I_PLL_2_PWR_VSSA_2_5				
$V_{SSA(PLLC\_I\_PLL3)(2v5)}$	PLL3 analog ground supply.	on pin PLLC_I_PLL_3PWR_VSSA_2_5				
	Operating temperature		[1]	0	85	°C
V_{ESD}	Electrostatic discharge voltage	human body model; all pins for ASC8848/49/50 M1 version		-1000	+1000	V
		human body model; all pins for ASC8848/49/50 M2 version and ASC8851		-2000	+2000	
VDDIO_SENSOR	Sensor I/O power supply	if sensor is not operating at 3.3V and level shifters are skipped	[4]	3.135	3.465	V
				2.85	3.15	
				2.66	2.94	
				2.375	2.625	
				1.71	1.89	

[1] Operating temperature is the case surface temperature

[2] For lot numbers smaller than 1037(e.g., 1036, 1030) these voltages should be 1.025(min), 1.050(typ), 1.075(max)

[3] For ASC8848/49/50 M2 version ASC8851 the min and max voltages are 0.95V and 1.05V respectively

[4] Applicable for ASC8848/49/50 M2 version and ASC8851 only

30. Recommended operating conditions

Table 376. Operating conditions [1][2][3][4]

Symbol	Parameter	Conditions[7]		Min	Typ	Max	Unit
T_{case}	Case temperature[5]		[1]	0		85	^{0}C
$V_{DD(C)(1v0)}$	Core power supply	on pin VDDC_1_0	[6][8]	0.975	1.000	1.025	V
$V_{DD(C\_DDR32SDMC\_IO\_PHY)(1v0)}$	DDR-II/III PHY core power supply	on pin DDR32SDMC_IO_PHY_PWR_VDDC_1_0					
$V_{DDA(PCIEC\_I\_PHY)(1v0)}$	PCI Express PHY low-voltage power supply	on pin PCIEC_I_PHY_PWR_VDDA_1_0					
$V_{DD(C\_USBC\_IO\_PHY)(1v0)}$	USBPHY digital power supply	On pin USBC_IO_PHY_PWR_VDDC_1_0					
$V_{DD(IO)(3v3)}$	input/output supply voltage (3.3 V)	on pin VDDIO_3_3		3.135	3.3	3.465	V
$V_{DD(IO)(3v3)}$	I/O power supply for GMII	on pin VDDIO_2_5_3_3					
$V_{DDA(USBC\_IO\_PHY)(3v3)}$	USBPHY analog power supply	on pin USBC_IO_PHY_PWR_VDDA_3_3					
$V_{DD(IO)(3v3)}$	I/O power supply for RGMII	on pin VDDIO_2_5_3_3		2.375	2.5	2.625	V
$V_{DDA(DDR32SDMC\_IO\_PHY)(2v5)}$	DDR-II/III PHY PLL power supply	on pin DDR32SDMC_IO_PHY_PWR_VDDA_2_5					
$V_{DDA(PCIEC\_I\_PHY)(2v5)}$	PCI Express PHY high-voltage power supply.	on pin PCIEC_I_PHY_PWR_VDDA_2_5					
$V_{DDA(PLLC\_I\_PLL0)(2v5)}$	PLL0 analog power supply	on pin PLLC_I_PLL_0_PWR_VDDA_2_5					
$V_{DDA(PLLC\_I\_PLL1)(2v5)}$	PLL1 analog power supply	on pin PLLC_I_PLL_1_PWR_VDDA_2_5					
$V_{DDA(PLLC\_I\_PLL2)(2v5)}$	PLL2 analog power supply	on pin PLLC_I_PLL_2_PWR_VDDA_2_5					
$V_{DDA(PLLC\_I\_PLL3)(2v5)}$	PLL3 analog power supply	on pin PLLC_I_PLL_3_PWR_VDDA_2_5					
$V_{DDA(USBC\_IO\_PHY)(2v5)}$	USBPHY analog power supply	on pin USBC_IO_PHY_PWR_VDDA_2_5		2.375	2.5	2.625	V
$V_{DD(IO\_DDR32SDMC\_IO)(1v8)}$	DDR-II SDRAM I/O power supply (VDDQ)	on pin DDR32SDMC_IO_PWR_VDDIO_1_8		1.71	1.8	1.89	V
	DDR-III SDRAM I/O power supply (VDDQ)			1.427	1.5	1.575	
$V_{REF(DDR32SDMC\_IO)(0v9)}$	DDR-II/III SDRAM reference power supply (VREF).	on pin DDR32SDMC_IO_PWR_VREF_0_9		0.49* VDDQ	0.5* VDDQ	0.51* VDDQ	V
V_{TT}	External termination voltage			VREF -0.04	VREF	VREF +0.04	V
VDDIO_SENSOR		Sensor I/O power supply		3.135	3.3	3.465	

Table 376. Operating conditions *…continued*[1][2][3][4]

Symbol	Parameter	Conditions[7]	Min	Typ	Max	Unit
			2.85	3.0	3.15	
			2.66	2.8	2.94	
			2.375	2.5	2.625	
			1.71	1.8	1.89	
$V_{SS(C)(1v0)}$	Core ground supply	on pin VSSC_1_0	0	0	0	V
$V_{SS(IO)(3v3)}$	I/O ground supply	on pin VSSIO_2_5_3_3				
$V_{SSA(DDR32SDMC\_IO\_PHY)(2v5)}$	DDR-II/III PHY PLL ground supply	on pin DDR32SDMC_IO_PHY_PWR_VSSA_2_5				
$V_{SS(C\_DDR32SDMC\_IO\_PHY)(1v0)}$	DDR-II/III PHY core ground supply	on pin DDR32SDMC_IO_PHY_PWR_VSSC_1_0				
$V_{SS(IO\_DDR32SDMC\_IO)(1v8)}$	DDR-II/III SDRAM I/O ground supply	on pin DDR32SDMC_IO_PWR_VSSIO_1_8				
$V_{SSA(PCIEC\_I\_PHY)(1v0, 2v5)}$	PCI Express PHY ground supply	on pin PCIEC_I_PHY_PWR_VSSA_1_0_2_5				
$V_{SS(C\_USBC\_IO\_PHY)(1v0)}$	USBPHY digital ground supply	on pin USBC_IO_PHY_PWR_VSSC_1_0				
$V_{SSA(USBC\_IO\_PHY)(1v0, 2v5)}$	USBPHY analog ground supply	on pin USBC_IO_PHY_PWR_VSSA_2_5_3_3				
$V_{SSA(PLLC\_I\_PLL0)(2v5)}$	PLL0 analog ground supply.	on pin PLLC_I_PLL_0_PWR_VSSA_2_5				
$V_{SSA(PLLC\_I\_PLL1)(2v5)}$	PLL1 analog ground supply.	on pin PLLC_I_PLL_1_PWR_VSSA_2_5	0	0	0	V
$V_{SSA(PLLC\_I\_PLL2)(2v5)}$	PLL2 analog ground supply.	on pin PLLC_I_PLL_2_PWR_VSSA_2_5				
$V_{SSA(PLLC\_I\_PLL3)(2v5)}$	PLL3 analog ground supply.	on pin PLLC_I_PLL_3_PWR_VSSA_2_5				
		Operating temperature	0		85	°C

[1] The power supply values specified in Table 378 are DC design criteria only. They represent the DC supply limits at the devices internal to the design, including the effects of internal IR drop.

[2] VREF of the receiving device(s) should track the variations in the DC value of VDDQ of the sending device for best noise margins. The value of VREF is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

[3] Peak-to-peak noise on VREF may not exceed 5 % VREF (DC).

[4] Power-up sequence for ASC8848/49/50/51 is V1.0 -> V1.8 -> V2.5 -> V3.3 and power-down sequence is VDD3.3 -> VDD2.5 -> VDD1.8 -> VDD1.0. Please refer to hardware application note for details.

[5] Operating temperature is the case surface temperature

[6] For lot numbers smaller than 1037(e.g., 1036, 1030) these voltages should be 1.025(min), 1.050(typ), 1.075(max)

[7] Applicable for ASC8848/49/50 M2 version and ASC8851 only

[8] For ASC8848/49/50 M2 version ASC8851 the min and max voltages are 0.95V and 1.05V respectively

31. Characteristics

Table 377. Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-free air	20.9	°C/W
θ_{JB}	Junction-to-board	15.0	°C/W
θ_{JC}	Junction-to-case	4.2	°C/W
Psi_{JT}	Junction-to-package top	13.5	°C/W

The simulation environment for the thermal information is as follows.

- PCB layers: 6 Layers
- Ambient temperature: 90 °C
- Substrate: 4 Layers (1/2/1)
- Maximum junction temperature: 125 °C
- The air flow of θ_{JA} is 0 m/s.

31.1 DC/AC I/O characteristics

31.1.1 DDR-II interface for ASC8848/49/50 M1 version

Table 378. DDR-II I/O DC Characteristics

Symbol	Parameter	Min	Type	Max	Units
V_{IHT}	DC input logic threshold high	-	-	VREF + 0.025	V
V_{ILT}	DC input logic threshold low	VREF-0.025	-	-	V
V_{IH}	DC input voltage high	-	-	VD33 + 0.3	V
V_{IL}	DC input voltage low	–0.3	-	-	V
V_{OH}	DC output voltage high	VDDQ-0.3	-	-	V
V_{OL}	DC output voltage low	-	-	0.3	V
R_{TT1}	RTT effective impedance value	–30 %	–50	+41 %	ohm
R_{TT2}	RTT effective impedance value	–42 %	75	+41 %	ohm
R_{TT3}	RTT effective impedance value	–42 %	150	+41 %	ohm
R_{serdrv}	Series output resistance	–10 %	34	+10 %	ohm

Table 379. DDR-II I/O AC Characteristics

Symbol	Parameter	Min	Type	Max	Units
t_{PDRV}	Output delay	0.41	-	0.86	ns
$t_{RISE/FALL}$	Output driver slew rate 30 % - 70 %	40	-	200	ps
t_{PVZ}	Output tri-state delay - valid data to high Z	0.43	-	0.82	ns
t_{PVZ}	Output tri-state delay - high Z to valid data	0.47	-	0.74	ns
t_{RCV}	Input delay	0.30	-	0.50	ns
t_{ipwd}	Input pulse width distortion	-	-	35	ps

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Table 379. DDR-II I/O AC Characteristics *…continued*

Symbol	Parameter	Min	Type	Max	Units
t_{opwd}	Output pulse width distortion	-	-	35	ps
F_{MAX}	Maximum operating frequency	-	-	400	MHz
D_{MAX}	Maximum operating data rate	-	-	800	Mb/s

[1] The values given are for the ASC8850/51 only, for further details please refer to Table 2

The following tables show DDR-II I/O AC and DC characteristics.

31.1.2 DDR-II interface for M2 version of ASC8848/8849/8850 and ASC8851

Table 380. DDR-II I/O DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
DC input voltage high	$V_{IH(DC)}$	VREF+0.125	--	VDDQ+0.3	V
DC input voltage low	$V_{IL(DC)}$	VSSQ-0.3	--	VREF-0.125	V
DC output voltage high	V_{OH}	VDDQ-0.28	--	--	V
DC output voltage low	V_{OL}	--	--	VSSQ+0.28	V
Input termination resistance (ODT) to VDDQ/2	R_{TT1}	120	150	180	ohm
		60	75	90	ohm
		40	50	60	ohm

Table 381. DDR-II I/O AC characteristics

Parameter	Symbol	Min	Typ	Max	Units
Output delay	t_{PDRV}	0.54	0.72	1.1	ns
Output driver slew rate (at SDRAM pin)	SR	3.07	3.5	4.02	V/ns
Output tri-state delay - valid data to highZ	t_{PVZ}	0.57	0.74	1.12	ns
Output tri-state delay - highZ to valid data	t_{PZV}	0.53	0.72	1.12	ns
Input delay	t_{PRCV}	0.25	0.34	0.5	ns
Maximum operating frequency (ASC8851/50/49/48 M2)	F_{MAX}	--	--	400/400/300/266	MHz
Maximum operating data rate (ASC8851/50/49/48 M2)	D_{MAX}	--	--	800/800/600/533	Mb/s
Input mode AC power (VDDQ rail)	P_{RCV}	0.7	0.8	0.93	uW/MHz

Table 381. DDR-II I/O AC characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input mode AC power (VDD rail)	P_{RCV}	0.12	0.14	0.17	uW/MHz
Output mode AC power (VDDQ rail)	P_{DRV}	14.87	15.72	17.81	uW/MHz
Output mode AC power (VDD rail)	P_{DRV}	0.36	0.44	0.54	uW/MHz

31.1.3 DDR-III for M2 version of ASC8848/8849/8850 and ASC8851

The following tables show DDR-III I/O AC and DC characteristics

Table 382. DDR-III I/O DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
DC input voltage high	$V_{IH(DC)}$	VREF+0.100	--	VDDQ	V
DC input voltage low	$V_{IL(DC)}$	VSSQ-0.3	--	VREF-0.100	V
DC output voltage high	V_{OH}	0.8^{VDDQ}	--	--	V
DC output voltage low	V_{OL}	--	--	0.2^{VSSQ}	V
Input termination resistance (ODT) to VDDQ/2	R_{TT1}	100	120	140	ohm
		54	60	66	ohm
		36	40	44	ohm

Table 383. DDR-III I/O AC characteristics

Parameter	Symbol	Min	Typ	Max	Units
Output delay	tPDRV	0.62	0.82	1.3	ns
Output driver slew rate (at SDRAM pin)	SR	2.74	3.14	3.44	V/ns
Output tri-state delay - valid data to highZ	tPVZ	0.63	0.82	1.32	ns
Output tri-state delay - highZ to valid data	tPZV	0.6	0.82	1.3	ns
Input delay	tPRCV	0.3	0.4	0.61	ns
Maximum operating frequency (ASC8851/50/49 /48 M2)	FMAX	--	--	400/400/300/266	MHz
Maximum operating data rate (ASC8851/50/49/ 48 M2)	DMAX	--	--	800/800/600/533	Mb/s
Input mode AC power (VDDQ rail)	PRCV	0.49	0.59	0.75	uW/MHz

Table 383. DDR-III I/O AC characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input mode AC power (VDD rail)	PRCV	0.12	0.14	0.18	uW/MHz
Output mode AC power (VDDQ rail)	PDRV	7.38	8.08	9.18	uW/MHz
Output mode AC power (VDD rail)	PDRV	0.36	0.44	0.54	uW/MHz

31.1.4 USB

DP, DM and VBUS are 5V-tolerant I/Os and Table 384 shows the USB I/O operating condition.

Table 384. USB I/O operating condition

Pad Name	Min	Type	Max	Units
USBC_IO_PHY_VBUS	-	-	5.25	V
USBC_IO_PHY_DP	-	-	5.25	V
USBC_IO_PHY_DM	-	-	5.25	V

31.1.5 General I/Os

All 3.3V I/Os except for GMII/RGMII I/Os use the Table 385 for I/O characteristics, such as GPIO, MSHC, NFC, SSI, UART, VIC, VOC.

Table 385. General I/O characteristics

Parameter		Symbol	Min	Type	Max	Units
Input high level voltage		V_{IH}	0.7 * DVDD[1]	-	DVDD + 0.3	V
Input low level voltage		V_{IL}	DVSS[2]-0.3	-	0.3 * DVSS	V
Input hysteresis voltage		V_{HYS}	0.4	-	-	V
DVDD supply leakage current with VDD core power down (DVDD=1.98V, VDD=0V)		I_{ILPD}	-	-	0.5	µA
DVDD supply leakage current with VDD core power down (DVDD=3.60V, VDD=0V)					1	µA
IO High-Z state leakage current (DVDD=1.98V, VI=0~DVDD)		I_{ILZ}	-	-	0.5	µA
IO High-Z state leakage current (DVDD=3.60V, VI=0~DVDD)			-	-	1	µA
Pull-down current (DVDD=1.8V)		I_{PO}	26.24	53.53	99.91	µA
Pull-down current (DVDD=3V)			52.4	105.9	184.3	µA
Pull-up current (DVDD=1.8V)		I_{PU}	–74.23	–42.30	–23.35	µA
Pull-up current (DVDD=3V)			–115.2	–71.61	–42.58	µA
IO High-Z state leakage current		I_{ILZ}	-	-	1	µA
Output high level		V_{OH}	DVDD-0.4	-	-	V
Output low level		V_{OL}	-	-	0.4	V
High level output current (DVDD=1.8V) V_{OH} =DVDD-0.4	2 mA	I_{OH}	3.42	5.63	8.77	mA
	4 mA		6.84	11.25	17.54	mA
	8 mA		9.12	15.00	23.39	mA
	12 mA		12.6	20.4	32.3	mA

Table 385. General I/O characteristics

Parameter		Symbol	Min	Type	Max	Units
Low level output current (DVDD=1.8V) V_{OL} =0.4V	2 mA	I_{OL}	4.93	8.53	13.18	mA
	4 mA		7.39	12.79	19.77	mA
	8 mA		12.32	21.32	32.95	mA
	12 mA		14.79	25.58	39.54	mA
High level output current (DVDD=3.3V) V_{OH} =DVDD-0.4	2 mA	I_{OH}	4.30	6.35	8.94	mA
	4 mA		6.44	9.52	13.41	mA
	8 mA		10.74	15.87	22.35	mA
	12 mA		12.89	19.05	26.82	mA
Low level output current (DVDD=3.3V) V_{OL} =0.4V	2 mA	I_{OL}	9.16	13.86	18.47	mA
	4 mA		13.73	20.78	27.70	mA
	8 mA		22.84	34.62	46.15	mA
	12 mA		27.41	41.54	55.38	mA

[1] 1. DVDD is a symbol for VDDIO_SENSOR (VIC) or VDDIO_COMMON_3_3 (others).

[2] DVSS is a symbol for VSSIO_COMMON.

[3] It is recommended to use 1K ohm resistor to pull the signal to the opposite supply

31.1.6 GMII/RGMII

GMII/RGMII I/Os have two operating voltages, 2.5 V and 3.3 V. Table 386 shows the I/O characteristics.

Table 386. GMII/RGMII I/O Characteristics

Symbol	Parameter	Min	Type	Max	Units
V_{IH}	Input high level voltage (RGMII)	1.7	-	-	V
V_{IL}	Input low level voltage (RGMII)	-	-	0.7	V
V_{IH}	Input high level voltage (GMII)	1.7	-	-	V
V_{IL}	Input low level voltage (GMII)	-	-	0.9	V
V_{OH}	Output high level (RGMII)	2.0	-	DVDD[1] + 0.3	V
V_{OL}	Output low level (RGMII)	-0.3	-	0.4	V
V_{OH}	Output high level (GMII)	2.1	-	3.6	V
V_{OL}	Output low level (GMII)	0	-	0.5	V

[1] DVDD is a symbol for VDDIO_2_5_3_3.

31.1.7 OSC

The OSC I/O is designed to generate an asynchronous on-chip clock signal with an appropriate external oscillator crystal. Most crystal manufacturers recommend a 10 pF capacitor to ground from both the input and output pins of the OSC I/O for crystal stability. The design has been characterized to allow a variation of 4 pF to 18 pF on each pin.

Table 387. OSC I/O Characteristics[1]

Symbol	Parameter	Min	Type	Max	Units
V_{IH}	Input high level voltage	0.9* VDD[2]	-	VDD + 0.3	V
V_{IL}	Input low level voltage	VSS[3] - 0.3	-	0.3*VSS	V
VHYS	Input hysteresis voltage	0.4	-	-	V
IDDQ	Bypass (using the external oscillator)	-	-	1	µA

[1] When using an external oscillator on SYS_I_OSC_0_CLK, SYS_I_OSC_1_CLK, or SYS_I_OSC_2_CLK, the voltage level must not exceed VDDC_1_0.

[2] VDD is a symbol for VDDC_1_0

[3] VSS is a symbol for VSSC_1_0

31.1.8 PCIe

31.1.8.1 Reference clock

The reference clock signal is differential and supports frequencies of 25 MHz or 50 MHz to 156.25 MHz (100 MHz and 125 MHz are common frequencies). The 100 MHz reference clock specifications are defined in PCI ExpressTM card electromechanical specification.

Table 388. PCIe reference clock characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{high}	high voltage	600	710	850	mV
V_{low}	low voltage	–150	0	-	mV
V_{cross}	voltage absolute crossing point	250	-	550	mV
ΔV_{cross}	total variation of V_{cross}	-	-	140	mV
$T_{ccjitter}$	cycle-to-cycle jitter	-	-	125	ps
T_{duty}	duty cycle	45	-	55	%

31.1.8.2 Tx/Rx Characteristics

It meets or exceeds the electrical compliance requirements in the PCIe base specification.

Table 389. PCIe Tx characteristics

Symbol	Parameter	Min	Typ	Max	Units
$V_{TX\_DIFF\_PP}$	output voltage peak-to-peak differential amplitude	0.937	-	1.24	V
V_{CTM}	transmit common mode voltage	0.4	-	0.6	V
Z_D	differential output impedance	85	-	115	Ω

Table 390. PCIe Rx characteristics

Symbol	Parameter	Min	Typ	Max	Units
$V_{RX\_DIFF\_PP}$	input voltage peak-to-peak differential amplitude	175	-		mV
Z_{IN}	differential input impedance	85	-	115	Ω
PPM	tolerance	–350	-	350	ppm

31.2 Solder Reflow Profile

ASC8848/49/50/51 SoC is available in a Pb-free package. The reflow profile is shown below which follows IPC/JEDEC J-STD-020 D. The time between reflows shall be 8 minutes minimum and 60 minutes maximum. It shall be 8 minutes maximum from 25°C to the peak temperature

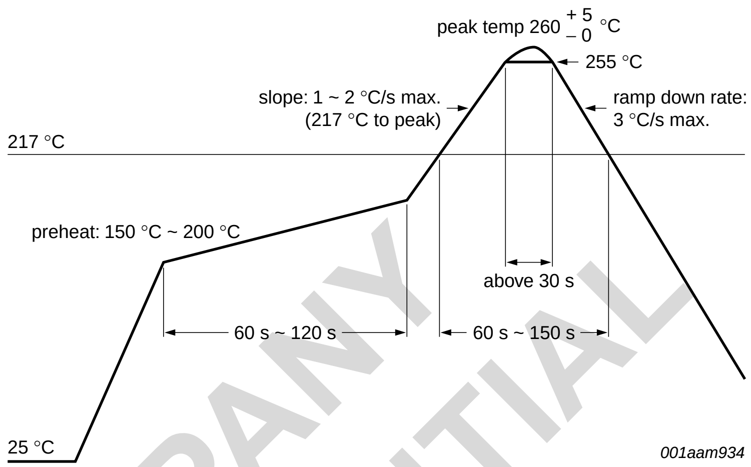
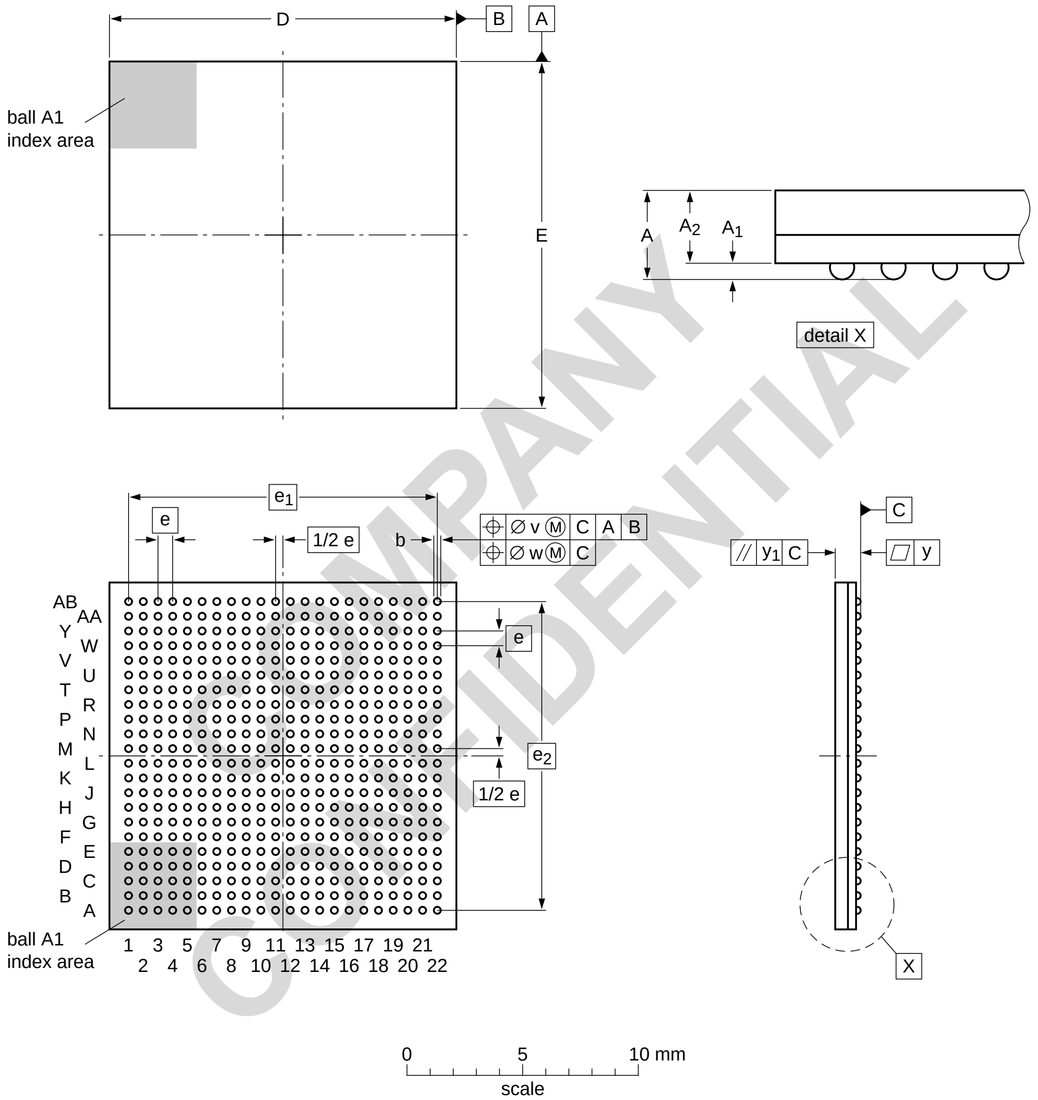


Fig 58. Reflow Profile

32. Package outline

Package description line **TFBGA484**



Dimensions

Unit[1]		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.2	0.26	0.94	0.35	15.1	15.1							
	nom		0.21	0.89	0.30	15.0	15.0	0.65	13.65	13.65	X	X	X	X
	min		0.16	0.84	0.25	14.9	14.9							

Note

1. xxxxxxx

tfbga484_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
TFBGA484						~~10-10-18~~ 11-02-01

Fig 59. ASC8848/49/50/51 SoC TFBGA-484 Package Physical Dimension

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33. Abbreviations

Table 391. Abbreviations

Acronym	Description
ADC	Analog-to-Digital converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
DAC	Digital-to-Analog Converter
DDR	Double Data Rate
DMA	Direct Memory Access
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MAC	Media Access Control
MII	Media Independent Interface
MPEG	Moving Picture Experts Group
MSHC	Memory Stick Host Controller
n.c.	not connected
RGMII	Reduced Gigabit Media Independent Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
SDRAM	Synchronous Dynamic Random Access Memory
SoC	System on Chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

34. References

[1] HDMI_Nand_Flash_App_Note.pdf

[2] Thermal Management for ASC8850.pdf

[3] ASC8850_M1_to_M2_migration_guide_v1.2.pdf

35. Revision history

Table 392. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ASC8848_49_50_M1 M2	24-09-2011	Preliminary Draft	Details on ASC8851 and ASC8848/49/50 M2 such as register settings, interfaces, pin-outs, ball map are provided. Fig. 3 updated for A13 and B13 pins Ball map for Pin V13 has been updated in Fig 5	ASC8848_49_50_51

36. Legal information

36.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

36.2 Definitions

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37. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section ‘Legal information’.

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