

# RJF0605JPD

## Silicon N Channel MOS FET Series Power Switching

R07DS0579EJ0300  
Rev.3.00  
Apr 13, 2012

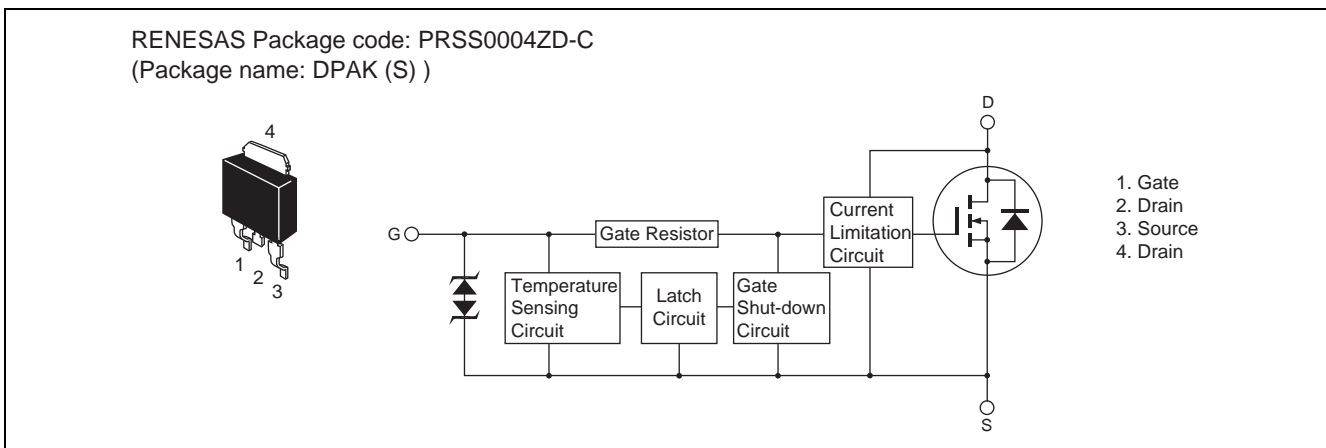
### Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

### Features

- Logic level operation (4 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101 Compliant

### Outline



### Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	16	V
Gate to source voltage	$V_{GSS}$	-2.5	V
Drain current	$I_D$ <sup>Note 3</sup>	20	A
Body-drain diode reverse drain current	$I_{DR}$ <sup>Note 2</sup>	20	A
Avalanche current	$I_{AP}$ <sup>Note 2</sup>	6.7	A
Avalanche energy	$E_{AR}$ <sup>Note 2</sup>	192	mJ
Channel dissipation	$P_{ch}$ <sup>Note 1</sup>	40	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

- Notes: 1. Value at  $T_c = 25^\circ\text{C}$   
 2.  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$   
 3. It provides by the current limitation lower bound value.

## Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	$V_{IH}$	3.5	—	—	V	
	$V_{IL}$	—	—	1.2	V	
Input current (Gate non shut down)	$I_{IH1}$	—	—	100	$\mu\text{A}$	$V_i = 8\text{ V}, V_{DS} = 0$
	$I_{IH2}$	—	—	50	$\mu\text{A}$	$V_i = 3.5\text{ V}, V_{DS} = 0$
	$I_{IL}$	—	—	1	$\mu\text{A}$	$V_i = 1.2\text{ V}, V_{DS} = 0$
Input current (Gate shut down)	$I_{IH(sd)1}$	—	0.8	—	mA	$V_i = 8\text{ V}, V_{DS} = 0$
	$I_{IH(sd)2}$	—	0.35	—	mA	$V_i = 3.5\text{ V}, V_{DS} = 0$
Shut down temperature	$T_{sd}$	—	175	—	°C	Channel temperature
Gate operation voltage	$V_{op}$	3.5	—	12	V	
Drain current (Current limitation value)	$I_{D\text{ limit}}$	20	—	—	A	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$ <sup>Note 4</sup>

Note: 4. Pulse test

## Electrical Characteristics

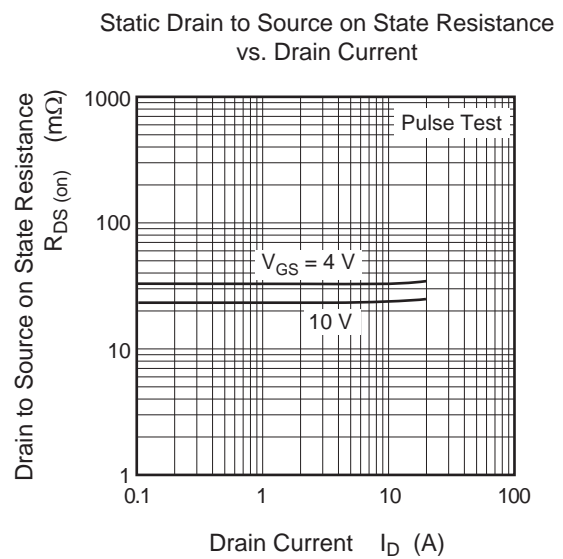
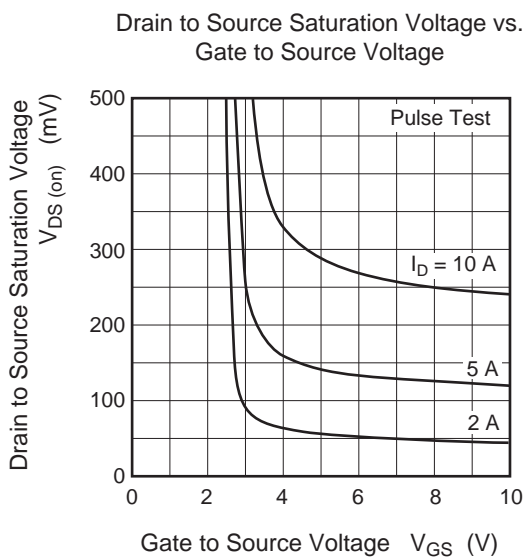
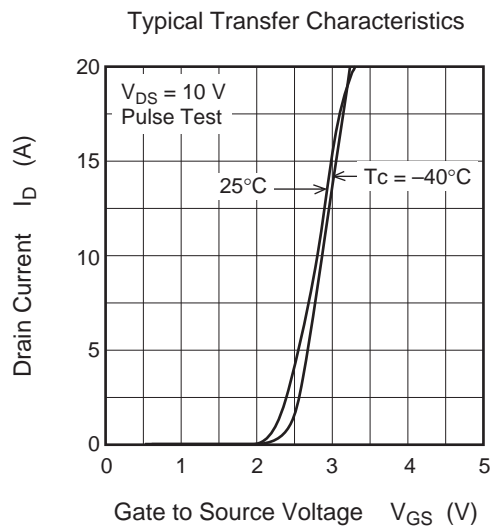
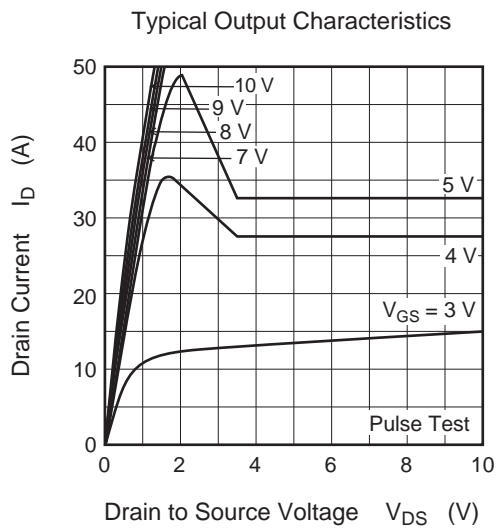
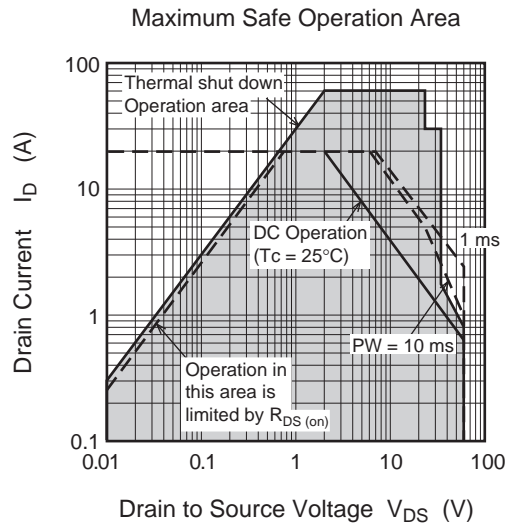
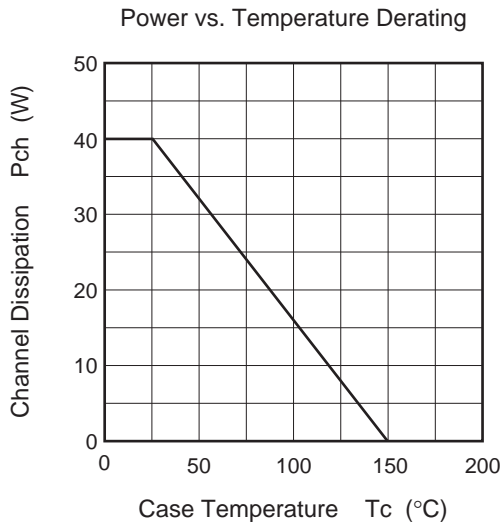
(Ta = 25°C)

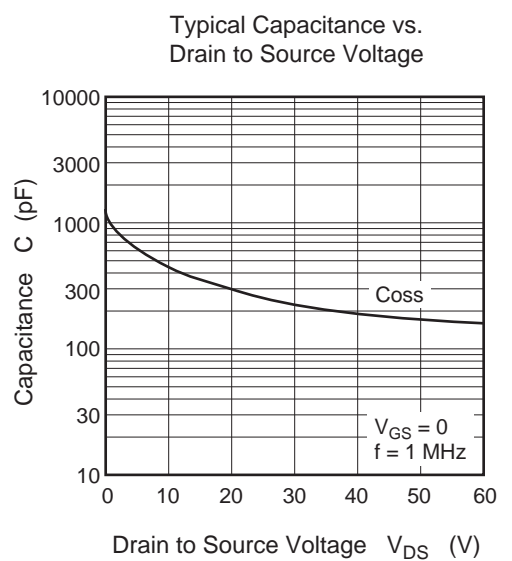
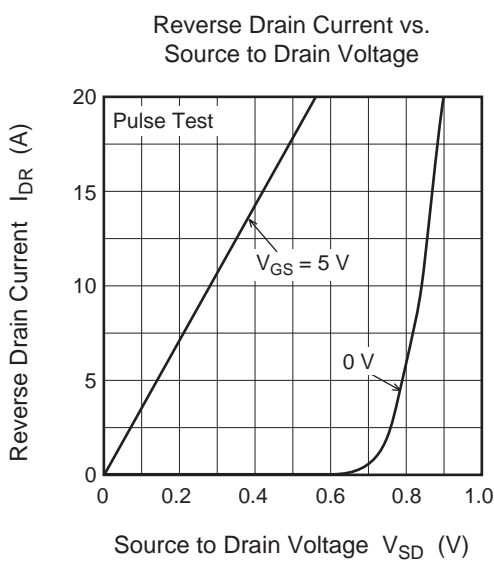
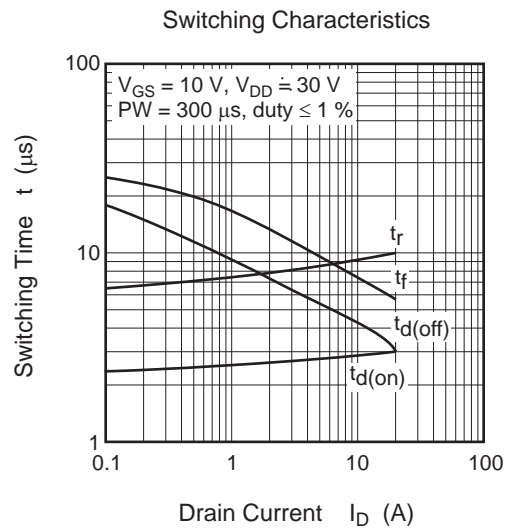
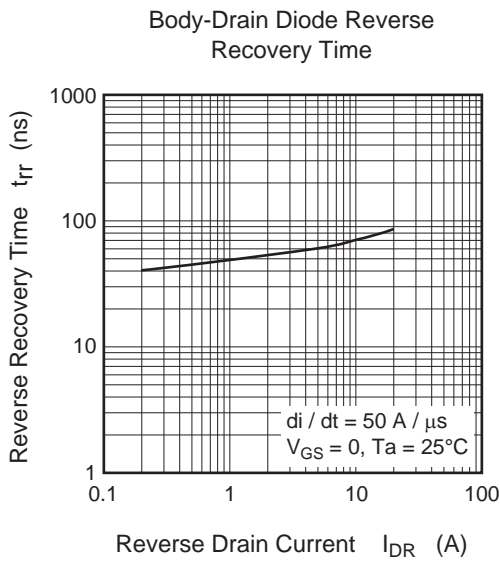
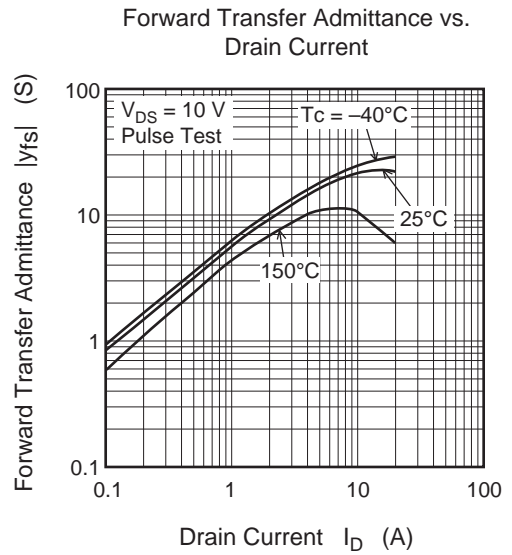
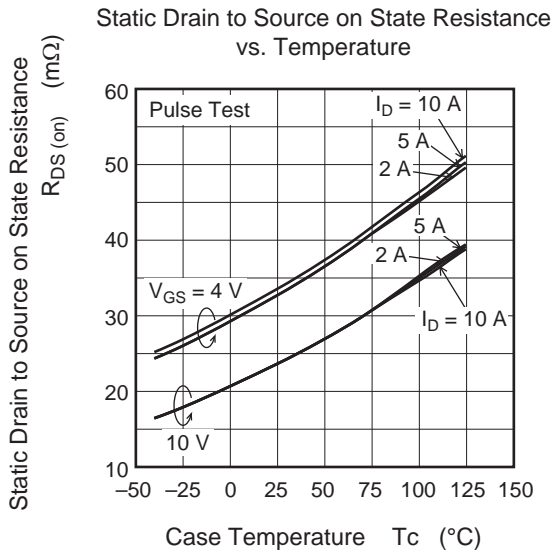
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	$I_{D1}$	—	—	35	A	$V_{GS} = 3.5\text{ V}, V_{DS} = 10\text{ V}$ <sup>Note 5</sup>
	$I_{D2}$	—	—	10	mA	$V_{GS} = 1.2\text{ V}, V_{DS} = 10\text{ V}$
	$I_{D3}$	20	—	—	A	$V_{GS} = 5\text{ V}, V_{DS} = 10\text{ V}$ <sup>Note 5</sup>
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10\text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	16	—	—	V	$I_G = 800\text{ }\mu\text{A}, V_{DS} = 0$
	$V_{(BR)GSS}$	-2.5	—	—	V	$I_G = -100\text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS1}$	—	—	100	$\mu\text{A}$	$V_{GS} = 8\text{ V}, V_{DS} = 0$
	$I_{GSS2}$	—	—	50	$\mu\text{A}$	$V_{GS} = 3.5\text{ V}, V_{DS} = 0$
	$I_{GSS3}$	—	—	1	$\mu\text{A}$	$V_{GS} = 1.2\text{ V}, V_{DS} = 0$
	$I_{GSS4}$	—	—	-100	$\mu\text{A}$	$V_{GS} = -2.4\text{ V}, V_{DS} = 0$
Input current (shut down)	$I_{GS(OP)1}$	—	0.8	—	mA	$V_{GS} = 8\text{ V}, V_{DS} = 0$
	$I_{GS(OP)2}$	—	0.35	—	mA	$V_{GS} = 3.5\text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 32\text{ V}, V_{GS} = 0, T_c = 110^\circ\text{C}$
Gate to source cutoff voltage	$V_{GS(off)}$	1.1	—	2.1	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
Forward transfer admittance	$ y_{fs} $	12	21	—	S	$I_D = 10\text{ A}, V_{DS} = 10\text{ V}$ <sup>Note 5</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	34	50	m $\Omega$	$I_D = 10\text{ A}, V_{GS} = 4\text{ V}$ <sup>Note 5</sup>
	$R_{DS(on)}$	—	24	38	m $\Omega$	$I_D = 10\text{ A}, V_{GS} = 10\text{ V}$ <sup>Note 5</sup>
Output capacitance	$C_{oss}$	—	450	—	pF	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	3	—	$\mu\text{s}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}, R_L = 3\text{ }\Omega$
Rise time	$t_r$	—	10	—	$\mu\text{s}$	
Turn-off delay time	$t_{d(off)}$	—	4.4	—	$\mu\text{s}$	
Fall time	$t_f$	—	7.7	—	$\mu\text{s}$	
Body-drain diode forward voltage	$V_{DF}$	—	0.9	—	V	$I_F = 20\text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	85.3	—	ns	$I_F = 20\text{ A}, V_{GS} = 0$ $di_F/dt = 50\text{ A}/\mu\text{s}$
Over load shut down operation time <sup>Note 6</sup>	$t_{os1}$	—	0.3	—	ms	$V_{GS} = 5\text{ V}, V_{DD} = 16\text{ V}$
	$t_{os2}$	—	0.2	—	ms	$V_{GS} = 5\text{ V}, V_{DD} = 24\text{ V}$

Notes: 5. Pulse test

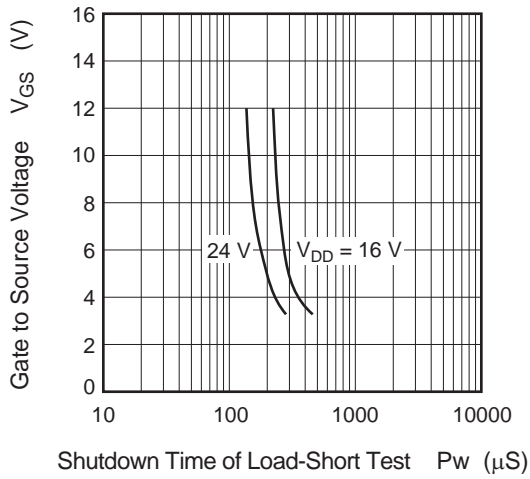
6. Including the junction temperature rise of the over loaded condition.

### Main Characteristics

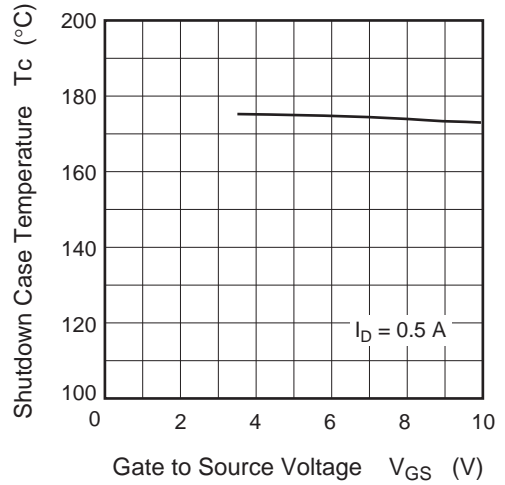




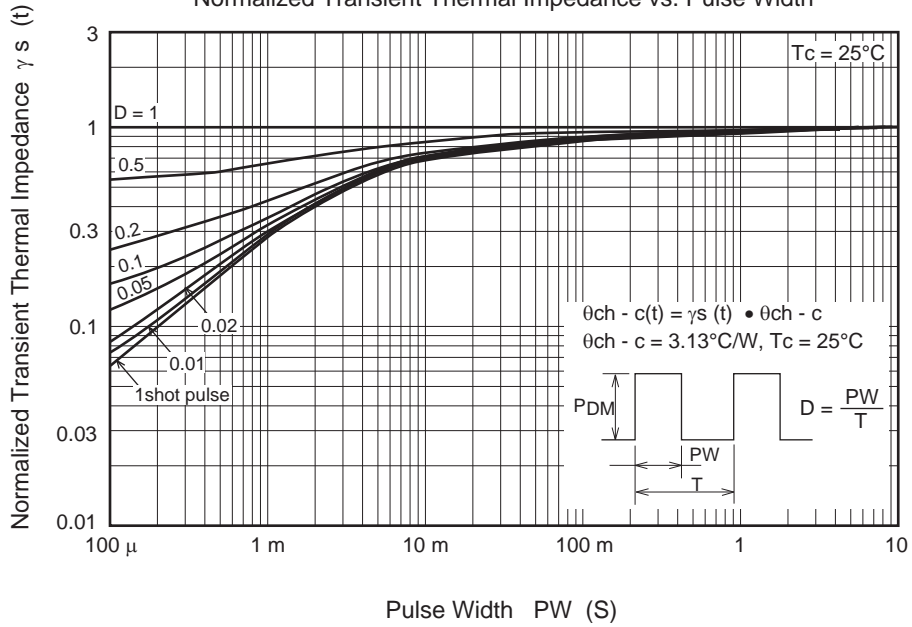
Gate to Source Voltage vs. Shutdown Time of Load-Short Test



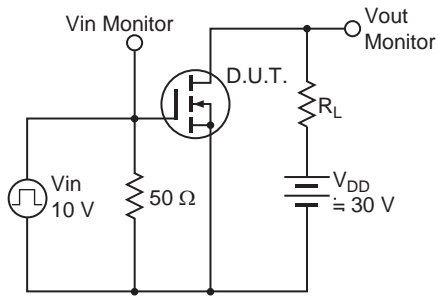
Shutdown Case Temperature vs. Gate to Source Voltage



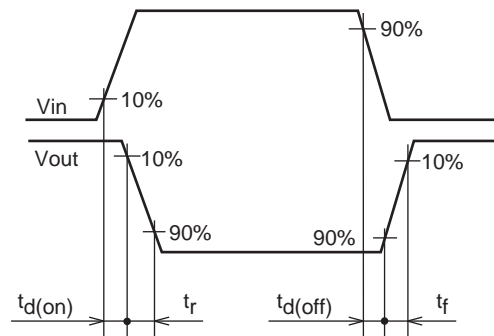
Normalized Transient Thermal Impedance vs. Pulse Width



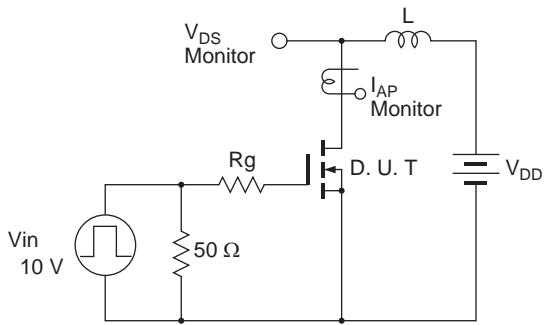
Switching Time Test Circuit



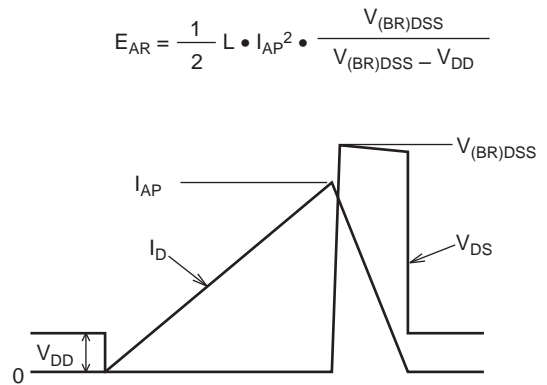
Waveform



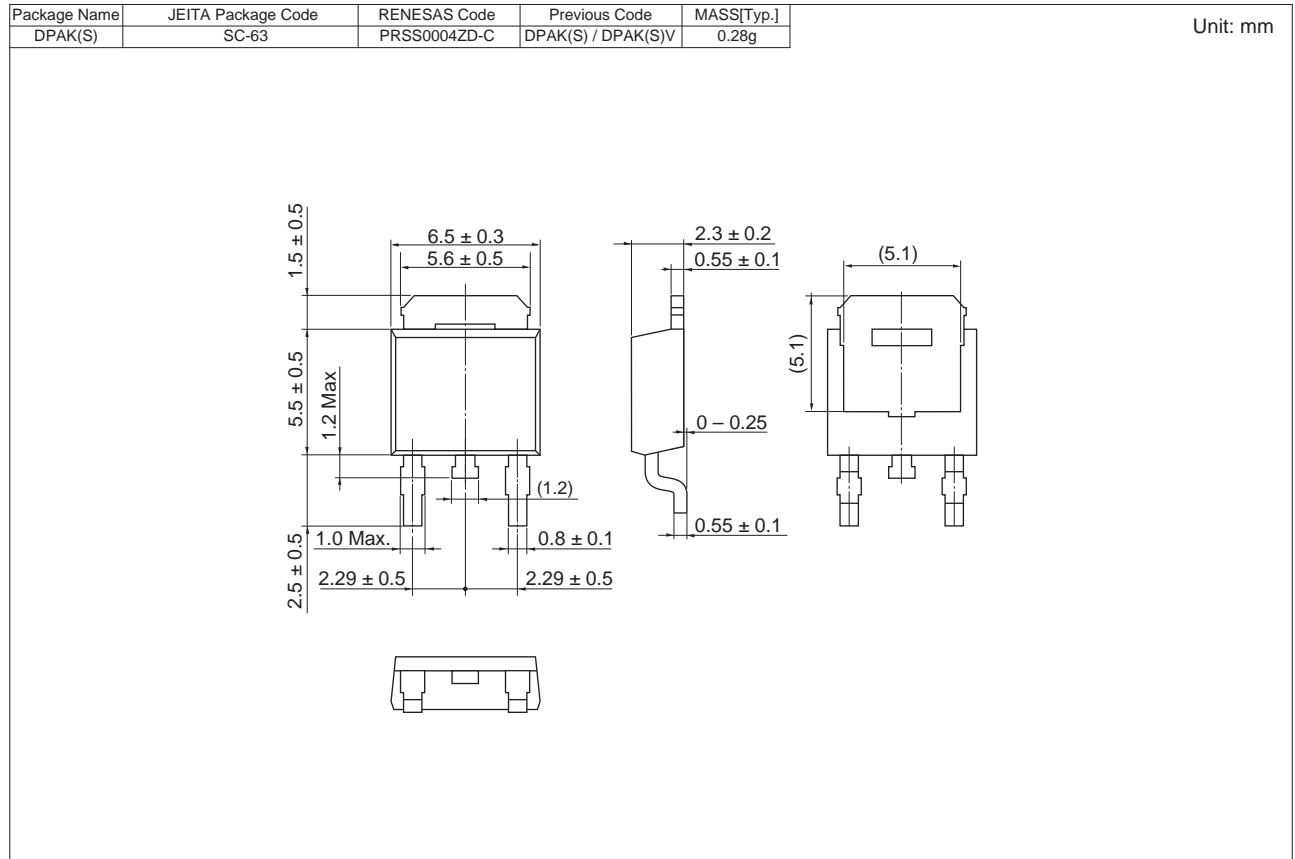
Avalanche Test Circuit



Avalanche Waveform



### Package Dimensions



### Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJF0605JPD-00-J3	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
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Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

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Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**  
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**Renesas Electronics Korea Co., Ltd.**  
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