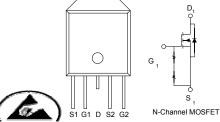
P & N-Channel 30-V (D-S) MOSFET

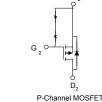
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low r_{DS(on)} and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY					
V _{DS} (V)	$r_{DS(on)} m(\Omega)$	$I_D(A)$			
30	$45@V_{CS} = 4.5V$	29			
50	$35@V_{CS} = 10V$	36			
20	$33@V_{CS} = -4.5V$	-32			
-30	$23@V_{CS} = -10V$	39			

S





ESD Protected 2000V

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)							
Parameter			N-Channel	P-Channel	Units		
Drain-Source Voltage			30	-30	v		
Gate-Source Voltage			±20	±20			
Continuous Drain Current ^a	$T_A = 25^{\circ}C$	L	36	-39	А		
Continuous Drain Current	T _A =70°C	ID	30	-26			
Pulsed Drain Current ^b			40	-40			
Continuous Source Current (Diode Conduct	Is	30	-30	Α			
Power Dissipation ^a T _A =25 ^o C		P_D	50	50	W		
Operating Junction and Storage Temperatur	TJ, Tstg	-55 to	°C				

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	°C/W			
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W			

Notes

Surface Mounted on 1" x 1" FR4 Board. a.

b. Pulse width limited by maximum junction temperature

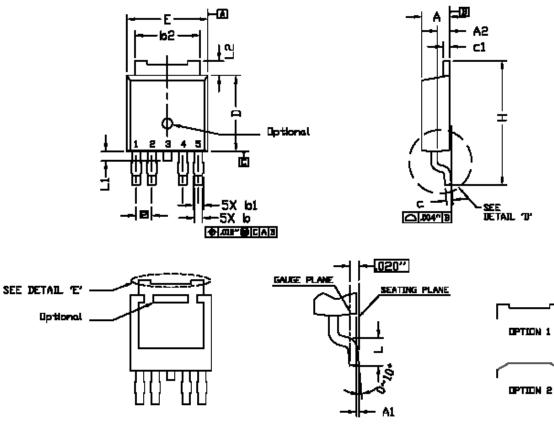
SPECIFICATIONS ($T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Conditions	Limits				Unit	
	Symbol		Ch	Min	Тур	Max	Om	
Static								
Gate-Threshold Voltage	V	$V_{GS} = V_{DS}, I_D = 250 \text{ uA}$	N	0.6			v	
Gate-Theshold Voltage	V _{GS(th)}	$V_{OS} = V_{DS}$, $I_D = -250 \text{ uA}$	Р	-0.6				
Gate-Body Leakage	I _{GSS}	$V_{CS} = -20 V$, $V_{DS} = 0 V$	P			± 100	nA	
	0.35	$V_{cs} = 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$	N P			±100	12 1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -24 V, V_{GS} = 0 V$	P N			-1	– uA	
	-	$\frac{V_{DS} = 24 V_{y} V_{CS} = 0 V}{V_{DS} = 5 V_{y} V_{CS} = 10 V}$	N	20		1		
On-State Drain Current ^a	I _{D(on)}	$V_{D8} = -5 V, V_{C8} = -10 V$	Р	-20			Α	
		$V_{OS} = 10 \text{ V}, \text{ I}_{D} = 6.9 \text{ A}$	N			35	mΩ	
Drain-Source On-Resistance ^a	r _{DS(on)}	$VCS=4.5 V, I_D=6 A$	11			45		
	-DS(on)	VGS = -10 V, ID = -5.2 A	Р			23 33		
		$\frac{VCS}{V_{DS}} = -4.5 \text{ V}, \text{ ID} = -4.2 \text{ A}}{V_{DS}} = 15 \text{ V}, \text{ I}_{D} = 6.9 \text{ A}}$	N		25	- 33		
Forward Tranconductance ^a	g _{ís}	$V_{DS} = -15 \text{ V}, I_D = -5.2 \text{ A}$	P		10		S	
Dynamic		100 D						
Total Gate Charge	0		Ν		6.0			
Total Gate Charge	Qg	N-Channel	Р		10			
Gate-Source Charge	Qgs	V_{DS} =15V, V_{CS} =10V, I_{D} =6.9A	N		1.0		nC	
	×6,	P-Channel	P N		2.4 1.5			
Gate-Drain Charge	Qgd	VDs=-15V, VGs=-10V, ID=-5.2A						
	~		P N		3.9			
Turn-On Delay Time	td(on)	N-Chaneel	P N		7.6			
		$V_{DD} = 15V, V_{GS} = 10V, I_D = 1A$,	I N		4		4	
Rise Time	tr	$R_{GEN} = 6\Omega,$	P		6.8		G	
Turn Off Dalay Ting		P-Channel	Ν		22.2		nS	
Tum-Off Delay Time	td(off)	VDD=15V, VGs=10V, ID=1A	Р		33.6			
Fall-Time	tf	$R_{GEN}=6\Omega$	N		3.6			
1.011-11110	u		Р		23.2			

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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DETAIL 'D'

DETAIL 'E'

8 Y M B	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES			
10 L	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	2.184	2.286	2.388	0.086	0.090	0.094	
A1	0.000	-	0.127	0.000	—	0.005	
A2	0.869	-	1.143	0.035	-	0.045	
b	0.508	-	0.711	0.020	-	0.028	
b1	0.584	-	0.787	0.023		0.031	
b2	4.953	—	5.461	0.195	-	0.215	
C	0.457	0.508	0.610	0.018	0.020	0.024	
c 1	0.457	—	0.610	0.018	_	0.024	
D	5.969	6.096	6.223	0.235	0.240	0.245	
Е	6.350	6.604	6.731	0.250	0.260	0.265	
8	1.270 BSC.			0.050 BSC.			
Н	9.398	_	10.414	0.370	—	0.410	
L	1.270	_	2.032	0.050	_	0.080	
L1	_	-	1.016	_	_	0.040	
12	0.889	-	1.270	0.035	_	0.050	

NOTE

- 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
- 2. DIMENSION L IS MEASURED IN GAUGE PLANE.
- 3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED.
- 4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
- 5. REFER TO JEDEC TO-252 (AD).