



# STL45N65M5

N-channel 650 V, 0.075  $\Omega$  typ., 22.5 A MDmesh™ V Power MOSFET in PowerFLAT™ 8x8 HV package

Datasheet — preliminary data

## Features

Order code	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL45N65M5	710 V	< 0.086 $\Omega$	22.5 A <sup>(1)</sup>

1. The value is rated according to R<sub>thj-case</sub> and limited by package.

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

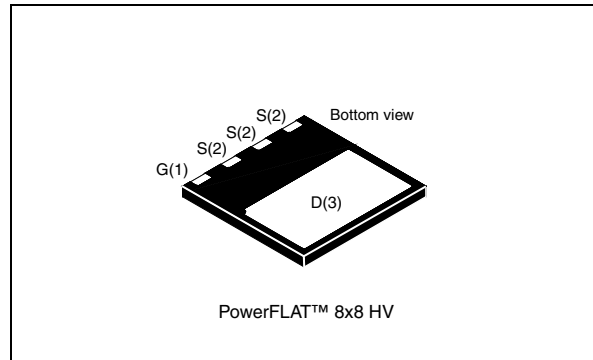


Figure 1. Internal schematic diagram

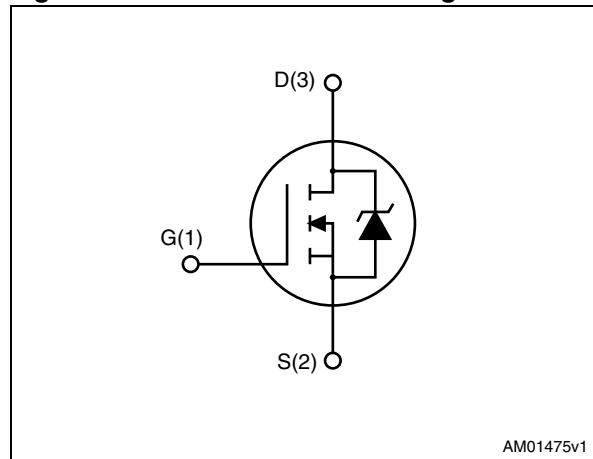


Table 1. Device summary

Order code	Marking	Package	Packaging
STL45N65M5	45N65M5	PowerFLAT™ 8x8 HV	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Packaging mechanical data</b> .....	<b>14</b>
<b>6</b>	<b>Revision history</b> .....	<b>16</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	18	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	90	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	3.8	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.4	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	160	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	9	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	810	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-case}$  and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.
4.  $I_{SD} \leq 22.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 400\text{ V}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.78	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 14.5\text{ A}$		0.075	0.086	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	3470	-	pF
$C_{oss}$	Output capacitance			82		pF
$C_{rss}$	Reverse transfer capacitance			7		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0,$ $V_{DS} = 0\text{ to }80\% V_{(BR)DSS}$	-	79	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related			280		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 17.5\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	82	-	nC
$Q_{gs}$	Gate-source charge			18.5		nC
$Q_{gd}$	Gate-drain charge			35		nC

1. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_d$ (v)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 22.5$ A, $R_G = 4.7$ $\Omega$ , $V_{GS} = 10$ V (see <a href="#">Figure 20</a> )		79.5		ns	
$t_r$ (v)	Voltage rise time			11		ns	
$t_f$ (i)	Current fall time				9.3		ns
$t_c$ (off)	Crossing time				16		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		22.5	A
$I_{SDM}^{(1).(2)}$	Source-drain current (pulsed)				90	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 22.5$ A, $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5$ A, $di/dt = 100$ A/ $\mu$ s $V_{DD} = 100$ V (see <a href="#">Figure 17</a> )	-	346		ns
$Q_{rr}$	Reverse recovery charge			6		$\mu$ C
$I_{RRM}$	Reverse recovery current			35		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5$ A, $di/dt = 100$ A/ $\mu$ s $V_{DD} = 100$ V, $T_j = 150$ °C (see <a href="#">Figure 17</a> )	-	432		ns
$Q_{rr}$	Reverse recovery charge			8.4		$\mu$ C
$I_{RRM}$	Reverse recovery current			39		A

1. The value is rated according to  $R_{thj-case}$  and limited by package.
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

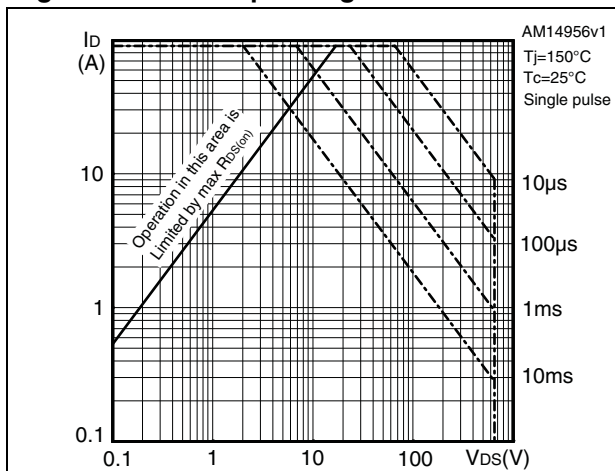


Figure 3. Thermal impedance

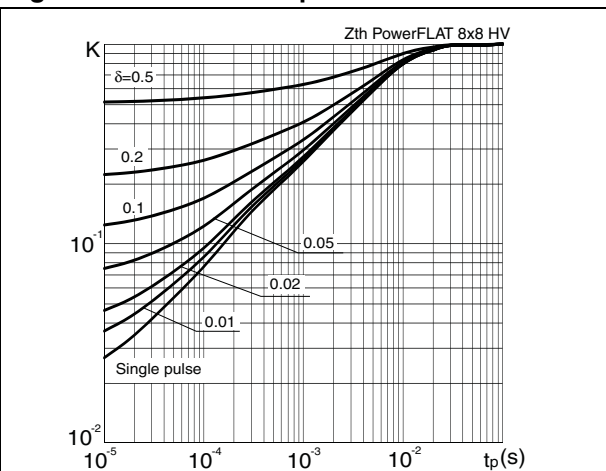


Figure 4. Output characteristics

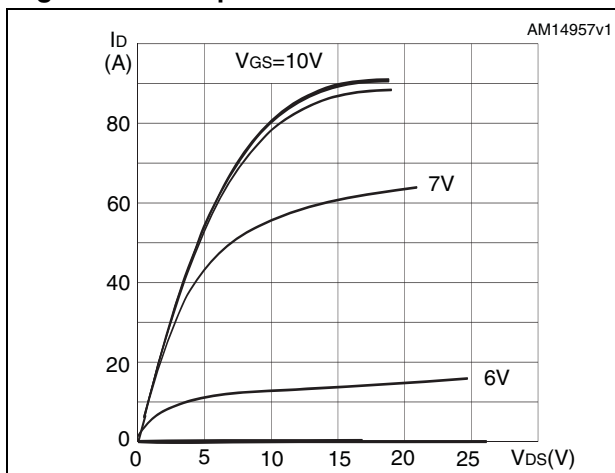


Figure 5. Transfer characteristics

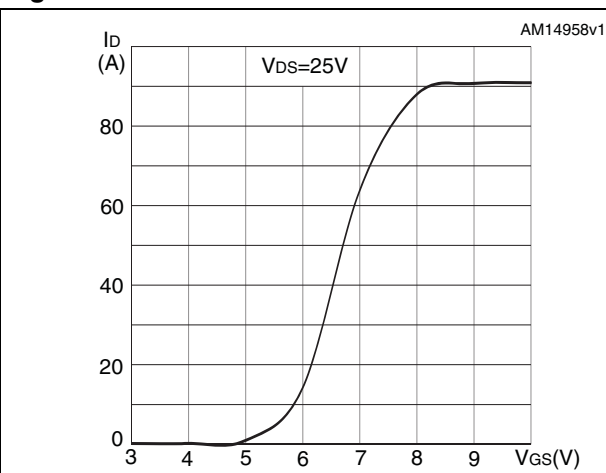


Figure 6. Gate charge vs gate-source voltage

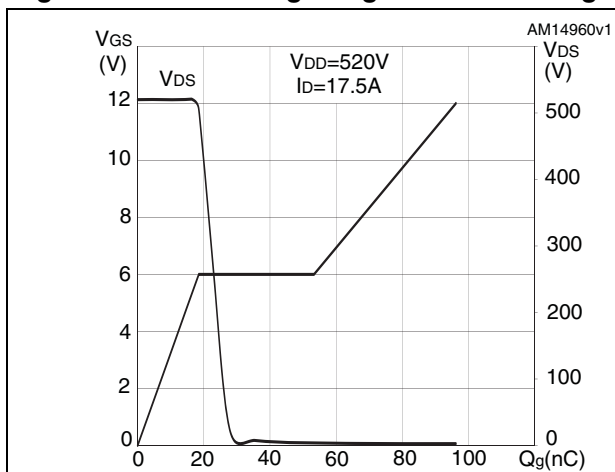


Figure 7. Static drain-source on-resistance

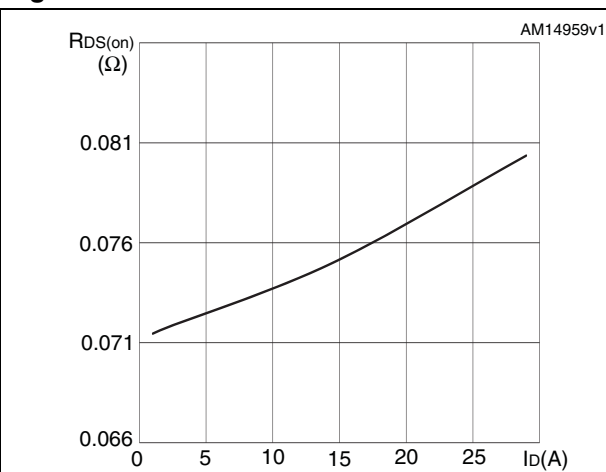


Figure 8. Capacitance variations

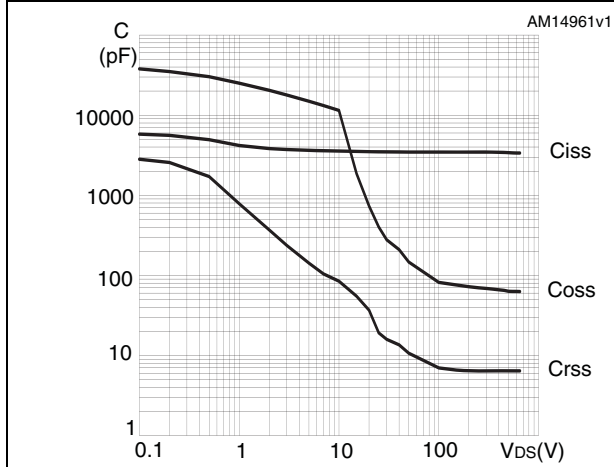


Figure 9. Output capacitance stored energy

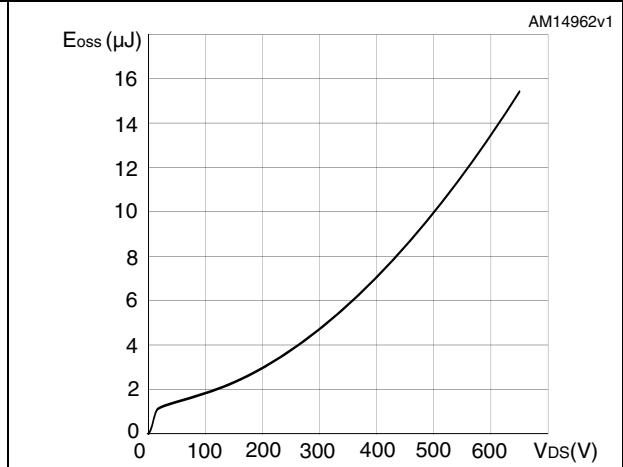


Figure 10. Normalized gate threshold voltage vs. temperature

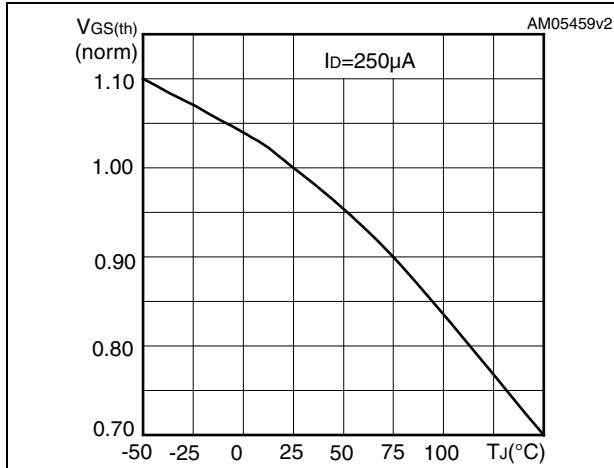


Figure 11. Normalized on-resistance vs. temperature

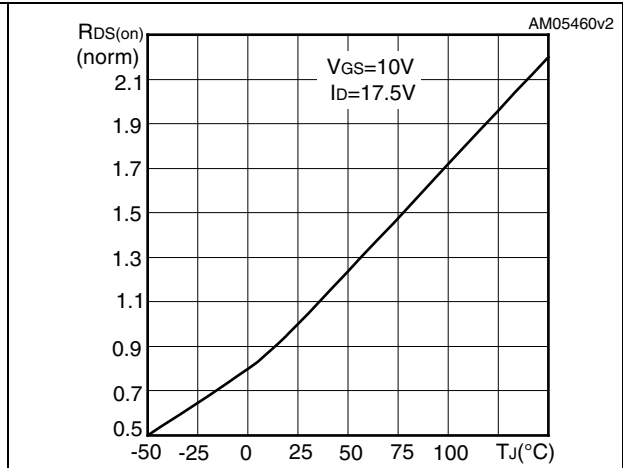


Figure 12. Drain-source diode forward characteristics

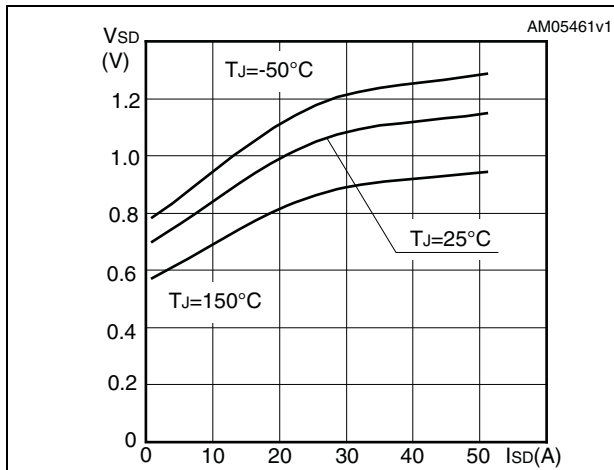


Figure 13. Normalized VDS vs. temperature

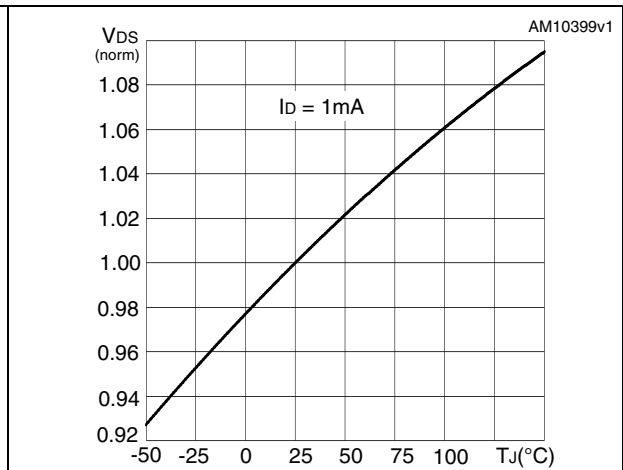
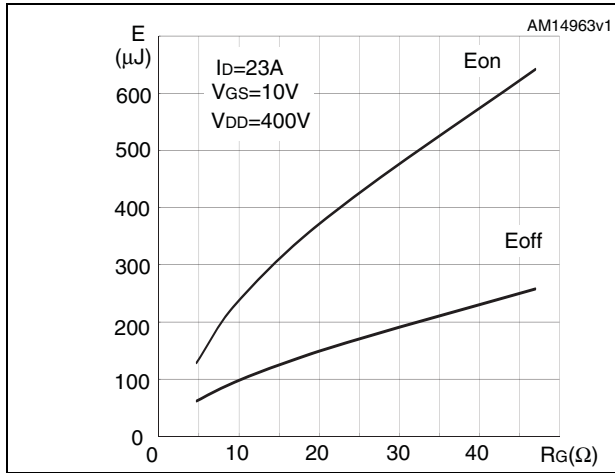


Figure 14. Switching losses vs. gate resistance (1)



1.  $E_{on}$  including reverse recovery of a SiC diode



### 3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit



Figure 17. Test circuit for inductive load switching and diode recovery times

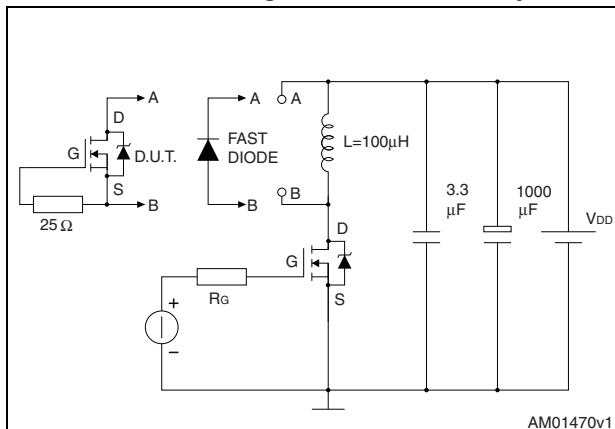


Figure 18. Unclamped inductive load test circuit



Figure 19. Unclamped inductive waveform

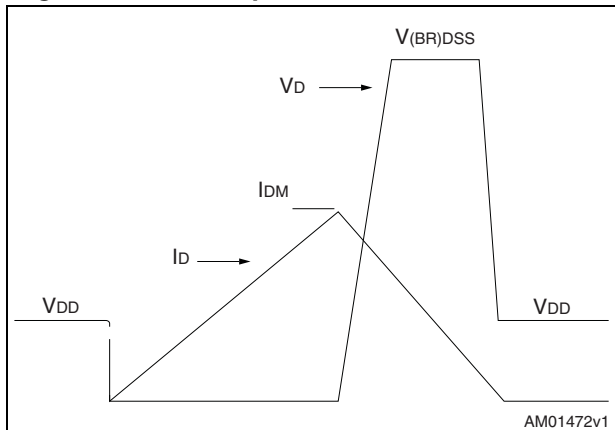
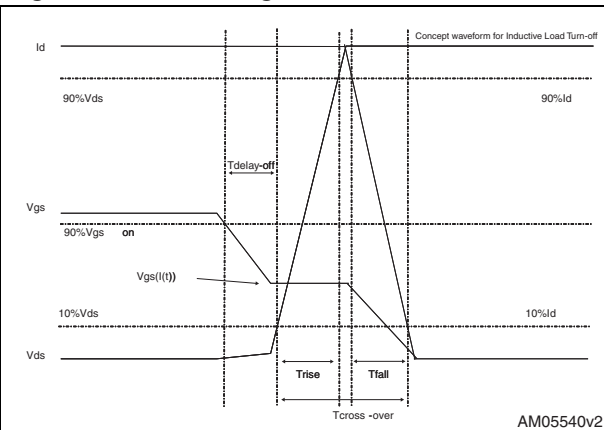


Figure 20. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 21. PowerFLAT™ 8x8 HV drawing mechanical data

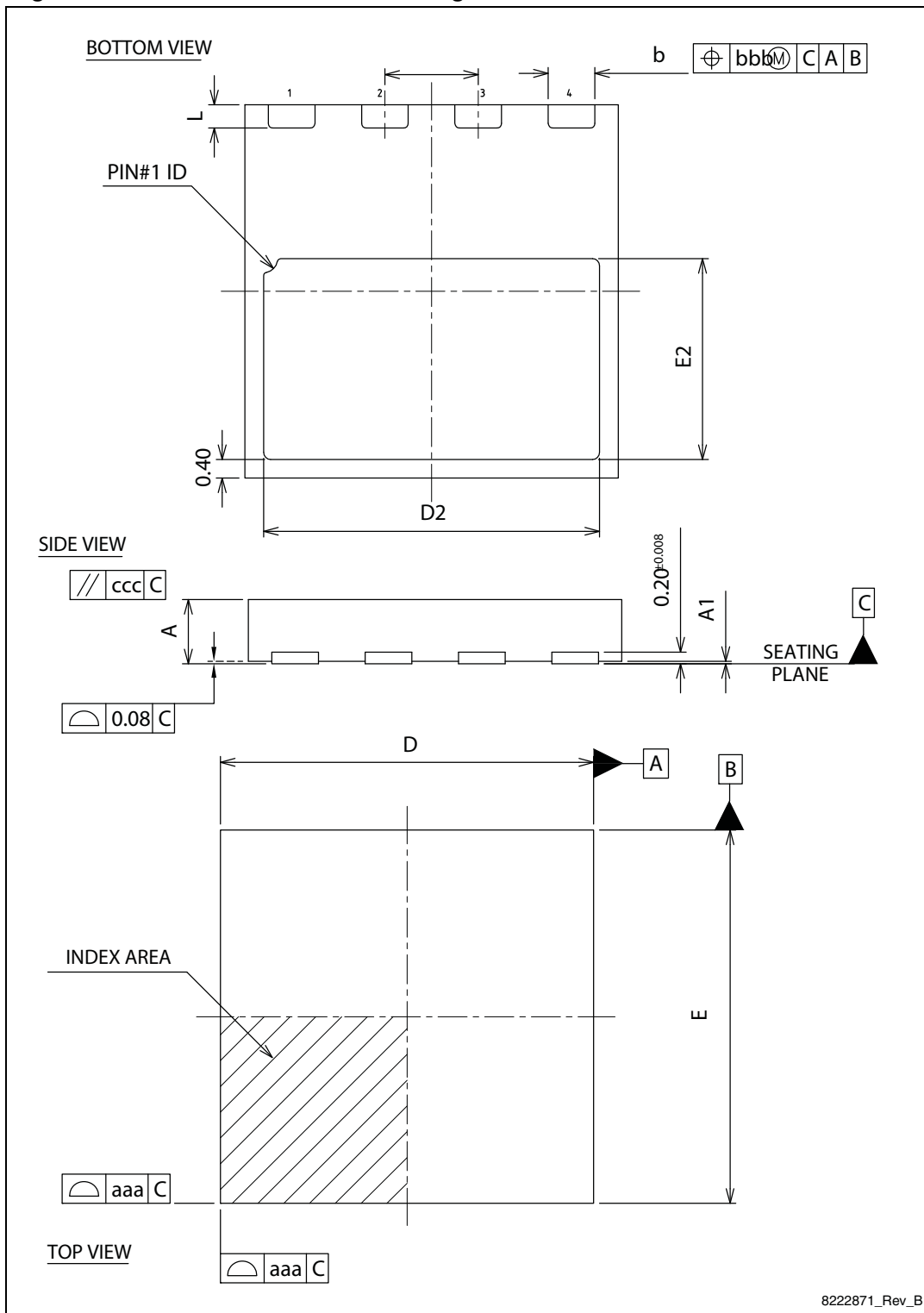
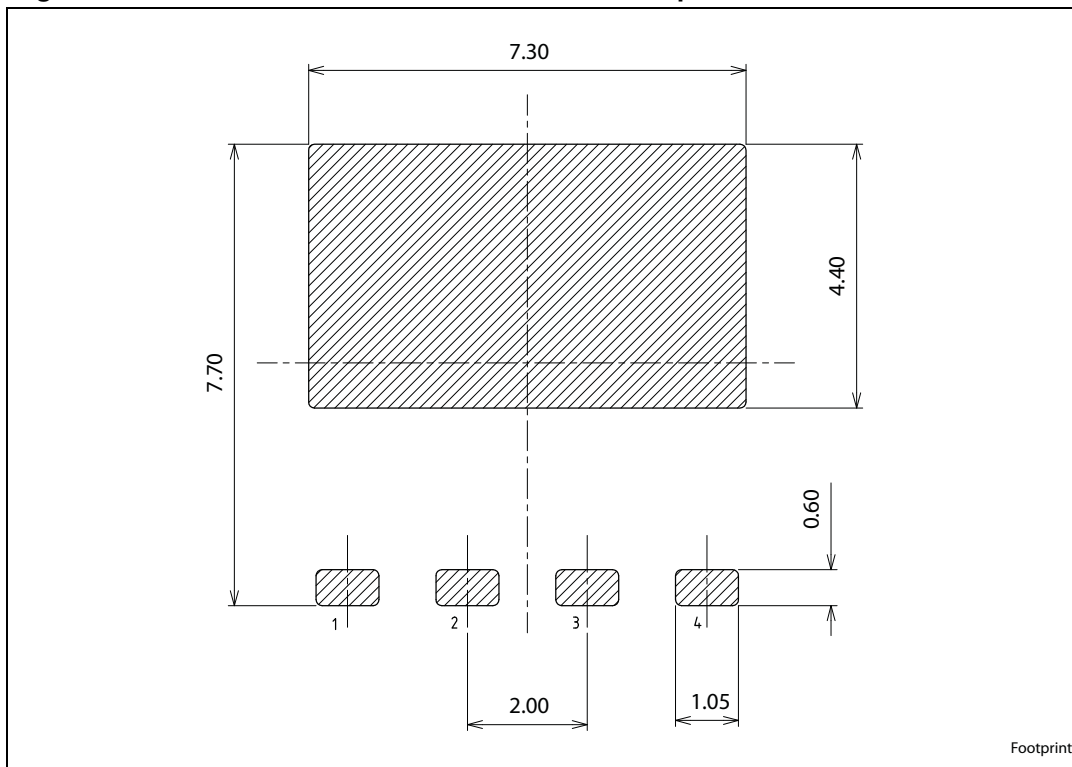


Figure 22. PowerFLAT™ 8x8 HV recommended footprint



# 5 Packaging mechanical data

Figure 23. PowerFLAT™ 8x8 HV tape

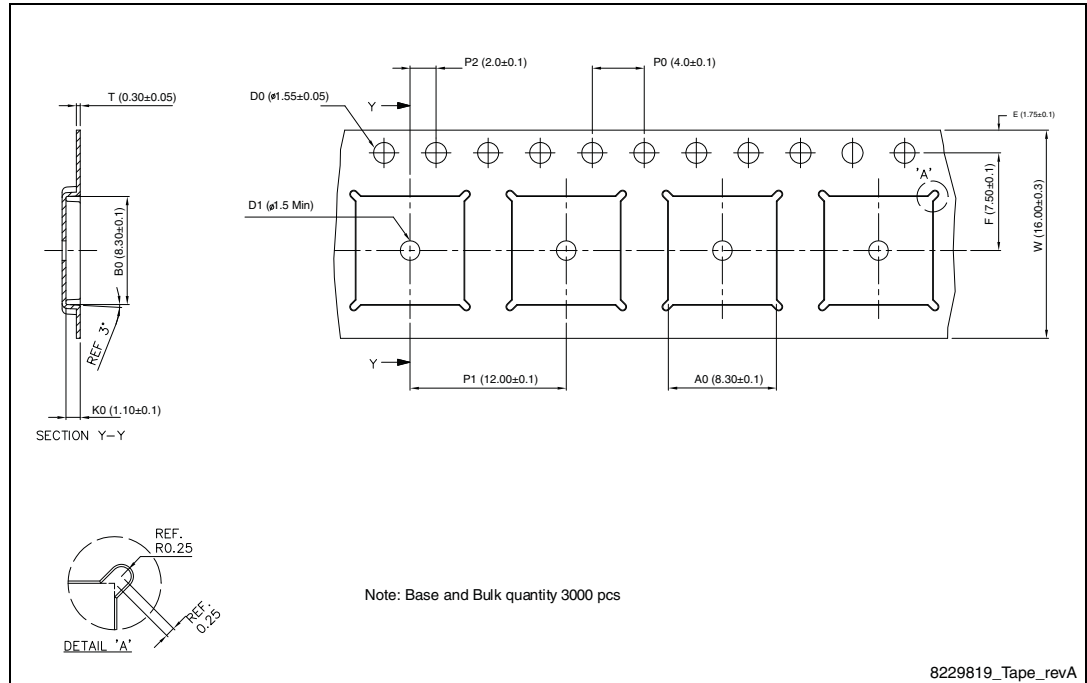
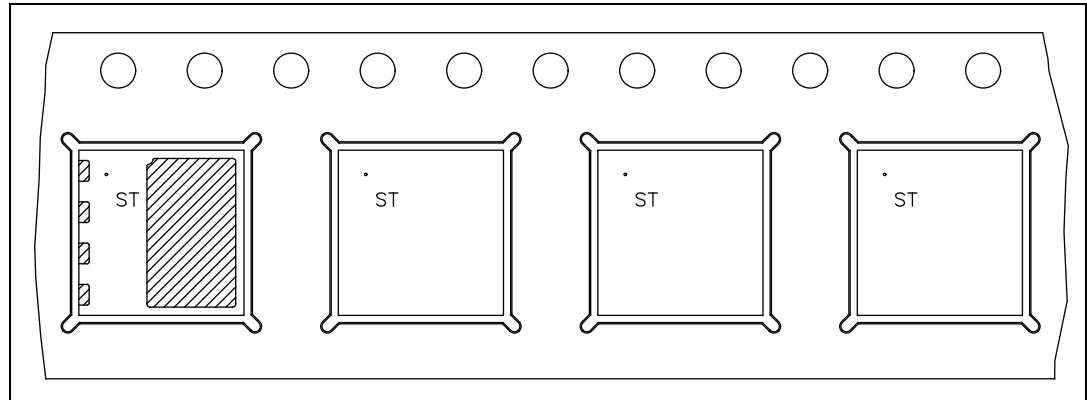


Figure 24. PowerFLAT™ 8x8 HV package orientation in carrier tape.





## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-Sep-2012	1	First release.



**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

