

High Voltage IGBT

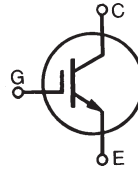
IXGH10N300

$$V_{CES} = 3000V$$

$$I_{C90} = 10A$$

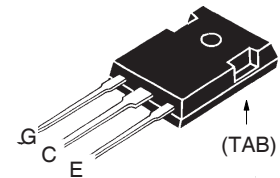
$$V_{CE(sat)} \leq 3.5V$$

For Capacitor Discharge Applications



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	3000	V
V_{CGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	18	A
I_{C90}	$T_C = 90^\circ C$	10	A
I_{CM}	$T_C = 25^\circ C$, 1ms	40	A
SSOA	$V_{GE} = 20V$, $T_{VJ} = 125^\circ C$, $R_G = 50\Omega$	$I_{CM} = 32$	A
(RBSOA)	Clamped Inductive Load	@ ≤ 1250	V
P_C	$T_C = 25^\circ C$	100	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting Torque	1.13/10	Nm/lb.in.
Weight		6	g

TO-247 AD



G = Gate C = Collector
E = Emitter TAB = Collector

Features

- High Peak Current Capability
- Low Saturation Voltage
- Low Gate Drive Requirement
- Molding Epoxies Meet UL 94 V-0 Flammability Classification

Applications

- Capacitor Discharge
- Pulser Circuits

Advantages

- High Power Density
- Easy to Mount

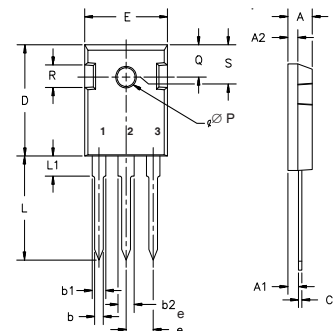
Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}$, $V_{GE} = 0V$ $T_J = 125^\circ C$			25 μA 500 μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 10A$, $V_{GE} = 15V$ $I_C = 30A$			3.5 V 5.2 V

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 20\text{A}$, $V_{CE} = 10\text{V}$, Note 1	3.6	6.0	S
$I_{C(ON)}$	$V_{GE} = 15\text{V}$, $V_{CE} = 15\text{V}$, Note 1		54	A
C_{ies}	$V_{CE} = 25\text{V}$, $V_{GE} = 0\text{V}$, $f = 1\text{MHz}$		560	pF
C_{oes}			24	pF
C_{res}			8	pF
$Q_{g(on)}$	$I_C = 10\text{A}$, $V_{GE} = 15\text{V}$, $V_{CE} = 0.5 \cdot V_{CES}$		32.0	nC
Q_{ge}			7.5	nC
Q_{gc}			12.0	nC
$t_{d(on)}$	Resistive Switching Times $I_C = 20\text{A}$, $V_{GE} = 15\text{V}$ $V_{CE} = 1250\text{V}$, $R_G = 50\Omega$		72	ns
t_r			227	ns
$t_{d(off)}$			154	ns
t_f			530	ns
R_{thJC}			1.25	$^\circ\text{C/W}$
R_{thCK}		0.21		$^\circ\text{C/W}$

Note

1. Pulse Test, $t \leq 300\mu\text{s}$; Duty Cycle, $d \leq 2\%$.
2. Additional provisions for lead-to-lead voltage isolation are required at $V_{CE} > 1200\text{V}$.

TO-247 (IXGH) Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
∅P	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ 25°C

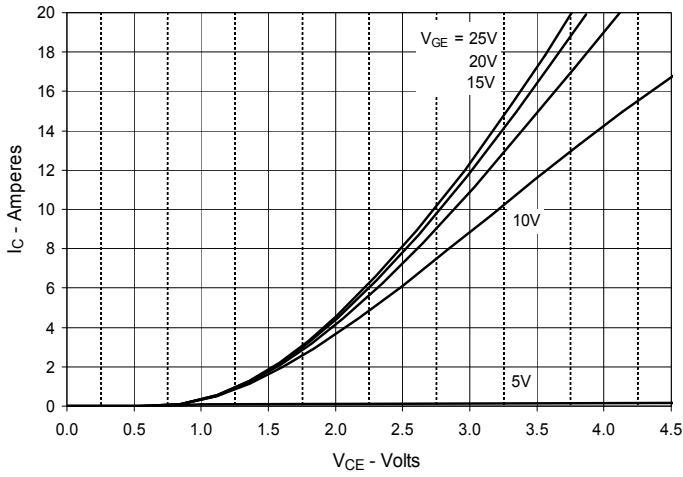


Fig. 2. Extended Output Characteristics @ 25°C

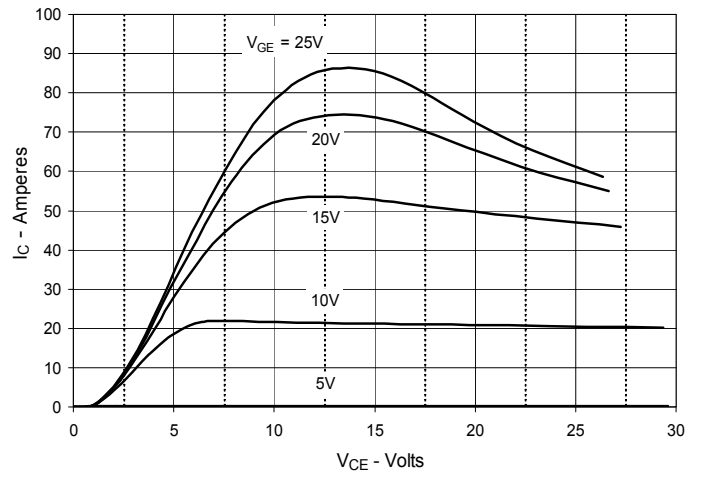


Fig. 3. Output Characteristics @ 125°C

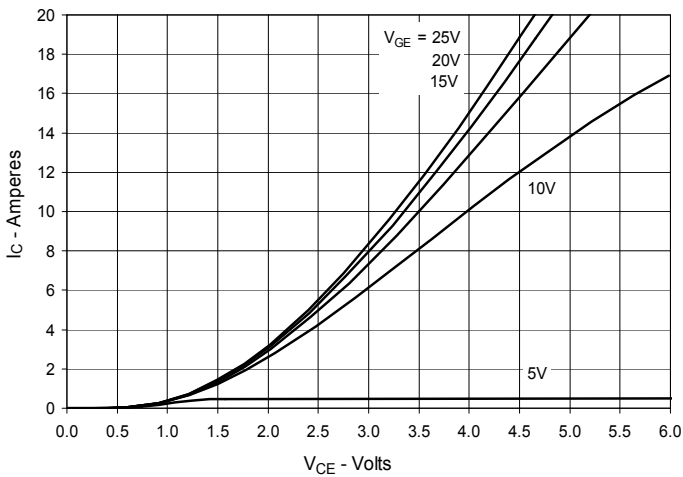


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

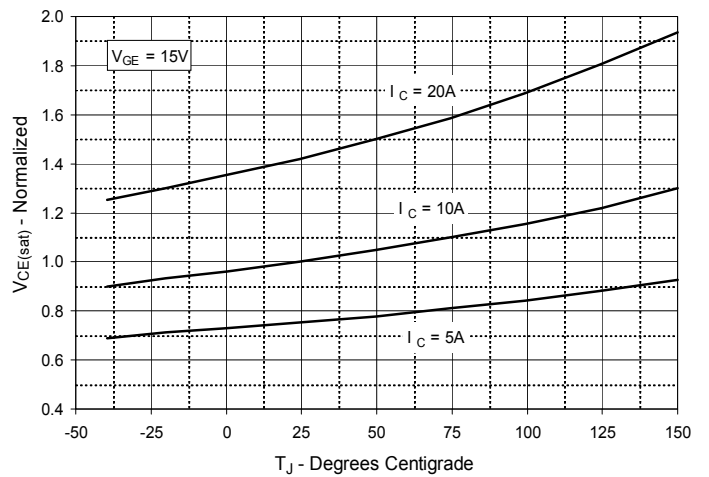


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

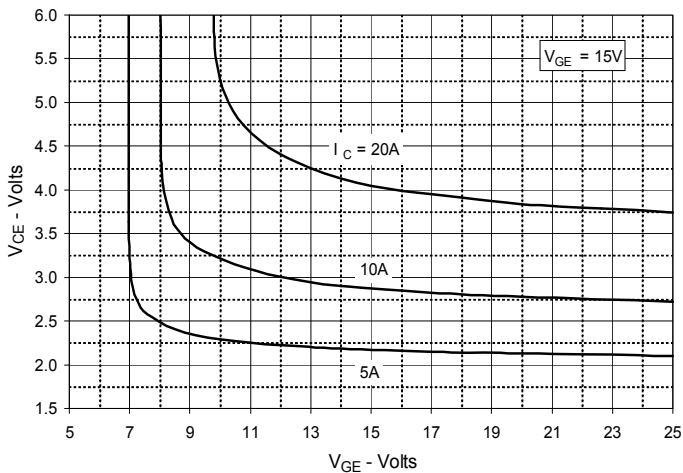


Fig. 6. Input Admittance

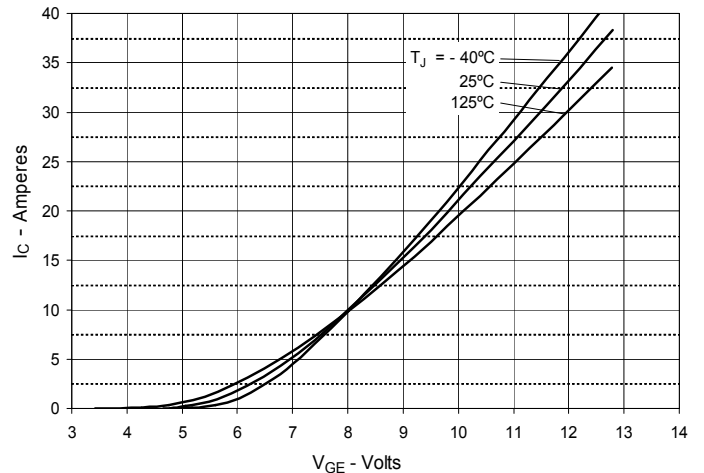


Fig. 7. Transconductance

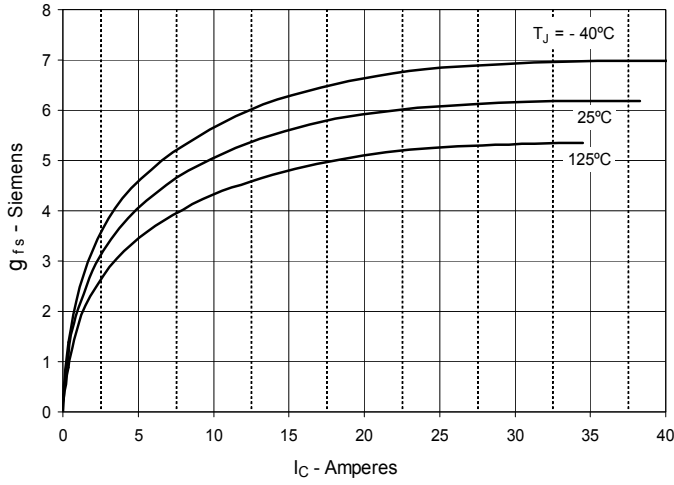


Fig. 8. Gate Charge

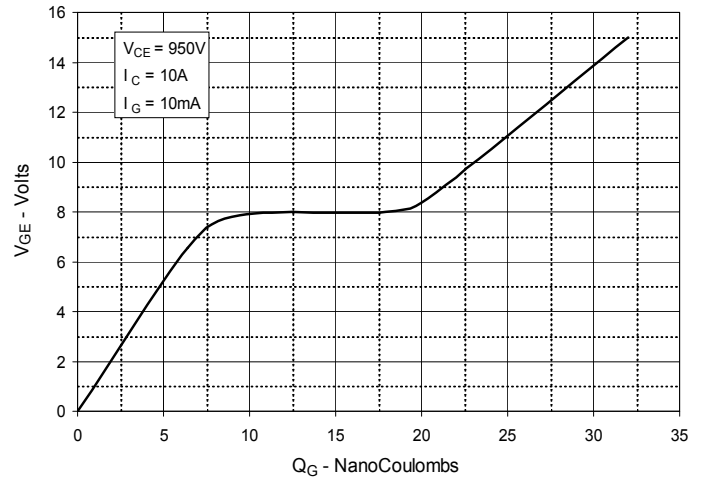


Fig. 9. Reverse-Bias Safe Operating Area

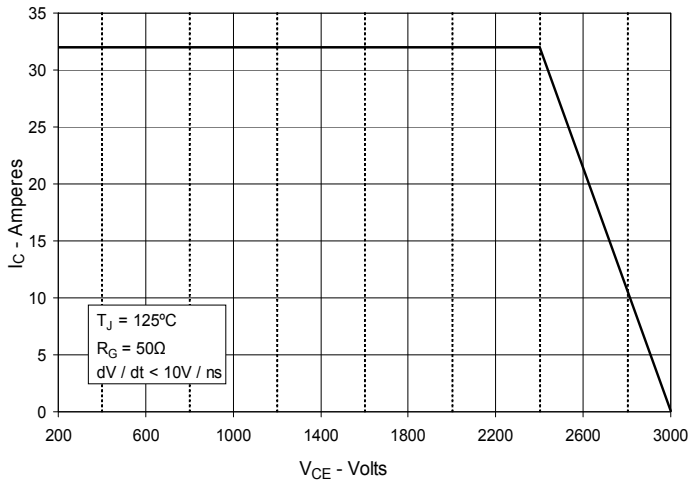


Fig. 10. Capacitance

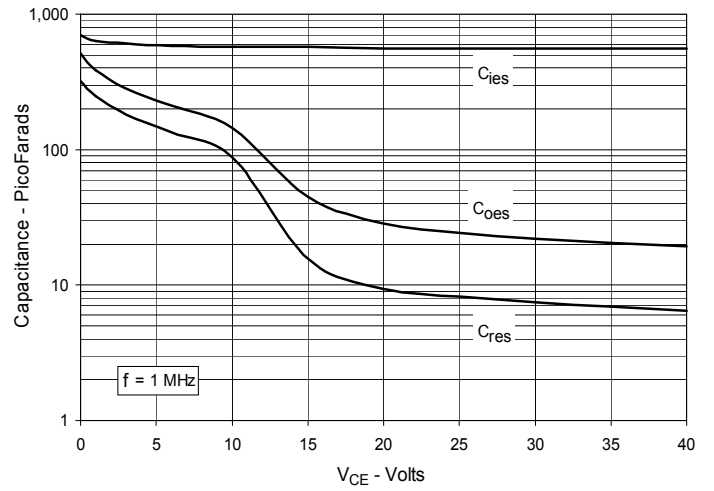


Fig. 11. Maximum Transient Thermal Impedance

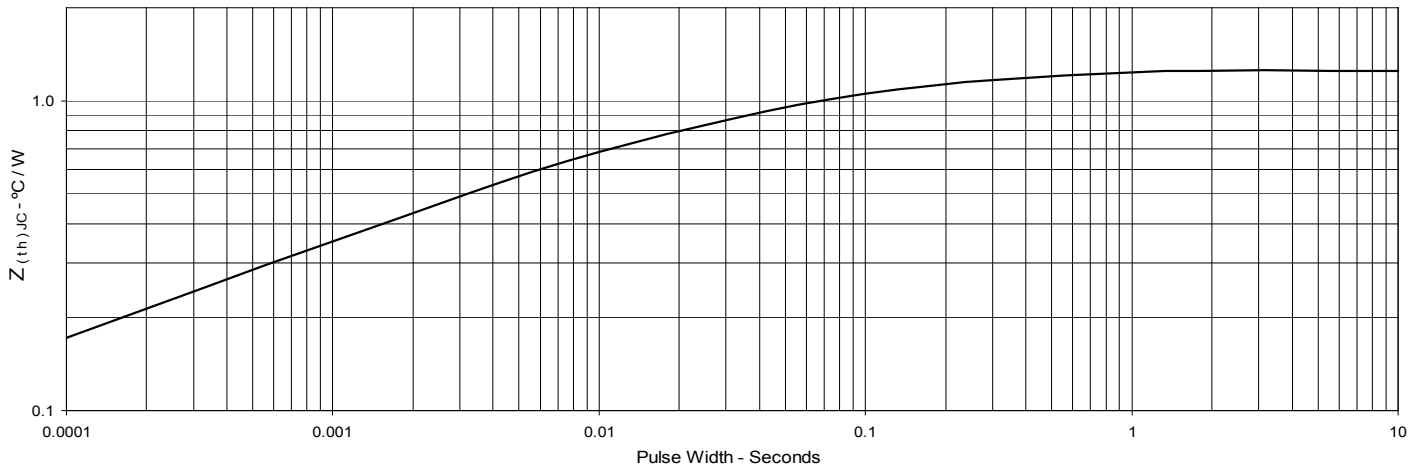


Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

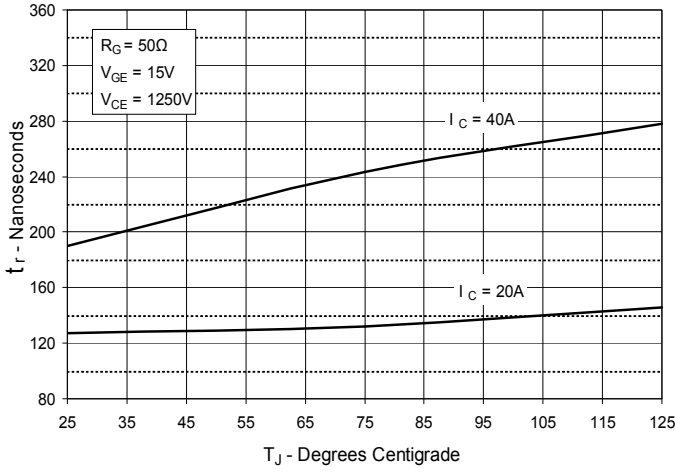


Fig. 13. Resistive Turn-on Rise Time vs. Collector Current

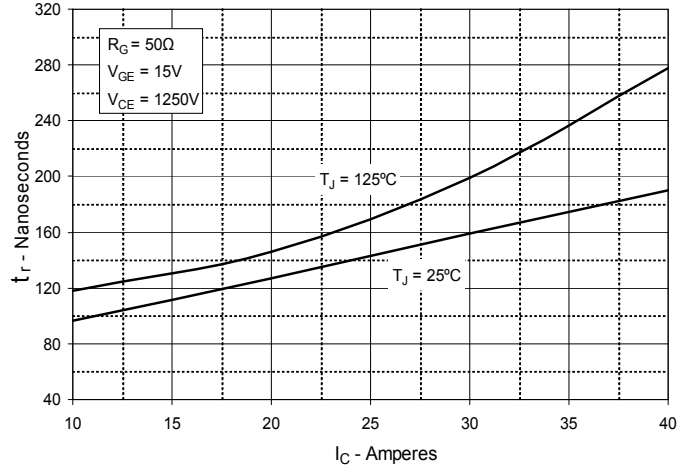


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

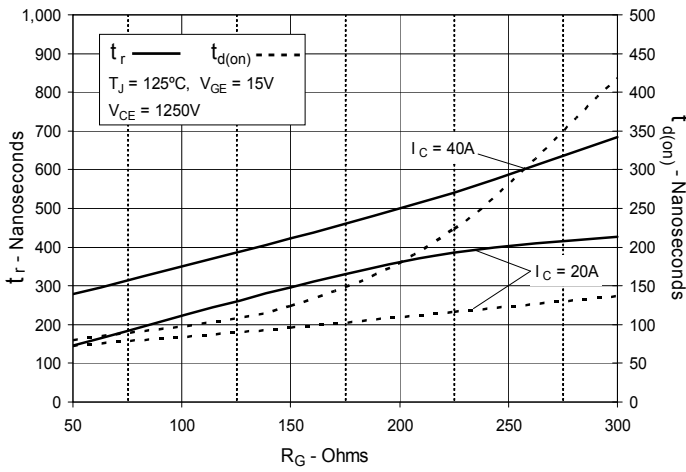


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

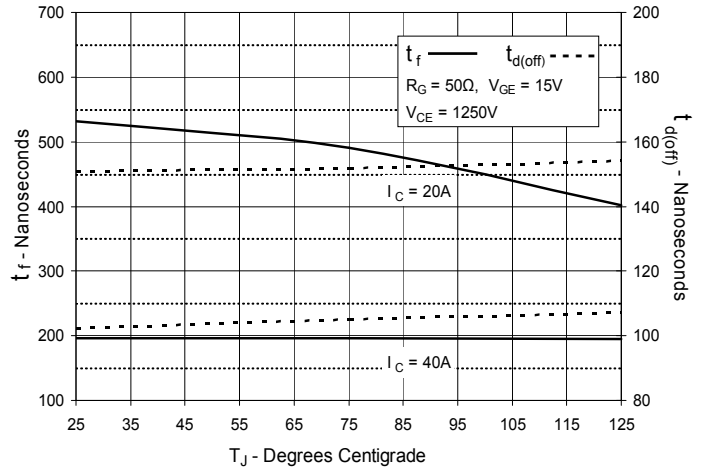


Fig. 16. Resistive Turn-off Switching Times vs. Collector Current

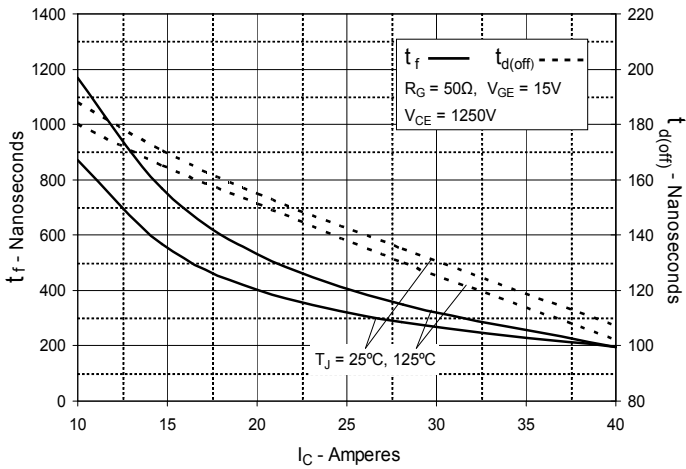


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance

