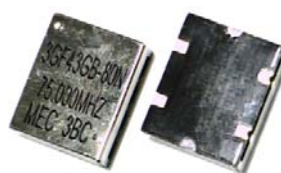
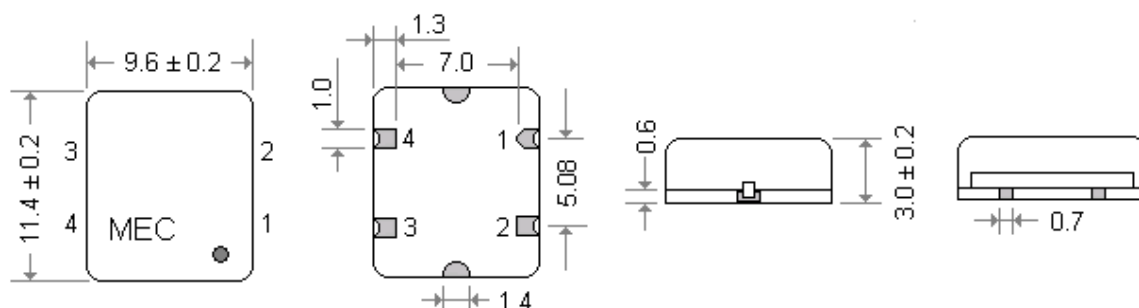


SMD CMOS output**11.4 x 9.6 x 3.0 mm****Phase Jitter < 4.0 ps [50.1 ~ 200.0 MHz]****Applications :**

- high-Q fundamental crystals and multiplier circuits with moderate jitter.

General Specifications

Parameters		Electrical Spec.							
Input Voltage (V_{DD})		3.3 V $\pm$ 5 %							
Frequency Range		50.1 ~ 200.0 MHz							
Output Wave Form		CMOS output							
Initial Freq. Accuracy (at 25 °C)		To tune to the nominal frequency with $V_c = 1.65V \pm 0.15V$							
Output Logic High " 1 "		90% V_{DD} (min.)							
Output Logic Low " 0 "		10% V_{DD} (max.)							
Frequency Deviation Range		Standard : ± 80 ppm (min.)							
Control Voltage Center / Control Voltage Range		1.65 VDC / 0.3 V to 3.0 V							
Integrated Phase Jitter (12 KHz to 20 MHz) .		2.3 ps (typical) ; 4.0 ps (max.) for 155.520 MHz							
Output Load		15 pF							
Rise Time (T_r) / Fall Time (T_f)		2.4 nSec. (typical) . Measured between 0.3V to 3.0V (15pF load)							
Duty Cycle		50% $\pm$ 10% [50% $\pm$ 5% is also available]							
Current Consumption		50 ~ 200 MHz : 40 mA (max.)							
Start - Up Time (T_s)		10 m sec. (max.) ; 5 m sec. (typical)							
Input Impedance		2 M Ω (min.)							
Storage Temperature		- 50°C to 100°C							
Aging		± 3 ppm per year (max.)							
Frequency Stability ⁽¹⁾ Codes	Frequency Stability over Operating Temperature Range	± 25 ppm	± 50 ppm	± 100 ppm	If non-standard , please enter the desired stability after the " C " or " I " For example : " C20 " ± 20 ppm over -10°C to +70°C ; " I20 " ± 20 ppm over -40°C to +85°C				
	Commercial (-10°C to +70°C)	A	B	C					
	Industrial (-40°C to +85°C)	D	E	F					
Phase Noise (typical) [155.520 MHz]		Offset	10 Hz	100 Hz	1K Hz	10 KHz	100KHz	1 MHz	10 MHz
		dBc / Hz	-65	-95	-120	-128	-122	-120	-140

Outline Dimensions (Unit : mm)

Pad Connections :
 Pad 1 : Voltage Control
 Pad 2 : Ground
 Pad 3 : Output
 Pad 4 : Supply Voltage

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