

Small Signal Product

Bi-directional ESD Protection Array

FEATURES

- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Meet IEC61000-4-5 (Lightning) rating. 5A (8/20µs)
- Protects two directional I/O lines
- Working voltage: 5V
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)

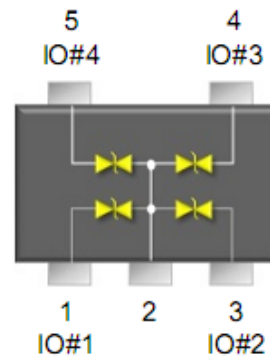


SOT-23-5



MECHANICAL DATA

- Case: SOT-23-5 small outline plastic package
- Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 208 guaranteed
- Moisture sensitivity: level 1, per J-STD-020
- High temperature soldering guaranteed : 260°C/10s
- Weight: 14 ± 0.5 mg
- Marking code: S5V



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T _A =25°C unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20µs waveform)	P _{PP}	100	W
Peak Pulse Current (tp=8/20µs)	I _{PP}	2.5	A
ESD per IEC 61000-4-2 (Air)	V _{ESD}	± 15	KV
ESD per IEC 61000-4-2 (Contact)		± 8	
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

PARAMETER	SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage	V _{RWM}	-	5	V
Reverse Breakdown Voltage	V _(BR)	6.5	-	V
Reverse Leakage Current				
Clamping Voltage	V _C	-	9.8	V
			15	
Junction Capacitance	C _J	20		pF

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RATINGS AND CHARACTERISTICS CURVES

($T_A=25^\circ\text{C}$ unless otherwise noted)

Fig. 1 Non-Repetitive Peak Pulse Power VS. Pulse Time

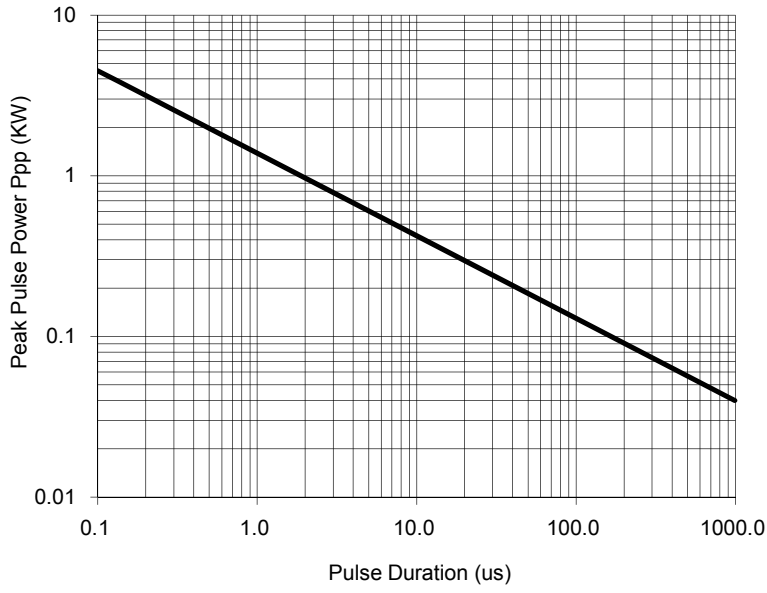


Fig. 2 Pulse Waveform

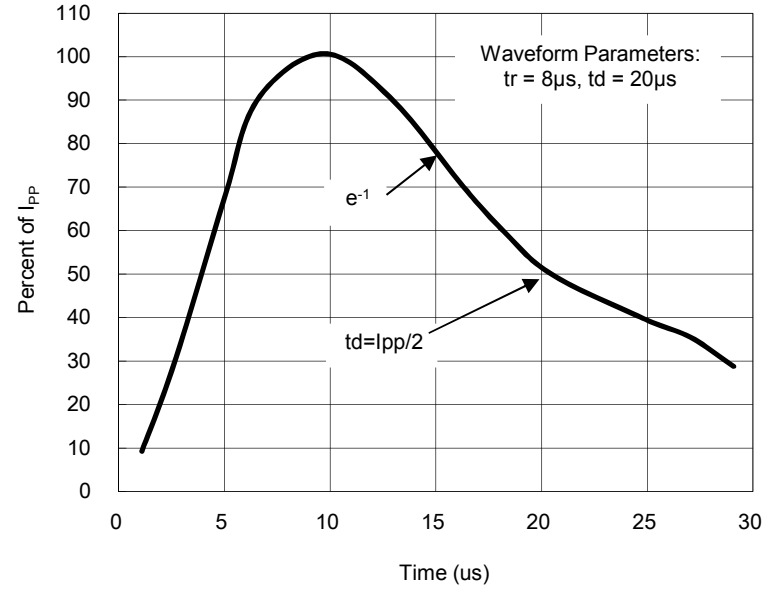


Fig.3 Admissible Power Dissipation Curve

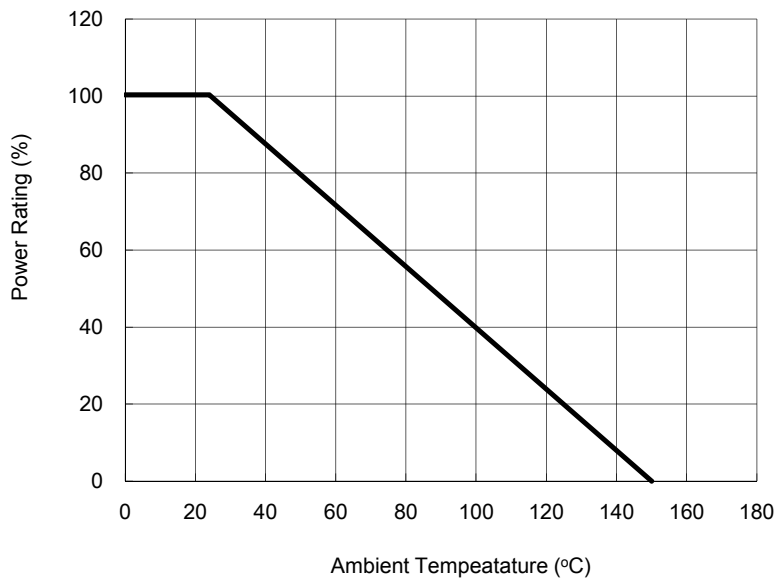


Fig. 4 Typical Junction Capacitance

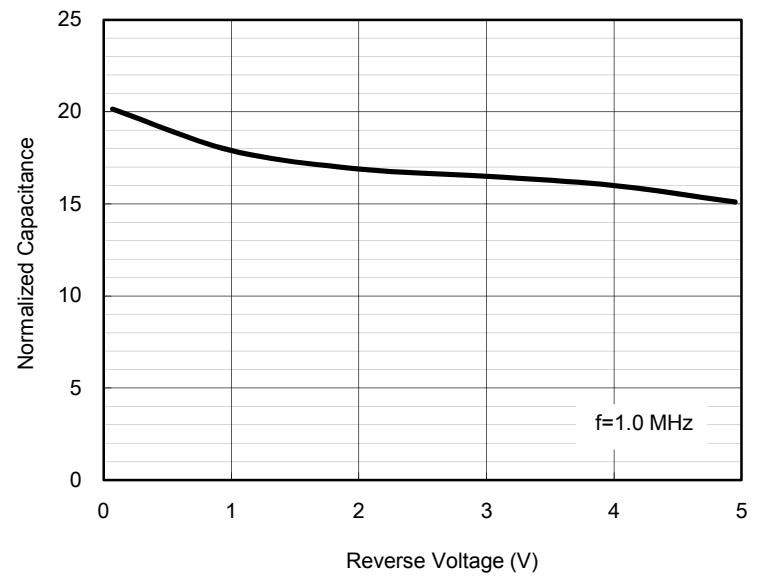
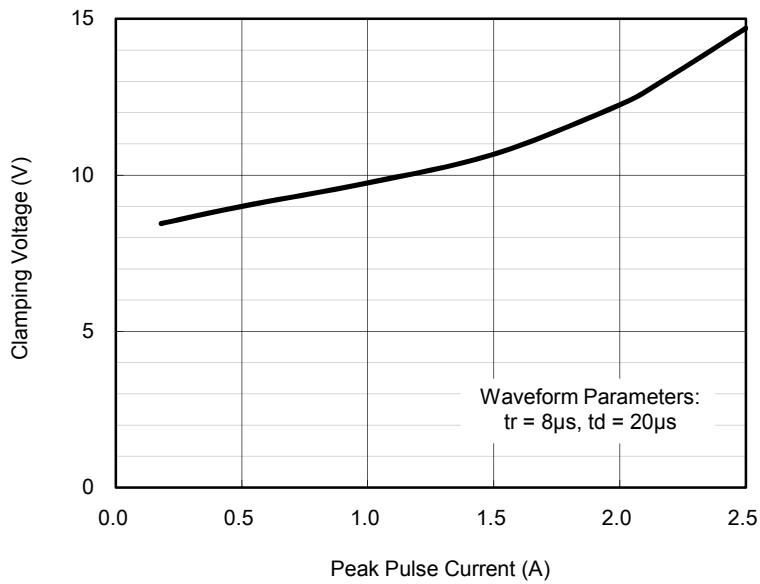
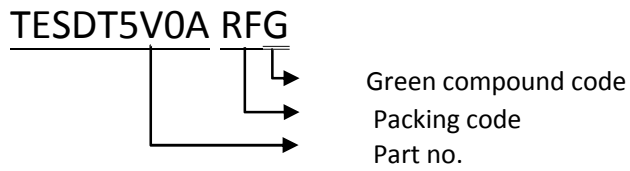


Fig. 5 Clamping Voltage VS. Peak Pulse Current

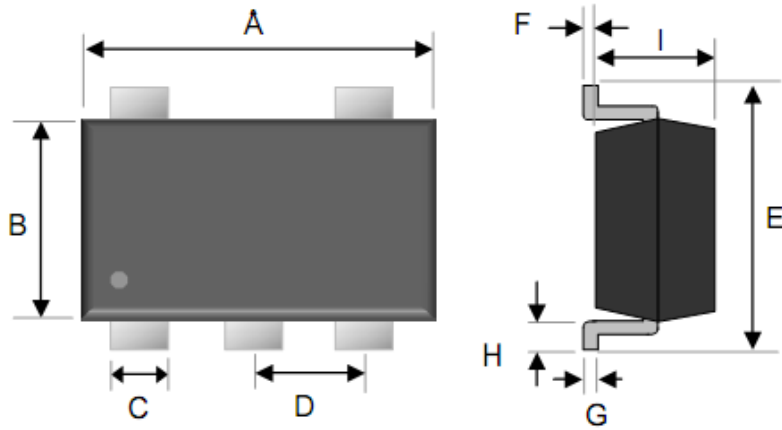


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ORDER INFORMATION (EXAMPLE)

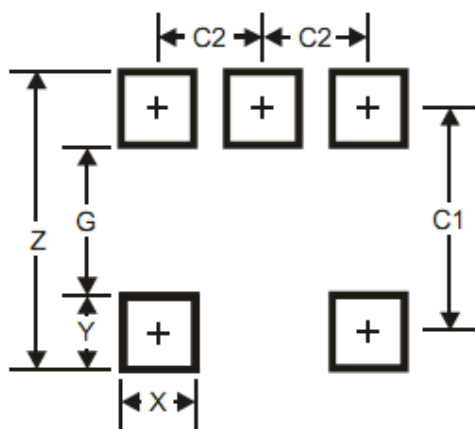


PACKAGE OUTLINE DIMENSIONS
SOT-23-5



DIM.	Unit(mm)		Unit(inch)	
	Min	Max	Min	Max
A	2.70	3.10	0.106	0.122
B	1.50	1.80	0.059	0.071
C	0.35	0.50	0.014	0.020
D	0.95 REF		0.037 REF	
E	2.60	3.00	0.102	0.118
F	-	0.10	-	0.004
G	0.10 REF		0.004 REF	
H	0.37	-	0.015	-
I	1.00	1.3	0.039	0.051

SUGGEST PAD LAYOUT



DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
Z	3.20	0.126
G	1.60	0.063
X	0.55	0.022
Y	0.80	0.031
C1	2.40	0.094
C2	0.95	0.037

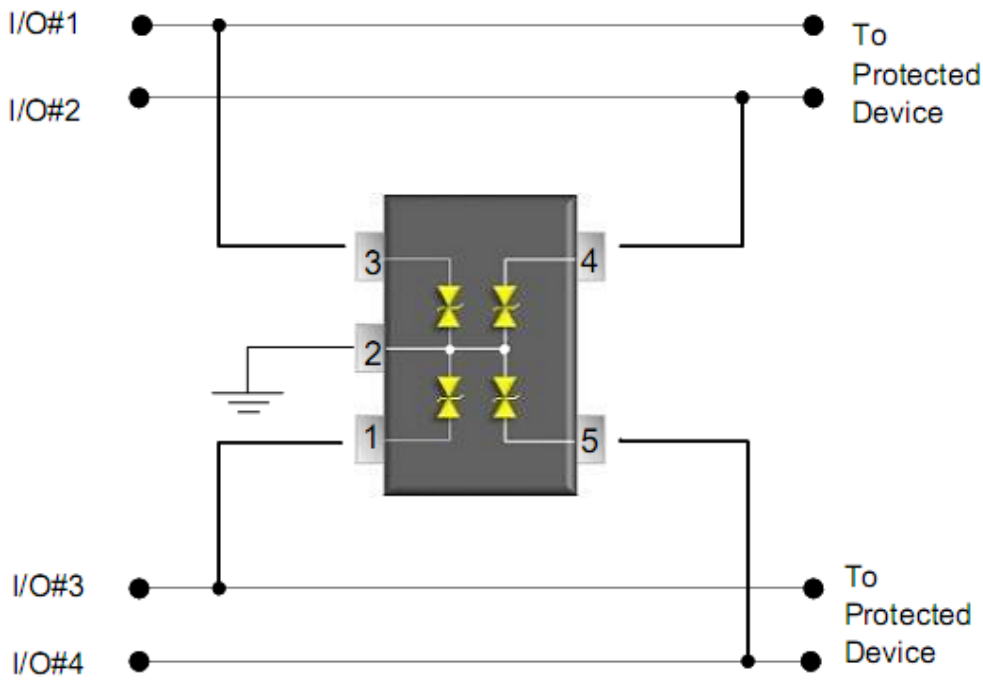
Note: 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

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APPLICATIONS INFORMATION

- ◇ Designed to protect data line interfaces
- ◇ Designed to protect four data lines from transient over-voltages by clamping them to a fixed reference
- ◇ Designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge (ESD), electrical fast transients (EFT), and Surge
- ◇ The internal TVS diode prevents over-voltage on the power line, protecting any downstream components

CIRCUIT BOARD LAYOUT RECOMMENDATIONS



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