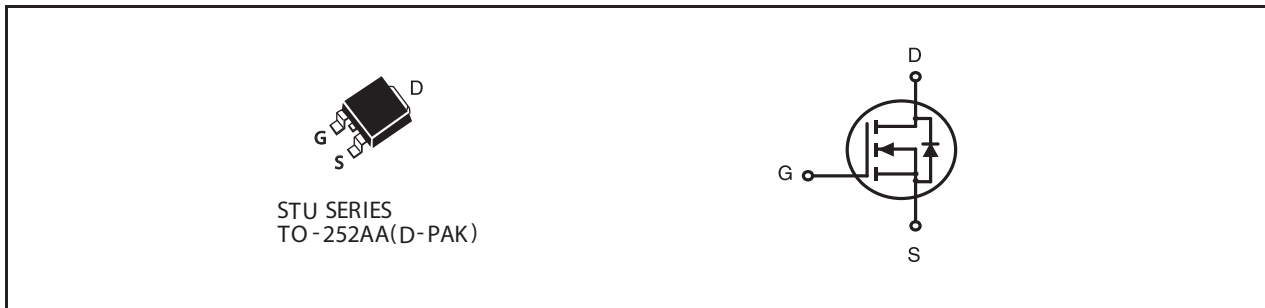


**N-Channel Logic Level Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

VDSS	ID	RDS(ON) (mΩ) Max
100V	12A	140 @ VGS=10V
		245 @ VGS=4.5V

**FEATURES**

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- TO-252 Package.

**ABSOLUTE MAXIMUM RATINGS (TA=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	100	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	12
		T <sub>C</sub> =70°C	9.6
I <sub>DM</sub>	-Pulsed <sup>b</sup>	35	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	25	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	50
		T <sub>C</sub> =70°C	32
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

**THERMAL CHARACTERISTICS**

R <sub>θ JC</sub>	Thermal Resistance, Junction-to-Case <sup>a</sup>	2.5	°C/W
R <sub>θ JA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	50	°C/W

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## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250μA	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.8	3	V
R <sub>DS(on)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =6A		110	140	m ohm
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =5A		170	245	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =6A		5		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		480		pF
C <sub>oss</sub>	Output Capacitance			47		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			29		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =50V I <sub>D</sub> =1A		9.8		ns
t <sub>r</sub>	Rise Time			10.2		ns
t <sub>D(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		18		ns
t <sub>f</sub>	Fall Time			8.5		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =6A, V <sub>GS</sub> =10V		7.8		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =6A, V <sub>GS</sub> =10V		1.3		nC
Q <sub>gd</sub>	Gate-Drain Charge			2.9		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A		0.775	1.3	V

### Notes

- Surface Mounted on FR4 Board, t ≤ 10sec.
- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.
- Starting T<sub>J</sub>=25°C, L=0.5mH, V<sub>DD</sub> = 50V. (See Figure13)

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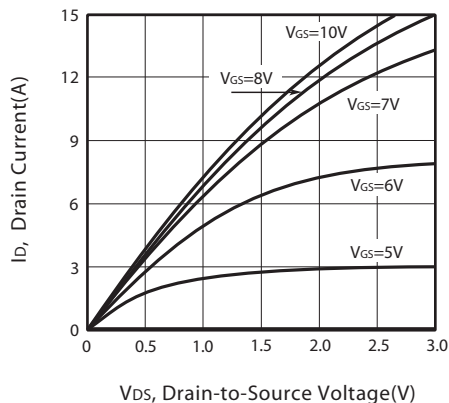


Figure 1. Output Characteristics

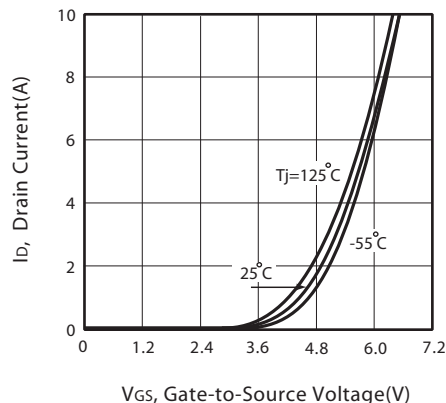


Figure 2. Transfer Characteristics

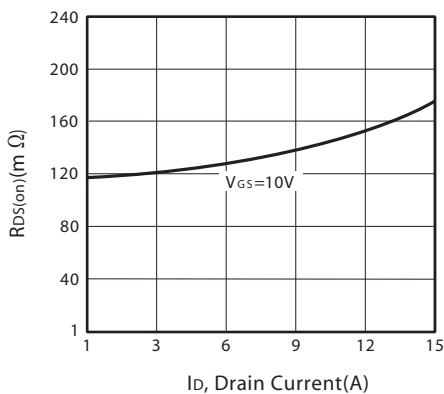


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

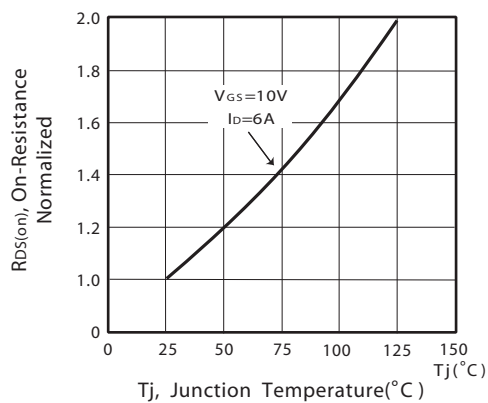


Figure 4. On-Resistance Variation with Drain Current and Temperature

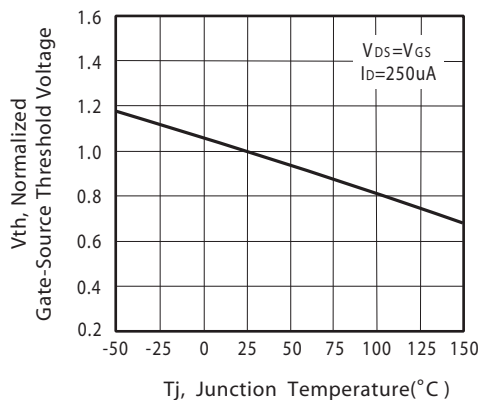


Figure 5. Gate Threshold Variation with Temperature

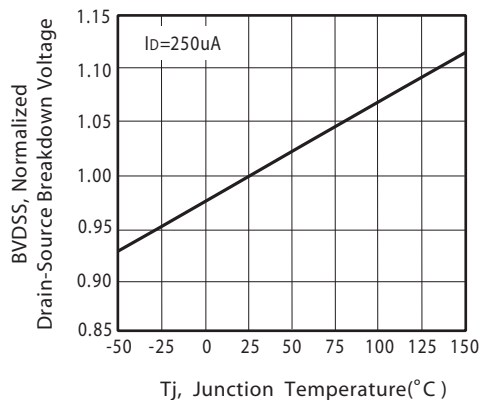


Figure 6. Breakdown Voltage Variation with Temperature

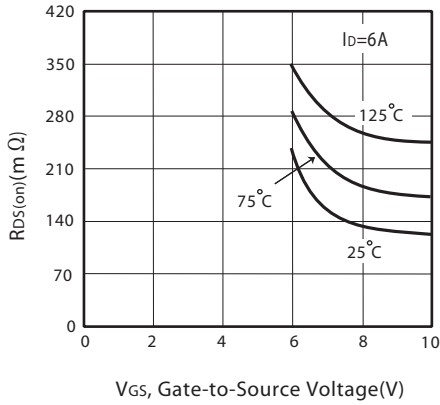


Figure 7. On-Resistance vs. Gate-Source Voltage

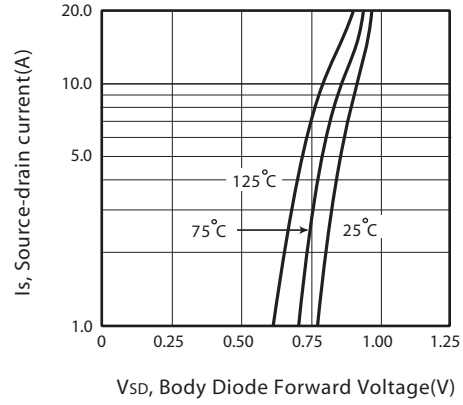


Figure 8. Body Diode Forward Voltage Variation with Source Current

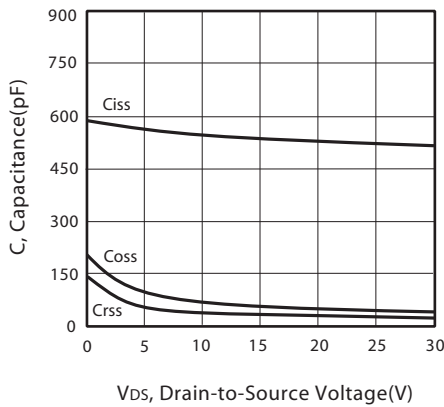


Figure 9. Capacitance

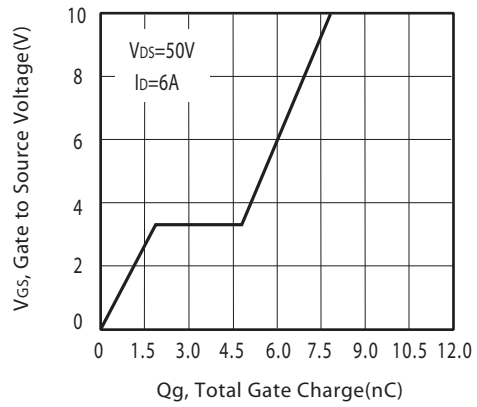


Figure 10. Gate Charge

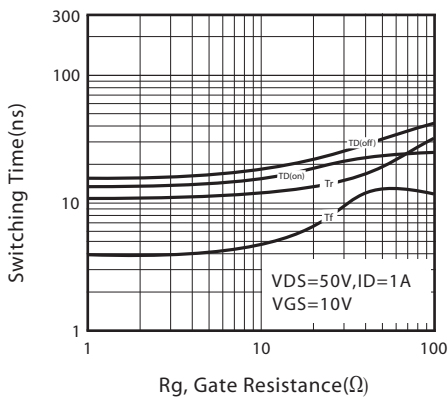


Figure 11. switching characteristics

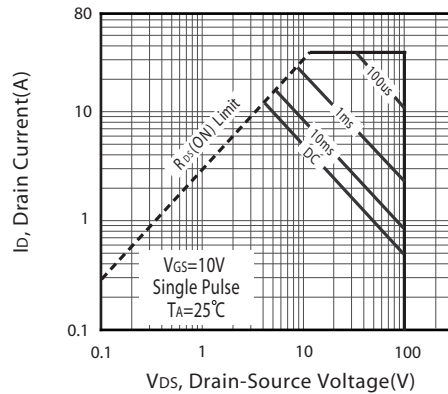
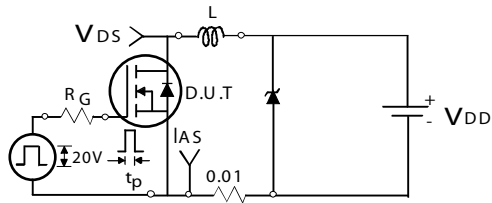
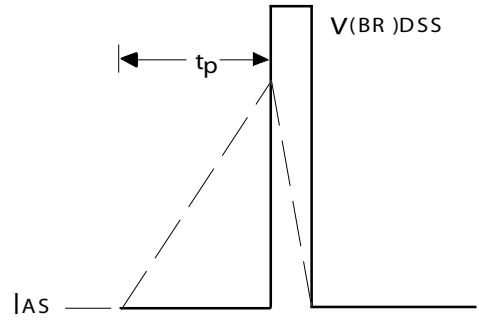


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

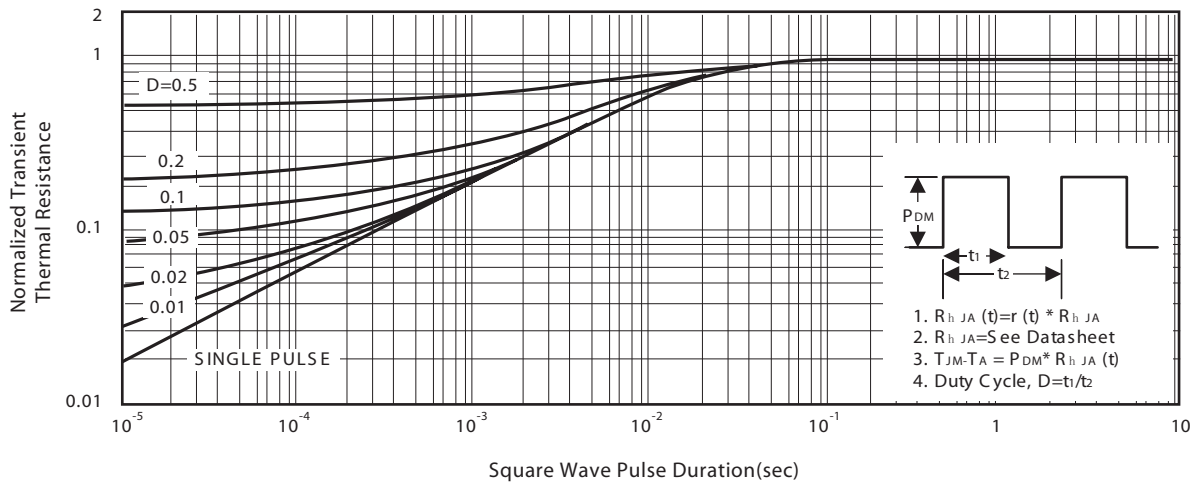
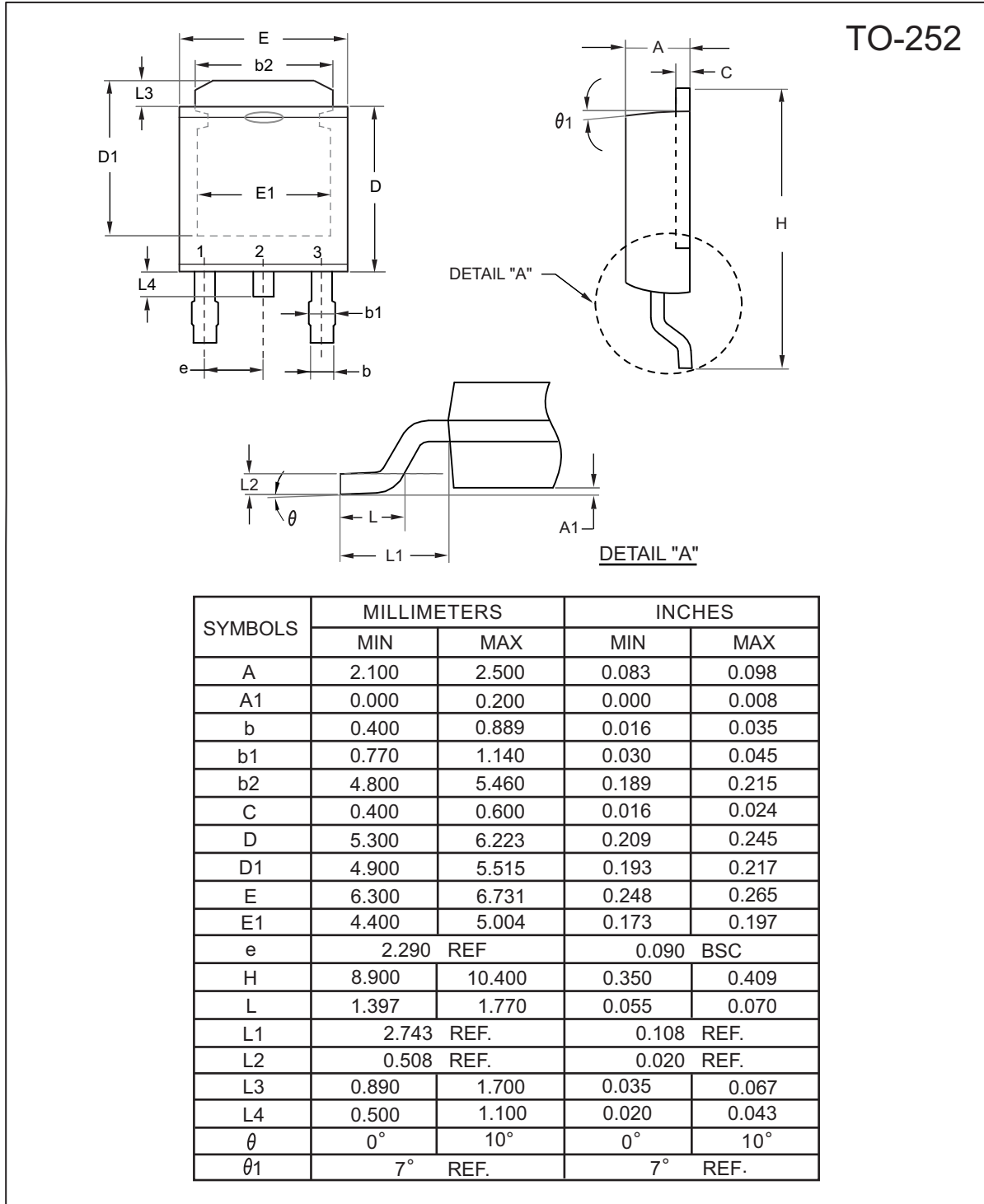


Figure 14. Normalized Thermal Transient Impedance Curve

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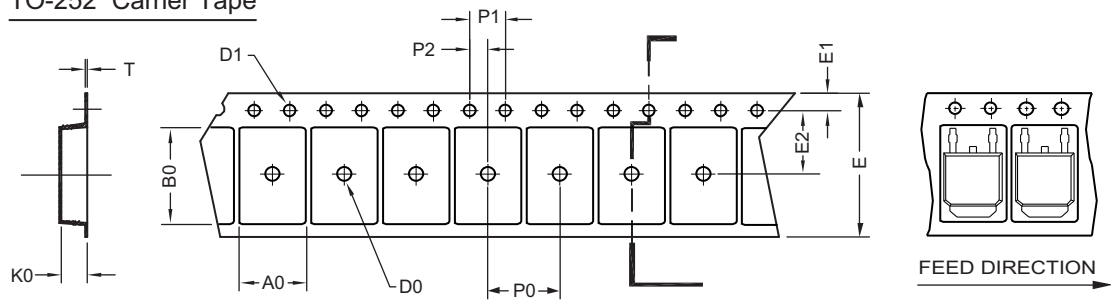
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## TO-252 Tape and Reel Data

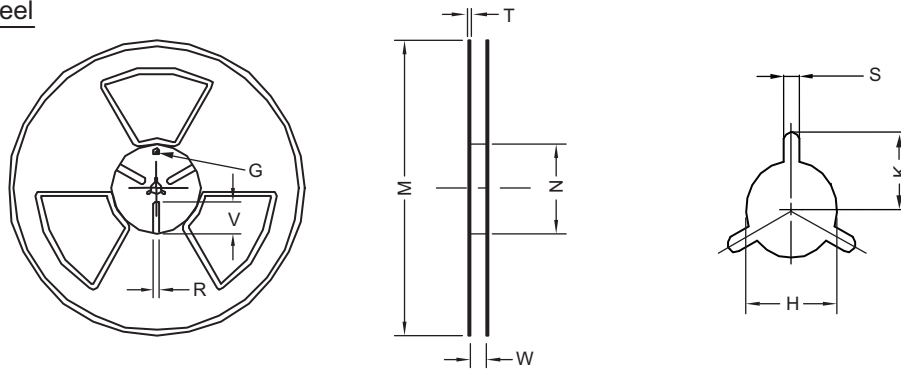
### TO-252 Carrier Tape



UNIT:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252 (16 mm)	6.96 ±0.1	10.49 ±0.1	2.79 ±0.1	φ2	φ1.5 +0.1 -0	16.0 ±0.3	1.75 ±0.1	7.5 ±0.15	8.0 ±0.1	4.0 ±0.1	2.0 ±0.15	0.3 ±0.05

### TO-252 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ 330	φ 330 ± 0.5	φ 97 ± 1.0	17.0 + 1.5 - 0	2.2	φ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---