MAX64180

HD H.264 CODEC

Data Sheet

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Revision History

This section describes the changes that were implemented in the Data Sheet. The changes are listed by revision.

REVISION	SECTION	DESCRIPTION
1.1	Revision History	Added table of abbreviations
	1	Changed video capture to video subsystem
	2.2.1	Moved Video Encoders and Decoders section to Chapter 3, Section 3.3 Encoder Subsystem
	3.1/3.2	Renamed Video Interface to Video Subsystem and Audio Interface to Audio Subystem
	3.1.3/3.1.4	Expanded abbreviations for video pixel clock signal names, video input signals
	3.3	Moved Section 2.2.1 to Section 3.3 Encoder Subsystem
	3.6.1	Added that the UART debug port should always be connected to a serial terminal
	3.6.4	Added contact Maxim Technical Support to program the device for drive strength. Expanded DS as Drive Strength
	3.8.1	Expanded signal names in Table 3-11
	3.11.4	Changed the title “Pin Multiplexing, GPIOs” to Pin Muxing
	4.2	Added Interface and Power Domain columns in Table 4-14
	5	Expanded signal names in Table 5-18, 5-19, 5-20, 5-22
	6.4	Modified text and removed pin entries that do not have multiple functions in Table 6-28
	6.4.4	Removed Figure 6-41 Host Connections
	6	Removed ALT. and GPIO columns in Tables 6-29 through 6-45
	7	Changed Thin Flipchip Ball Grid to Chip Scale Thin Ball Grid Array
	7.4	Updated chip revision in marking from A0 to A1
	8	Updated Ordering Information MAX64180CXO+
1.0	-	First Release

Abbreviations

Product-specific abbreviations are defined wherever applicable in the text. The most commonly used industry abbreviations applicable to the product are listed below.

ABBREVIATION	DESCRIPTION
AAC-LC	Advanced Audio Coding-Low Complexity
ADC	Analog to Digital Converter
CSBGA	Chip Scale Ball Grid Array
DMA	Direct Memory Access
EAV	End of Active Video
FPS	Frames per Second
GPIO	General Purpose Input/Output
HD	High Definition
HDMI	High Definition Multimedia Interface
HDR	High Dynamic Range
I^2C	Intelligent Interface Controller
I^2S	Inter-IC Sound
IPC	Interconnecting and Packaging Electronic Circuits
ISP	Image Signal Processing
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
MJPEG	Moving Joint Photographic Experts Group
MPEG-TS	Moving Photographic Experts Group - Transport Stream
PC	Personal Computer
PCM	Pulse Code Modulation
PLL	Phase Lock Loop
PHY	Physical Interface
PWM	Pulse Width Modulator
RAM	Random Access Memory
RGB	Red Green Blue
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances
SAV	Start of Active Video
SD	Standard Definition
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SMS	Short Message Service
SNR	Signal to Noise Ratio
TWI	Two-wire Interface
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
VGA	Video Graphics Array

1 Introduction

The MAX64180 is a compression camera System-on-Chip (SoC) that enables high-quality internet video conferencing in environments with poor lighting and poor acoustics such as a home living room. It performs all video and audio processing required for an internet compression camera application, including video compression, image signal processing, audio echo cancellation, audio beamforming, audio noise suppression, and audio compression and decompression. Combining high integration with advanced video processing, the MAX64180 SoC is a cost-effective ideal solution for Skype TVs, web, and IP camera applications.

The MAX64180 is a highly integrated, low-power, H.264 codec device that supports encoding of video up to 720p30 High Definition (HD) resolution. It incorporates the latest video encoding capabilities including Baseline, Main, and High profile H.264 codec. It also supports a MJPEG codec and a MPEG-2 decoder.

The MAX64180 contains a configurable hardware-based Video subsystem, Encoder subsystem, and an Audio subsystem. It also includes an ARM9 based on-chip subsystem and a host of peripherals: USB, UART, Pulse Width Modulator, and SPI serial interfaces.

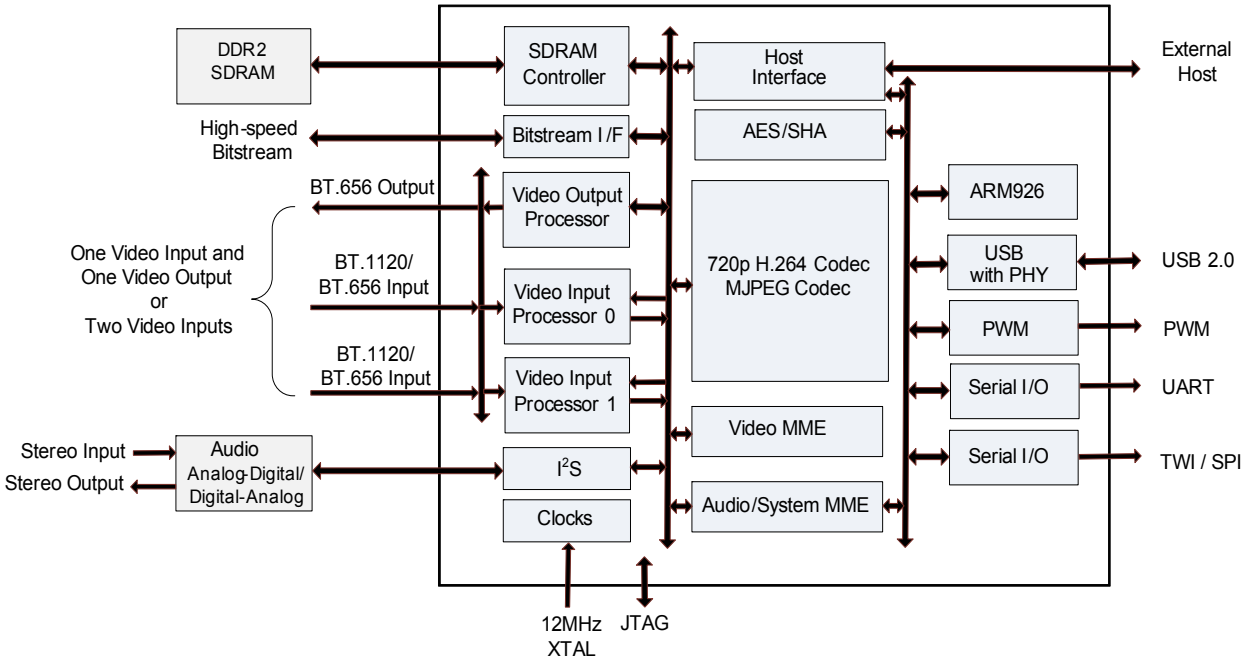


Figure 1-1. MAX64180 Block Diagram

The Video and Audio subsystems comprise two real-time, programmable Multimedia Engines (MMEs). One MME controls the video codecs and input output processors, while the other MME implements audio codecs.

The Video Input Processors (VIPs) in the Video subsystem accept video from external video ports, capture the video, and store it in memory. The VIPs support filtering, cropping, and rescaling the captured video. The Video Output Processor (VOP) streams video to output.

1.1 Features

High-Quality Video and Audio Encoding

- 720p30 video resolution
- H.264 Main, Baseline, and High profile tools
- Spatial filter
- Edge preserving noise reduction filter
- Motion Adaptive Temporal filter

Flexible User Configurations

- Skype TV compatibility
- Video input: resolution (scaling or cropping), frame rate, filtering
- Compression: number of streams, bit rate, H.264 tools
- Video output: compositing, scaling, cropping, frame rate, graphics overlay

High Level of System Integration

- USB connection to the Host device
- Low power consumption
- 200MHz ARM9 processor
- Dedicated audio processor
- Hardware acceleration for data security: Advanced Encryption Standard (AES) and Secure Hashing Algorithm (SHA)
- USB 2.0 including PHY

1.2 Applications

- Television based internet video conferencing
- Table PC based internet video conferencing

1.3 Additional Documentation

In addition to the Data Sheet, the Maxim web site offers an extensive library of documentation, support files, and application materials specific to each device. Visit and register as a member on the Maxim web site to keep abreast of the latest innovations from research and development teams and the most current product and application documentation. The address of the Maxim web site is www.maxim-ic.com.

1.4 Trademark Information

The following provides registered trademarks and trademarks listed in the MAX64180 Data Sheet.

- ARM926 is a trademark of ARM Limited.
- Skype is a trademark owned by Skype Limited, Skype Technologies, S.A..
- SPI is a trademark owned by Motorola, Inc.
- I^2C is a registered trademark owned by NXP Semiconductors N.V., founded by Philips Electronics.

2 General Description

The MAX64180 H.264 codec SoC is a 720p30 codec. The chip encompasses an ARM9 processor and a complete set of SoC features as shown in Table 2-1.

Table 2-1. MAX64180 SoC Features

FEATURES	MAX64180
High Definition (HD) H.264 Codec	720p30
MPEG-2 Decoder	✓
JPEG Codec	✓
Video: One Video Input/One Video Output: Two 8-bit interfaces or Two Video Inputs: One 16-bit interface, no output	✓
Video Input Processors	2
Video Output Processor	1
Audio Input Port	1
Audio Output Port	1
Audio Codecs	✓
High-speed Bitstream I/O or SPI	✓
Embedded ARM926-EJ Processor	✓
Host Slave Mode Operation	✓
USB 2.0 Host or Device	✓
16-bit DDR2 SDRAM Interface	✓
Two-wire Interface	1
UART	1
Pulse Width Modulator	1
GPIO, Shared	20
GPIO, Dedicated	4

2.1 Features

Video Inputs

- Two advanced Video Input Processors (VIPs)
- Two 8-bit video ports: one input port, one bidirectional port
- 100MHz maximum speed I/O

Video Processing

- Spatial and temporal noise filtering
- Edge enhancement
- Statistic extraction for better compression
- Vertical and horizontal scalars using 8-tap polyphase filters
- Four field motion adaptive deinterlacer
- Impulse noise filter

Video Outputs

- One Video Output Processor (VOP)
- One 8-bit output
- 75MHz video output I/O

Video Codecs

- High Definition (HD) or Standard Definition (SD) H.264 codecs
  - High, Main, and Baseline profiles support for resolutions up to 1280 x 720 at 30fps
  - Single HD or multi-stream encoding support
  - H.264 codec up to level 4.1
  - Programmable resolutions and frame rates
  - Video bit rates: 64Kbps to 62.5Mbps
  - Interlaced and Frame capturing and encoding support
- MPEG-2 Decoder
  - HD and SD decoder
  - Real time MPEG-2 to H.264 transcoding
  - Multi-stream SD MPEG-2 decoding
- JPEG Codec
  - JPEG encoder and decoder
  - HD or SD MJPEG support
  - Exchangeable Image File Format (EXIF) support

Audio Codecs

- High-fidelity, 2-channel Audio Coding-Low Complexity (AAC-LC) codec
- MPEG-1/2 Audio Layer II codec (MP2)
- MPEG-1/2 Audio Layer I and III decoder (MP1)
- Pulse Code Modulation (PCM) format
- G.711, G.722, G.726 codec
- Flexible bit rates and sample rates

Audio I/O

- One I^2S Audio input port and one I^2S Audio output port
- One Sony/Philips Digital Interface (S/PDIF) output port

Integrated ARM9 Processor

- 240MHz general purpose processor
- 16kByte Data cache
- 16kByte Instruction cache
- 16kByte Scratch pad memory

Memory Interface

- DDR2 SDRAM memory
- 16-bit data at 233MHz

Peripheral Interfaces

- One Two-wire interface port
- One UART port
- One Pulse Width Modulator (PWM)
- High-speed Bitstream I/O or one SPI
- USB 2.0 port including the physical layer
- AES and SHA hardware acceleration
- Up to 24 GPIO with four dedicated GPIO pins

Power and Voltage

- Core voltage: 1.05V ±5%
- SDRAM voltage: 1.8V ±0.1V
- I/O voltages: 1.8V, 2.5V, 3.3V ±5%
- On-chip audio, video Phase Lock Loops (PLLs) driven from a single crystal
- Typical power consumption is 950mW or less

Packaging

- 248-pin CTBGA, 10x10mm, 0.5mm pitch, RoHS compliant

2.2 General Overview

The sections below provide a high-level description on the various modules inside the MAX64180.

2.2.1 Video I/O Ports

The MAX64180 includes two 8-bit video ports: video port 0 and video port 2. Video port 0 is a dedicated 8-bit input port. Video port 2 is a bidirectional 8-bit port that can be configured as an input or output. The two 8-bit ports can be combined to a single 16-bit input port. Output is not available when both the ports are used as a single 16-bit input port.

Each video input supports independent clocks and synchronization signals. The clock frequency can be driven up to 75MHz to support non-standard video inputs including HD sensors with 8-bit interfaces.

The MAX64180 receives video inputs in either BT.656 format on an 8-bit interface or BT.1120 format on a 16-bit interface. The MAX64180 can support the following configurations with the two video I/O ports:

Table 2-2. Video Input Formats

VIDEO RESOLUTION	FRAMES PER SEC.	PORTS
1600 x 1200	15	1 (8-bit)
1280 x 720	30	1 (8-bit)
640 x 480	30	1 (8-bit)

2.2.2 Video Input Processor

The two identical Video Input Processors (VIPs) perform high-quality image scaling. The VIPs extract video statistics, which is used to improve the compression efficiency of the codec. The VIPs process the brightness, contrast, and gamma correction of the luma component and adjust the hue and saturation characteristics of the chroma component. The maximum pixel rate that the VIPs can process corresponds to the video input resolution of 1280 x 720p at 30 frames per seconds.

2.2.3 Video Output Processor

The Video Output Processor (VOP) performs high-quality image scaling of uncompressed video, overlays it with two graphic planes, performs gamma and chroma adjustment, overlays a hardware cursor, and outputs the combined video to a video port. Each graphic plane can be from 1 to 32 bits. Graphic planes using less than eight bits use a Look-Up Table (LUT).

The video output can either be YUV 4:2:2 or RGB format via an 8-bit interface.

Table 2-3. Video Output Formats

VIDEO MODE	VIDEO OUTPUT
8-bit	YUV 4:2:2
RGB	8-8-8 over an 8-bit

The RGB (8-8-8) output can be used for driving LCD displays.

2.2.4 Video and Audio Multimedia Engines

The Video Multimedia Engine (MME) is a proprietary Reduced Instruction Set Computer (RISC) that is optimized for single cycle context switching and low power. The Video MME controls all aspects of the VIPs, video cores, and the VOP.

The Audio MME implements all audio codecs in firmware.

2.2.5 Audio Interface

The audio interface contains a single audio input and single audio output interface. The audio interface receives audio inputs from an I^2S interface. The audio interface comprises:

- One I^2S input,
- One I^2S output, and
- One S/PDIF output

The I^2S input shares a common clock, sample rate, and a common format with I^2S audio output and S/PDIF output.

2.2.6 Memory Interface

The DDR2 SDRAM external memory device stores video, audio, and computational data during encoding or decoding video. The memory controller addresses 16-bit data at 233MHz.

2.2.7 ARM Processor

The MAX64180 has an embedded ARM9 processor that handles system functions and manages peripheral interfaces. The processor runs at speeds of up to 200MHz. The processor acts as the overall system controller and performs all system level functions. It is not used for any audio or video codec functions.

2.2.8 AES and SHA Hardware Acceleration

The MAX64180 design includes hardware acceleration for Advanced Encryption Standard (AES) and Secure Hashing Algorithm (SHA). The AES accelerator supports CBC (Cipher Block Chaining), CTR (Counter mode), ECB (Electronic Code Book), and CCM (CTR with CBC) modes with 128-, 192-, and 256-bit keys for secure data storage and transmission. The SHA accelerator supports the creation of 128-, 224-, and 256-bit digests for digital signatures and digital time stamps.

2.3 Peripheral Interfaces

A number of peripheral interfaces for I/O control and system integration are described below.

2.3.1 USB 2.0 Interface

The high-speed USB 2.0 interface can operate as Device or Host at speeds of up to 480Mbps. The USB interface includes the Physical Layer.

2.3.2 Serial Interfaces

The MAX64180 serial interfaces include UART for communication, Pulse Width Modulator (PWM) for control, Two-wire Interface (TWI) and Serial Peripheral Interface (SPI) for device control.

The MAX64180 comprises four dedicated General Purpose Input/Output (GPIO) pins and up to 20 shared GPIO pins for system control. The shared GPIO pins are multiplexed with other functions, which are available only when the primary or alternate function is not being used. For example, if a design does not require an SPI interface (see “SPI/Bitstream Interface AC Timing” on page 72), the four pins dedicated to SPI interface can be used as GPIO pins.

3 Functional Description

This section provides detailed information on the architecture of the MAX64180.

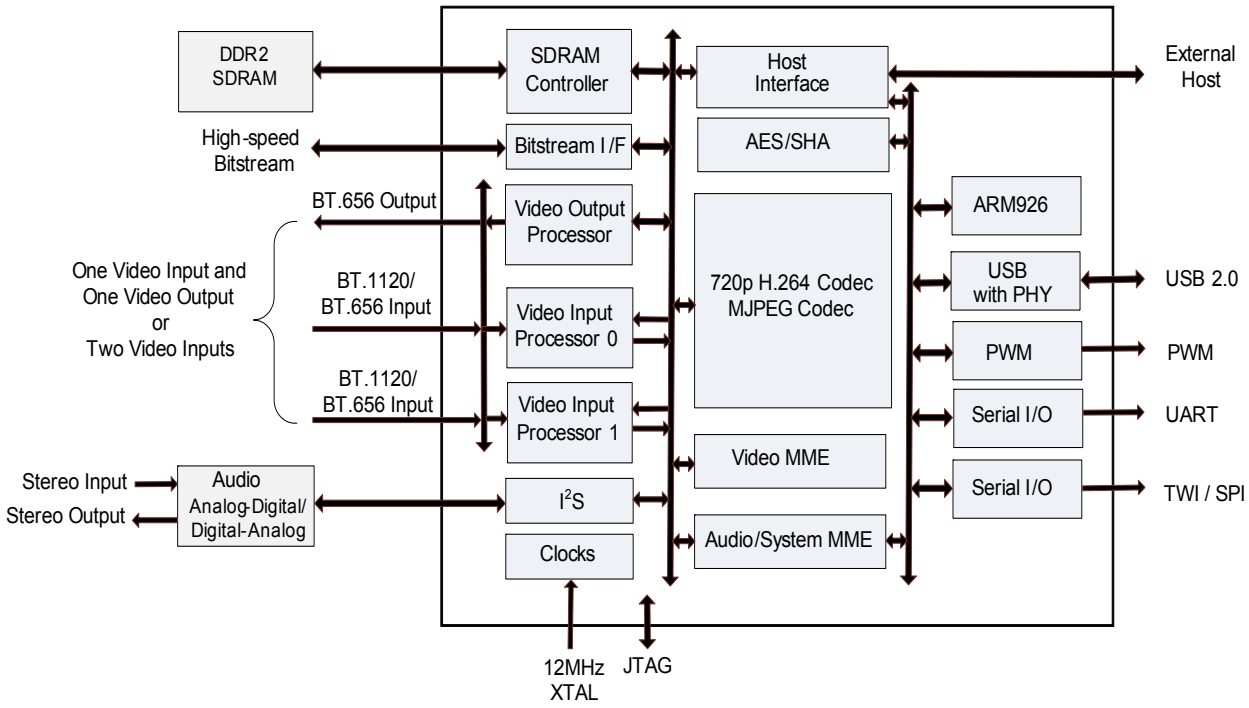


Figure 3-2. Functional Block Diagram

3.1 Video Subsystem

The Video subsystem consists of two Video Input Processors (VIPs) and one Video Output Processor (VOP). The VIP captures input video while the VOP outputs video from the chip. The video input signals are routed through two video ports to the VIPs.

The MAX64180 provides two dedicated video I/O ports: video port 0 and video port 2. The ports can receive either two 8-bit video inputs in BT.656 format or a combined 16-bit video input in BT.1120 format for HD video.

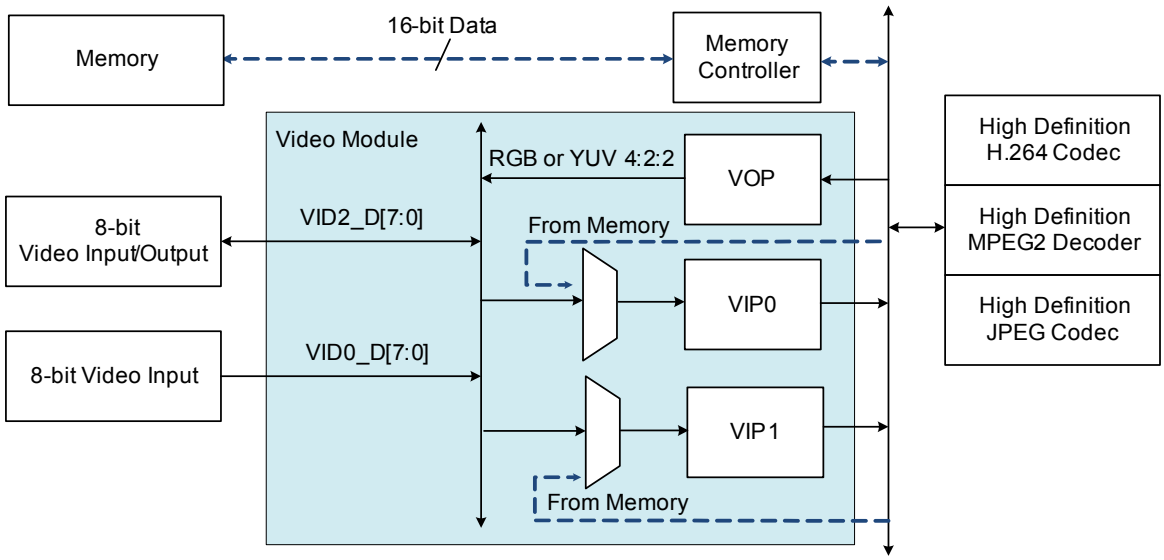


Figure 3-3. Video Subsystem

The MAX64180 can be configured to support a maximum of two inputs or one input and one output. Typical scenarios for video input and output include:

- One 8-bit input, one 8-bit output
- Two 8-bit inputs, no output
- One 16-bit input, no output

Video port 0 is a dedicated input port. Video port 2 can be reconfigured in the system depending on the system use-case since the port can be either an input or an output port.

3.1.1 Video Ports

Table 3-4 shows the video input connections for video port 0 which can be used only as an input port. Table 3-4 and Table 3-5 show the video input connections for video port 2, which can be used either as an input or output port.

Table 3-4. Video Input Signals for Video Port 0 and Video Port 2

PIN	8-BIT VIDEO PORT 0	8-BIT VIDEO PORT 2	16-BIT VIDEO PORTS 0 AND 2
VID0_D0	Video In Bit 0	-	Video In Bit 0
VID0_D1	Video In Bit 1	-	Video In Bit 1
VID0_D2	Video In Bit 2	-	Video In Bit 2
VID0_D3	Video In Bit 3	-	Video In Bit 3
VID0_D4	Video In Bit 4	-	Video In Bit 4
VID0_D5	Video In Bit 5	-	Video In Bit 5
VID0_D6	Video In Bit 6	-	Video In Bit 6
VID0_D7	Video In Bit 7	-	Video In Bit 7
VID0_FIELD	Video In Field	-	Video In Field
VID0_HSYNC	Horizontal Sync/HValid Signal 0	-	Horizontal Sync/HValid Signal 0
VID0_VSYNC	Vertical Sync/VValid Signal 0	-	Vertical Sync/VValid Signal 0
VID2_D0	-	Video In Bit 0	Video In Bit 8
VID2_D1	-	Video In Bit 1	Video In Bit 9
VID2_D2	-	Video In Bit 2	Video In Bit 10
VID2_D3	-	Video In Bit 3	Video In Bit 11
VID2_D4	-	Video In Bit 4	Video In Bit 12
VID2_D5	-	Video In Bit 5	Video In Bit 13
VID2_D6	-	Video In Bit 6	Video In Bit 14
VID2_D7	-	Video In Bit 7	Video In Bit 15
VID2_FIELD	-	Video In Field	-
VID2_HSYNC	-	Horizontal Sync/HValid Signal 2	-
VID2_VSYNC	-	Vertical Sync/VValid Signal 2	-

Table 3-5. Video Output Connections: Video Port 2

PIN	8-BIT VIDEO PORT 2
VID2_D0	Video Out Bit 0
VID2_D1	Video Out Bit 1
VID2_D2	Video Out Bit 2
VID2_D3	Video Out Bit 3
VID2_D4	Video Out Bit 4
VID2_D5	Video Out Bit 5
VID2_D6	Video Out Bit 6
VID2_D7	Video Out Bit 7
VID2_FIELD	Video Out Field
VID2_HSYNC	Video Out Horizontal Sync
VID2_VSYNC	Video Out Vertical Sync

3.1.2 Video Control Signals

The MAX64180 has two sets of video control signals: Video Control 0 (VCO) and Video Control 2 (VC2). Each video control signal group consists of Horizontal Sync, Vertical Sync, and Field signals, which can also be used as line valid and frame valid signals.

Table 3-6. Video Control Signal Groups

VIDEO CONTROL SIGNAL GROUP	VIDEO SIGNALS
VC0	VID0_FIELD
	VID0_VSYNC
	VID0_HSYNC
VC2	VID2_FIELD
	VID2_VSYNC
	VID2_HSYNC

When the output port is active, the Video Output Processor is configured to output the correct video timing appropriate to the interface. The video control signals VC0 and VC2 can be assigned to any of the video ports with the following restriction:

- Video control signal group VC0 is always associated with the power plane for video port 0. Video control signal group VC2 is associated with the power plane for video port 2. If the power planes are connected to different power sources, the video control signal group must be assigned to a video port in the same power plane. See “Video I/O Power Domains,” page 29.

3.1.3 Video Clocks

Data and control signals are timed against the two video pixel clock signals: video pixel clock 0 and video pixel clock 2. The video pixel clock 0 (VID0_PIXCLK) is associated with video port 0 and video pixel clock 2 (VID2_PIXCLK) is associated with video port 2. The video pixel clock pins can be configured either as input or output pins. For example, VID0_PIXCLK drives the image sensor clock as an input. VID2_PIXCLK drives the external audio device as an output. The Video Input Processors and Video Output Processor can select any of the video pixel clock inputs as the reference for interface timing.

The video output clock pin, VID0_OUTCLK drives the video clock. The video output clock is only a clock source, and video interface signals are not timed against this pin. The video output clock is associated with only video port 0.

3.1.4 Video I/O Power Domains

The video input signals (VID0_D[7:0]) for video port 0, video control signal 0 (VC0), video pixel clock 0 (VID0_PIXCLK), and video output clock (VID0_OUTCLK) are all in the VID0 power domain.

The video input signals (VID2_D[7:0]) for video port 2, video control signal 2 (VC2), and video pixel clock 2 (VID2_PIXCLK) are in the VID2 power domain.

The video I/O power domains can be either tied to the same voltage on the board or tied to different voltages on the board. If the video I/O powered domains are tied to different voltages on the board, use the video control signal group associated with that power domain.

3.1.5 Video Input Processor (VIP)

The MAX64180 comprises two VIPs: VIP0 and VIP1. The VIPs perform:

- Scaling
- Cropping (can be used to reduce input prior to up-scaling)
- Luma processing
- Chroma processing
- Horizontal scaling
- Motion adaptive deinterlacing
- Vertical scaling
- Motion adaptive temporal filtering
- Pixel processing extracts video statistics to guide compression

Each VIP has a digital Video Interface (VIN) and a Video Preprocessor (VPP) module.

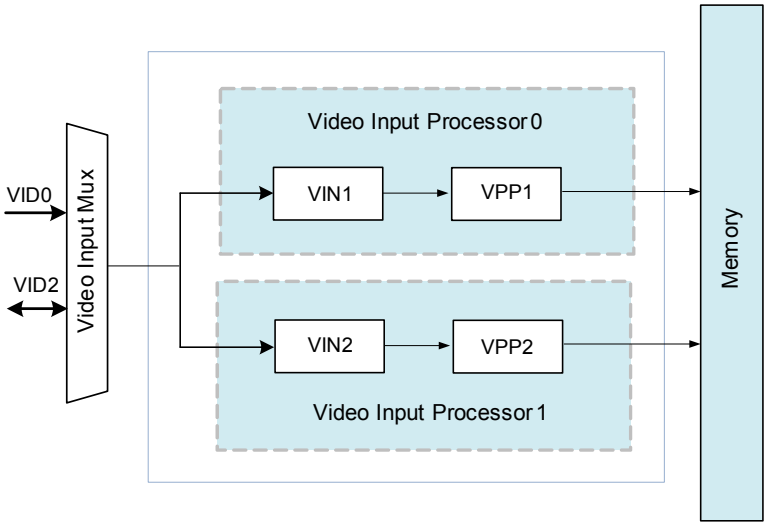


Figure 3-4. Video Input Processor

The key benefit of MAX64180 is the ability to support different resolutions for displays, such as local previewing and remote hosting. The MAX64180 accomplishes this by processing each input independently in the VIN and VPP blocks inside each VIP. For systems with a single 8-bit data input, the video input is replicated into two streams. Each stream is individually cropped, filtered, resized, and stored in memory. For systems with two 8-bit data inputs, each stream is individually processed and stored in memory.

Each VIN receives video input through the video ports, detects correct synchronization, performs cropping, reframes data, and provides separate luma and chroma outputs to the corresponding VIP for further processing.

The VPP receives data from VIP, performs spatial and temporal filtering on the data to reduce video noise. The VPP alters brightness, contrast, and performs gamma correction on the luma component of the video. It also adjusts the saturation and hue characteristics by processing the chroma component of the video. The input video is resized and stored in memory.

The data flow in the VIP is shown in Figure 3-5.

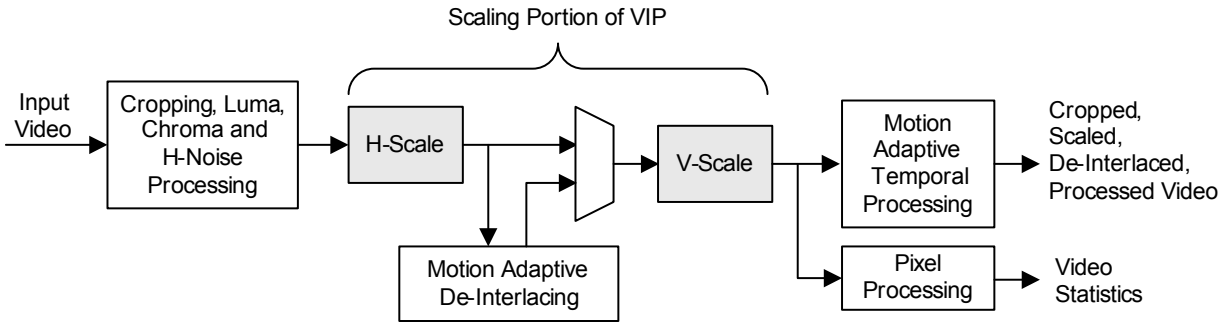


Figure 3-5. Video Input Processing Data Flow

The Horizontal and Vertical scale modules use an eight-tap, eight-phase programmable Finite Impulse Response (FIR) filter. The Deinterlacer uses a Four-field Motion Adaptive algorithm.

3.1.6 Video Output Processor (VOP)

The Video Output Processor is a data driven process that occurs at the VOP clock rate. The VOP performs:

- Luma and chroma vertical and horizontal scaling
- Luma edge enhancement
- Video and graphics mixing
- Hardware cursor
- Color processing
- Video formatting for desired output: RGB or YUV 4:2:2

Figure 3-6 shows the data flow during video output scaling.

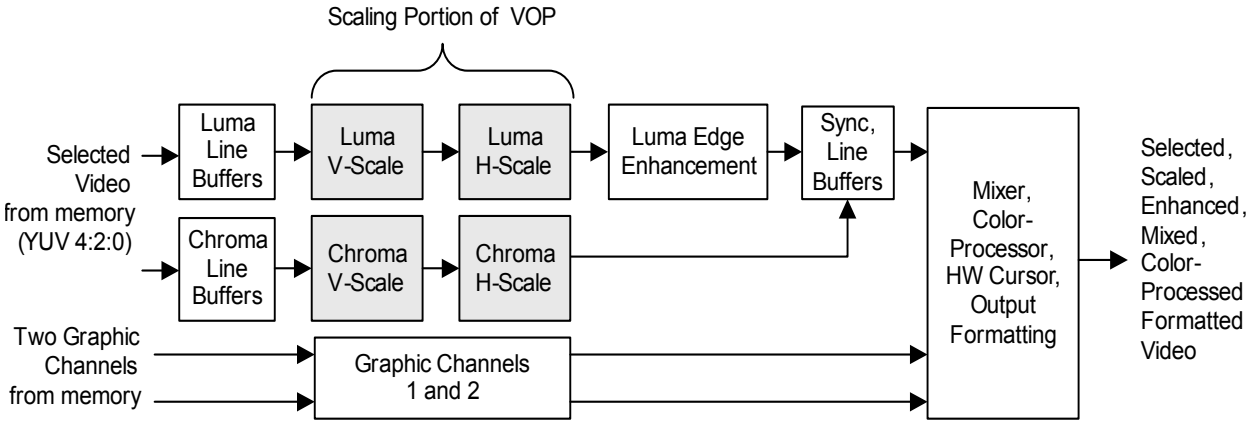


Figure 3-6. Video Output Processing Data Flow

Vertical scaling uses up to an eight-tap, eight-phase programmable FIR filter for luma and chroma. The down-sampling ratio is limited by the quality achievable with two taps and the frequency of the video output clock. There is no limit on the up-sampling ratio other than the frequency limit imposed by the video output clock.

3.2 Audio Subsystem

The main functional blocks of the Audio subsystem include Audio Input Interface and Audio Output Interface. The Audio interface signal group comprises one stereo input and one stereo output.

3.2.1 Audio Group Signals

Figure 3-7 illustrates the signal paths and timing for the audio interface.

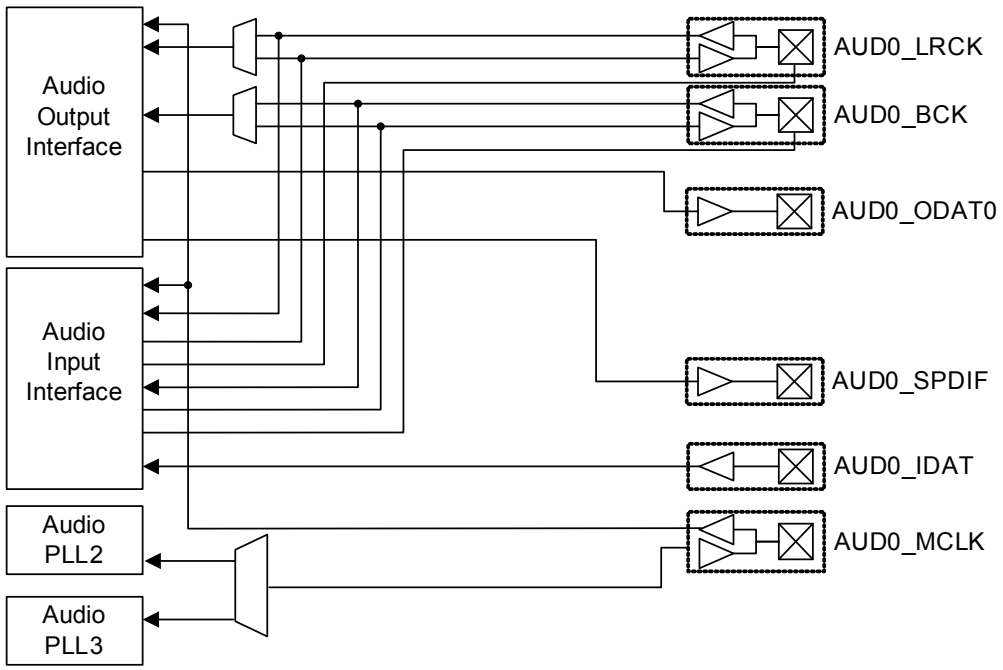


Figure 3-7. Audio Group Signals

3.2.2 Audio Clocks

The MAX64180 operates at the following sampling frequencies.

- 48, 24, 12kHz
- 44.1, 22.05, 11.025kHz
- 32, 16, 8kHz

The signal group has an independent master clock (MCLK) associated with it. The master clock runs at 256 * fs, where fs is the sampling frequency. The master clock can be sourced either from an internal PLL or an external clock source.

3.3 Encoder Subsystem

The MAX64180 codec supports the following HD encoders and decoders:

- H.264 Encoder/Decoder
- MPEG2 Decoder
- JPEG/MJPEG Encoder/Decoder

The H.264 codec, MPEG2 decoder, and JPEG/MJPEG codec are implemented as three independent blocks in the hardware. As a result, the codecs can run in parallel to support real time transcoding from one format to another.

The hardware allows the highest processing power at the lowest power consumption to support tools as specified by the H.264 standard. The processing power, which encodes or decodes HD resolutions, can also encode or decode multiple reduced resolutions or SD streams.

The H.264 codec encodes or decodes up to 1280 pixels per line (horizontally) and 720 lines (vertically).

Table 3-7. Supported Encoding and Decoding Modes

FEATURES	BASELINE PROFILE	MAIN PROFILE	HIGH PROFILE
Field Encoding	-	Yes	Yes
Macroblock Adaptive Frame Field (MBAFF)	-	Yes	Yes
B Frames	-	Yes	Yes
Context-based Adaptive Binary Arithmetic Coding (CABAC)	-	Yes	Yes
8 x 8 Transforms	-	-	Yes
Quantization Matrix	-	-	Yes
Weighted Prediction	-	Yes	Yes

MPEG2 Decoder

The HD MPEG2 decoder decodes up to a maximum of 1280 pixels per line (horizontally) and 720 lines (vertically). It does not have encoding capabilities. The MPEG2 decoder in conjunction with H.264 encoder can be used to create a transcoding application.

JPEG/MJPEG Encoder/Decoder

The JPEG/MJPEG codec encodes or decodes up to a maximum of 1280 pixels per line (horizontally) and 720 lines (vertically) at 30fps. The codec supports both YUV 4:2:0 and 4:2:2 modes.

3.4 Host Interface

An external system Host CPU controls the MAX64180 through the Host Interface. The Host Interface serves as the compressed data interface providing direct addressable access to the external DDR2 SDRAM, Bitstream Write FIFO, registers and all resources on the codec side of the MAX64180. The address lines H_ADDR[6:1] address the desired resource.

3.4.1 Host Interface Connections

Figure 3-8 shows the Host interface connections for the MAX64180.

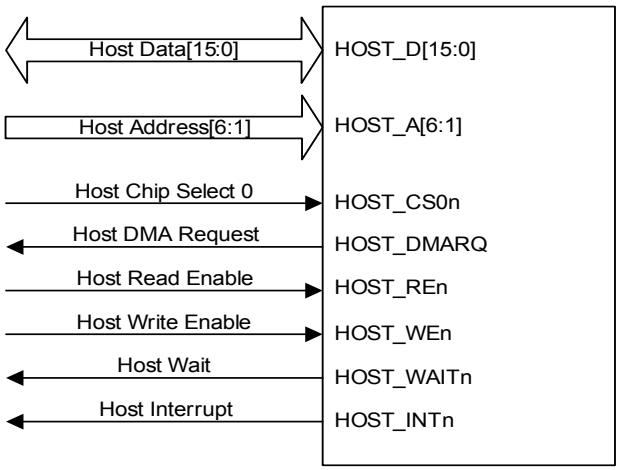


Figure 3-8. Host Interface Connections

3.4.2 Host Interface Signals

The signals that comprise the Host interface are described in Table 3-8.

Table 3-8. Host Interface Pin Description

PIN NAME	SIGNAL NAME	DIRECTION	DESCRIPTION
HOST_D[15:0]	Data [15:0]	Bidirectional	16-bit bidirectional Host Data Bus
HOST_A[6:1]	Address [6:1]	Input	Host Address input pins
HOST_CS0n	Host Chip Select 0	Input	Active Low Host Chip Select. This signal acts as a chip select input and accesses the MAX64180's internal registers, external memory, and bitstream read and write FIFO registers.
HOST_REn	Read Enable	Input	Active Low Read Enable. The external host processor asserts this input to indicate that it wants to read data from an address inside the MAX64180.
HOST_INTn	Interrupt	Output	Active Low Host Interrupt Request. This signal has an open-collector output and requires a 1KOhm pull-up resistor.
HOST_DMARQ	Host DMA Request	Output	HOST Direct Memory Access Request
HOST_WAITn	Wait	Output	Host Wait pin. The MAX64180 asserts this pin to extend the bus cycle until it is able to accept data (during a write cycle) or present data (during a read cycle). This signal has an open-collector output and requires a 1KOhm pull-up resistor.

3.5 Memory Interface

The MAX64180 supports a single external DDR2 SDRAM memory.

DDR2 SDRAM specifications:

- Type supported: DDR2 SDRAM
- Clock frequencies: 233MHz or lower
- Bus width: 16-bit
- Voltage levels DDR2 SDRAM: 1.8V (supported by DDR parts)
- Maximum density: 64Mbytes, one 512Mbit x 16-bit DDR2 SDRAM device

3.5.1 DDR2 SDRAM Connections

Figure 3-9 shows the DDR2 SDRAM connections for a single 16-bit DDR2 SDRAM.

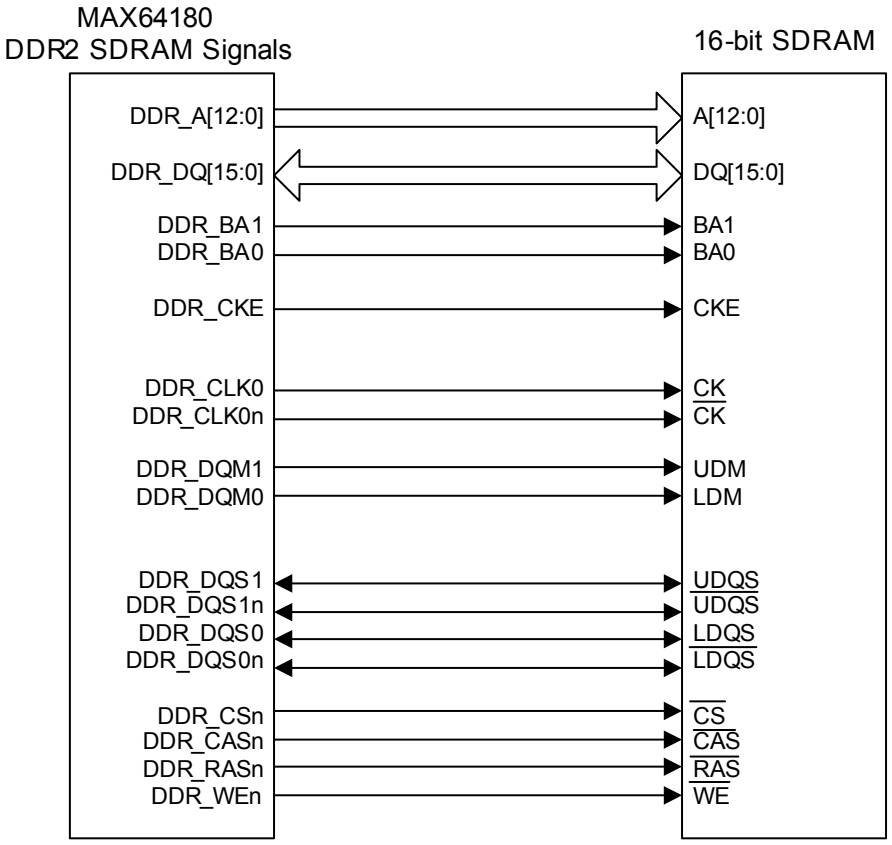


Figure 3-9. DDR2 SDRAM Connections for 512Mb 16-Bit

3.6 Serial Interfaces

The UART, I^{2}C compatible Two-wire interface, and SPI comprise the serial interfaces.

Table 3-9. Serial I/O Interfaces

INTERFACE	NUMBER OF INTERNAL INSTANCES	NUMBER OF INTERFACE PORTS
UART	1 ARM + 1 MME	1
TWI	1	1
SPI	1	1

3.6.1 UART Interface

The MAX64180 Debug UART port consists of the Transmit Data (TXD) and Receive Data (RXD) signals (see Figure 3-10). The MME and ARM debug ports along with their TXD and RXD signals share the UART port. The Debug port is useful for debugging the system and should always be connected to a serial terminal.

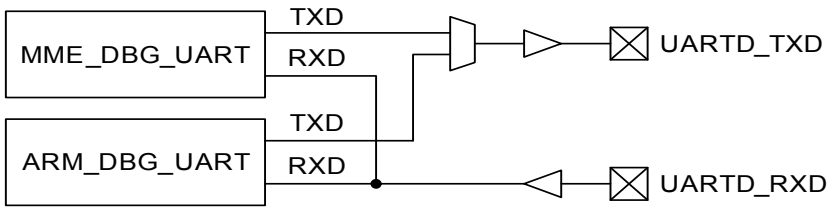


Figure 3-10. UART Module to Interface Signal Mapping

The UART supports one stop bit, 8 data bits, and even parity. The baud rate for the UART can be set to any of the values listed in Table 3-10.

Table 3-10. UART Baud Rate Frequencies

BAUD RATE	BAUD RATE	BAUD RATE	BAUD RATE
300	19200	64000	250000
600	28800	76800	256000
1200	38400	115200	460800
2400	51200	128000	500000
4800	56000	153600	576000
9600	57600	230400	921600

3.6.2 Two-Wire (TWI) Interface

The I^2C compatible Two-wire interface comprises one TWI module and one TWI interface port as shown in Figure 3-11.

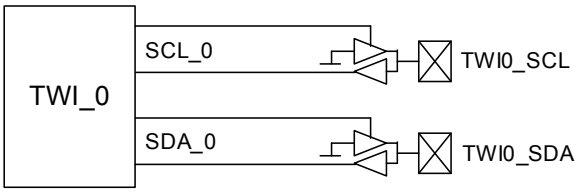


Figure 3-11. TWI Module to Interface Signal Mapping

3.6.3 SPI Interface

The SPI interface comprises two SPI modules with one SPI port:

- SPI_0 (Master) is configured to support two devices; therefore, it has two Slave Select (MSS) signals. It connects to the primary SPI port.
- SPI_2 (Slave) is configured to support one device; therefore, it has a single Slave Select (MSS) signal. It connects to the primary SPI port.

SPI_0 and SPI_2 can be multiplexed because SPI_0 is the master and SPI_2 is the slave. After reset, this interface comes up in GPIO mode, so all signals are inputs.

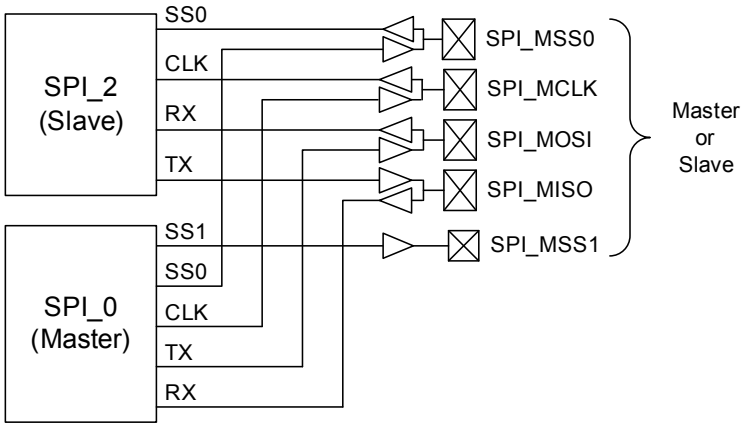


Figure 3-12. SPI Module to Interface Signal Mapping

3.6.4 Pulse Width Modulators

The MAX64180 supports one PWM module. The clock for the module is 1MHz. For programming the PWM pulse width, contact Maxim Technical Support.

3.6.4.1 Serial I/O Pad Programmable Features

For programming the following features in the MAX64180, contact Maxim Technical Support.

- Drive Strength
- Slew Rate
- Pull-up
- Pull-down

The drive strength groups in MAX64180 are categorized as follows:

- Drive Strength 0 (DS0): UART, I^2C, GPIO, PWM
- Drive Strength 1 (DS1): SPI
- Drive Strength 4 (DS4): Video port 0
- Drive Strength 6 (DS6): Video port 2
- Drive Strength 8 (DS8): Host
- Drive Strength 10(DS10): Audio

A three-bit encoding is used for the actual drive strength value.

3.7 USB 2.0 High-Speed Interface

The MAX64180 contains a High-speed USB 2.0 interface with the ability to operate as a Device or Host at speeds of up to 480Mbps. The USB 2.0 Transceiver Macrocell Interface (UTMI) is an interface between the USB controller and the PHY inside the chip. Figure 3-13 shows a high-level block diagram of the USB interface.

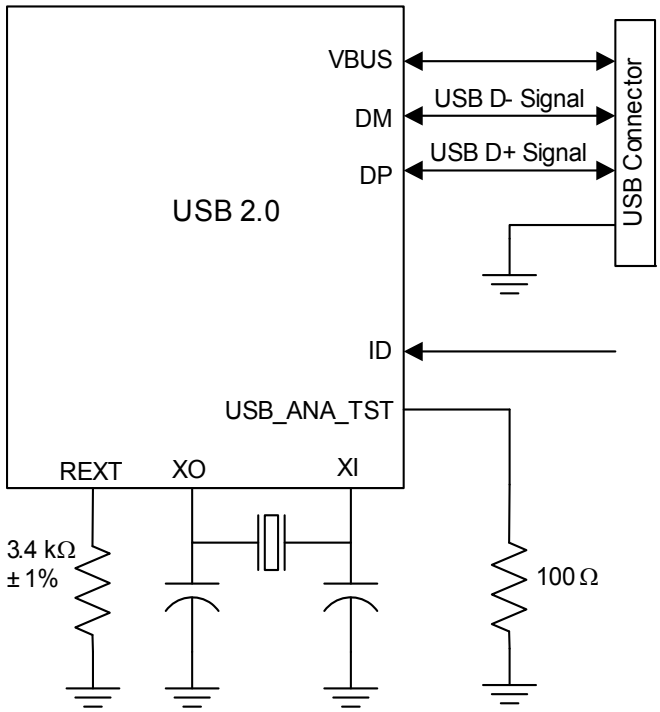


Figure 3-13. USB Interface Block Diagram

3.7.1 Physical Layer (PHY)

The USB 2.0 PHY port provides three distinct external interfaces:

- The USB Data Plus (D+) and Data Minus (D–) lines: These lines are USB 1.1 and 2.0 specification-compliant. The USB 2.0 PHY supports high-speed, 480Mbps transfers, as well as USB 1.1 full-speed and low-speed transfers.
- USB 2.0 Transceiver Macrocell Interface (UTMI): The USB PHY supports the following modes through the UTMI:
    - High-Speed (HS)
    - Full-Speed (FS)
    - Full-Speed-Only (FS-Only)
    - Full-Speed Power-Save (FS Power-Save)
    - Low-Speed Power-Save (LS Power-Save)
    - Low-Speed Preamble (LS Preamble)
    - Low-Speed Preamble Power-Save (LS Preamble Power-Save)
- The UTMI contains a receive port, a transmit port, and associated control lines to interface with a USB host controller or device controller. The receive and transmit ports can be configured as 8/16-bit parallel ports for all modes of operation.
- Serial interface: This interface supports full-speed (FS-Serial mode) and low-speed (LS-Serial mode) data transmission rates to and from a controller.

The USB 2.0 PHY handles low-level USB protocol and signaling. The USB 2.0 PHY supports Sync detection, data serialization and deserialization, and data recovery.

Features

The USB 2.0 PHY supports the following features.

General Features

- Low power dissipation while active, idle, or on standby
- Integrates high-, full-, and low-speed (Host mode only) termination and signal switching
- Requires minimal external components: a single resistor and single crystal with two capacitors for best operation
- Provides an on-chip PLL to reduce clock noise and eliminate the need for an external clock generator
- Integrates short-to-5-V and short-to-ground protection for D+ and D– lines (requires only global electrostatic discharge (ESD) and 5V-compliant dp/dm pads)

USB 2.0 Features

- Complies with *Universal Serial Bus Specification*, Revision 2.0
- Complies with *UTMI+ Specification*, Revision 1.0 (Level 3)
- Integrates 45Ohm termination, 1.5KOhm pull-up and 15KOhm pull-down resistors, with support for independent control of the pull-down resistors
- Supports 480Mbps high-speed (HS), 12Mbps full-speed (FS), and 1.5Mbps low-speed (LS) (Host mode only) data transmission rates
- Supports 8/16-bit unidirectional parallel interfaces for HS, FS, and LS (Host mode only) modes of operation, in accordance with the UTMI specification
- Provides dual (HS/FS) mode host/device support (LS operation is not supported for device applications)
- Implements data recovery from serial data on the USB connector
- Implements SYNC/End-of-Packet (EOP) generation and checking
- Implements bit stuffing and unstuffing, and bit-stuffing error detection
- Implements Non Return to Zero Invert (NRZI) encoding and decoding
- Implements bit serialization and deserialization
- Implements holding registers for staging transmit and receive data
- Implements logic to support suspend, resume, and remote wakeup operations
- Implements VBUS pulsing and discharge Session Request Protocol (SRP) circuit
- Implements VBUS threshold comparators

3.7.2 USB Controller

The USB Controller is a Dual-Role Device (DRD) controller that supports both device and host functions. It can be configured as a Host-only or Device-only controller, fully compliant with the *USB 2.0 Specification*. The USB 2.0 configurations support high-speed (HS, 480Mbps), full-speed (FS, 12Mbps), and low-speed (LS, 1.5Mbps) transfers. Additionally, the USB Controller can be configured as a USB 1.1 full-speed/low-speed DRD.

The USB Controller is optimized for the following applications and systems:

- Portable electronic devices
- Point-to-point applications (no hub, direct connection to HS, FS, or LS device)
- Multi-point applications (as an embedded USB host) to devices (hub and split support)

Figure 3-14 shows a block diagram of the USB Controller.

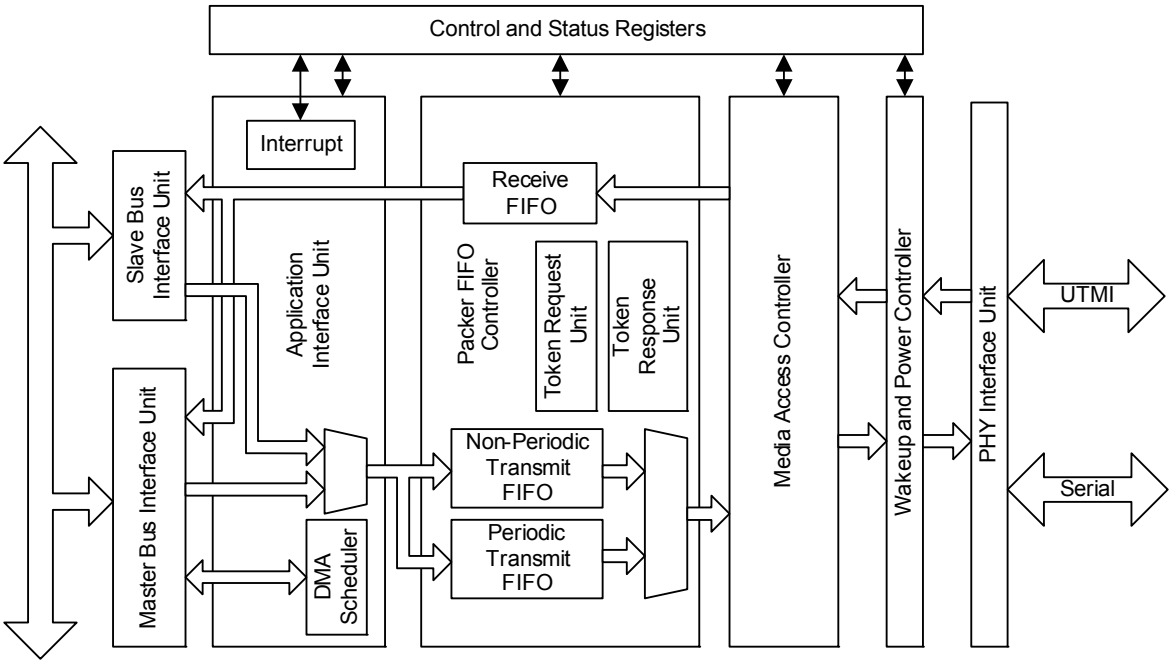


Figure 3-14. USB Controller

General Features

- Includes USB power management features
- Includes clock gating to save power
- Supports packet-based, dynamic FIFO memory allocation for endpoints for small FIFOs and flexible, efficient use of RAM
- Supports the Keep-Alive in Low-Speed mode and Start-of-Frames (SOFs) in High/Full-Speed modes
- Power-optimized design

USB 2.0 Supported Features

- Operates in High-Speed (HS, 480Mbps), Full-Speed (FS, 12Mbps) and Low-Speed (LS, 1.5Mbps) modes
- Supports Session Request Protocol (SRP)
- Supports Host Negotiation Protocol (HNP)
- I^2C interface
- Supports a generic root hub
- Includes automatic ping capabilities

Power Optimization Features

- PHY clock gating support during USB Suspend mode and Session-Off mode
- Partial power-off during USB Suspend mode and Session-Off mode
- Input signals to powered-off blocks driven to safe 0
- Data FIFO RAM chip-select deasserted when not active
- Data FIFO RAM clock-gating support

Host Architecture

The host uses one transmit FIFO for all non-periodic OUT transactions and one transmit FIFO for all periodic OUT transactions. The transmit FIFOs operate as transmit buffers to hold data (payload of the transmit packet) to be transmitted over USB. The host pipes the USB transactions through Request queues (one for periodic and one for non-periodic). Each entry in the request queue holds the IN or OUT channel number along with the information to perform a transaction on the USB. The order in which the requests are written into the queue determines the sequence of transactions on the USB. The host processes the periodic request queue first, followed by the non-periodic request queue at the beginning of each (micro) frame.

The host uses one receive FIFO for all periodic and non-periodic transactions. The FIFO acts as a receive buffer to hold received data (payload of the received packet) from the USB until it is transferred to the system memory. The status of each packet received also goes into the FIFO. The status entry holds the IN channel number along with other information, such as received byte count and validity status, to perform a transaction on the AMBA High-speed Bus (AHB).

Device Architecture

The device uses a single transmit FIFO to store data for all non-periodic endpoints, and one transmit FIFO per periodic endpoint to store data to be transmitted in the next (micro) frame. The data is fetched by the DMA engine or is written by the application into the transmit FIFOs and is transmitted on the USB when the IN token is received. The request queue contains the number of endpoints for which the data is written into the Data FIFO.

To improve performance, the application can use the learning queue to help predict the order in which the USB host will access the non-periodic endpoints and writes the data into the non-periodic FIFO accordingly. Since each periodic IN endpoint has its own FIFO, no order prediction is needed for periodic IN transfers.

The device uses a single receive FIFO to receive the data and status for all OUT endpoints. The status of the packet includes the size of the received OUT data packet, data Parameter Identification Data (PID), and validity of the received data. The data in the receive FIFO is read by the DMA or the application when the data is received.

3.8 High-Speed Bitstream

The Bitstream port provides a bidirectional serial data port for input and output of compressed bitstreams with an associated valid signal. The bitstream interface streams high-speed bitstream data directly to and from the MAX64180 codec or SoC mode at 30 to 74.5MHz. The bitstream interface multiplexes with the Serial Peripheral Interface (SPI) signals.

Note: The maximum frequency when running with the internal clock is 67.5MHz. This is due to a limitation in the granularity (step size) of the PLL.

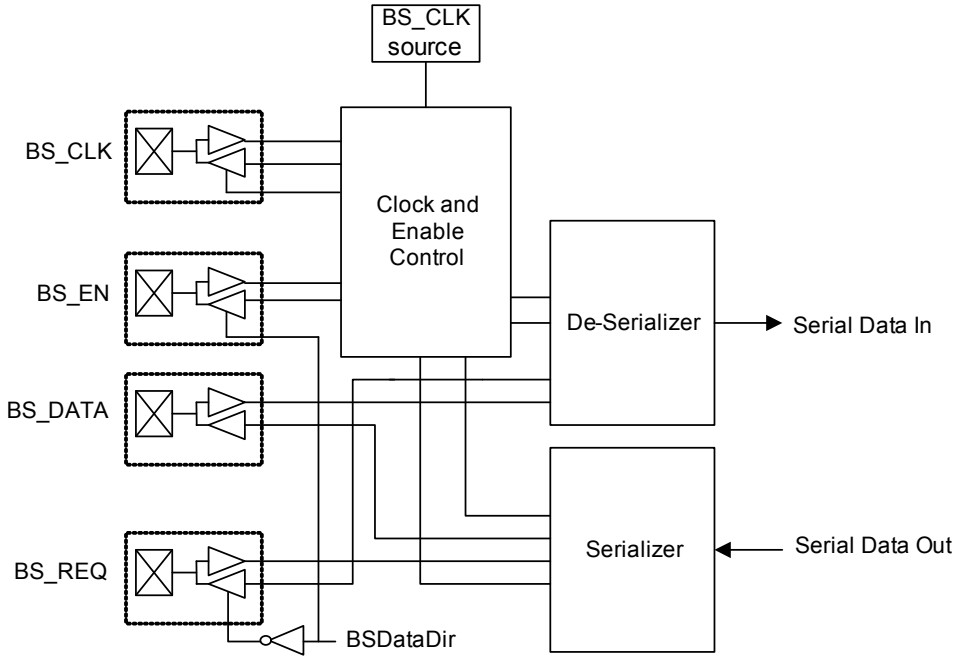


Figure 3-15. High-Speed Bitstream Signals

3.8.1 Bitstream Signals

Table 3-11. Bitstream Signals

SIGNAL	DIRECTION		DESCRIPTION
	TRANSMITTER	RECEIVER	
BS_CLK	Input or Output	Output or Input	Bitstream Clock. Data gets latched by this signal. It can be provided either by the MAX64180 or externally. The Bitstream interface supports data transfers up to 74MHz.
BS_DATA	Output	Input	Bitstream Data
BS_EN	Output	Input	Bitstream Enable. This signal can be used to qualify BS_CLK. BS_EN is always in the same direction to BS_DATA.
BS_REQ	Input	Output	Bitstream Request. A request signal used for flow control. BS_REQ is always in the opposite direction to BS_DATA.

3.8.2 Bitstream Mode

In Bitstream mode, all signals are active high or active rising edge. BS_CLK and BS_EN can be programmed to be active falling edge or active Low. “Clock Plus Enable Mode” on page 49 explains the primary way in which the control signals are used.

3.8.3 Clock Plus Enable Mode

The Clock Plus Enable Mode is BS_CLK enabled, which is qualified by BS_EN. When BS_EN is active and a BS_CLK edge event occurs, the data on BS_DATA is latched.

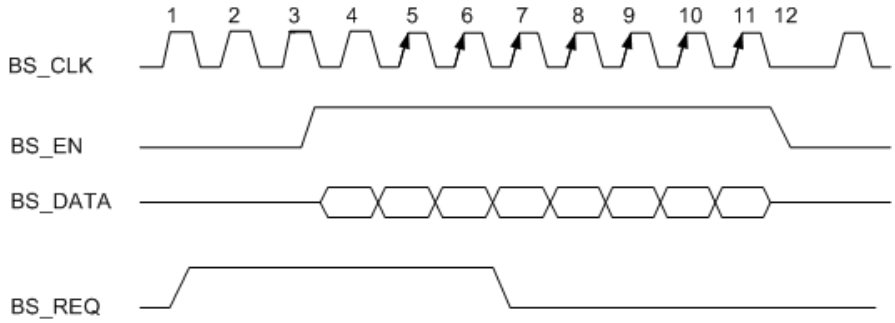


Figure 3-16. Receive with Bitstream Clock and Bitstream Enable Timing

Some points to note about the waveform figure are given below:

- Cycle 1: The receiver is not ready for data, so BS_REQ is not asserted.
- Cycle 2 and 3: The receiver is ready since BS_REQ is asserted. The transmitter is not yet sending data because BS_EN is not asserted.
- Cycle 4-6: Both the transmitter and receiver are ready and data is being transferred.
- Cycle 7: The receiver has de-asserted BS_REQ indicating it cannot receive any more data. However, it is necessary that the receiver be designed to accept all bits in the current byte being transferred. When the MAX64180 is in transmit mode, it can stop transfers only at byte boundaries. In receive mode, the MAX64180 expects the transmitter to stop only at a byte boundary.
- Cycle 8: The clock does not need to be free-running.

3.9 Reset Logic

The Reset block resets the core logic along with the peripheral blocks that surround it.

The core reset signal consists of the power-on reset signal from an external pin (RESETn), a watchdog reset, and software controlled chip reset signal.

3.9.1 Power-On Reset

The power-on reset signal comes directly from the external RESETn pin and is asynchronous with respect to the clock. It is assumed that the clock is not running both at the time of assertion and deassertion of the power-on reset signal.

3.9.2 Watchdog Reset

The watchdog reset is asserted when the internal watchdog logic detects an internal error. The watchdog reset needs to be enabled before it can take effect. Resetting the watchdog timer will cause the watchdog reset to be de-asserted, so it is self-clearing.

3.9.3 Software Chip Reset

The software chip reset is ORed with the watchdog reset. Resetting the software chip reset register causes the software chip reset signal to be deasserted, so it provides a form of self-clearing mechanism.

All three of these resets get combined into a signal that resets both the core and the peripheral blocks that surround it. In addition, the reset registers allow each of the peripheral blocks to be reset independently. Since control of these reset signals is done using software APIs, they are not discussed in this manual.

3.9.4 Reset Timing

Figure 3-17 shows the timing for the active low reset signal RESETn. This signal must remain low for a minimum of 300µsecond after the power supplies and input clocks stabilize.

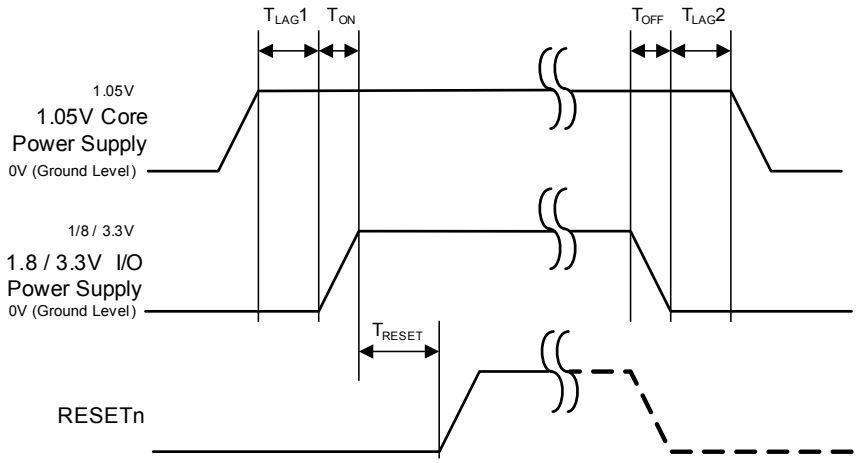


Figure 3-17. Reset Timing

3.10 Clocks and Phase Lock Loops (PLLs)

The MAX64180 internally creates multiple clocks to minimize power consumption and maximize performance. All of the clocks are derived from a single 12MHz crystal oscillator that is built into the USB Interface block. The oscillator can be used even when the USB interface is not used.

3.10.1 Clock and PLL inputs

The MAX64180 can source the system clock from a 12MHz crystal or a 27MHz oscillator. The oscillator is used in systems that require the video input to be synchronized to a clock source. For systems that need USB functionality and video synchronized to a clock source, both the crystal and oscillator are required. In such a case, the 12MHz crystal generates the clock to the USB controller and the input from the oscillator will be used to generate the clocks to the rest of the system. Refer "Crystal and External Clock Connected to External CLK_IN Pin" on page 57. The CLK_SEL pin shown in Figure 3-18 selects the clock source for system clock generation.

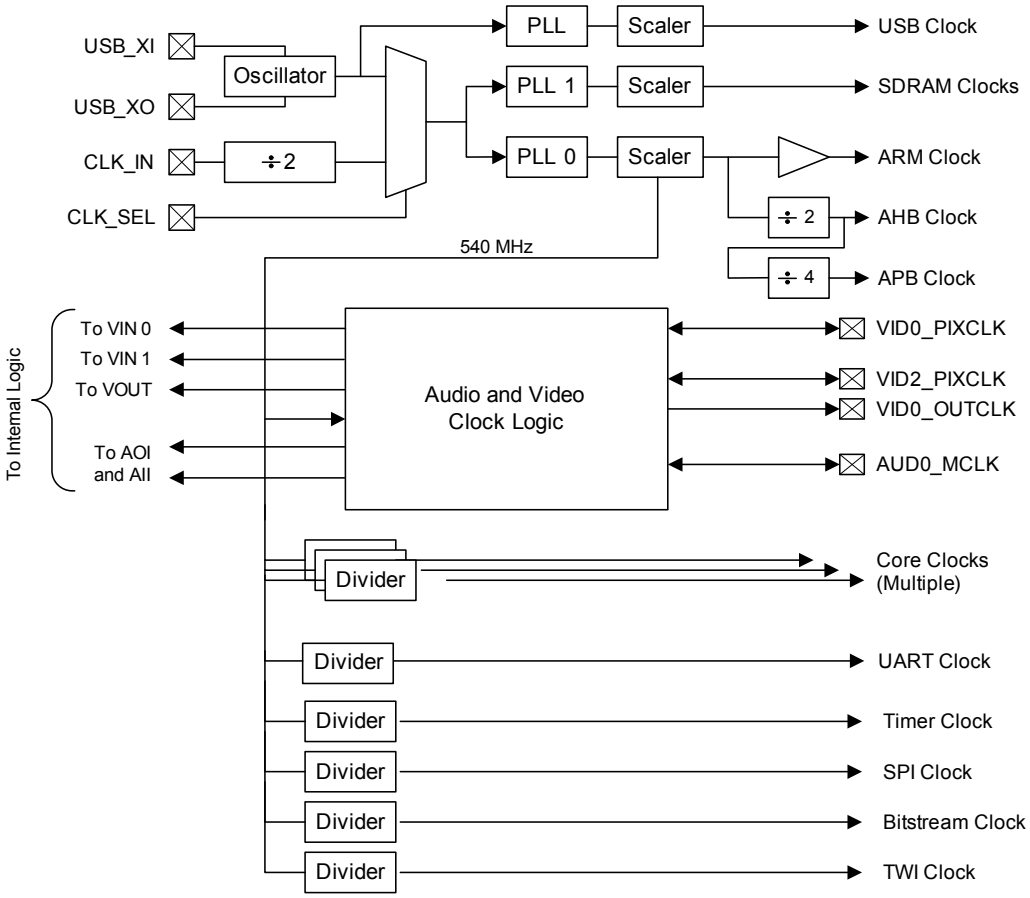


Figure 3-18. Clocking Structure

3.10.2 Phase Lock Loops

A total of five PLLs exist in the MAX64180. One PLL is included as part of USB PHY, which is used for USB PHY clocking and UTMI interfacing to the internal USB MAC. The remaining four PLLs generate the other required clock frequencies. PLL1 generates the four-phase SDRAM clocking. PLL0 generates the codec core clocks, ARM processor, host bus clocks, and input clocks for PLL2 and PLL3. Audio and video clocks can be generated from either PLL2 or PLL3, depending on the configuration of the multiplexers.

The remainder of the clocks are used for peripheral I/O circuitry and are discussed in their individual sections.

3.10.3 Video and Audio Clocks

Figure 3-19 shows the circuitry which generates the video input, video output, and audio clocks. Each is discussed in the sections that follow.

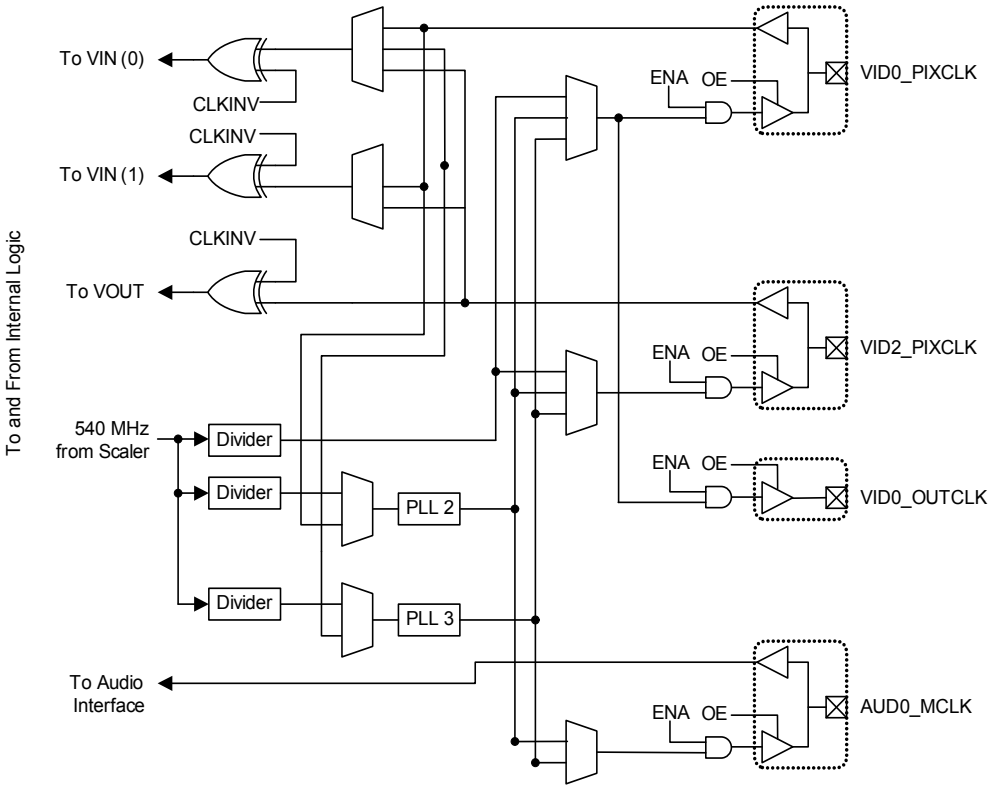


Figure 3-19. Video and Audio Clocks

3.10.3.1 Video Input Clocks

The two video input interfaces VIN0 and VIN1 provide the video pixel clock signals: VID0_PIXCLK and VID2_PIXCLK. The video pixel clock signals are the synchronization clocks for video data. Alternately, an inverted version of the video pixel clock can be used to time the interface. The video pixel clock pad can be configured to be either an input or output.

In input mode, the pixel clock is driven from an external source. In output mode, the pixel clock is driven from an internal clock generator, and the clock is routed to drive both the internal logic and external devices through the I/O cell. In other words, the clock supplied to the video input circuitry is always the signal from the I/O pad regardless of whether the video pixel clock is in input or output mode.

3.10.3.2 Video Output Clocks

The MAX64180 also has the capability to generate the video output clock source, VID0_OUTCLK. This mode is useful in interfacing to sensors that require a clock input and send a clock output (which is typically a recovered, delayed version of the input clock) with the data.

The internal video out (VOUT) signal (see Figure 3-19) that goes to the internal video output circuitry can only be sourced by VID2_PIXCLK. Alternately, an inverted version of VID2_PIXCLK can be used to time the interface.

The VID2_PIXCLK pad can be either an output or input. In output mode, VID2_PIXCLK is driven from the internal clock generators. In input mode, VID2_PIXCLK is driven from an external source.

3.10.3.3 Audio Clocks

When the bidirectional audio master clock pin, AUD0_MCLK, is configured as an input, it provides the clock for the internal Audio Input Interface and Audio Output Interface blocks. In output mode, the audio clock is driven from internal clock generators, and the clock is routed to drive the logic through the I/O cell. PLL0 generates the main clock from which all other clocks in the system are derived.

3.11 Device Configuration

The section below describes how the device can be configured.

3.11.1 Reset

When the device is first powered on, the power supplies must be brought up in the order shown in “Power Supply Sequencing” on page 59. When the power supplies become stable, follow this procedure to reset the MAX64180.

To reset the MAX64180 to Master (SoC) mode:

1. Set CLK_SEL pin to select the source clock for the PLLs. The clock can come from either the internal USB oscillator or the CLK_IN pin.
2. Set the HOST_CFG_0 pin to 1 to select **Master configuration mode**.
3. Set the boot mode using (CFG) pin. See Table 3-12 for more information.
4. Assert the RESETn pin low for at least one microsecond and then release it.

At this point, the boot ROM in the chip will start the initialization process.

To reset the MAX64180 to Slave (Coprocessor) mode:

1. Set CLK_SEL pin to select the source clock for the PLLs. The clock can come from either the internal USB oscillator or the CLK_IN pin.
2. Set the HOST_CFG_0 pin to 0 to select **Parallel Slave configuration mode**.
3. Set the boot mode using CFG pin. See Table 3-12 for more information.
4. Assert the RESETn pin low for at least one microsecond and then release it.

At this point, the Video Multi-Media Engine (MME) is ready to accept the downloaded firmware image. Configure the Configuration/Status Registers, download the firmware, and start the other clocks. Wait for the MAX64180 to return a valid GPB (Global Pointer Block).

3.11.2 Boot Mode for the MMEs and the ARM

At power-on, an on-chip ROM that contains the bootrom code executes the code and checks the clock source (CLK_SEL) and boot mode (CFG). The bootrom code then copies the boot loader from the specified boot device.

Table 3-12. Boot Modes

CONFIGURATION (CFG)	BOOT MODE
0	Load from SPI EEPROM (SPI 0)
1	Load from UART Debug using XModem

3.11.3 API Configuration

The APIs initialize the internal registers as part of the configuration process. The registers include:

- Configuration and Control registers
- Drive Strength, Slew Rate control registers
- Clock and PLL registers

The default configuration for the Clock and PLL registers assumes that the 12MHz USB crystal is being used as the primary clock source. An externally generated 24 or 27MHz clock can also be used to drive the MAX64180. If an external clock is being used, contact Maxim Technical Support for a specialized version of the API.

3.11.4 Pin Muxing

All shared I/O pins come up in the primary interface mode, and they must be programmed to be used in the Alternate interface mode or GPIO mode. Dedicated GPIO pins come up as input pins and must be programmed to be used as output pins.

3.11.5 Debug Mode

The API supports communication between the ARM processor and the Debug port. The Debug port is useful in debugging the system and should always be connected to a serial terminal.

3.12 Oscillator Connections

The USB 2.0 PHY supports the following reference clock sources.

3.12.1 Crystal Connected to USB_XIN and USB_XO Pins

Figure 3-20 shows the clock configuration with an external crystal.

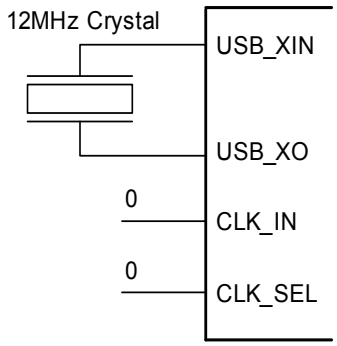


Figure 3-20. Clock Configuration with an External Crystal

The crystal must have a fundamental frequency of 12MHz and must meet the specifications shown in Table 3-13.

Table 3-13. Crystal Specifications

PARAMETER	VALUE
Frequency Tolerance	± 200ppm
Peak Jitter	± 100ps
Output Differential Voltage	> 500mV w.r.t Xi
Shunt Capacitance	5 – 8pF
Load Capacitance	15-30pF
Series Resistance	20-60Ohms
Drive Level	50-500µW

3.12.2 Crystal and External Clock Connected to External CLK_IN Pin

Figure 3-21 shows the clock configuration when the external CLK_IN pin is used. In this mode, both the external crystal and the external CLK_IN pin are connected.

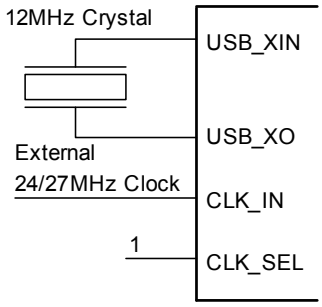


Figure 3-21. Clock Configuration with an External Crystal

The crystal must have a fundamental frequency of 12MHz and meet the specifications shown in Table 3-13. The external clock must have a fundamental frequency of 24 or 27MHz with a frequency tolerance of ±200ppm, a peak jitter of ±100ps., a duty cycle between 40/60 and 60/40, and a signal swing equal to the host power supply voltage.

Figure 3-22 shows the clock configuration where the crystal clock is not connected in the design, but only the external clock is connected to CLK_IN.

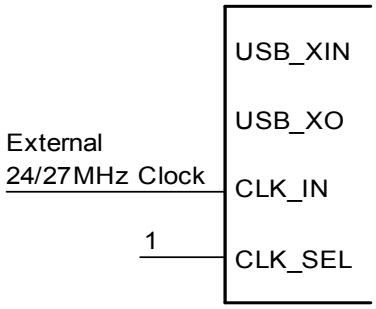


Figure 3-22. Clock Configuration with an External Crystal

In this mode, the USB will not be operational because the USB runs only when using the crystal. This configuration is typically used in coprocessor applications.

The external clock must have a fundamental frequency of 24 or 27MHz with a frequency tolerance of ±200 ppm, a peak jitter of ±100ps., a duty cycle between 40/60 and 60/40, and a signal swing equal to the host power supply voltage.

4 Power Supply Considerations

This section provides detailed information concerning the power supply considerations of the MAX64180 to help ensure first time success in implementing a functional design, which has been optimized for signal quality.

4.1 Power Supply Sequencing

Figure 4-23 provides the recommended power-up and power-down sequences. In an ideal design, all of the power supplies become stable at the same time to prevent any direct feed-through current. In real designs, however, there is typically a time delay before the power supplies stabilize. This section describes the restrictions on the time differences between the power supplies.

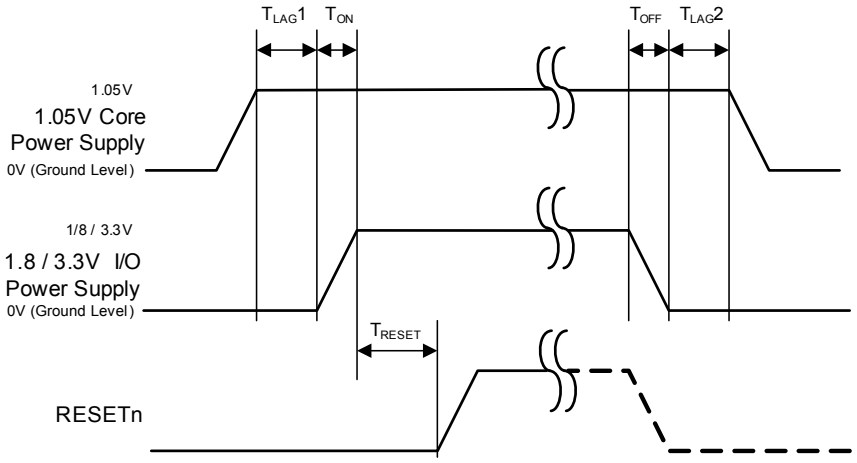


Figure 4-23. Power Supply Sequencing

The MAX64180 uses three different power rails: 1.5V for the core, 1.8V for DDR I/Os, and 3.3V for all other I/Os. When the 1.5V core supply becomes stable, the 1.8V and 3.3V I/O voltages can be brought up at any time and in any order. During power-down, the I/O voltages must be brought down before the core voltage.

The T_{RESET} has to be greater than 1 micro second.

The restrictions are listed below:

$T_{LAG}1$, $T_{LAG}2$ >= 0 ms.

T_{ON}, T_{OFF} >= 0 ms.

4.2 Power Supply

The current requirements are different for each power domain and are dependent on the target application. Table 4-14 shows the peak current requirements for each domain. The peak current is used for regulator and decoupling capacitors sizing. It does not represent typical power consumption.

Table 4-14. Peak Power Supply Currents for the Different Power Domains

INTERFACE	POWER DOMAIN	CONDITIONS	PEAK	UNITS
Core	CORE_VDD	1.0 Volt Supply Voltage	1000	mA
Audio	AUD_VDD	3.3 Volt Supply Voltage	25	mA
Host	HOST_VDD	3.3 Volt Supply Voltage	60	mA
DDR2 SDRAM Memory	DDR_VDD	1.8 Volt Supply Voltage (VDDA)	250	mA
USB	USB_VDD	3.3 Volt Supply Voltage	60	mA
Video	VID0_VDD	3.3 Volt Supply Voltage	25	mA
	VID2_VDD	3.3 Volt Supply Voltage	65	mA

Maximum power consumption for the supported application is less than 1.5W.

5 Electrical Specifications

This section provides the absolute maximum ratings, stress ratings, recommended operating conditions, DC characteristics, and AC characteristics for the MAX64180.

5.1 Operating Parameters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range on CORE_VDD 1.5V
Supply Voltage Range on DDR_VDD 2.5V
Supply Voltage Range on VID0_VDD and VID2_VDD 4.5V
Supply Voltage Range on AUD_VDD 4.5V
Supply Voltage Range on HOST_VDD 4.5V
Supply Voltage Range on USB_VDD 4.5V
Maximum Input Voltage (VREF) ..... VDD_VREF+700mV
Maximum Input Voltage, DDR ..... DDR_VDD+300mV 2.1V
Storage Temperature Range ..... –40°C to 150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-15. Recommended DC Operating Conditions

INTERFACE	SIGNAL NAME	MIN	TYP	MAX	UNITS	DESCRIPTION
Core	CORE_VDD PLL_VDD	1.0	1.05	1.10	V	1.05V ±5%
Video	VID0_VDD VID2_VDD	1.71	1.8	1.89	V	±5%
		2.37	2.5	2.62		
		3.13	3.3	3.46		
Audio	AUD_VDD	1.71	1.8	1.89		±5%
		2.37	2.5	2.62	V	
		3.13	3.3	3.46		
Host	HOST_VDD	3.13	3.3	3.46	V	3.3V ±5%
USB	USB_VDD	2.97	3.3	3.63	V	3.3V ±10%
	USB_VBUS[1]	4.8	5	5.2	V	5V ±4%
Memory	DDR_VDD	1.7	1.8	1.9	V	1.8V ±0.1V
	DDR_VREF	-	0.60 x DDR_VDD	-	V	This should be tuned for every design. Refer to the DDR design guideline, "*MG3500/MG2580 DDR2 User's Guide*." Use 1% resistors
Operating Temperature Range		0	-	70	°C	Ambient temperature

1. The VBUS pin can sink or source 8mA of current. Therefore, to meet the design specification, the external power supply must be able to source at least 10mA at a voltage level of 5V ±4%. The VBUS pin presents a worst-case load of 500fF. This worst-case load is for the USB 2.0 PHY only and does not account for capacitance due to routing, pads, package, or board traces.

5.2 DC Characteristics

Table 5-16 defines the DC characteristics for all interfaces except the DDR2 SDRAM interface.

Table 5-16. DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	VID0_VDD, VID2_VDD, AUD_VDD, 3.3V ±5%		VID0_VDD, VID2_VDD, AUD_VDD, 2.5V ±5%		VID0_VDD, VID2_VDD, AUD_VDD, 1.8 V ±5%		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Input High-level Voltage	V_{DD} = Maximum	2.00	—	1.6	—	1.3	—	V
V_{IL}	Input Low-level Voltage	V_{DD} = Minimum	—	0.4	—	0.4	—	0.4	V
V_{OH}	Output High-level Voltage	V_{DD} = Minimum, I_{OH} = –4mA	2.70	—	1.9	—	1.4	—	V
V_{OL}	Output Low-level Voltage	V_{DD} = Minimum, I_{OL} = –4mA	—	0.35	—	0.35	—	0.35	V
I_{IH}	Input High-level Leakage	V_{DD} = Maximum, V_{IN} = V_{DD}	–5	+5	–5	+5	–5	+5	µA
I_{IL}	Input Low-level Leakage	V_{DD} = Maximum, V_{IN} = 0V	–5	+5	–5	+5	–5	+5	µA
C_{PIN}	Capacitance	—	—	5	—	5	—	5	pF

Table 5-17 defines the DC and AC characteristics for DDR2 SDRAM interface.

Table 5-17. DC and AC Characteristics for DDR2 SDRAM

SYMBOL	PARAMETER	CONDITIONS	DDR_VDD 1.8 V ±100mV		UNITS
			MIN	MAX	
V_{DCIH}	Input DC High-level Voltage	V_{DD} = Maximum	DDR_VREF +125mV	DDR_VDD +300mV	V
V_{DCIL}	Input DC Low-level Voltage	V_{DD} = Minimum	0	DDR_VREF –125mV	V
V_{ACIH}	Input AC High-level Voltage	V_{DD} = Maximum	DDR_VREF +250mV	DDR_VDD +300mV	V
V_{ACIL}	Input AC Low-level Voltage	V_{DD} = Minimum	0	DDR_VREF –250mV	V
V_{DCOH}	Output DC High-level Voltage	V_{DD} = Maximum	1.4	DDR_VDD	V
V_{DCOL}	Output DC Low-level Voltage	V_{DD} = Minimum	0	DDR_VREF – 250mV	V
V_{ACOH}	Output AC High-level Voltage	V_{DD} = Maximum	1.3	DDR_VDD	V
V_{ACOL}	Output AC Low-level Voltage	V_{DD} = Minimum	0	0.5	V
C_{PIN}	Capacitance	—	—	5	pF

5.3 AC Timing

This section provides the AC timing for the MAX64180's various interfaces. This section is divided into the following subsections:

- "Video Interface AC Timing" on page 64
- "Audio Interface AC Timing" on page 66
- "Host Interface AC Timing" on page 68
- "SPI/Bitstream Interface AC Timing" on page 72

5.3.1 Video Interface AC Timing

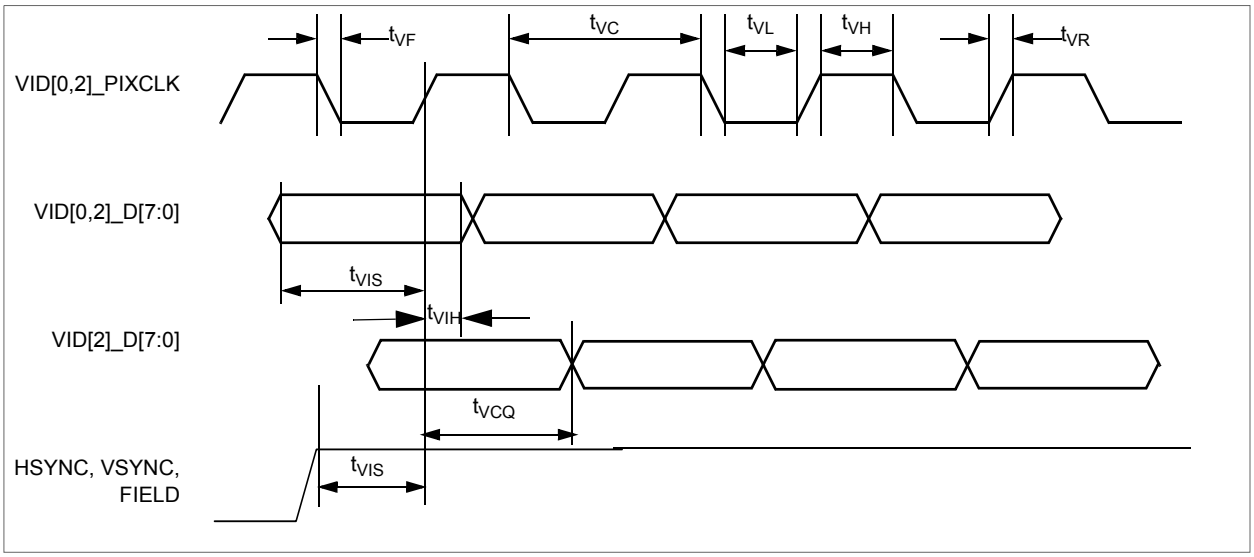


Figure 5-24. Video Interface Timing

Table 5-18. Standard Definition Video Interface Timing Parameters

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)[1]		
			MIN	TYP	MAX
VID[0,2]_PIXCLK	t_{VC}	Video Pixel Clock cycle time (27MHz)	—	37.037	
	t_{VH}	Video Pixel Clock high time	16.67	18.5	20.37
	t_{VL}	Video Pixel Clock low time	$t_{VC} - t_{VH}$		
	t_{VR}	Video Pixel Clock slew (rise time)	Not Applicable		
	t_{VF}	Video Pixel Clock slew (fall time)	Not Applicable		
VID0_D[7:0], HSYNC[0], VSYNC[0], FIELD[0]	t_{VIS}	Video Data, Horizontal Sync, Vertical Sync, Field setup time to Video Pixel Clock 0	3.5	—	—
	t_{VIH}	Video Data, Horizontal Sync, Vertical Sync, Field hold time from Video Pixel Clock 0	2.8	—	—
VID2_D[7:0], HSYNC[2], VSYNC[2], FIELD[2]	t_{VIS}	Video Data, Horizontal Sync, Vertical Sync, Field setup time to Video Pixel Clock 2	3.5	—	—
	t_{VIH}	Video Data, Horizontal Sync, Vertical Sync, Field hold time from Video Pixel Clock 2	2.8	—	—
VID[2]_D[7:0], HSYNC[2], VSYNC[2], FIELD[2] *VID2 port is output.	t_{VCQ}	Video Data, Horizontal Sync, Vertical Sync, Field delay from Video Pixel Clock 2. Video Pixel Clock 2 is configured as output clock.	4.0	—	13

1. All timing values are with respect to the rising edge on the VID_PIXCLK pin. This clock can be supplied either by an external device or by the MAX64180.

Table 5-19. High Definition Video Interface Timing Parameters

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)[1]		
			MIN	TYP	MAX
VID[0,2]_PIXCLK	t_{VC}	Video Pixel Clock cycle time (74.25MHz)	—	13.468	
	t_{VH}	Video Pixel Clock high time	6.06	6.73	7.41
	t_{VL}	Video Pixel Clock low time	$t_{VC} - t_{VH}$		
	t_{VR}	Video Pixel Clock slew (rise time)	Not Applicable		
	t_{VF}	Video Pixel Clock slew (fall time)	Not Applicable		
VID0_D[7:0][2], HSYNC[0], VSYNC[0], FIELD[0]	t_{VIS}	Video Data, Horizontal Sync, Vertical Sync, Field setup time to Video Pixel Clock 0	2.5	—	—
	t_{VIH}	Video Data, Horizontal Sync, Vertical Sync, Field hold time from Video Pixel Clock 0	2.8	—	—
VID[2]_DATA[2], HSYNC[2], VSYNC[2], FIELD[2]	t_{VIS}	Video Data, Horizontal Sync, Vertical Sync, Field setup time to Video Pixel Clock 2	2.5	—	—
	t_{VIH}	Video Data, Horizontal Sync, Vertical Sync, Field hold time from Video Pixel Clock 2	2.8	—	—

1. All timing values are with respect to the rising edge on the VID_PIXCLK pin. This clock should be supplied either by an external device or by the MAX64180.
2. The external device should drive the data on the falling edge of VID_PIXCLK to satisfy the input hold requirements.

Table 5-20. High-Speed Video Interface Timing Parameters

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)[1]		
			MIN	TYP	MAX
VID[0,2]_PIXCLK	t_{VC}	Video Pixel Clock cycle time (100MHz)	—	10	
	t_{VH}	Video Pixel Clock high time	4	5	6
	t_{VL}	Video Pixel Clock low time	$t_{VC} - t_{VH}$		
	t_{VR}	Video Pixel Clock slew (rise time)	Not Applicable		
	t_{VF}	Video Pixel Clock slew (fall time)	Not Applicable		
VID0_D[7:0][2], HSYNC[0], VSYNC[0], FIELD[0]	t_{VIS}	Video Data, Horizontal Sync, Vertical Sync, Field setup time to Video Pixel Clock 0	2.5	—	—
	t_{VIH}	Video Data, Horizontal Sync, Vertical Sync, Field hold time from Video Pixel Clock 0	2.8	—	—
VID[2]_DATA[2], HSYNC[2], VSYNC[2], FIELD[2]	t_{VIS}	Video Data, Horizontal Sync, Vertical Sync, Field setup time to Video Pixel Clock 2	2.5	—	—
	t_{VIH}	Video Data, Horizontal Sync, Vertical Sync, Field hold time from Video Pixel Clock 2	2.8	—	—

1. All timing values are with respect to the rising edge on the VID_PIXCLK pin. This clock should be supplied either by an external device or by the MAX64180.
2. The external device should drive the data on the falling edge of VID_PIXCLK to satisfy the input hold requirements.

5.3.2 Audio Interface AC Timing

Figure 5-25 shows the I2S protocol, where the most significant bit is sent one Audio Bit Clock (AUD0_BCK) cycle after the Audio Left Right Clock (AUD0_LRCK) signal has transitioned. In this mode, when LRCK is high, the data is from the right channel, and when LRCK is low, the data is from the left channel.

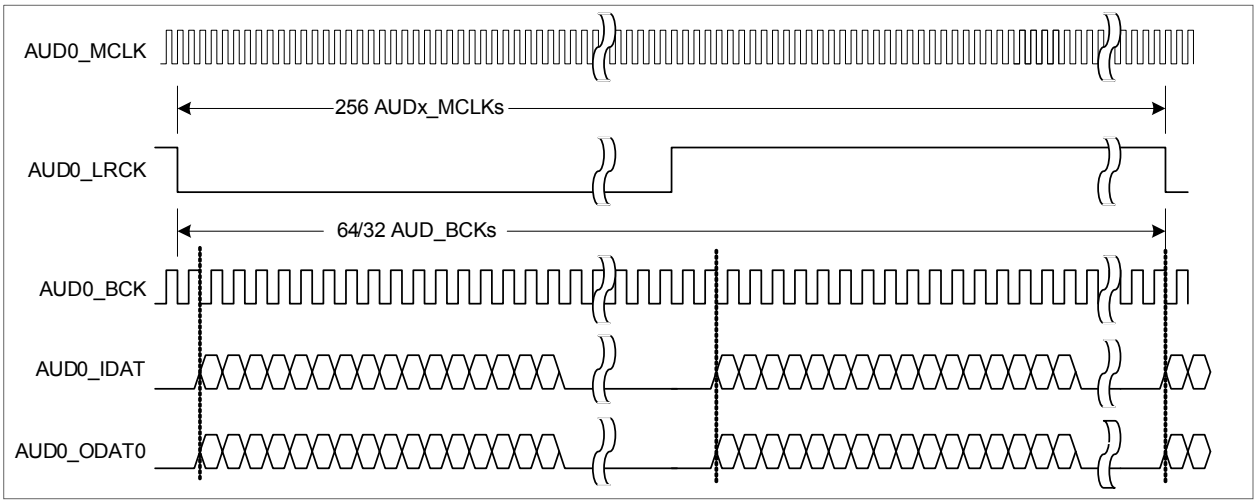


Figure 5-25. Standard Audio Timing

Figure 5-26 shows sample waveforms for 16-bit left-justified audio. The most significant bit for each audio sample is aligned with LRCK's transition. The Audio Input Interface ignores the data bus after the least significant bit for each sample.

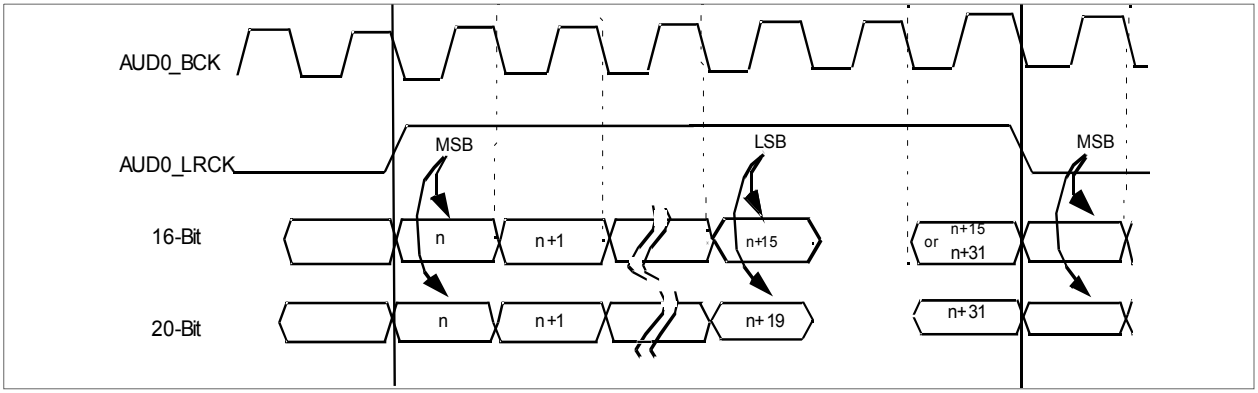


Figure 5-26. 16-, 20-Bit Left Justified Audio Waveform

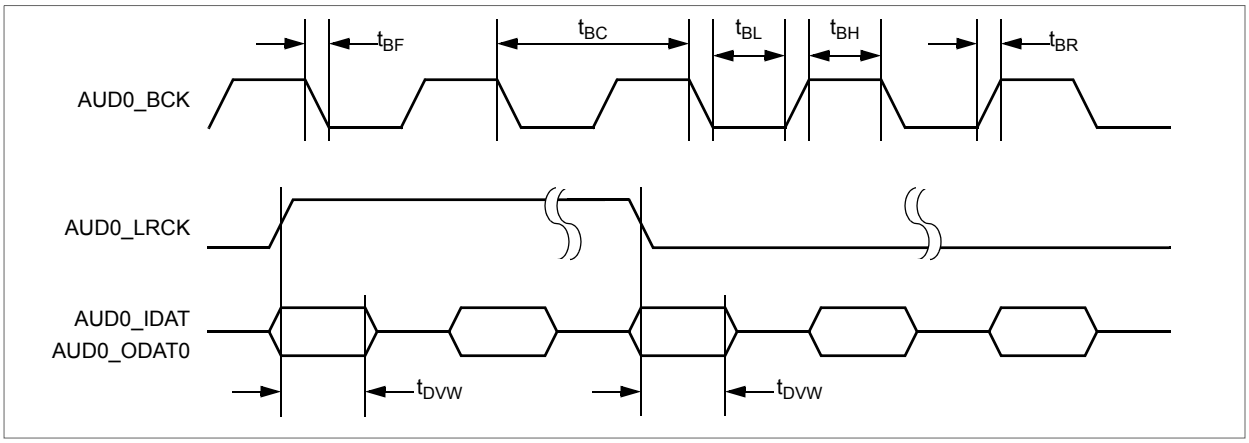


Figure 5-27. Audio Interface Timing

Table 5-21 lists the AC timing for audio operations.

Table 5-21. Audio Interface Timing Parameters

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)		
			MIN	TYP	MAX
AUD0_BCK	t_{BC}	Audio Bit Clock cycle time (Fs = 48kHz, 64 BCK/Sample)	—	325.5	—
	t_{BC}	Audio Bit Clock cycle time (Fs = 48kHz, 32 BCK/Sample)	—	651.04	—
	t_{BC}	Audio Bit Clock cycle time (Fs = 32kHz, 64 BCK/Sample)	—	488.28	—
	t_{BC}	Audio Bit Clock cycle time (Fs = 32kHz, 32 BCK/Sample)	—	976.56	—
	t_{BH}	Audio Bit Clock high time	$t_{BC}/2 * 0.8$	$t_{BC}/2$	$t_{BC}/2 * 1.2$
	t_{BL}	Audio Bit Clock low time ($t_{BC} - t_{BH}$)	$t_{BC} – t_{BH}$		
	t_{BR}	Audio Bit Clock slew (rise time)	—	—	3
	t_{BF}	Audio Bit Clock slew (fall time)	—	—	3
AUD0_LRCK AUD0_ODAT0 AUD0_IDAT	t_{DVW} [1]	Data valid window for slave mode operation (Fs = 48kHz or 32kHz)	$t_{BC}/4 + 15$	—	—
	t_{DVW}	Data valid window for master mode operation (Fs = 48kHz or 32kHz)	$t_{BC}/4 – 15$	—	—

1. There is no restriction on the position of the data valid window relative to BCK. The internal data sampling position is programmable and can be repositioned in t_{BC}.

5.3.3 Host Interface AC Timing

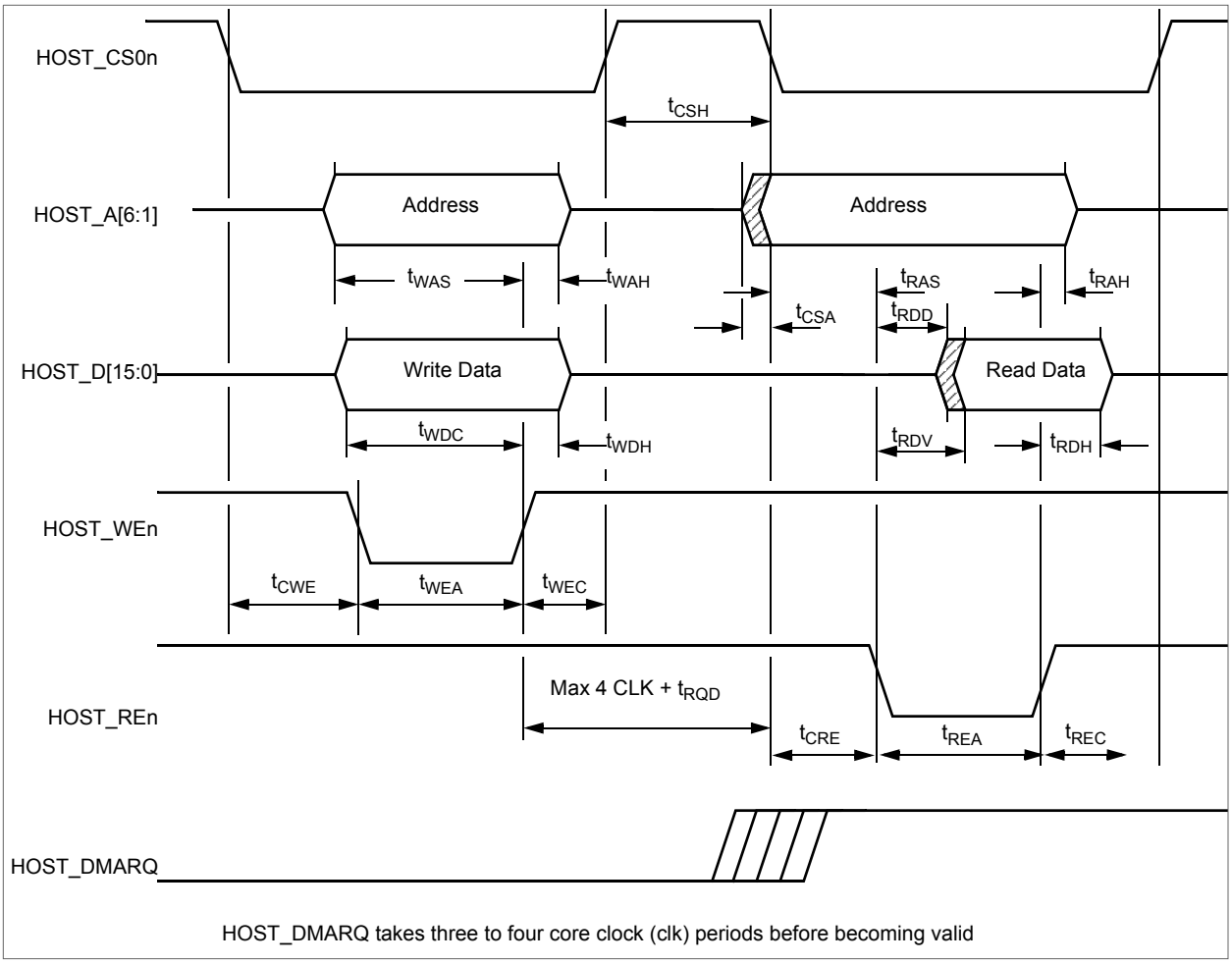


Figure 5-28. Host Interface Timing

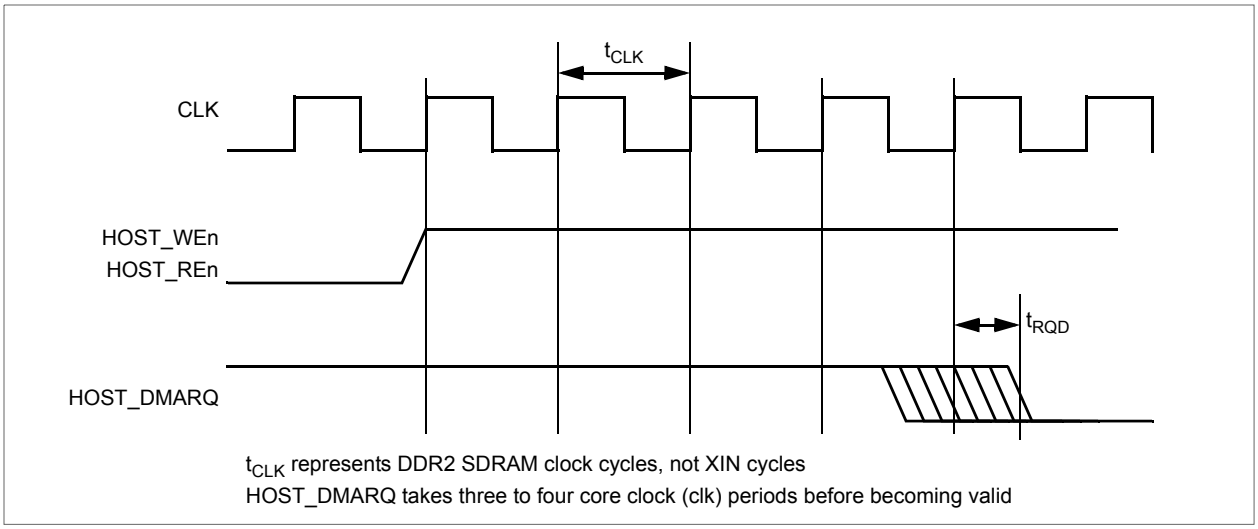


Figure 5-29. Host Direct Memory Access (DMA) Timing

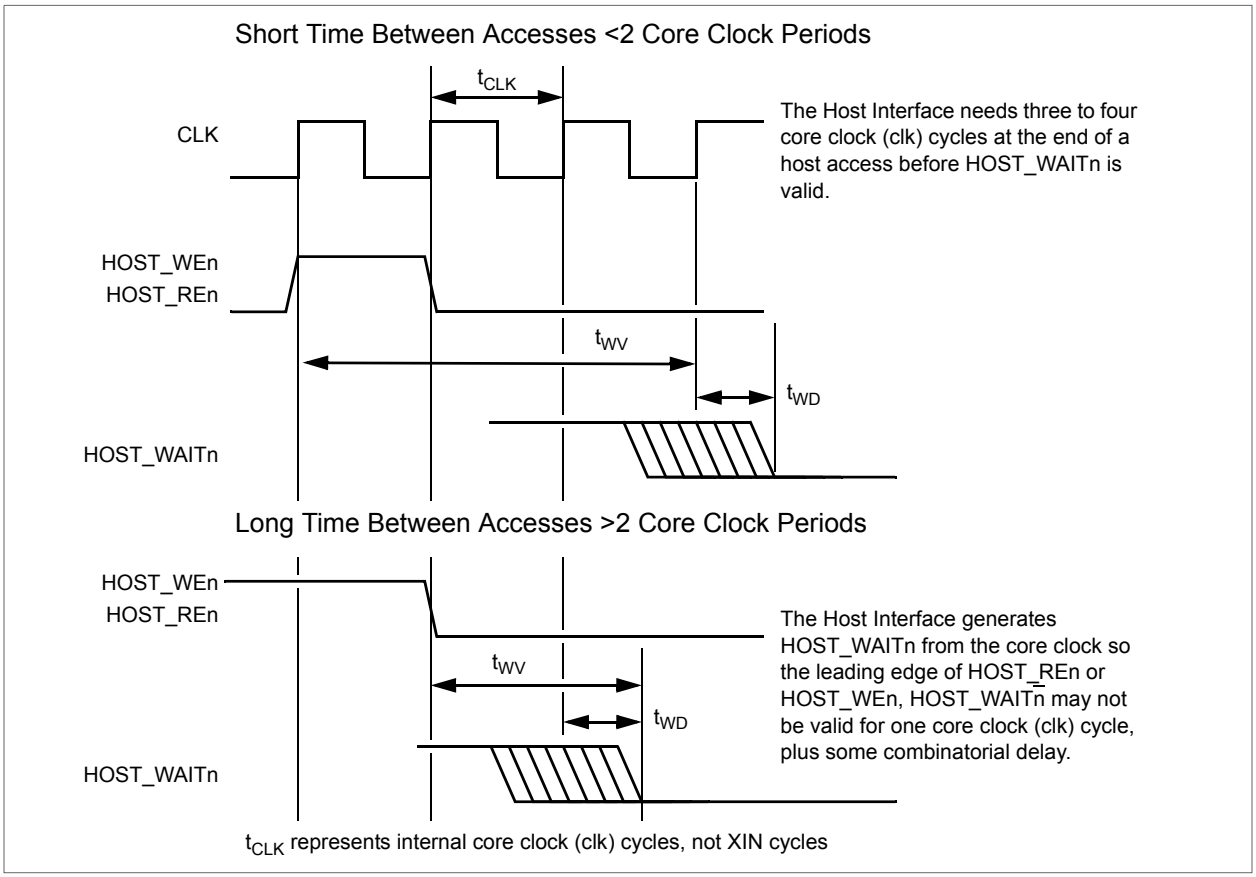


Figure 5-30. Host Wait Timing

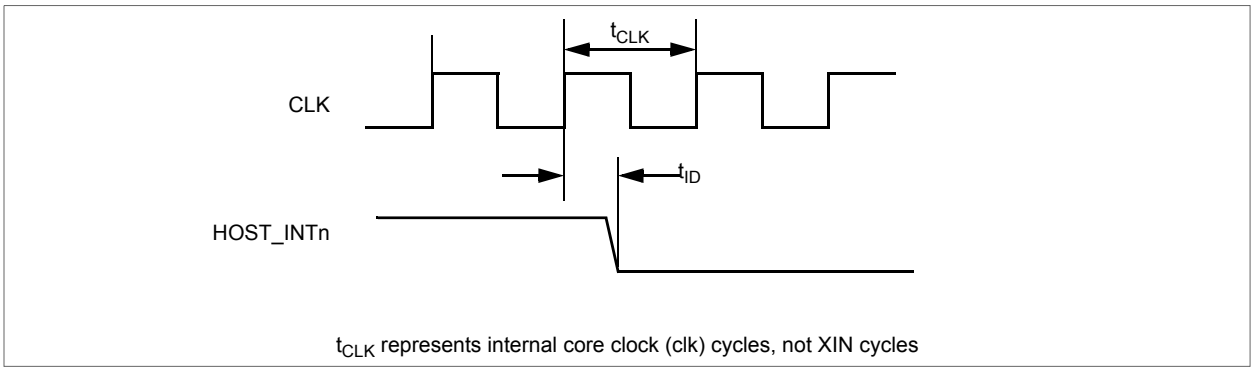


Figure 5-31. Host Interrupt Timing

Table 5-22. Host Interface Timing Parameters

SIGNAL	PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Core Clock	t_{CLK}	Crystal Oscillator (XIN x PLL) frequency	—	180	MHz
HOST_A[6:1]	t_{WAS}	Host Address setup to trailing edge Host Write Enable for write cycles	20	—	ns
	t_{WAH}	Host Address hold from trailing edge Host Write Enable for write cycles	3	—	ns
	t_{RAS}	Host Address setup to leading edge Host Read Enable for read cycles	0	—	ns
	t_{RAH}	Host Address hold from trailing edge Host Read Enable for read cycles	0	—	ns
	t_{CSA}	Host Address setup to leading edge of Host Chip Select	0	—	ns
HOST_D[15:0]	t_{WDC}	Host Data setup to trailing edge Host Write Enable for write cycles	12	—	ns
	t_{WDH}	Host Data hold from trailing edge Host Write Enable for write cycles	3	—	ns
	t_{RDD}	Host Data driven from leading edge Host Read Enable for read cycles	0	—	ns
	t_{RDV}	Host Data valid from leading edge Host Read Enable for read cycles	—	17	ns
	t_{RDH}	Host Data hold from trailing edge Host Read Enable for read cycles	2	11	ns
HOST_WEn	t_{CWE}	Host Chip Select active to Host Write Enable active	0	—	ns
	t_{WEC}	Host Write Enable inactive to Host Chip Select inactive	3	—	ns
	t_{WEA}	Host Write Enable active time	20	—	ns
HOST_REn	t_{CRE}	Host Chip Select active to Read Enable active	0	—	ns
	t_{REC}	Host Read Enable inactive to Host Chip Select inactive	0	—	ns
	t_{REA}	Host Read Enable active time	20	—	ns
HOST_CS0n	t_{CSH}	Host Chip Select inactive time between accesses	10	—	ns

SIGNAL	PARAMETER	DESCRIPTION	MIN	MAX	UNITS
HOST_DMARQ	t_{RQD}	Host Direct Memory Access Request valid from internal clock	—	8	ns
HOST_INTn	t_{ID}	Host Interrupt valid from internal clock			
HOST_WAITn	t_{WD}	Host Wait valid from internal clock	—	8	ns
	t_{WV}	Host Wait valid from Host Read Enable/Host Write Enable	—	12	ns

5.3.4 DDR2 SDRAM Interface AC Timing

The MAX64180 adheres to the JEDEC definition of timing for SDRAMs. Refer to the appropriate specifications when designing the SDRAM Interface: JEDEC Standard JESD79-2C DDR2 SDRAM Specification, http://www.jedec.org/download/search/JESD79-2C.pdf

5.3.5 SPI/Bitstream Interface AC Timing

This section shows the timing for the Serial Peripheral interface and Bitstream interface. The timing for the two interfaces is identical irrespective of the interface being used.

Timing is shown for the following set of conditions:

1. BS_CLK driven from a source external to the MAX64180 and data mastered by a source external to the MAX64180.
2. BS_CLK driven from a source external to the MAX64180 and data mastered by the MAX64180.
3. BS_CLK mastered from the MAX64180 internal source and data mastered by a source external to the MAX64180.
4. BS_CLK mastered from the MAX64180 internal source and data mastered by the MAX64180.

BS_CLK driven from a Source External to the MAX64180 and Data Mastered by a Source External to the MAX64180

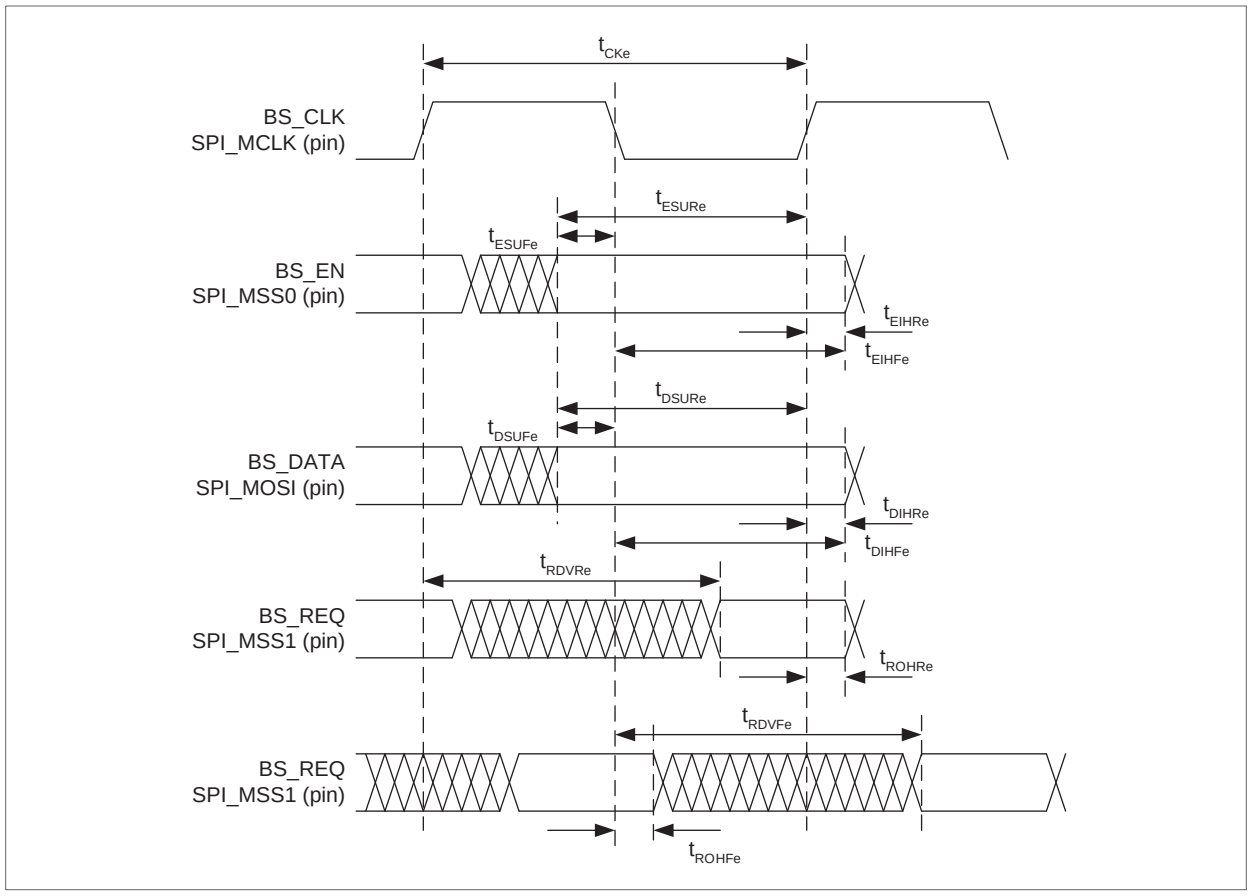


Figure 5-32. Bitstream Timing with an External Clock and External Data Master

Table 5-23. Bitstream Timing Parameters 1

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)		
			MIN	TYP	MAX
BS_CLK SPI_MCLK	t_{CKe}	External Clock period	12.0		
BS_EN SPI_MSS0	t_{ESUFe}	Bitstream Enable setup to falling edge of BS_CLK	4.0		
	t_{ESURe}	Bitstream Enable setup to rising edge of BS_CLK	4.0		
	t_{EIHFe}	Bitstream Enable input hold from falling edge of BS_CLK	0.5		
	t_{EIHRe}	Bitstream Enable input hold from rising edge of BS_CLK	0.5		
BS_DATA SPI_MOSI	t_{DSUFe}	Bitstream Data setup to falling edge of BS_CLK	3.5		
	t_{DSURe}	Bitstream Data setup to rising edge of BS_CLK	3.5		
	t_{DIHFe}	Bitstream Data input hold from falling edge of BS_CLK	0.5		
	t_{DIHRe}	Bitstream Data input hold from rising edge of BS_CLK	0.5		
BS_REQ SPI_MSS1	t_{RDVFe}	Bitstream Request data valid from falling edge of BS_CLK			12.5
	t_{RDVRe}	Bitstream Request data valid from rising edge of BS_CLK			12.5
	t_{ROHFe}	Bitstream Request output hold from falling edge of BS_CLK	2.0		
	t_{ROHRe}	Bitstream Request output hold from rising edge of BS_CLK	2.0		

BS_CLK Driven from a Source External to the MAX64180 and Data Mastered by the MAX64180

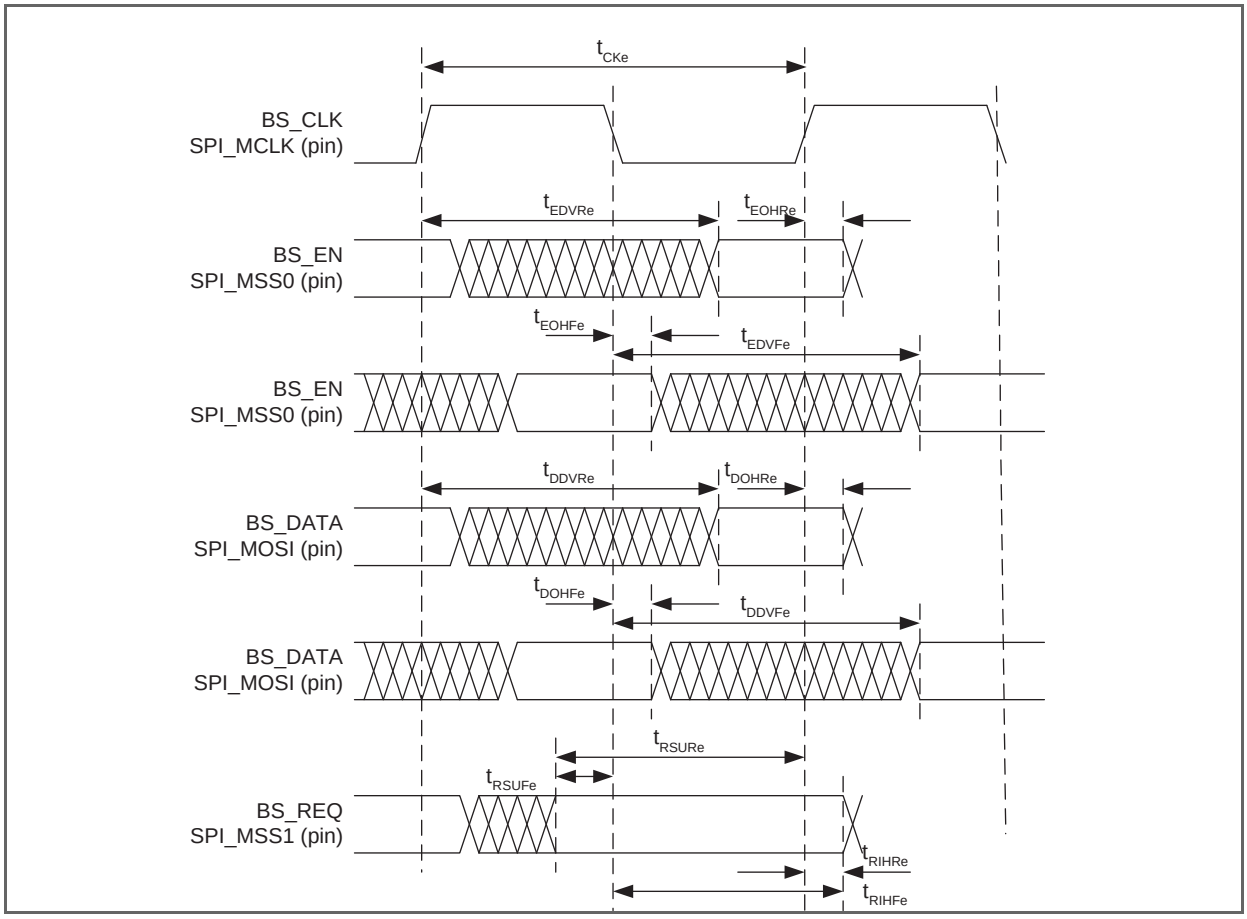


Figure 5-33. Bitstream Timing with an External Clock and Internal Data Master

Table 5-24. Bitstream Timing Parameters 2

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)		
			MIN	TYP	MAX
BS_CLK SPI_MCLK	t_{CKe}	External Clock period	12.0		
BS_EN SPI_MSS0	t_{EDVFe}	Bitstream Enable data valid from falling edge of BS_CLK			12.5
	t_{EDVRe}	Bitstream Enable data valid from rising edge of BS_CLK			12.5
	t_{EOHFe}	Bitstream Enable output hold from falling edge of BS_CLK	2.0		
	t_{EOHRe}	Bitstream Enable output hold from rising edge of BS_CLK	2.0		
BS_DATA SPI_MOSI	t_{DDVFe}	Bitstream Data valid from falling edge of BS_CLK			12.0
	t_{DDVRe}	Bitstream Data valid from rising edge of BS_CLK			12.0
	t_{DOHFe}	Bitstream Data output hold from falling edge of BS_CLK	2.0		
	t_{DOHRe}	Bitstream Data output hold from rising edge of BS_CLK	2.0		
BS_REQ SPI_MSS1	t_{RSUFe}	Bitstream Request setup to falling edge of BS_CLK	3.0		
	t_{RSURe}	Bitstream Request setup to from rising edge of BS_CLK	3.0		
	t_{RIHFe}	Bitstream Request input hold from falling edge of BS_CLK	0.5		
	t_{RIHRe}	Bitstream Request input hold from rising edge of BS_CLK	0.5		

BS_CLK Mastered from the MAX64180 Internal Source and Data Mastered by a Source External to the MAX64180

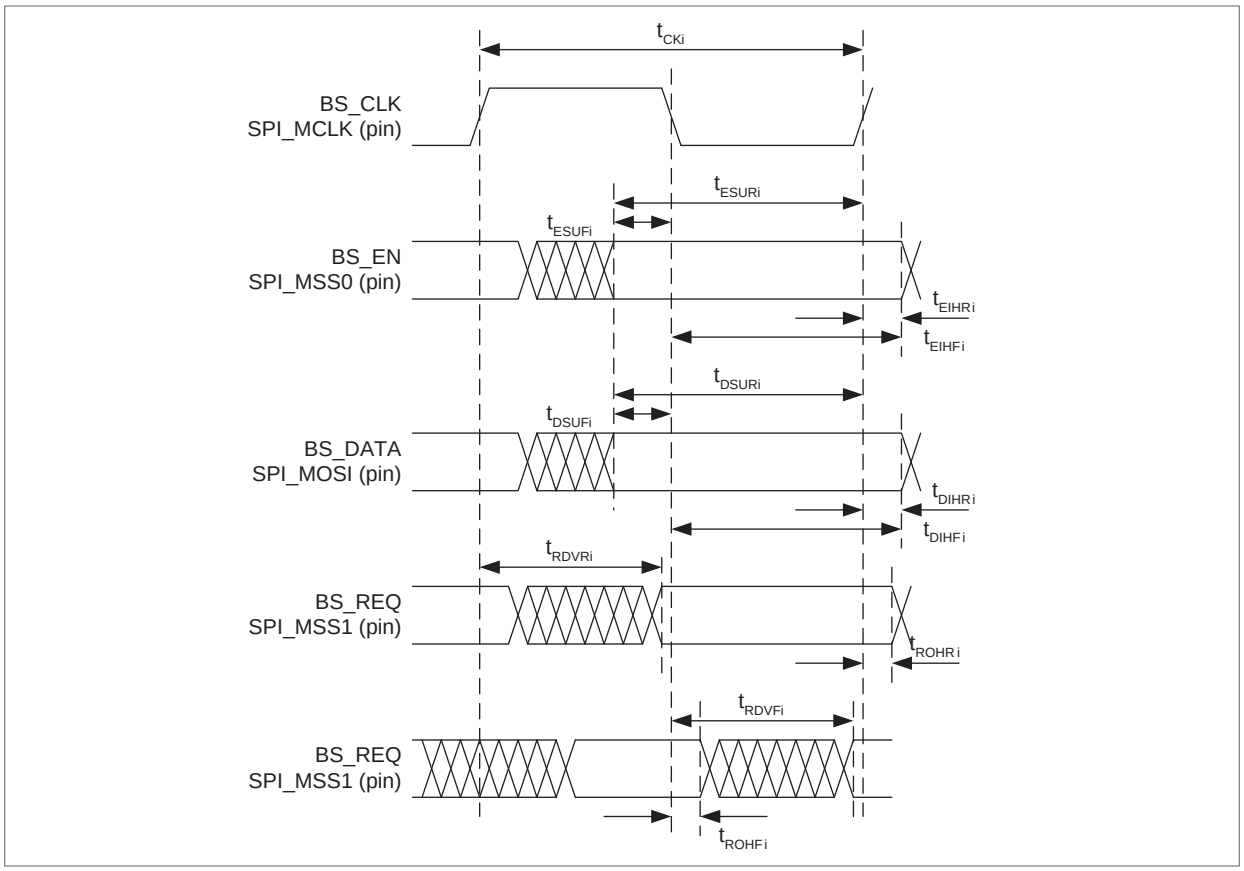


Figure 5-34. Bitstream Timing with an Internal Clock and External Data Master

Table 5-25. Bitstream Timing Parameters 3

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)		
			MIN	TYP	MAX
BS_CLK SPI_MCLK	t_{CKi}	External Clock period	14.8		
BS_EN SPI_MSS0	t_{ESUFi}	Bitstream Enable setup to falling edge of BS_CLK	2.5		
	t_{ESURi}	Bitstream Enable setup to rising edge of BS_CLK	2.5		
	t_{EIHFi}	Bitstream Enable input hold from falling edge of BS_CLK	0.5		
	t_{EIHRi}	Bitstream Enable input hold from rising edge of BS_CLK	0.5		
BS_DATA SPI_MOSI	t_{DSUFi}	Bitstream Data setup to falling edge of BS_CLK	2.0		
	t_{DSURi}	Bitstream Data setup to rising edge of BS_CLK	2.0		
	t_{DIHFi}	Bitstream Data input hold from falling edge of BS_CLK	0.5		
	t_{DIHRi}	Bitstream Data input hold from rising edge of BS_CLK	0.5		
BS_REQ SPI_MSS1	t_{RDVFi}	Bitstream Request data valid from falling edge of BS_CLK			5.0
	t_{RDVRi}	Bitstream Request data valid from rising edge of BS_CLK			5.0
	t_{ROHFi}	Bitstream Request output hold from falling edge of BS_CLK	2.0		
	t_{ROHRi}	Bitstream Request output hold from rising edge of BS_CLK	2.0		

BS_CLK Mastered from the MAX64180 Internal Source and Data Mastered by the MAX64180

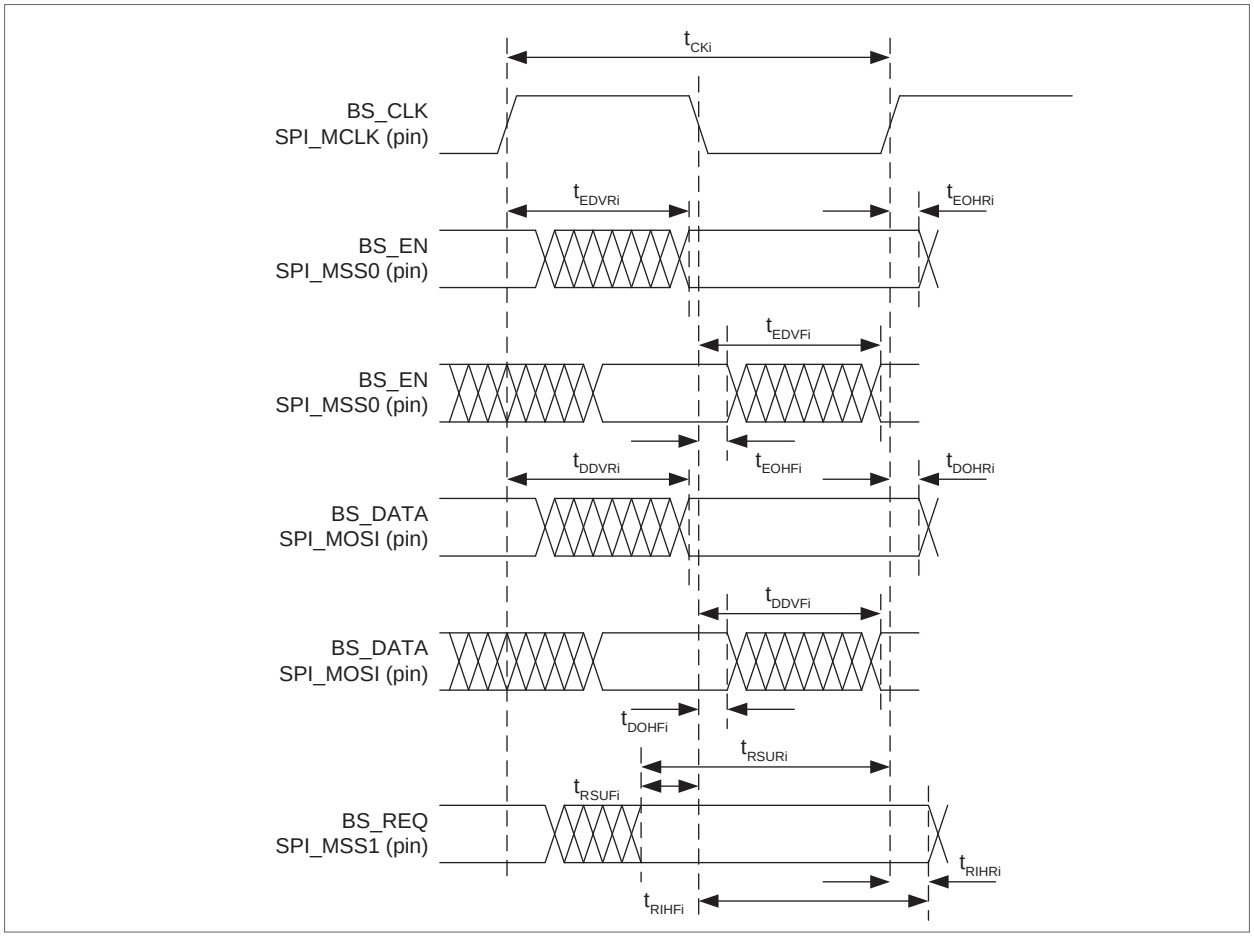


Figure 5-35. Bitstream Timing with an Internal Clock and Internal Data Master

Table 5-26. Bitstream Timing Parameters 4

SIGNAL	PARAMETER	DESCRIPTION	TIMING VALUE (ns)		
			MIN	TYP	MAX
BS_CLK SPI_MCLK	t_{CKi}	External Clock period	14.8		
BS_EN SPI_MSS0	t_{EDVFi}	Bitstream Enable data valid from falling edge of BS_CLK			5.0
	t_{EDVRi}	Bitstream Enable data valid from rising edge of BS_CLK			5.0
	t_{EOHFi}	Bitstream Enable output hold from falling edge of BS_CLK	2.0		
	t_{EOHRi}	Bitstream Enable output hold from rising edge of BS_CLK	2.0		
BS_DATA SPI_MOSI	t_{DDVFi}	Bitstream Data valid from falling edge of BS_CLK			4.5
	t_{DDVRi}	Bitstream Data valid from rising edge of BS_CLK			4.5
	t_{DOHFi}	Bitstream Data output hold from falling edge of BS_CLK	2.0		
	t_{DOHRi}	Bitstream Data output hold from rising edge of BS_CLK	2.0		
BS_REQ SPI_MSS1	t_{RSUFi}	Bitstream Request setup to falling edge of BS_CLK	1.0		
	t_{RSURi}	Bitstream Request setup to from rising edge of BS_CLK	1.0		
	t_{RIHFi}	Bitstream Request input hold from falling edge of BS_CLK	0.5		
	t_{RIHRi}	Bitstream Request input hold from rising edge of BS_CLK	0.5		

6 Pin Definitions

This section contains an illustration of the device pin layout and pin identification tables for the MAX64180.

6.1 MAX64180 Pin Configuration—248-Pin CTBGA

The MAX64180 device is available in a 248-pin, Chip Scale Thin Ball Grid Array (CTBGA). Figure 6-36 shows the top view of the device.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	HOST_WEn	HOST_D1	HOST_D3	HOST_D6	HOST_D4	HOST_D9	HOST_D14	HOST_D12	GPIO_0	GPIO_2	UARTD_TXD	SPI_MCLK	SPI_MSS1	SPI_MISO	VID2_D0	VID2_D2	VID2_D4	VID2_FIELD	A
B	HOST_REn	HOST_D0	HOST_D7	HOST_D11	HOST_D5	HOST_D15	HOST_D8	HOST_D13	GPIO_1	GPIO_3	UARTD_RXD	TWI0_SCL	SPI_MOSI	SPI_MSS0	VID2_HSYNC	VID2_VSYNC	VID2_D6	VID2_D7	B
C	HOST_A5	HOST_DMARQ	HOST_INTn	HOST_WAITn	HOST_D2	HOST_VDD	HOST_D10	GND	PWM_0	GND	TWI0_SDA	GND	VID23_VDD	VID23_VDD	VID2_D3	VID2_D1	VID2_D5	GPIO_02_07	C
D	HOST_A3	HOST_A2	HOST_A6													GPIO_02_08	VID2_PIXCLK	USB_GND	D
E	HOST_CS0n	HOST_A1	HOST_A4		HOST_VDD	HOST_VDD	HOST_VDD	CORE_VDD	CORE_VDD	CORE_VDD	CORE_VDD	CORE_VDD	CORE_VDD	CORE_VDD		GPIO_02_06	USB_GND	USB_XIN	E
F	CLK_IN	CLK_SEL	PLL_VDD		HOST_VDD									USB_DVDD		USB_GND	USB_ANA_TST	USB_XO	F
G	GND	GND	GND		GND		GND	GND	GND	GND	GND	GND		USB_GND		USB_GND	USB_ID	USB_VBUS	G
H	DDR_VDD	DDR_VDD	DDR_VDD		CORE_VDD		GND		GND	GND		GND		USB_AVDD		USB_AVDD	USB_REXT	USB_DM	H
J	DDR_A3	DDR_A2	DDR_VDD		DDR_VDD		GND	GND	GND	GND	GND	GND		GND		USB_AVDD	USB_AVDD	USB_DP	J
K	DDR_A1	DDR_A0	DDR_A10		DDR_VDD		GND	GND	GND	GND	GND	GND		VID01_VDD		HOST_CFG_0	CFG	USB_AVDD	K
L	DDR_BA1	DDR_A5	DDR_BA0		DDR_VDD		GND		GND	GND		GND		VID01_VDD		VID0_VSYNC	VID0_FIELD	VID0_PIXCLK	L
M	DDR_A8	DDR_A4	DDR_A12		DDR_VDD		GND	GND	GND	GND	GND	GND		VID01_VDD		VID0_HYSNC	VID0_D0	VID0_OUTCLK	M
N	DDR_A7	DDR_A6	DDR_A11		DDR_VDD									VID01_VDD		VID0_D1	VID0_D2	VID0_D3	N
P	DDR_A9	DDR_RASn	DDR_CASn		DDR_VDD	DDR_VDD	DDR_VDD	DDR_VDD	CORE_VDD	CORE_VDD	CORE_VDD	CORE_VDD	CORE_VDD	CORE_VDD		VID0_D4	VID0_D5	VID0_D6	P
R	DDR_CSn	DDR_CKE	DDR_WEn													RESETn	JTAG_TAP_SEL	VID0_D7	R
T	DDR_DQ5	DDR_DQ7	DDR_VREF0	DDR_DQ6	DDR_DQ14	DDR_DQ9	DDR_VREF1	DDR_DQ13	DDR_VDD	DDR_VDD	DDR_VDD	GND	CORE_VDD	AUD_VDD	AUD0_ODATA0	AUD0_SPDIF	TEST	JTAG_TRSTn	T
U	DDR_DQ0	DDR_DQ4	DDR_DQS0	DDR_DQ2	DDR_DQ8	DDR_DQS1	DDR_DQ10	DDR_DQ12	DDR_CLK0	DDR_PADHI	DDR_VDD	GND	CORE_VDD	AUD_VDD	AUD0_LRCK	AUD0_IDAT	JTAG_TDI	JTAG_TDO	U
V	DDR_DQM0	DDR_DQ1	DDR_DQS0n	DDR_DQ3	DDR_DQ15	DDR_DQS1n	DDR_DQM1	DDR_DQ11	DDR_CLK0n	DDR_PADLO	DDR_VDD	GND	CORE_VDD	AUD_VDD	AUD0_MCLK	AUD0_BCK	JTAG_TCK	JTAG_TMS	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 6-36. MAX64180 SoC Signal Positions (Top View)

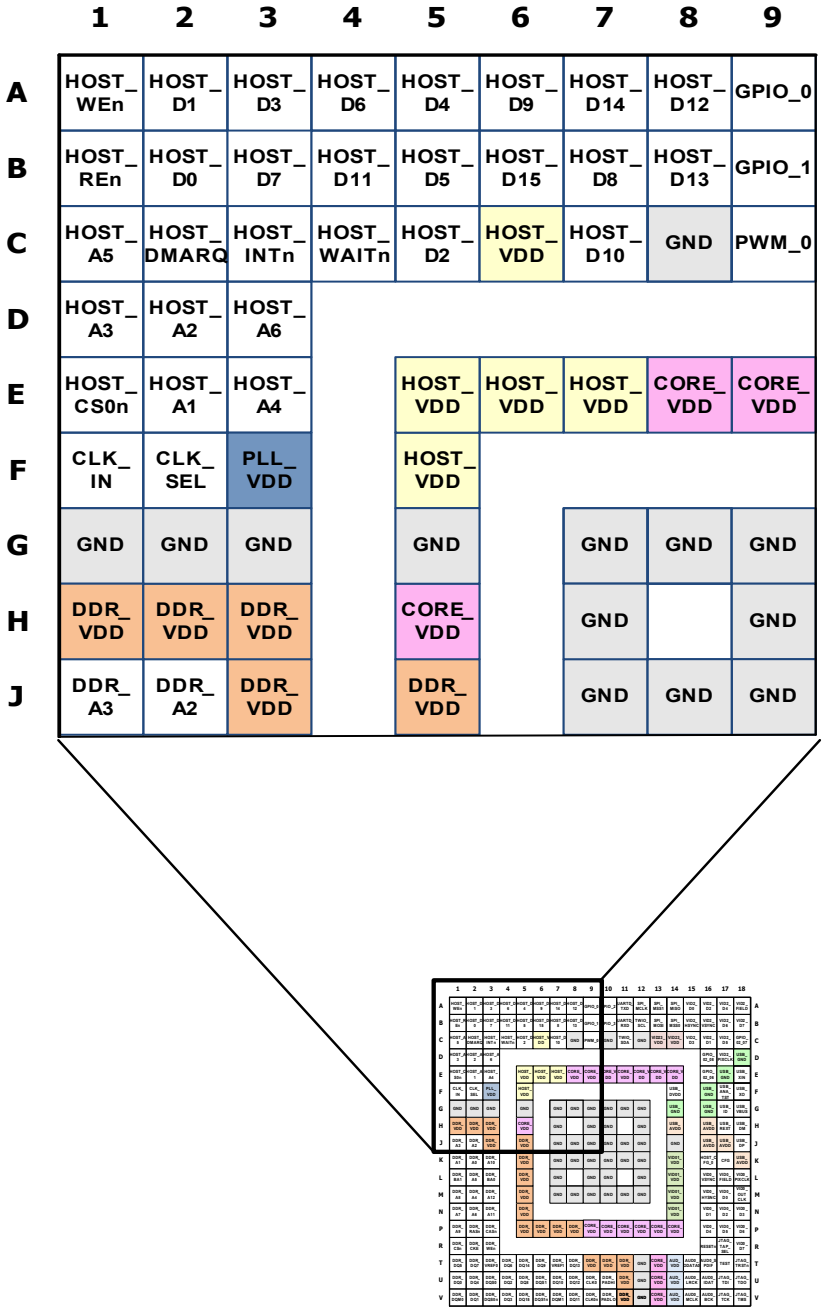


Figure 6-37. Upper-Left Quadrant

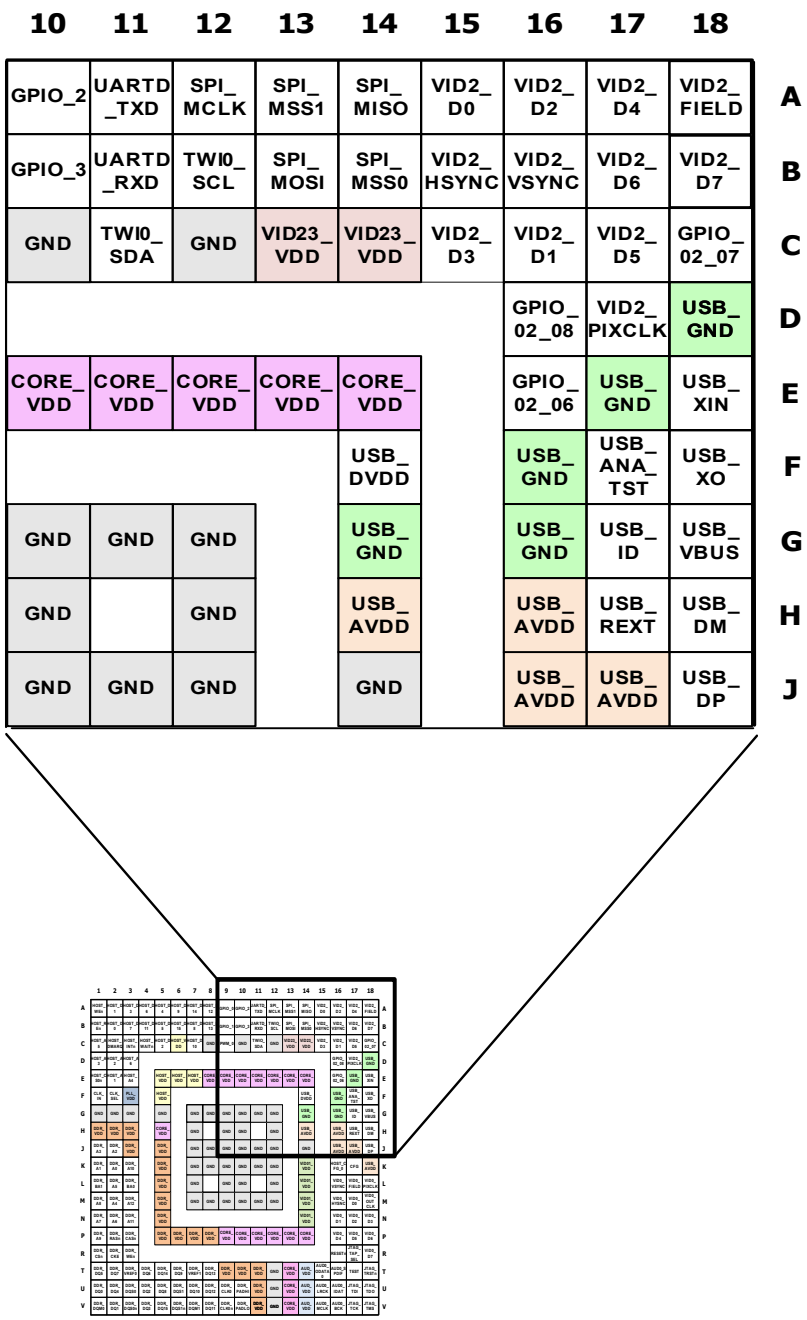


Figure 6-38. Upper-Right Quadrant

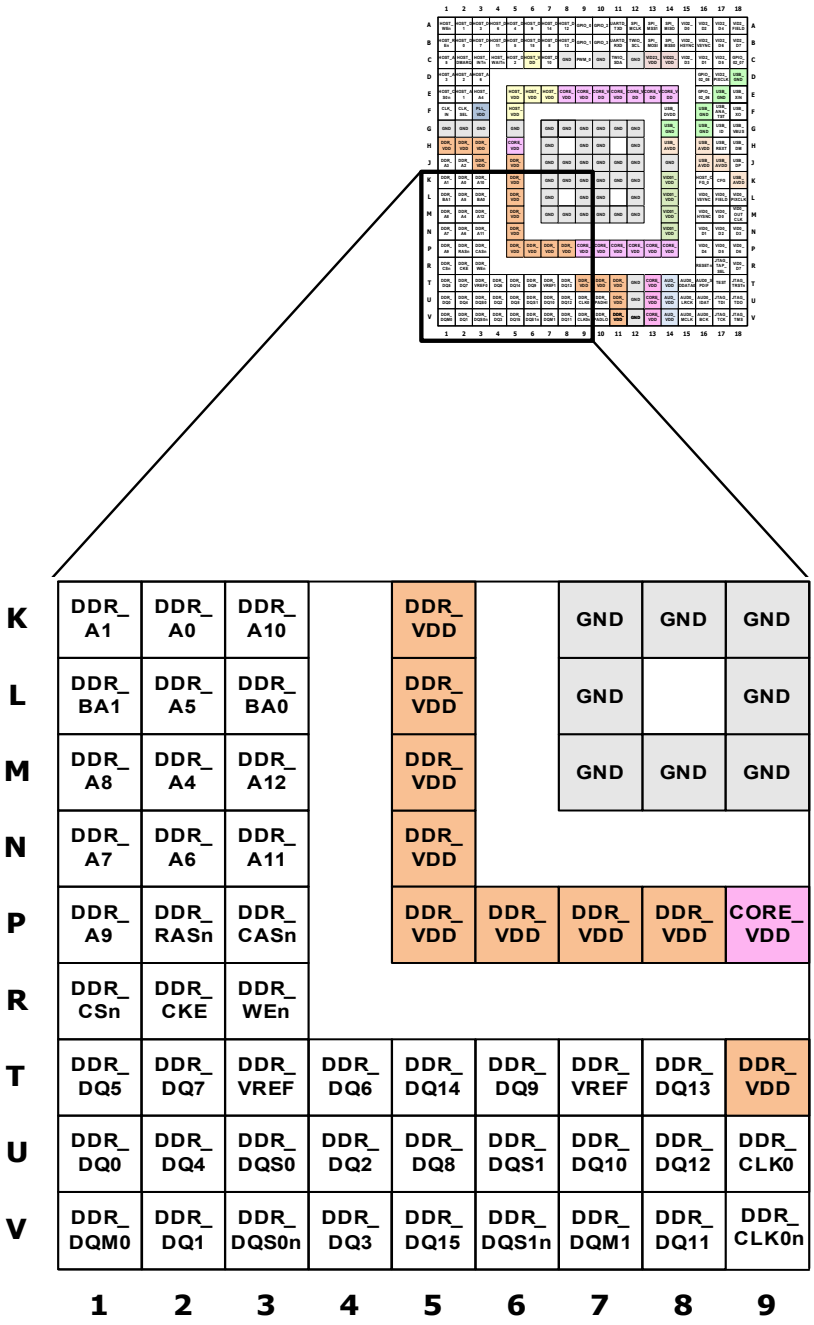


Figure 6-39. Bottom-Left Quadrant

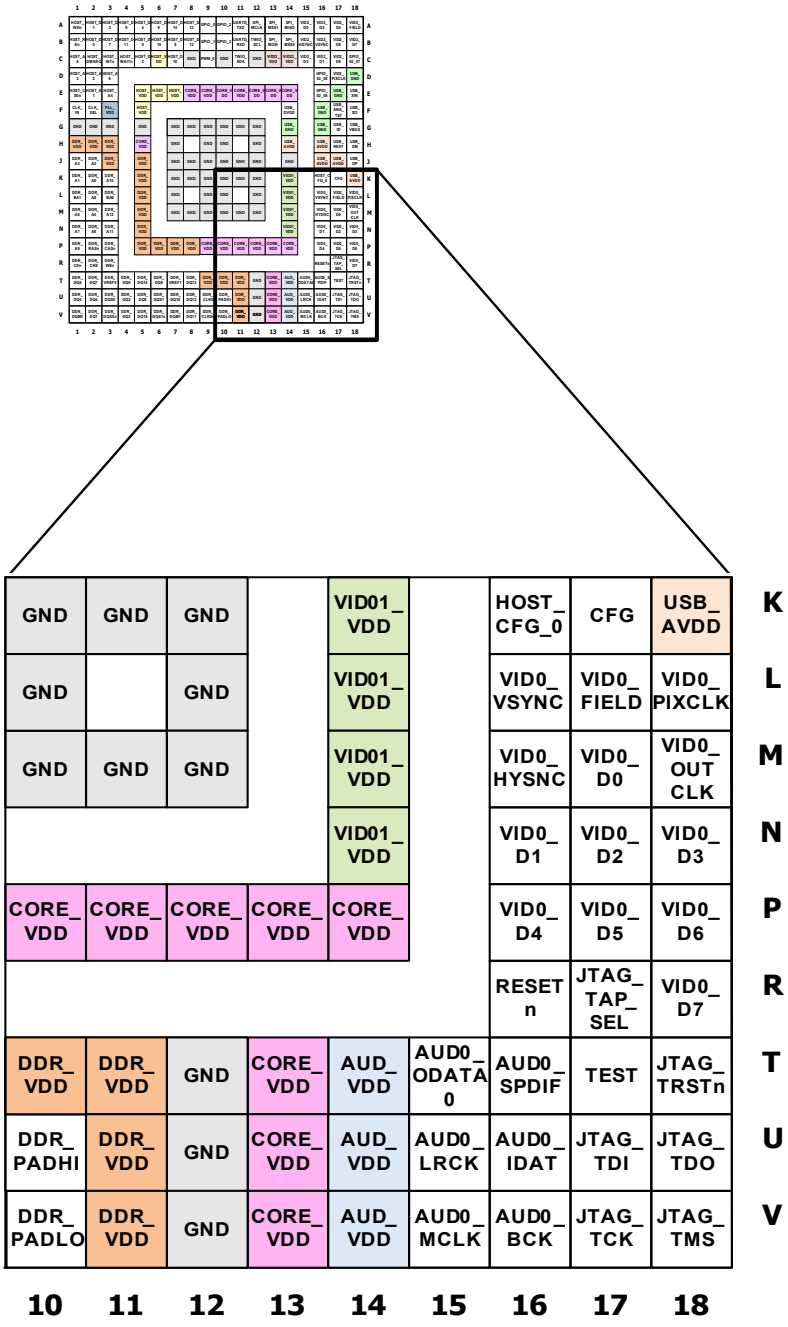


Figure 6-40. Bottom-Right Quadrant

6.2 Signal Definitions

The I/O signal descriptions in the pin identification tables use the following terms:

- I—Input only
- O—Output only
- I/O— Input or output
- IOD—Input/Open Drain output
- A—Analog

6.3 Pin Identifications

This section contains the functional pin descriptions for the MAX64180. The 248 signals are divided into signal groups as shown in Table 6-27.

Table 6-27. Signal Group Names

SIGNAL GROUP	REFERENCE
Audio	"Audio Signal Group," page 90
Video Port 0	"Video Port 0 Signal Group," page 91
Video Port 2	"Video Port 2 Signal Group," page 92
Host	"Host Signal Group," page 93
DDR2 SDRAM	"DDR2 SDRAM Signal Group," page 94
USB	"USB Signal Group," page 96
UART	"UART Signal Group," page 96
SPI	"SPI/Bitstream Signal Group," page 97
TWI	"TWI Signal Group," page 97
PWM	"PWM Signal Group," page 98
GPIO	"GPIO Signal Group," page 98
JTAG	"JTAG Signal Group," page 100
Configuration	"Configuration," page 100
Clock	"Clock," page 101
Reset	"Reset," page 101
Power and Ground	"Power and Ground Pins," page 102

6.4 Pin Muxing

Many pins are multiplexed which means they can have more than one function. All pins have a primary function, and the name that is assigned to the pin reflects the primary function. Many pins have an alternate (ALT) function that can be used when their primary function is not being used. GPIO function is available as an additional third option on few pins. GPIO pins are available for customer use.

Table 6-28 shows pins that have multiple functions. Signals that are active low end with a lower case ‘n’.

Table 6-28. Pin Muxing

PIN	PRIMARY FUNCTION	ALTERNATE FUNCTION	GPIO FUNCTION
Audio			
T16	AUD0_SPDIF	–	GPIO_1_21
Video Port 0			
M16	VID0_HSYNC	–	GPIO_2_00
L16	VID0_VSYNC	–	GPIO_2_01
L17	VID0_FIELD	–	GPIO_1_19
Video Port 1			
A18	VID2_FIELD	–	GPIO_2_09
B15	VID2_HSYNC	–	GPIO_2_10
B16	VID2_VSYNC	–	GPIO_2_11
Host			
C3	HOST_INTn	–	GPIO_1_00
Configuration			
K17	CFG	–	GPIO_2_03
UART			
B11	UARTD_RXD	MME_RXD	–
A11	UARTD_TXD	MME_TXD	–
SPI/Bitstream			
A14	SPI_MISO	–	GPIO_2_16
B14	SPI_MSS0	BS_EN	GPIO_2_17
A13	SPI_MSS1	BS_REQ	GPIO_2_18
A12	SPI_MCLK	BS_CLK	GPIO_2_19
B13	SPI_MOSI	BS_DATA	GPIO_2_20
TWI			
B12	TWI0_SCL	TWI1_SCL	GPIO_2_21
C11	TWI0_SDA	TWI1_SDA	GPIO_2_22
PWM			
C9	PWM_0	–	GPIO_2_29
GPIO			

PIN	PRIMARY FUNCTION	ALTERNATE FUNCTION	GPIO FUNCTION
A9	GPIO_0	–	GPIO_0_00
B9	GPIO_1	–	GPIO_0_01
A10	GPIO_2	–	GPIO_0_02
B10	GPIO_3	–	GPIO_0_03

6.4.1 Audio Signal Group

The Audio signal group has six signals as shown in Table 6-29. The Audio group contains one I^2S input and one I^2S output that share common clocking. These signals are all in the AUD power domain.

Table 6-29. Audio Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
V16	AUD0_BCK	I/O	Audio Port 0 I^2S Bit Clock
U16	AUD0_IDAT	I	Audio Port 0 I^2S Input Data
U15	AUD0_LRCK	I/O	Audio Port 0 I^2S Left Right Clock indicates whether data is for the left or right channel
V15	AUD0_MCLK	I/O	Audio Port 0 I^2S Master Clock (256 times the sampling clock)
T15	AUD0_ODAT0	O	Audio Port 0 I^2S Output Data
T16	AUD0_SPDIF	O	Audio Port 0 Sony/Philips Digital Interface

6.4.2 Video Port 0 Signal Group

Video Port 0 signal group includes 13 signals to support an 8-bit video input port. These signals are in the VID0 power domain.

Table 6-30. Video Port 0 Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
R18	VID0_D7	I	Video Port 0 Data [7:0]
P18	VID0_D6	I	
P17	VID0_D5	I	
P16	VID0_D4	I	
N18	VID0_D3	I	
N17	VID0_D2	I	
N16	VID0_D1	I	
M17	VID0_D0	I	
M16	VID0_HSYNC	I	Video Port 0 Horizontal Sync
L16	VID0_VSYNC	I	Video Port 0 Vertical Sync
L17	VID0_FIELD	I	Video Port 0 Field
M18	VID0_OUTCLK	O	Video Port 0 Output Clock
L18	VID0_PIXCLK	I/O	Video Port 0 Pixel Clock

6.4.3 Video Port 2 Signal Group

The Video Port 2 signal group includes 15 signals to support an 8-bit bidirectional video port. These signals are in the VID2 power domain.

Table 6-31. Video Port 2 Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
B18	VID2_D7	I/O	Video Port 2 Data [7:0]
B17	VID2_D6	I/O	
C17	VID2_D5	I/O	
A17	VID2_D4	I/O	
C15	VID2_D3	I/O	
A16	VID2_D2	I/O	
C16	VID2_D1	I/O	
A15	VID2_D0	I/O	
A18	VID2_FIELD	I/O	Video Port 2 Field
B15	VID2_HSYNC	I/O	Video Port 2 Horizontal Sync
D17	VID2_PIXCLK	I/O	Video Port 2 Pixel Clock
B16	VID2_VSYNC	I/O	Video Port 2 Vertical Sync

6.4.4 Host Signal Group

The Host signal group has 28 signals as shown in Table 6-32. When the MAX64180 is in slave mode, the signals allow external processors to access resources inside the MAX64180. The signals are in the HOST power domain.

Table 6-32. Host Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
D3	HOST_A6	I	Host Address bits [6:1]
C1	HOST_A5	I	
E3	HOST_A4	I	
D1	HOST_A3	I	
D2	HOST_A2	I	
E2	HOST_A1	I	
E1	HOST_CS0n	I	Host Chip Select
B6	HOST_D15	I/O	Host Data bits [15:0]
A7	HOST_D14	I/O	
B8	HOST_D13	I/O	
A8	HOST_D12	I/O	
B4	HOST_D11	I/O	
C7	HOST_D10	I/O	
A6	HOST_D9	I/O	
B7	HOST_D8	I/O	
B3	HOST_D7	I/O	
A4	HOST_D6	I/O	
B5	HOST_D5	I/O	
A5	HOST_D4	I/O	
A3	HOST_D3	I/O	
C5	HOST_D2	I/O	
A2	HOST_D1	I/O	
B2	HOST_D0	I/O	
C2	HOST_DMARQ	O	Host Direct Memory Access Request
C3	HOST_INTn	IOD	Host Interrupt. In host slave mode, this signal is an open-collector output and requires a 1KOhm pull-up resistor.
B1	HOST_REn	I	Host Read Enable
C4	HOST_WAITn	IOD	Host Wait. This signal is always active low. In host slave mode, this signal is an open-collector output and requires a 1KOhm pull-up resistor.
A1	HOST_WEn	I	Host Write Enable

6.4.5 DDR2 SDRAM Signal Group

The DDR2 SDRAM signal group has 48 signals as shown in Table 6-33. The MAX64180 supports a single 16-bit DDR2 SDRAM configuration. These signals are in the DDR power domain.

Table 6-33. DDR2 SDRAM Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
U10	DDR_PADHI	A	Driver compensation for DDR2
V10	DDR_PADLO	A	Driver compensation for DDR2
M3	DDR_A12	O	SDRAM Address bits [12:0]
N3	DDR_A11	O	
K3	DDR_A10	O	
P1	DDR_A9	O	
M1	DDR_A8	O	
N1	DDR_A7	O	
N2	DDR_A6	O	
L2	DDR_A5	O	
M2	DDR_A4	O	
J1	DDR_A3	O	
J2	DDR_A2	O	
K1	DDR_A1	O	
K2	DDR_A0	O	
L3	DDR_BA0	O	Bank Address bit [0]
L1	DDR_BA1	O	Bank Address bit [1]
P3	DDR_CASn	O	Column Access Strobe
R2	DDR_CKE	O	Clock Enable
U9	DDR_CLK0	O	Primary Clock
V9	DDR_CLK0n	O	Primary Clock complement
R1	DDR_CSn	O	Chip Select

Table 6-33. DDR2 SDRAM Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
V5	DDR_DQ15	I/O	SDRAM Data bits [15:0]
T5	DDR_DQ14	I/O	
T8	DDR_DQ13	I/O	
U8	DDR_DQ12	I/O	
V8	DDR_DQ11	I/O	
U7	DDR_DQ10	I/O	
T6	DDR_DQ9	I/O	
U5	DDR_DQ8	I/O	
T2	DDR_DQ7	I/O	
T4	DDR_DQ6	I/O	
T1	DDR_DQ5	I/O	
U2	DDR_DQ4	I/O	
V4	DDR_DQ3	I/O	
U4	DDR_DQ2	I/O	
V2	DDR_DQ1	I/O	
U1	DDR_DQ0	I/O	
V7	DDR_DQM1	O	Data Mask for Byte Lane 1
V1	DDR_DQM0	O	Data Mask for Byte Lane 0
U6	DDR_DQS1	I/O	Data Strobe for for Byte Lane 1
U3	DDR_DQS0	I/O	Data Strobe for for Byte Lane 0
V6	DDR_DQS1n	I/O	Data Strobe Complement for Byte Lane 1
V3	DDR_DQS0n	I/O	Data Strobe Complement for Byte Lane 0
P2	DDR_RASn	O	Row Access Strobe
T7	DDR_VREF1	A	This pin should be set to ½ of VDD (0.9v) for DDR2
T3	DDR_VREF0	A	This pin should be set to ½ of VDD (0.9v) for DDR2
R3	DDR_WEn	O	Write Enable control

6.4.6 USB Signal Group

The USB signal group consists of eight signals to support a USB 2.0 High-speed interface, a Host or Device interface (Table 6-34). These signals are in the USB power domain.

Table 6-34. USB Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
F17	USB_ANA_TST	A	Connect this signal to GND. Test mode signal for the USB analog sections.
H18	USB_DM	A	USB D- signal
J18	USB_DP	A	USB D+ signal
G18	USB_VBUS	A	Separate 5.0V supply for USB
G17	USB_ID	A	This signal differentiates a Mini-A from a Mini-B plug. The ID Detector senses the ID line's state to indicate which type of plug is connected. The ID Detector can differentiate the following conditions: ID pin floating (>100KOhm) = The connected plug is a mini-B plug. ID pin shorted to ground (<10Ohms) = The connected plug is a mini-A plug.
H17	USB_REXT	A	External 3.4KOhm ±1% resistor connection that sets the bias current for the USB PHY
E18	USB_XIN	A	Crystal Oscillator XI pin. Connects a 12MHz oscillator
F18	USB_XO	A	Crystal Oscillator XO pin. Connects a 12MHz oscillator

6.4.7 UART Signal Group

Table 6-35 shows the Universal Asynchronous Receiver Transmitter (UART) signal group. These signals are in the HOST power domain.

Table 6-35. UART Signals

PIN	PRIMARY FUNCTION		ALT.	DESCRIPTION
	NAME	TYPE		
B11	UARTD_RXD	I	MME_RXD	Debug UART Received Data [1]
A11	UARTD_TXD	O	MME_TXD	Debug UART Transmitted Data

1.The Debug UART port is useful in debugging the system and should always be connected to the serial terminal.

The alternate functions MME_RXD and MME_TXD are selected using the DBGUARTSel bit in the Serial I/O Control register.

6.4.8 SPI/Bitstream Signal Group

Table 6-36 shows the Serial Peripheral Interface/Bitstream (BS) signal group. These signals are in the HOST power domain.

Table 6-36. Serial Peripheral Interface/Bitstream Interface Signals

PIN	PRIMARY FUNCTION		ALT. FUNCTION	DESCRIPTION
	NAME	TYPE		
A12	SPI_MCLK	I/O	BS_CLK[1]	SPI Master Clock Bitstream Clock
A14	SPI_MISO	I/O		SPI Master In/Slave Out
B13	SPI_MOSI	I/O	BS_DATA	SPI Master Out/Slave In Bitstream Data
B14	SPI_MSS0	I/O	BS_EN	SPI Master/Slave Select 0 Bitstream Data Enable
A13	SPI_MSS1	I/O	BS_REQ	SPI Master/Slave Select 1 Bitstream Data Request

1. The alternate function BS_CLK, BS_DATA, BS_EN, and BS_REQ are selected using bits in the Serial I/O Control register.

6.4.9 TWI Signal Group

Table 6-37 shows the I^2C compatible Two-wire Interface (TWI) signal group. These signals are in the HOST power domain.

Table 6-37. Two-Wire Interface Signals

PIN	PRIMARY FUNCTION		ALT. FUNCTION	DESCRIPTION
	NAME	TYPE		
B12	TWI0_SCL	IOD	TWI1_SCL[1]	TWI Serial Clock
C11	TWI0_SDA	IOD	TWI1_SDA	TWI Serial Data

1. The alternate functions TWI1_SCL and TWI1_SDA are selected using the TWI1Cfg bit in the Serial I/O Control register.

6.4.10 PWM Signal Group

Table 6-38 shows the Pulse Width Modulator (PWM) signal group. These signals are in the HOST power domain.

Table 6-38. Pulse Width Modulator Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
C9	PWM_0	O	Pulse Width Modulator interface

6.4.11 GPIO Signal Group

The GPIO signal group has four signals as shown in Table 6-39. They are dedicated General Purpose Input/Output (GPIO) signals. These dedicated GPIO signals are all in the HOST power domain.

The I/O pins in the GPIO signal group have programmable 15KOhm ±20% pull-up and pull-down resistors. The pull-up resistors are enabled by default and can be disabled using the associated bit in the GPIO 0 Pull-up Enable register. The pull-down resistors are disabled by default and can be enabled using the GPIO 0 Pull-down Enable register.

Table 6-39. GPIO Signals

PIN	PRIMARY FUNCTION		GPIO FUNCTION	DESCRIPTION
	NAME	TYPE		
A9	GPIO_0	I/O	GPIO_0_00	GPIO bit [0]
B9	GPIO_1	I/O	GPIO_0_01	GPIO bit [1]
A10	GPIO_2	I/O	GPIO_0_02	GPIO bit [2]
B10	GPIO_3	I/O	GPIO_0_03	GPIO bit [3]

There are 20 other GPIO signals that are multiplexed with other signals. These pins can be used as GPIO pins when their Primary or Alternate functions (ALT) are not used. These additional GPIO signals are broken into two groups as shown in Table 6-40 and Table 6-41. These signals are not necessarily in the HOST power domain. Refer to the primary signal name to check the power domain.

The multiplexed signals associated with GPIO_1 are disabled by default and enabled using the associated bits in the GPIO 1 Sel register. When enabled, the I/O function has priority over both the Primary and the Alternate function (ALT). The I/O pins in the GPIO_1 Signal Group have programmable 15KOhm ±20% pull-up and pull-down resistors. The pull-up resistors are enabled by default and can be disabled using the associated bit in the GPIO 1 Pull-up Enable register. The pull-down resistors are disabled by default and can be enabled using the GPIO 1 Pull-down Enable register.

Table 6-40. GPIO Signals

PIN	SIGNAL NAME		TYPE	ALTERNATE FUNCTION
	GPIO FUNCTION	PRIMARY FUNCTION		
C3	GPIO_1_00	HOST_INTn	IOD	–
L17	GPIO_1_19	VID0_FIELD	I	–
T16	GPIO_1_21	AUD0_SPDIF	O	–

The multiplexed signals associated with GPIO_2 are enabled using the associated bits in the GPIO 2 Sel register. GPIO_2 are enabled by default, which forces the signals to be an input after reset.

When enabled, the I/O function has priority over both the Primary and the Alternate function (ALT). The I/O pins in the GPIO_2 Signal Group have programmable 15KOhm ±20% pull-up and pull-down resistors. The pull-up resistors are enabled by default and can be disabled using the associated bit in the GPIO 2 Pull-up Enable register. The pull-down resistors are disabled by default and can be enabled using the GPIO 2 Pull-down Enable register.

Table 6-41. Additional GPIO Signals

PIN	SIGNAL NAME		TYPE	ALTERNATE FUNCTION
	GPIO FUNCTION	PRIMARY FUNCTION		
M16	GPIO_2_00	VID0_HSYNC	I	–
L16	GPIO_2_01	VID0_VSYNC	I	–
K17	GPIO_2_03	CFG		–
E16	GPIO_2_06	–	I/O	
C18	GPIO_2_07	–	I/O	
D16	GPIO_2_08	–	I/O	
A18	GPIO_2_09	VID2_FIELD	I/O	–
B15	GPIO_2_10	VID2_HSYNC	I/O	–
B16	GPIO_2_11	VID2_VSYNC	I/O	–
A14	GPIO_2_16	SPI_MISO	I/O	–
B14	GPIO_2_17	SPI_MSS0	I/O	BS_EN
A13	GPIO_2_18	SPI_MSS1	I/O	BS_REQ
A12	GPIO_2_19	SPI_MCLK	I/O	BS_CLK
B13	GPIO_2_20	SPI_MOSI	I/O	BS_DATA
B12	GPIO_2_21	TWI0_SCL	IOD	TWI1_SCL
C11	GPIO_2_22	TWI0_SDA	IOD	TWI1_SDA
C9	GPIO_2_29	PWM_0	O	–

6.4.12 JTAG Signal Group

The JTAG signal group has seven signals as shown in Table 6-42. These signals are in the AUD power domain.

Table 6-42. JTAG Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
R17	JTAG_TAP_SEL	I	This signal is used to select between the ARM tap controller and the test mode tap controller. 0: ARM debugger 1: Boundary scan
T17	TEST	I	When set to 1, the chip is placed in test mode
V17	JTAG_TCK	I	JTAG Test Clock
U17	JTAG_TDI	I	JTAG Test Data Input
U18	JTAG_TDO	O	JTAG Test Data Output
V18	JTAG_TMS	I	JTAG Test Mode Select
T18	JTAG_TRSTn	I	JTAG Test Reset Active Low

6.4.13 Configuration

The Configuration signal group has two signals as shown in Table 6-43. These signals are in the VID0 power domain. The configuration mode is determined during device boot-up. See “Boot Mode for the MMEs and the ARM” for more information.

Table 6-43. Configuration Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
K17	CFG	I	0: SPI EEPROM 1: XModem
K16	HOST_CFG_0	I	0: Parallel slave 1: Master

6.4.14 Clock

The Clock signal group has two signals as shown in Table 6-44. These signals are in the HOST power domain. See "Clock and PLL inputs" on page 52.

Table 6-44. Clock Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
F1	CLK_IN	I	Clock Input
F2	CLK_SEL	I	Selects the source clock for the PLLs to come from either the USB oscillator or CLK_IN. 0: USB Oscillator 1: External CLK_IN

6.4.15 Reset

The Reset signal group has one signal as shown in Table 6-45. This signal is in the AUD power domain.

Table 6-45. Reset Signals

PIN	PRIMARY FUNCTION		DESCRIPTION
	NAME	TYPE	
R16	RESETn	I	Active Low Chip Reset

6.4.16 Power and Ground Pins

Table 6-46. Power Pins

PIN	SIGNAL NAME	FUNCTION	VOLTAGE
T14	AUD_VDD	Power for Audio Circuitry	1.8, 2.5, 3.3V
U14	AUD_VDD		
V14	AUD_VDD		
E8	CORE_VDD	Power for Core Logic	1.05V
E9	CORE_VDD		
E10	CORE_VDD		
E11	CORE_VDD		
E12	CORE_VDD		
E13	CORE_VDD		
E14	CORE_VDD		
H5	CORE_VDD		
P9	CORE_VDD	Power for Core Logic	1.05V
P10	CORE_VDD		
P11	CORE_VDD		
P12	CORE_VDD		
P13	CORE_VDD		
P14	CORE_VDD		
T13	CORE_VDD		
U13	CORE_VDD		
V13	CORE_VDD		
C8	GND	Common Ground	–
C10	GND		
C12	GND		
G1	GND		
G2	GND		
G3	GND		
G5	GND		
G7	GND		
G8	GND		
G9	GND		

Table 6-46. Power Pins

PIN	SIGNAL NAME	FUNCTION	VOLTAGE
G10	GND	Common Ground	–
G11	GND		
G12	GND		
H7	GND		
H9	GND		
H10	GND		
H12	GND		
J7	GND		
J8	GND		
J9	GND		
J10	GND	Common Ground	–
J11	GND		
J12	GND		
J14	GND		
K7	GND		
K8	GND		
K9	GND		
K10	GND		
K11	GND		
K12	GND		
L7	GND	Common Ground	–
L9	GND		
L10	GND		
L12	GND		
M7	GND		
M8	GND		
M9	GND		
M10	GND		
M11	GND		
M12	GND		
T12	GND		
U12	GND		
V12	GND		

Table 6-46. Power Pins

PIN	SIGNAL NAME	FUNCTION	VOLTAGE
C6	HOST_VDD	Power for Host Processor	3.3V
E5	HOST_VDD		
E6	HOST_VDD		
E7	HOST_VDD		
F5	HOST_VDD		
F3	PLL_VDD	Power for Phase Lock Loop	1.05V
H1	DDR_VDD	Power for DDR Memory Controller	1.8V
H2	DDR_VDD		
H3	DDR_VDD		
J3	DDR_VDD		
J5	DDR_VDD		
K5	DDR_VDD		
L5	DDR_VDD		
M5	DDR_VDD		
N5	DDR_VDD		
P5	DDR_VDD		
P6	DDR_VDD		
P7	DDR_VDD		
P8	DDR_VDD		1.8V
T9	DDR_VDD		
T10	DDR_VDD		
T11	DDR_VDD		
U11	DDR_VDD		
V11	DDR_VDD		
F14	USB_DVDD	Digital power for USB port	1.05V
H14	USB_AVDD	Power for USB port	3.3V
H16	USB_AVDD		
J16	USB_AVDD		
J17	USB_AVDD		
K18	USB_AVDD		
D18	USB_GND	Ground for USB port	–
E17	USB_GND		
F16	USB_GND		
G14	USB_GND		
G16	USB_GND		

Table 6-46. Power Pins

PIN	SIGNAL NAME	FUNCTION	VOLTAGE
K14	VID01_VDD	Power for Video port 0	1.8, 2.5, 3.3V
L14	VID01_VDD		
M14	VID01_VDD		
N14	VID01_VDD		
C13	VID23_VDD	Power for Video port 2	1.8, 2.5, 3.3V
C14	VID23_VDD		

6.5 Pin List by Power Group

Table 6-47 shows the signals associated with each of the power domains.

Table 6-47. Signal Group Names

INTERFACE	POWER DOMAIN	VOLTAGE	SIGNALS
Host	HOST	3.3V	HOST_A[6:1], HOST_D[15:0], HOST_CS0n, HOST_DMARQ, HOST_INTn, HOST_REn, HOST_WAITn, HOST_WEn
UART			UARTD_RXD, UARTD_TXD
SPI/Bitstream			SPI_MCLK, SPI_MISO, SPI_MOSI, SPI_MSS0, SPI_MSS1
TWI			TWI0_SCL, TWI0_SDA
PWM			PWM_0
GPIO			GPIO_[0:3][1] GPIO_1_00 GPIO_2_16, GPIO_2_17, GPIO_2_18, GPIO_2_19, GPIO_2_20, GPIO_2_21, GPIO_2_22, GPIO_2_29
CLK			CLK_IN, CLK_SEL
Audio	AUD	1.8, 2.5, 3.3V	AUD0_BCK, AUD0_IDAT, AUD0_LRCK, AUD0_MCLK, AUD0_ODAT0, AUD0_SPDIF
Reset			RESETn
GPIO			GPIO_1_21
JTAG		3.3V	JTAG_TAP_SEL, TEST, JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS, JTAG_TRSTn
Core	CORE	1.05V	No core signals are brought out directly to the I/O pins.
DDR	DDR	1.8V	DDR_PADHI, DDR_PADLO, DDR_A[12:0], DDR_BA[1:0], DDR_CASn, DDR_CKE, DDR_CLK0, DDR_CLK0n, DDR_CSn, DDR_DQ[15:0], DDR_DQM[1:0], DDR_DQS[1:0], DDR_DQSn[1:0], DDR_RASn, DDR_VREF1, DDR_VREF0, DDR_WEn
USB	USB	3.3V	USB_ANA_TST, USB_DM, USB_DP, USB_ID, USB_REXT, USB_XIN, USB_XO
		5.0V	USB_VBUS

Table 6-47. Signal Group Names

INTERFACE	POWER DOMAIN	VOLTAGE	SIGNALS
Video	VID0	1.8, 2.5, 3.3V	VID0_D[7:0], VID0_FIELD, VID0_HSYNC, VID0_OUTCLK, VID0_PIXCLK, VID0_VSYNC
Configuration CFG			CFG, HOST_CFG_0
GPIO			GPIO_1_19, GPIO_2_00, GPIO_2_01, GPIO_2_03
Video	VID2	1.8, 2.5, 3.3V	VID2_D[7:0], VID2_FIELD, VID2_HSYNC, VID2_PIXCLK, VID2_VSYNC
GPIO			GPIO_2_09, GPIO_2_10, GPIO_2_11, GPIO_2_06, GPIO_2_07, GPIO_2_08

1. Only GPIO_0_[3:0] are dedicated GPIOs; all other GPIO signals are multiplexed with other signals listed in Table 6-47. For example, the primary function of GPIO_1_00 is a “host interrupt.” See Table 6-40 and Table 6-41 for a detailed description.

6.5.1 Hookup Recommendations when Interfaces are Unused

Table 6-48 shows the hookup recommendations when some of the interfaces are unused. The pull-up/pull-down column indicates:

- UP: The pin has the internal pull-up enabled at power-on/reset.
- DOWN: The pin has the internal pull-down enabled at power-on/reset.
- DIS: The pin has pull-up/pull-down control, but they are disabled at power-on/reset.
- NONE: The pin has no control over pull-up/pull-down.

The Default column indicates the state of the pin at reset:

- 0: The pin is driven to 0.
- 1: The pin is driven to 1.
- 0(p): The pin is pulled by a resistor to a value of 0.
- 1(p): The pin is pulled by resistor to a value of 1.
- Hi-Z: The pin is not driven.
- —: The pin is an Input Only and must be driven.
- NC: The pin is a no connect (leave it unconnected).

Note: Memory (DDR2 SDRAM) and power pins are not included in this list, since they must always be connected for the device to operate correctly. This also applies when the USB block is not used on the MAX64180.

Internal pull-up and pull-down values are 15KOhm ± 20%.

Table 6-48. Hookup Recommendations when Interfaces are Unused

PIN NAME	DIR	PAD	TYPE	PULL-UP/ PULL-DOWN	DEFAULT	RECOMMENDATION IF THE INTERFACE IS NOT USED
VIDEO_PORT 0						
VID0_D7	I	I	input_only	NONE	—	GND
VID0_D6	I	I	input_only	NONE	—	GND
VID0_D5	I	I	input_only	NONE	—	GND
VID0_D4	I	I	input_only	NONE	—	GND
VID0_D3	I	I	input_only	NONE	—	GND
VID0_D2	I	I	input_only	NONE	—	GND
VID0_D1	I	I	input_only	NONE	—	GND
VID0_D0	I	I	input_only	NONE	—	GND
VID0_FIELD	I	IO	GPIO	UP	1(p)	NC, pulled up by default
VID0_HSYNC	I	IO	GPIO	UP	1(p)	NC, pulled up by default
VID0_OUTCLK	O	O	output_only	NONE	Hi–Z	NC
VID0_PIXCLK	IO	IO		NONE	Hi–Z	GND
VID0_VSYNC	I	IO	GPIO	UP	1(p)	NC, pulled up by default
VID2_D7	IO	IO		NONE	Hi–Z	NC, configure as output after reset
VID2_D6	IO	IO		NONE	Hi–Z	NC, configure as output after reset
VID2_D5	IO	IO		NONE	Hi–Z	NC, configure as output after reset
VID2_D4	IO	IO		NONE	Hi–Z	NC, configure as output after reset
VID2_D3	IO	IO		NONE	Hi–Z	NC, configure as output after reset
VID2_D2	IO	IO		NONE	Hi–Z	NC, configure as output after reset
VID2_D1	IO	IO		NONE	Hi–Z	NC, Configure as output after reset
VID2_D0	IO	IO		NONE	Hi–Z	NC, configure as output after reset
VID2_FIELD	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
VID2_HSYNC	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
VID2_PIXCLK	IO	IO		NONE	Hi–Z	NC, Configure as output after reset
VID2_VSYNC	IO	IO	GPIO	UP	1(p)	NC, pulled up by default

Table 6-48. Hookup Recommendations when Interfaces are Unused

PIN NAME	DIR	PAD	TYPE	PULL-UP/ PULL-DOWN	DEFAULT	RECOMMENDATION IF THE INTERFACE IS NOT USED
USB[1]						
USB_ANA_TST	A	IO				NC
USB_DM	A	IO				NC
USB_DP	A	IO				NC
USB_VBUS	A	IO				NC
USB_ID	A	IO				NC
USB_REXT	A	IO				USB_AVDD
USB_XIN	A	IO				NC
USB_XO	A	IO				NC
AUDIO						
AUD0_BCK	IO	IO		NONE	Hi–Z	NC, configure as output after reset
AUD0_IDAT	I	I	GPIO (input_only)	NONE	Hi–Z	GND
AUD0_LRCK	IO	IO		NONE	Hi–Z	NC, configure as output after reset
AUD0_MCLK	IO	IO		NONE	Hi–Z	NC, configure as output after reset
AUD0_ODAT0	O	O	output_only	NONE	0	NC
AUD0_SPDIF	O	IO	GPIO	UP	0	NC
PWM						
PWM_0	O	IO	GPIO	UP	1	NC
GPIO						
GPIO_0	IO	IO	GPIO	UP	1(p)	NC
GPIO_1	IO	IO	GPIO	UP	1(p)	NC
GPIO_2	IO	IO	GPIO	UP	1(p)	NC
GPIO_3	IO	IO	GPIO	UP	1(p)	NC
TWI						
TWI0_SCL	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
TWI0_SDA	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
SPI						
SPI_MCLK	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
SPI_MISO	IO	IO	GPIO	UP	1(p)	NC, pulled up by default

Table 6-48. Hookup Recommendations when Interfaces are Unused

PIN NAME	DIR	PAD	TYPE	PULL-UP/ PULL-DOWN	DEFAULT	RECOMMENDATION IF THE INTERFACE IS NOT USED
SPI_MOSI	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
SPI_MSS0	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
SPI_MSS1	IO	IO	GPIO	UP	1(p)	NC, pulled up by default
UART						
UARTD_RXD	I	I	input_only	NONE	—	Hook up to DBG_TXD
UARTD_TXD	O	O	output_only	NONE	1	Hook up to DBG_RXD
HOST						
HOST_A6	O	IO		NONE	Hi–Z	GND
HOST_A5	O	IO		NONE	Hi–Z	GND
HOST_A4	O	IO		NONE	Hi–Z	GND
HOST_A3	O	IO		NONE	Hi–Z	GND
HOST_A2	O	IO		NONE	Hi–Z	GND
HOST_A1	O	IO		NONE	Hi–Z	GND
HOST_CS0n	O	IO		NONE	1	NC
HOST_D15	IO	IO		NONE	Hi–Z	GND
HOST_D14	IO	IO		NONE	Hi–Z	GND
HOST_D13	IO	IO		NONE	Hi–Z	GND
HOST_D12	IO	IO		NONE	Hi–Z	GND
HOST_D11	IO	IO		NONE	Hi–Z	GND
HOST_D10	IO	IO		NONE	Hi–Z	GND
HOST_D9	IO	IO		NONE	Hi–Z	GND
HOST_D8	IO	IO		NONE	Hi–Z	GND
HOST_D7	IO	IO		NONE	Hi–Z	GND
HOST_D6	IO	IO		NONE	Hi–Z	GND
HOST_D5	IO	IO		NONE	Hi–Z	GND
HOST_D4	IO	IO		NONE	Hi–Z	GND
HOST_D3	IO	IO		NONE	Hi–Z	GND
HOST_D2	IO	IO		NONE	Hi–Z	GND
HOST_D1	IO	IO		NONE	Hi–Z	GND
HOST_D0	IO	IO		NONE	Hi–Z	GND
HOST_DMARQ	I	IO		NONE	0	GND

Table 6-48. Hookup Recommendations when Interfaces are Unused

PIN NAME	DIR	PAD	TYPE	PULL-UP/ PULL-DOWN	DEFAULT	RECOMMENDATION IF THE INTERFACE IS NOT USED
HOST_INTn	I	IO		UP	1(p)	GND
HOST_REn	O	IO		NONE	1	NC
HOST_WAITn	I	IO		NONE	Hi–Z	GND
HOST_WEn	O	IO		NONE	1	NC
HOST_CFG_0	I	I	input_only	NONE	0	GND
CFG	I	IO	GPIO	UP	1(p)	NC, pulled up by default
JTAG						
JTAG_TAP_SEL	I	I	input_only	NONE	1	GND
TEST	I	I	input_only	NONE	0	GND
JTAG_TCK	I	I	input_only	UP	1(p)	GND
JTAG_TDI	I	I	input_only	UP	1(p)	Hook up to TEST_TDO
JTAG_TDO	O	O	output-only	UP	1(p)	Hook up to TEST_TDI
JTAG_TMS	I	I	input_only	UP	1(p)	GND
JTAG_TRSTn	I	I	input_only	UP	1(p)	GND
CLOCK						
CLK_IN	I	I	input_only			GND

1. When the USB block is not used, in addition to connecting the USB pins as recommended in Table 6-48, the USB VDD pins still must be connected to their standard supply levels, as shown below:
   - USB_DVDD 1.05 V
   - USB_AVDD 3.3 V
   - USB_ACVDD 3.3 V

7 Package Information

The MAX64180 is available in a lead(Pb)-free package. The MAX64180 is a 248-pin, Chip Scale Thin Ball Grid Array (CTBGA) package with a 10mm ×10mm footprint and 0.5mm pin pitch.

Lead(Pb)-free products from Maxim comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020.

This section provides the package outline for the MAX64180 device.

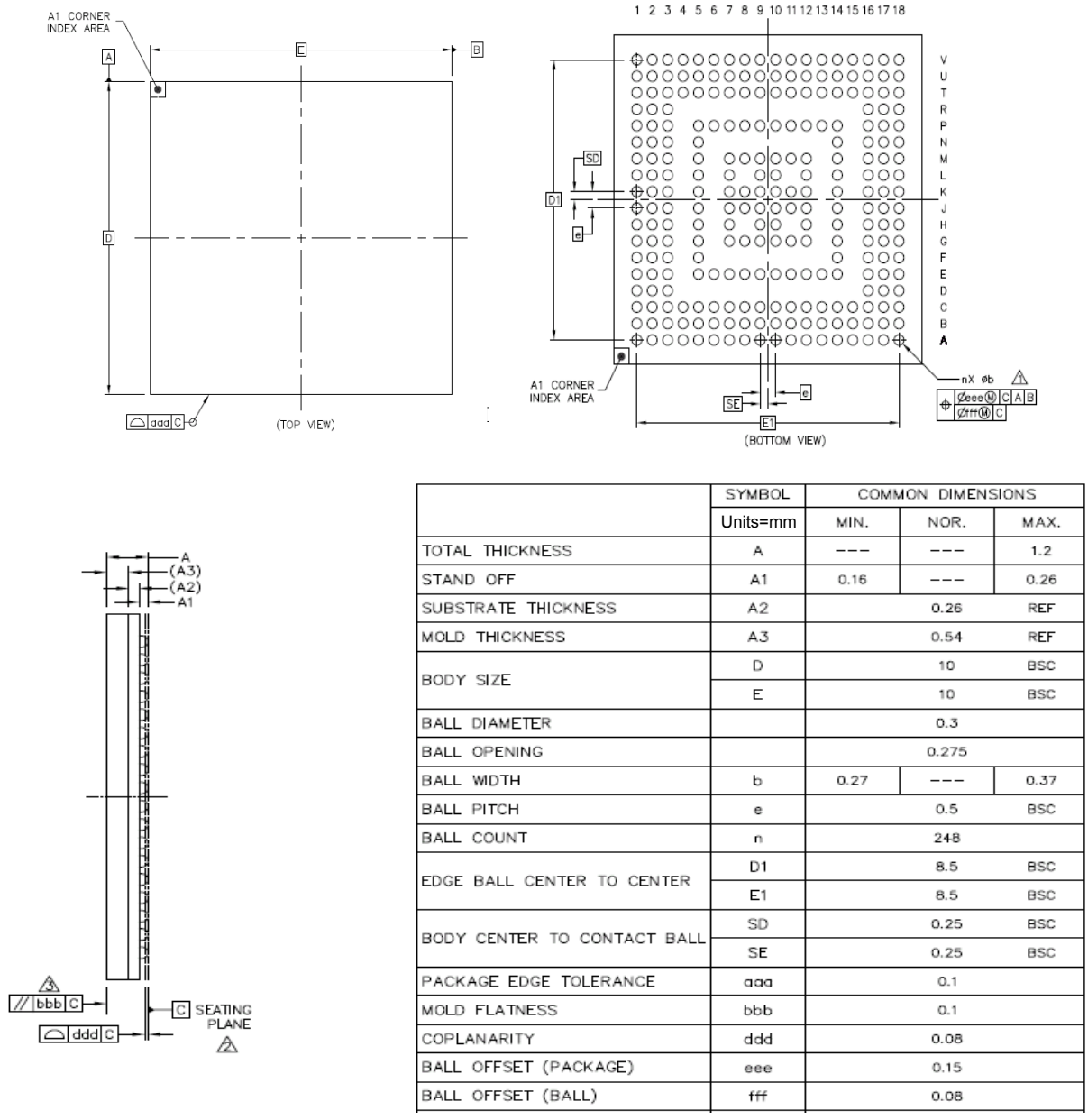
For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
CTBGA	X24800+1	90-0352, 21-0503

7.1 Package Outline—248-Pin CTBGA, 10mm × 10mm

Figure 7-41 illustrates the package outline for the MAX64180 device. The outline contains the top view, bottom view, and side view.

7.2 Package Diagram



	SYMBOL	COMMON DIMENSIONS		
	Units=mm	MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.2
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.5	BSC
BALL COUNT	n		248	
EDGE BALL CENTER TO CENTER	D1		8.5	BSC
	E1		8.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.25	BSC
	SE		0.25	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Figure 7-41. MAX64180 248-Pin CTBGA Package Physical Drawing

7.3 Thermal Data

Table 7-49 shows the case thermal conductivity data for the MAX64180 248-pin CTBGA package using JESD51-7 standard.

Table 7-49. Case Thermal Conductivity Data

SYMBOL	PARAMETER	VALUE
ΘJA	Junction to Ambient	20.7°C/Watt
ψJT	Junction to Case	4.2°C/Watt
T_{Jmax}	Maximum Junction Temperature	125°C
T_{Amax}	Maximum Ambient Temperature	70°C
T_{Amin}	Minimum Ambient Temperature	0°C

7.3.1 Thermal Resistance

The thermal resistance of any device is dependent on the board size. Figure 7-42 shows how the thermal resistance of MAX64180 varies from the standard JEDEC board size to small boards used in camera applications. It is recommended that for small form factor boards, connect the device and the board to the system chassis to dissipate the heat of the device and the board.

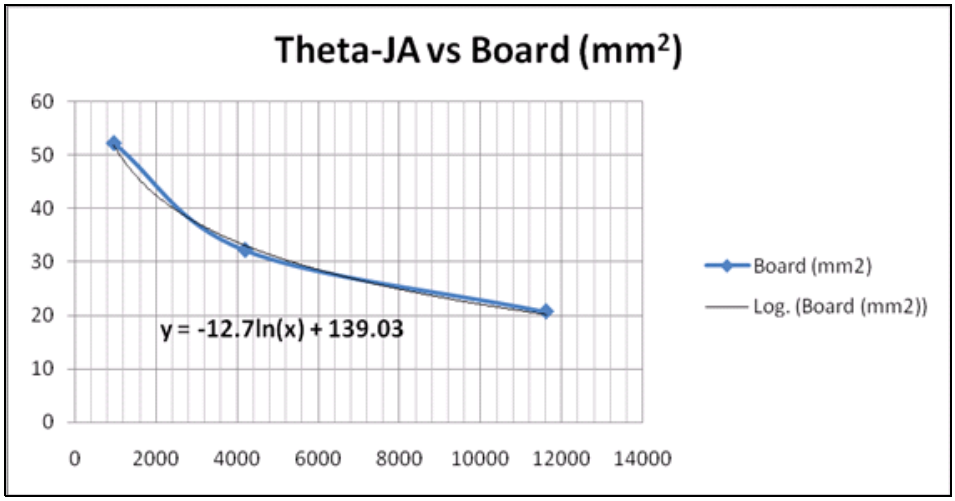


Figure 7-42. Thermal Resistance

NOTE: Contact your local Maxim representative for more details.

7.4 Marking

1. Product Name: MAX64180CXO+
2. Date and Revision: YY-year, WW-week, XX-chip revision of die which is A1
3. Lot Number: NNN-number, LL-letter
4. Manufactured at: Taiwan

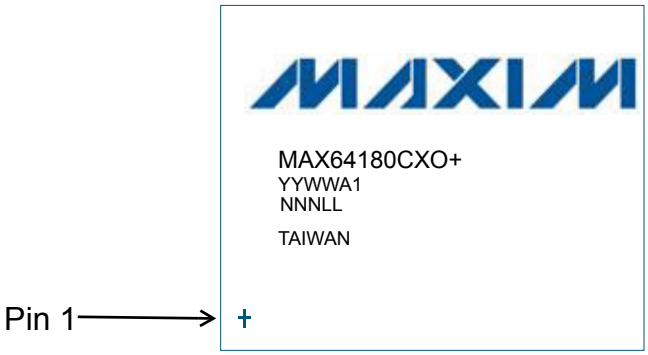


Figure 7-43. MAX64180 Marking

8 Ordering Information

Table 8-50 describes the ordering information for the MAX64180 device.

Table 8-50. Ordering Information

PART ORDER NUMBER	DESCRIPTION
MAX64180CXO+	Lead(Pb)-free, 248-pin, CTBGA package with a 10mm × 10mm footprint, 0.5mm ball spacing