

## Silicon Carbide Junction Transistor/Schottky Diode Co-pack

$V_{DS}$	=	1200 V
$R_{DS(ON)}$	=	25 m $\Omega$
$I_D$ ( $T_C = 25^\circ\text{C}$ )	=	100 A
$h_{FE}$ ( $T_C = 25^\circ\text{C}$ )		100

### Features

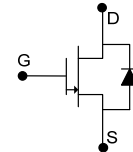
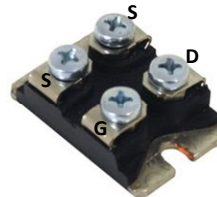
- 175°C Maximum Operating Temperature
- Gate Oxide free SiC switch
- Exceptional Safe Operating Area
- Integrated SiC Schottky Rectifier
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low output capacitance
- Positive temperature co-efficient of  $R_{DS,ON}$
- Suitable for connecting an anti-parallel diode

### Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20  $\mu\text{s}$  Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal distortion
- High Amplifier Bandwidth
- Reduced cooling requirements
- Reduced system size

### Package

- RoHS Compliant



SOT-227

### Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

### Maximum Ratings at $T_J = 175^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values	Unit
<b>SiC Junction Transistor</b>				
Drain – Source Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$	1200	V
Continuous Drain Current	$I_D$	$T_{C,MAX} = 95^\circ\text{C}$	50	A
Gate Peak Current	$I_{GM}$		10	A
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 175^\circ\text{C}$ , $I_G = 1\text{ A}$ , Clamped Inductive Load	$I_{D,max} = 50$ @ $V_{DS} \leq V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 175^\circ\text{C}$ , $I_G = 1\text{ A}$ , $V_{DS} = 800\text{ V}$ , Non Repetitive	20	$\mu\text{s}$
Reverse Gate – Source Voltage	$V_{SG}$		30	V
Reverse Drain – Source Voltage	$V_{SD}$		25	V
Power Dissipation	$P_{tot}$	$T_C = 95^\circ\text{C}$	67	W
Storage Temperature	$T_{stg}$		-55 to 175	$^\circ\text{C}$
<b>Free-wheeling Silicon Carbide diode</b>				
DC-Forward Current	$I_F$	$T_C \leq 150^\circ\text{C}$	50	A
Non Repetitive Peak Forward Current	$I_{FM}$	$T_C = 25^\circ\text{C}$ , $t_p = 10\ \mu\text{s}$	1625	A
Surge Non Repetitive Forward Current	$I_{F,SM}$	$t_p = 10\text{ ms}$ , half sine, $T_C = 25^\circ\text{C}$	350	A

### Thermal Characteristics

Thermal resistance, junction - case	$R_{thJC}$	SiC Junction Transistor	1.19	$^\circ\text{C/W}$
Thermal resistance, junction - case	$R_{thJC}$	SiC Diode	1.19	$^\circ\text{C/W}$

### Mechanical Properties

		Values		
		min.	typ.	max.
Mounting Torque	$M_d$		1.5	Nm
Terminal Connection Torque		1.3		Nm
Weight			29	g
Case Color		Black		
Dimensions		38 x 25.4 x 12 mm		

**Electrical Characteristics at  $T_j = 175\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Values			Unit	
			min.	typ.	max.		
<b>SJT On-State Characteristics</b>							
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 50\text{ A}, I_G = 1000\text{ mA}, T_j = 25\text{ }^\circ\text{C}$		25		m $\Omega$	
		$I_D = 50\text{ A}, I_G = 2000\text{ mA}, T_j = 125\text{ }^\circ\text{C}$		30			
		$I_D = 50\text{ A}, I_G = 4000\text{ mA}, T_j = 175\text{ }^\circ\text{C}$		44			
Gate Forward Voltage	$V_{GS(FWD)}$	$I_G = 500\text{ mA}, T_j = 25\text{ }^\circ\text{C}$		3.3		V	
		$I_G = 500\text{ mA}, T_j = 175\text{ }^\circ\text{C}$		3.1			
DC Current Gain	$h_{FE}$	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}, T_j = 25\text{ }^\circ\text{C}$		100			
		$V_{DS} = 5\text{ V}, I_D = 50\text{ A}, T_j = 175\text{ }^\circ\text{C}$		TBD			
<b>SJT Off-State Characteristics</b>							
Drain Leakage Current	$I_{DSS}$	$V_R = 1200\text{ V}, V_{GS} = 0\text{ V}, T_j = 25\text{ }^\circ\text{C}$		18		$\mu\text{A}$	
		$V_R = 1200\text{ V}, V_{GS} = 0\text{ V}, T_j = 125\text{ }^\circ\text{C}$		26			
		$V_R = 1200\text{ V}, V_{GS} = 0\text{ V}, T_j = 175\text{ }^\circ\text{C}$		35			
Gate Leakage Current	$I_{SG}$	$V_{SG} = 20\text{ V}, T_j = 25\text{ }^\circ\text{C}$		20		nA	
<b>SJT Capacitance Characteristics</b>							
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_D = 1\text{ V}, f = 1\text{ MHz}$		tbd		pF	
Reverse Transfer/Output Capacitance	$C_{rss}/C_{oss}$	$V_D = 1\text{ V}, f = 1\text{ MHz}$		tbd		pF	
<b>SJT Switching Characteristics</b>							
Turn On Delay Time	$t_{d(on)}$	$V_{DD} = 800\text{ V}, I_D = 50\text{ A},$ $R_{G(on)} = R_{G(off)} = \text{tbd } \Omega,$ $\text{FWD} = \text{GB50SLT12},$ $T_j = 25\text{ }^\circ\text{C}$ Refer to Figure 15 for gate current waveform		tbd		ns	
Rise Time	$t_r$			tbd		ns	
Turn Off Delay Time	$t_{d(off)}$			tbd		ns	
Fall Time	$t_f$			tbd		ns	
Turn-On Energy Per Pulse	$E_{on}$			tbd		$\mu\text{J}$	
Turn-Off Energy Per Pulse	$E_{off}$			tbd		$\mu\text{J}$	
Total Switching Energy	$E_{ts}$			tbd		$\mu\text{J}$	
Turn On Delay Time	$t_{d(on)}$		$V_{DD} = 800\text{ V}, I_D = 50\text{ A},$ $R_{G(on)} = R_{G(off)} = \text{tbd } \Omega,$ $\text{FWD} = \text{GB50SLT12},$ $T_j = 175\text{ }^\circ\text{C}$ Refer to Figure 15 for gate current waveform		tbd		ns
Rise Time	$t_r$				tbd		ns
Turn Off Delay Time	$t_{d(off)}$				tbd		ns
Fall Time	$t_f$			tbd		ns	
Turn-On Energy Per Pulse	$E_{on}$			tbd		$\mu\text{J}$	
Turn-Off Energy Per Pulse	$E_{off}$			tbd		$\mu\text{J}$	
Total Switching Energy	$E_{ts}$			tbd		$\mu\text{J}$	
<b>Free-wheeling Silicon Carbide Schottky Diode</b>							
Forward Voltage	$V_F$	$I_F = 50\text{ A}, V_{GE} = 0\text{ V},$ $T_j = 25\text{ }^\circ\text{C} (175\text{ }^\circ\text{C})$		1.5		V	
Diode Knee Voltage	$V_{D(knee)}$	$T_j = 25\text{ }^\circ\text{C}, I_F = 1\text{ mA}$		0.8		V	
Peak Reverse Recovery Current	$I_{rrm}$	$I_F = 50\text{ A}, V_{GE} = 0\text{ V}, V_R = 800\text{ V},$ $-di_f/dt = 625\text{ A}/\mu\text{s}, T_j = 175\text{ }^\circ\text{C}$		tbd		A	
Reverse Recovery Time	$t_{rr}$			tbd		ns	
Rise Time	$t_r$	$V_{DD} = 800\text{ V}, I_D = 50\text{ A},$ $R_{gon} = R_{goff} = \text{tbd } \Omega,$ $T_j = 25\text{ }^\circ\text{C}$		tbd		ns	
Fall Time	$t_f$			tbd		ns	
Turn-On Energy Loss Per Pulse	$E_{on}$			tbd		$\mu\text{J}$	
Turn-Off Energy Loss Per Pulse	$E_{off}$			tbd		$\mu\text{J}$	
Reverse Recovery Charge	$Q_{rr}$	$V_{DD} = 800\text{ V}, I_D = 50\text{ A},$ $R_{gon} = R_{goff} = \text{tbd } \Omega,$ $T_j = 175\text{ }^\circ\text{C}$		tbd		nC	
Rise Time	$t_r$			tbd		ns	
Fall Time	$t_f$			tbd		ns	
Turn-On Energy Loss Per Pulse	$E_{on}$			tbd		$\mu\text{J}$	
Turn-Off Energy Loss Per Pulse	$E_{off}$			tbd		$\mu\text{J}$	
Reverse Recovery Charge	$Q_{rr}$		tbd		nC		

**Figures**

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TBD

**Figure 1: Typical Output Characteristics at 25 °C**

TBD

**Figure 2: Typical Output Characteristics at 125 °C**

TBD

**Figure 3: Typical Output Characteristics at 175 °C**

TBD

**Figure 4: Typical Gate Source I-V Characteristics vs. Temperature**

TBD

**Figure 5: Normalized On-Resistance and Current Gain vs. Temperature**

TBD

**Figure 6: Typical Blocking Characteristics**

TBD

Figure 7: Capacitance Characteristics

TBD

Figure 8: Capacitance Characteristics

TBD

Figure 9: Typical Hard-switched Turn On Waveforms

TBD

Figure 10: Typical Hard-switched Turn Off Waveforms

TBD

Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

TBD

Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

TBD

Figure 13: Typical Turn On Energy Losses vs. Drain Current

TBD

Figure 14: Typical Turn Off Energy Losses vs. Drain Current

TBD

Figure 15: Typical Gate Current Waveform

TBD

Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency<sup>1</sup>

TBD

Figure 17: Power Derating Curve

TBD

Figure 18: Forward Bias Safe Operating Area

<sup>1</sup> – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

TBD

TBD

Figure 19: Turn-Off Safe Operating Area

Figure 20: Transient Thermal Impedance

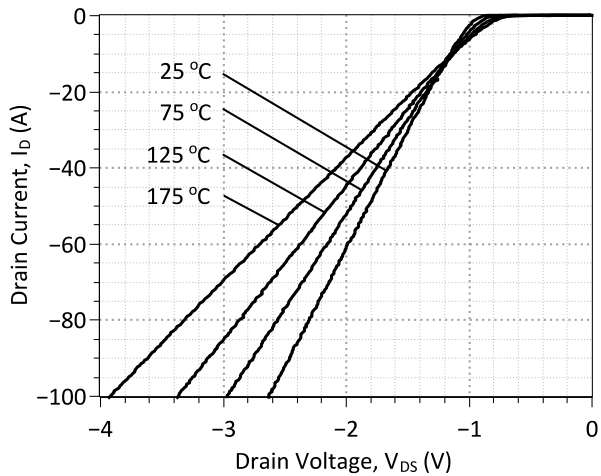
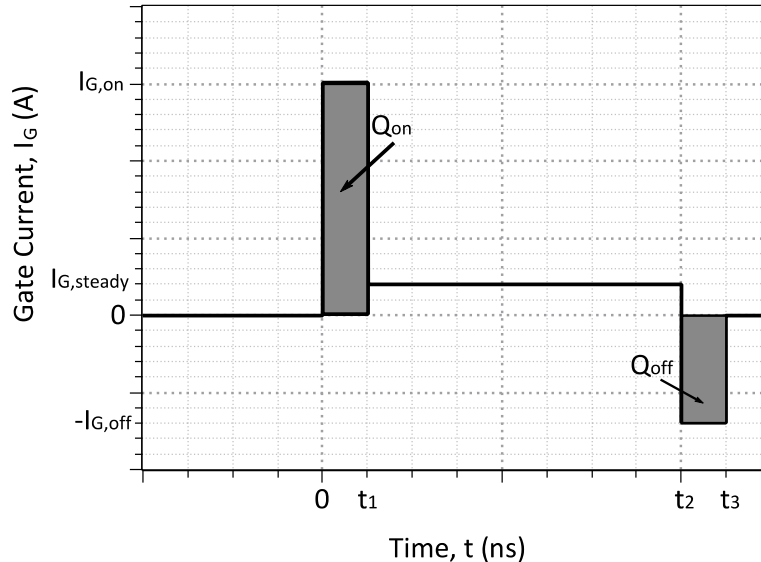


Figure 21: Typical FWD Forward Characteristics

## Gate Drive Theory of Operation for the GA50SICP12-227

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 22.



**Figure 22: Idealized Gate Current Waveform**

### Gate Currents, $I_{G,pk}/-I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge,  $Q_G$ , for turn-on is supplied by a burst of high gate current,  $I_{G,on}$ , until the gate-source capacitance,  $C_{GS}$ , and gate-drain capacitance,  $C_{GD}$ , are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

The  $I_{G,on}$  pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the  $I_{G,on}$  pulse is affected by the parasitic inductances,  $L_{par}$  in the module and drive circuit. A voltage developed across the parasitic inductance in the source path,  $L_s$ , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the  $V_{GS,ON}$  level to counter these effects.

A high negative peak current,  $-I_{G,off}$  is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with  $V_{GS} = 0$  V, a negative gate voltage  $V_{GS}$  may be used in order to speed up the turn-off transition.

### Steady On-State

After the device is turned on,  $I_G$  may be advantageously lowered to  $I_{G,steady}$  for reducing unnecessary gate drive losses. The  $I_{G,steady}$  is determined by noting the DC current gain,  $h_{FE}$ , of the device

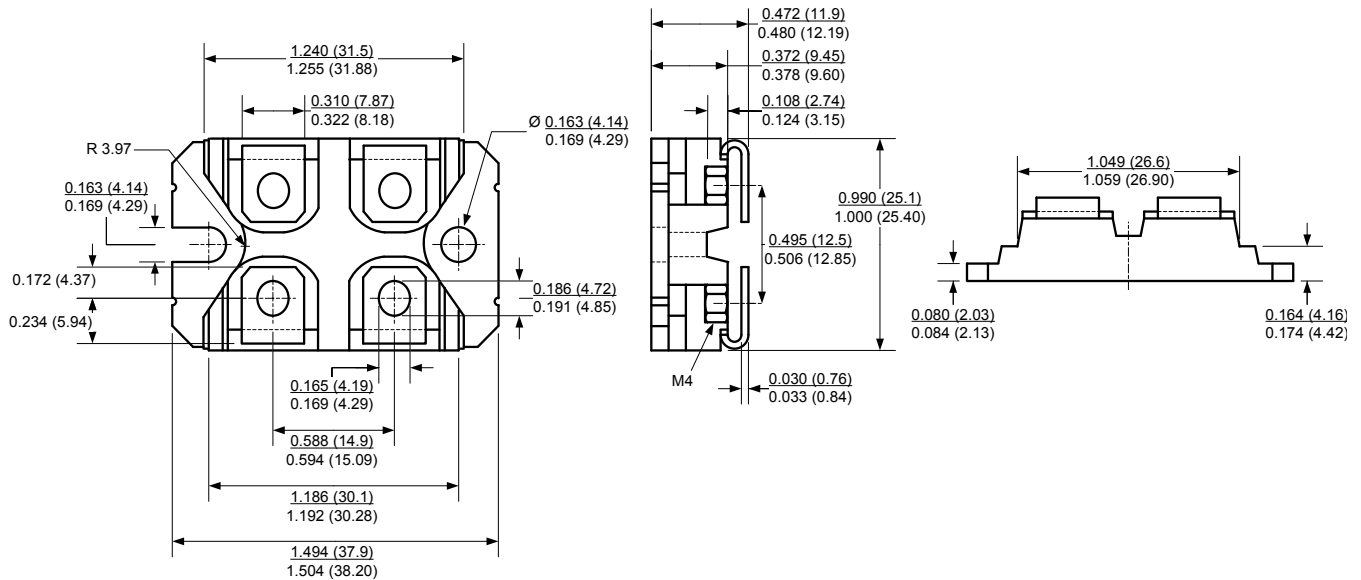
The desired  $I_{G,steady}$  is determined by the peak device junction temperature  $T_J$  during operation, drain current  $I_D$ , DC current gain  $h_{FE}$ , and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Package Dimensions:

SOT-227

PACKAGE OUTLINE



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2014/08/25	1	Gate Drive Theory Update	
2013/09/12	0	Initial release	

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 43670 Trade Center Place Suite 155  
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**SPICE Model Parameters**

This is a secure document. Please copy this code from the SPICE model PDF file on our website ([http://www.genesicsemi.com/images/products\\_sic/igbt\\_copack/GA50SICP12-227\\_spice.pdf](http://www.genesicsemi.com/images/products_sic/igbt_copack/GA50SICP12-227_spice.pdf)) into LTSPICE (version 4) software for simulation of the GA50SICP12-227.

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*      MODEL OF GeneSiC Semiconductor Inc.
*      $Revision: 1.1          $
*      $Date:      23-JUN-2014    $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*      http://www.genesicsemi.com/index.php/sic-products/copack
*
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*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
* Start of GA50SICP12-227 SPICE Model
*
.SUBCKT GA50SIPC12 DRAIN GATE SOURCE
Q1 DRAIN GATE SOURCE GA50SIPC12_Q
D1 SOURCE DRAIN GA50SIPC12_D1
D2 SOURCE DRAIN GA50SIPC12_D2
*
.model GA50SIPC12_Q NPN
+ IS      5.00E-47          ISE      1.26E-28          EG      3.2
+ BF      100              BR       0.55              IKF     3500
+ NF      1                NE       2                RB      0.9
+ RE      0.01             RC       0.011             CJC     1.75E-09
+ VJC     3                MJC     0.5              CJE     5.57E-09
+ VJE     3                MJE     0.5              XTI     3
+ XTB     -1.2             TRC1    7.00E-03          MFG     GeneSiC_Semi
.MODEL GA50SIPC12_D1 D
+ IS      1.99E-16          RS      0.015652965      N       1
+ IKF     1000              EG      1.2                XTI     3
+ TRS1    0.0042            TRS2    1.3E-05          CJO     3.86E-09
+ VJ      1.362328465      M       0.48198551      FC      0.5
+ TT      1.00E-10          IAVE    50
.MODEL GA50SIPC12_D2 D
+ IS      1.54E-19          RS      0.1              N       3.941
+ EG      3.23              TRS1    -0.004             IKF     19
+ XTI     0                FC      0.5              TT      0
.ENDS
* End of GA50SICP12-227 SPICE Model

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