User’s Guide

ATM12864D

Liquid Crystal Display Module

Contents

CHAPTER 1

Introduction to ATM12864D LCM

VT12864D is a dot matrix graphic LCD module which is fabricated by low power COMS technology. It can display 128*64 dots size LCD panel using a 128*64 bit-mapped Display Data RAM (DDRAM). It interfaces with an 8-bit microprocessor.

Features

- Display format: 128*64 dots matrix graphic
- STN yellow-green mode
- Easy interface with 8-bit MPU
- Low power consumption
- LED back-light
- Viewing angle: 6 O'clock
- Driving method : 1/64 duty , 1/9 bias
- LCD driver IC: KS0108B(2 个)、KS0107B
- Connector: Zebra

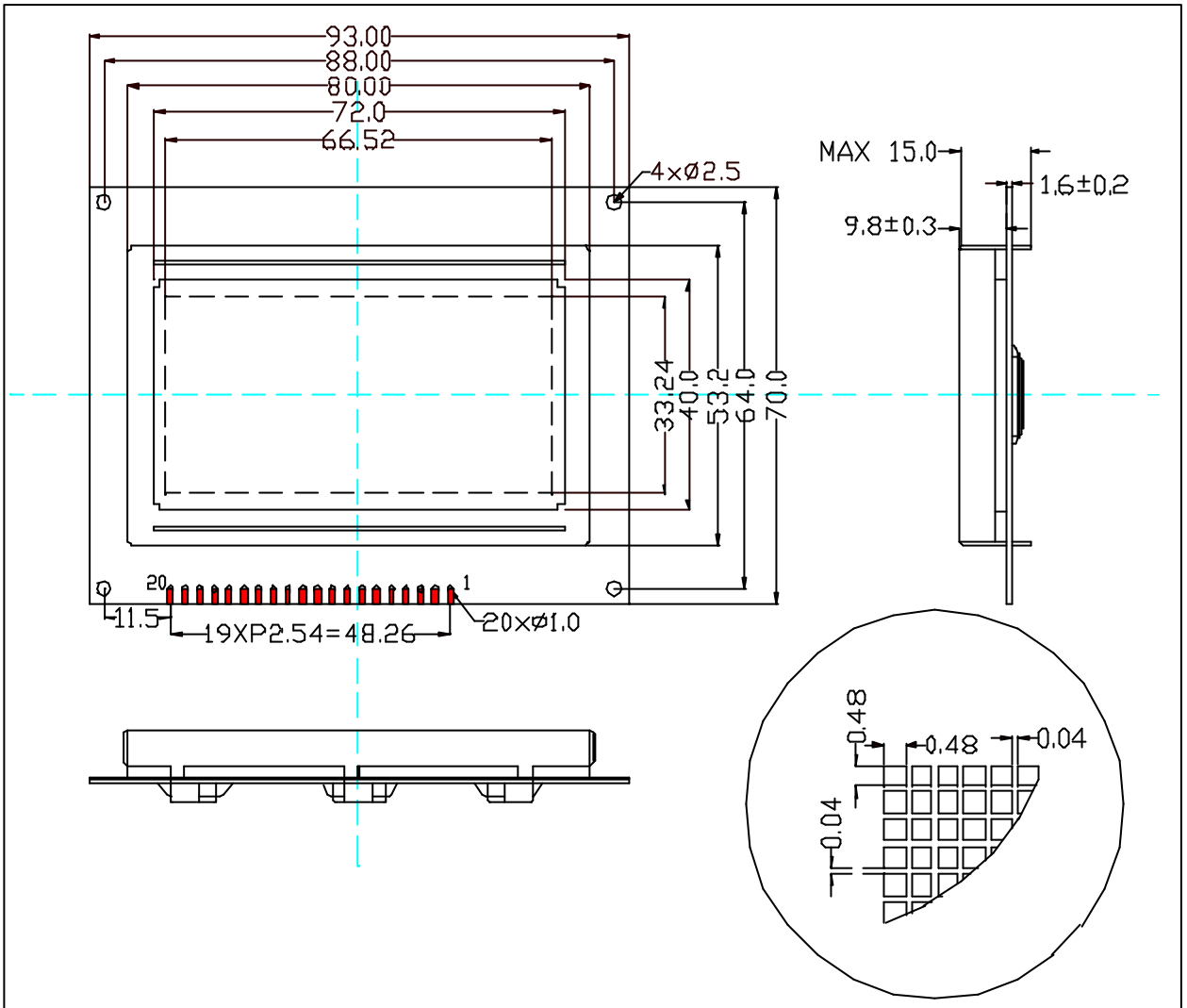
Mechanical Specifications

ITEM	DIMENSION	UNIT
Module Size(W*H*T)	93.0*70.0*10.0	mm
Viewing Area(W*H)	72.0*40.0	mm
Number of Dots	128.0*64.0	PCS
Dot Size(W*H)	0.48*0.48	mm
Dot Pitch(W*H)	0.52*0.52	mm
Module Size With B/L	93.0*70.0*15.0	mm

Temperature Characteristics

PARAMETER	SYMBOL	RATING	UNIT
Operating temperature	Topr	-25~+65	℃
Storage temperature	Tstg	-30~+70	℃

Figure 1. External Dimensions

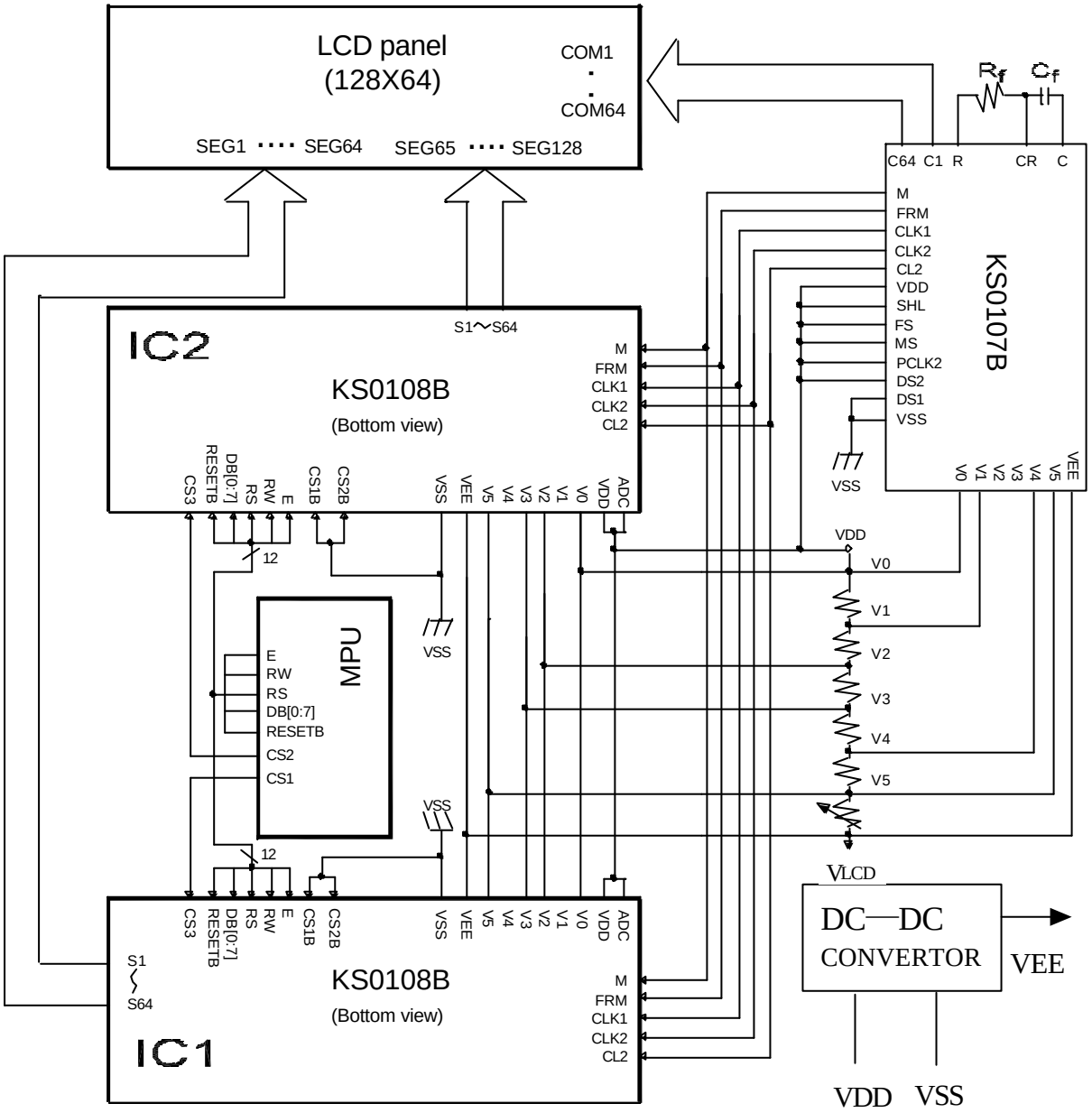


PIN	1	2	3	4	5	6	7	8	9	10
SIGNAL	Vss	VDD	V0	D/I	R/W	E	DB0	DB1	DB2	DB3
PIN	11	12	13	14	15	16	17	18	19	20
SIGNAL	DB4	DB5	DB6	DB7	CS1	CS2	RES	VEE	A	K

***NOTE:** **1**.All units are mm.

2.Tolerances unless otherwise specified ±0.2.

Figure 2. Application Diagram



***Note**

1/64 duty, 1/9 bias

$V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$

Electro-Optical characteristics

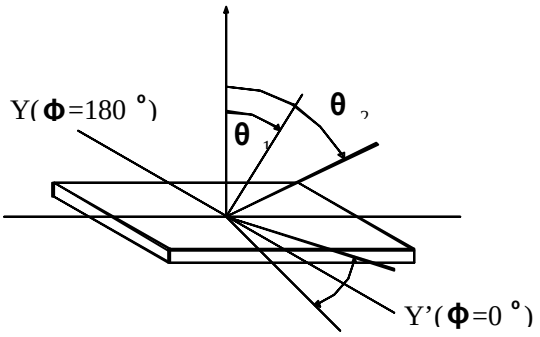
TN Type (Twisted Nematic)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	NOTE
Viewing Angle	$\frac{\theta_2 - \theta_1}{\phi}$	40	-	-	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	θ=20° ϕ= 0°	3
Response Time (rise)	t_R	-	110	-	ms	θ=20° ϕ= 0°	4
Response Time (fall)	t_F	-	110	-	ms	θ=20° ϕ= 0°	4

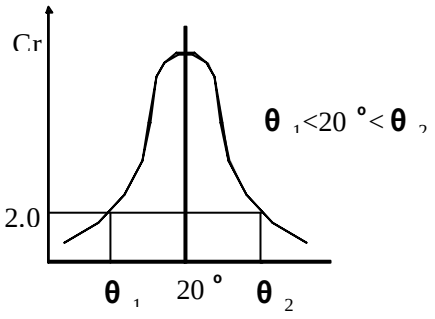
STN Type (Super Twisted Nematic)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	NOTE
Viewing Angle	$\frac{\theta_2 - \theta_1}{\phi}$	70 -90	-	+90	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	θ=20° ϕ= 0°	3
Response Time (rise)	t_R	-	110	-	ms	θ=20° ϕ= 0°	4
Response Time (fall)	t_F	-	110	-	ms	θ=20° ϕ= 0°	4

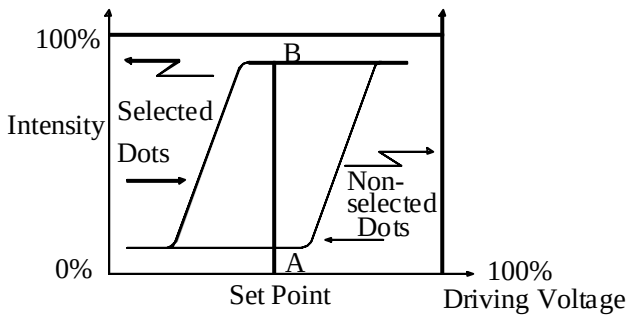
1. Definition of angle θ & ϕ



2. Definition of viewing angle θ_1 & ϕ_2



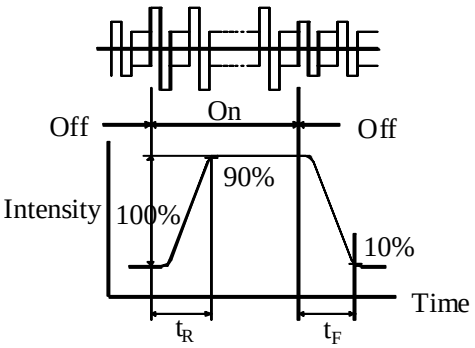
3. Definition of contrast Cr



$Cr = (A / B)^{p}$ Negative : P = -1

Positive : P = +1

4. Definition of optical response



Interface Pin Connections

PIN NO.	SYMBOL	I/O TYPE	DESCRIPTION
1	VSS	Supply	Ground
2	VDD	Supply	Power supply
3	V0	Supply	LCD driver supply voltage
4	D/I		Data input/output pin of internal shift register MS SHL DIO1 DIO2 H H Output Output H L Output Output L H Input Output L L Output Input
5	R/W		Read or Write RW Description H Data appears at DB[7:0] and can be read by the CPU while E= H CS1B=L,CS2B=L and CS3=H. L Display data DB[7:0] can be written at falling edge of E when CS1B=L, CS2B=L and CS3=H.
6	E		Enable signal E Description H Read data in DB[7:0] appears while E= “High”. L Display data DB[7:0] is latched at falling edge of E.
7	DB0	I/O	Data bus [0~7] Bi-directional data bus
8	DB1		
9	DB2		
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		
15 16	CS1 CS2	I	Chip selection When CS1=H,CS2=L, select IC1 When CS1=L,CS2=H, select IC2
17	RESETB	I	Reset signal. When RSTB=L 【1】ON/OFF register becomes set by 0.(display off) 【2】display start line register becomes set by 0 (Z-address 0 set, display from line 0) 【3】After releasing reset , this condition can be changed only by instruction.
18	VEE	Power	VEE is connected by the same voltage.
19	A		Back-light anode
20	K		Back-light cathode

Electrical Absolute Maximum Ratings (KS0107B)

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Operating voltage	V_{DD}	-0.3 ~ +7.0	V	*1
Supply voltage	V_{EE}	V_{DD}-19.0 ~ V_{DD}+0.3	V	*4
Driver supply voltage	V_B	-0.3 ~ V_{DD}+0.3	V	*1,2
	V_{LCD}	V_{EE}-0.3 ~ V_{DD}+0.3	V	*3,4

***Notes:**

*1. Based on V_{SS} = 0V

*2. Applies to input terminals and I/O terminals at high impedance. (Except V0L, V1L, V4L, and V5L)

*3. Applies to V0L, V1L, V4L, and V5L.

*4. Voltage level: $V_{DD} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$

DC Electrical Characteristics(KS0107B)

(VDD= 4.5 to 5.5V, VSS=0V,VDD-VEE=8~17V,Ta= -30 to +85℃)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Operating voltage	V_{DD}	-	4.5	-	5.5	V	
Input voltage	V_{IH}	-	0.7_{VDD}	-	V_{DD}		*1
	V_{IL}	-	V_{SS}	-	$0.3V_{DD}$		
output voltage	V_{OH}	I_{OH}= -0.4mA	V_{DD}-0.4	-	-		*2
	V_{OL}	I_{OL}= 0.4mA	-	-	0.4		
Input leakage current	I_{LKG}	V_{IN}= V_{DD} ~ V_{SS}	-1.0	-	+1.0	μA	*1
OSC Frequency	fosc	Rf=47kΩ±2% Cf=20pF±5%	315	450	585	kHz	
On Resistance (Vdiv-Ci)	R_{ONS}	V_{DD}-V_{EE}=17V Load current± 150μA	-	-	1.5	kΩ	
Operating current	I_{DD1}	Master mode 1/128 Duty	-	-	1.0	mA	*3
	I_{DD2}	Master mode 1/128 Duty	-	-	0.2		*4
Supply Current	IEE	Master mode 1/128 Duty	-	-	0.1		*5
Operating	f_{op1}	Master mode External Duty	50	-	600	kHz	
Frequency	f_{op2}	Slave mode	0.5	-	1500		

Notes

*1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M , and CL2 in the input state.

*2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M , and CL2 in the output state.

*3. This value is specified about current flowing through VSS.

Internal oscillation circuit: Rf=47kΩ, cf=20pF

Each terminals of DS1, DS2, FS, SHL, and MS is connected to VDD and out is no load.

*4. This value is specified about current flowing through VSS.

Each terminals is DS1, DS2, FS, SHL, PCLK2 and CR is connected to VDD,MS is connected to VSS

and CL2, M, DIO1 is external clock.

*5. This value is specified about current flowing through VEE, Don't connect to VLCD (V1~V5).

Electrical Absolute Maximum Ratings(KS0108B)

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Operating voltage	V_{DD}	-0.3 ~ +7.0	V	*1
Supply voltage	V_{EE}	V_{DD}-19.0 ~ V_{DD}+0.3	V	*4
Driver supply voltage	V_B	-0.3 ~ V_{DD}+0.3	V	*1,3
	V_{LCD}	V_{EE}-0.3 ~ V_{DD}+0.3	V	*2

***Notes:**

*1. Based on V_{SS} = 0V
*2. Applies the same supply voltage to V_{EE}. $V_{LCD}=V_{DD}-V_{EE}$.
*3. Applies to M, FRM, CLK1,CLK2, CL, RESETB, ADC, CS1B, CS2B,CS3, E, R/W, RS and DB0~DB7.
*4. Applies V0L,V2L,V3L and V5L.

Voltage level: $V_{DD} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$

DC Electrical Characteristics(KS0108B)

(VDD= 4.5 to 5.5V, VSS=0V,VDD-VEE=8~17V,Ta= -30 to +85℃)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Operating voltage	V_{DD}	-	4.5	-	5.5	V	
Input High voltage	V_{IH1}	-	0.7_{VDD}	-	V_{DD}		*1
	V_{IH2}	-	2.0	-	V_{DD}		*2
Input Low voltage	V_{IL1}	-	0	-	$0.3V_{DD}$		*1
	V_{IL2}	-	0	-	0.8		*2
Output High Voltage	V_{OH}	I_{OH}= -0.2mA	2.4	-	-		*3
Output Low Voltage	V_{OL}	I_{OL}= 1.6mA	-	-	0.4		*3
Input leakage current	I_{LKG}	$V_{IN}= V_{SS} \sim V_{DD}$	-1.0	-	+1.0	μA	*4
Three-state (OFF) Input Current	I_{TSL}	$V_{IN}= V_{SS} \sim V_{DD}$	-5.0	-	5.0		*5
Driver Input leakage current	I_{DIL}	$V_{IN}= V_{EE} \sim V_{DD}$	-2.0		2.0		*6
On Resistance (Vdiv-Ci)	R_{ONS}	V_{DD}-V_{EE}=15V Load current± 100μA	-	-	7.5	kΩ	*8
Operating current	I_{DD1}	During Display	-	-	0.1	mA	*7
	I_{DD2}	During Access Access Cycle=1MHz	-	-	0.5		*7

Notes

*1. CL, FRM, M, RSTB, CLK1, CLK2
*2. CS1B, CS2B, CS3, E, R/W, RS, DB0~DB7
*3. DB0~DB7
*4. Except DB0~DB7
*5. DB0~DB7 at high impedance
*6. V0, V1, V3, V3, V4, V5
*7. 1/64 duty , FCLK=250KHZ, Frame Frequency=70HKZ, Output: No Load
*8. V_{DD}-V_{EE}=13.5V
V0L>V2L>= V_{DD}-2/7(V_{DD}-V_{EE})>V3L= V_{EE}+2/7(V_{DD}-V_{EE})>V5L

CHAPTER 2

Driver IC Function Description

KS0107 Driver IC
64COM graphic driver for dot matrix LCD

Introduction

The KS0107B is an :CD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems.

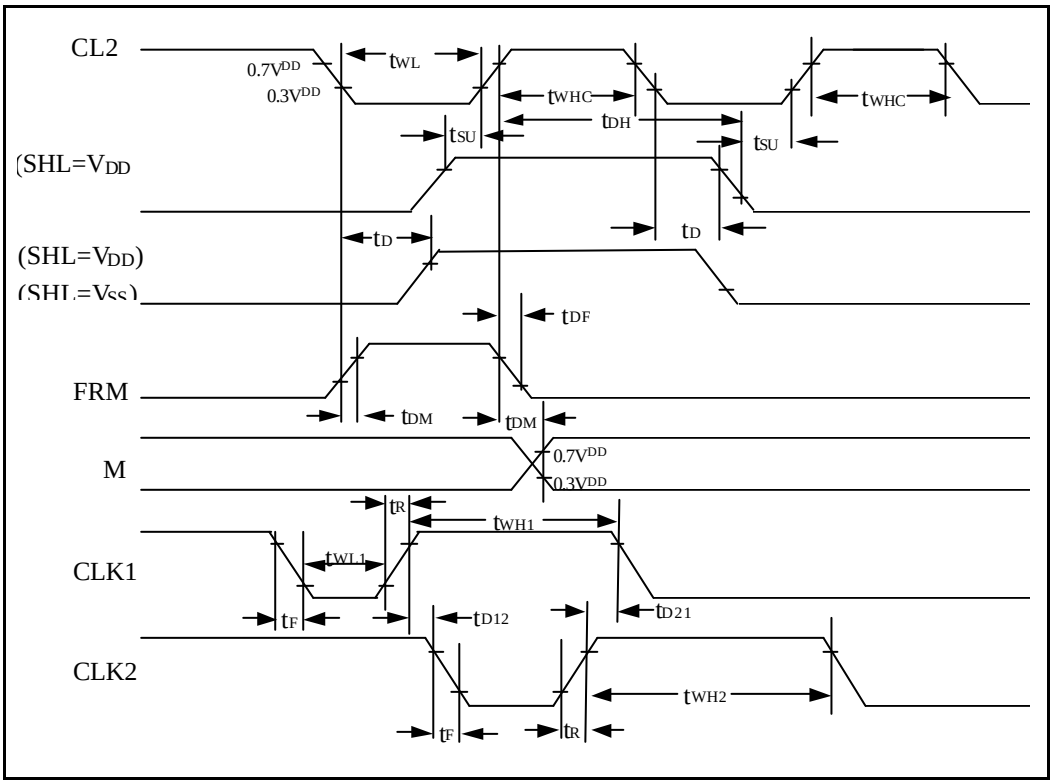
This device provides 64 shift registers and 64 output drivers.

It generates the timing signal to control the KS0108B (64 channel segment drover.).

The KS0107B is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the KS0108B (64 channel segment drover.).

AC Characteristics (VDD=4.5~5.5V, Ta=-30℃~+85℃)

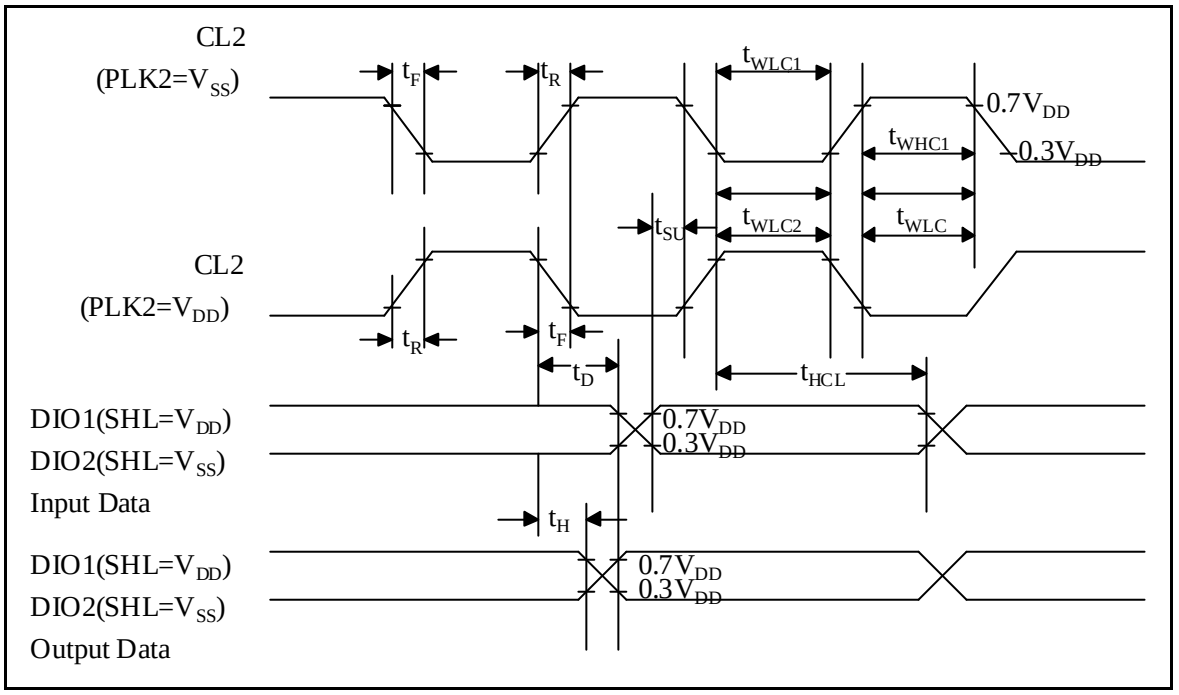
1. Master mode (MS=V_{DD}, PCLK2=V_{DD}, Cf=20pF, Rf=47KΩ)



CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Data Setup Time	t_{SU}	20	-	-	
Data Hold Time	t_{DH}	40	-	-	

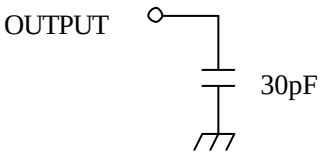
Data Delay Time	t_D	5	-	-	μs
FRM Delay Time	t_{DF}	-2	-	2	
M Delay Time	t_{DM}	-2	-	2	
CL2 Low Level Width	t_{WLC}	35	-	-	
CL2 High Level Width	t_{WHC}	35	-	-	
CLK1 Low Level Width	t_{WL1}	700	-	-	ns
CLK2 Low Level Width	t_{WL2}	700	-	-	
CLK1 High Level Width	t_{WH1}	2100	-	-	
CLK2 High Level Width	t_{WH2}	2100	-	-	
CLK1-CLK2 Phase Difference	t_{D12}	700	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	700	-	-	
CLK1,CLK2 Rise/Fall Time	t_R/t_F	-	-	150	

Slave mode (MS=V_{SS})



CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
CL2 Low Level Width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 High Level Width	t_{WHC1}	150	-	-		PCLK2=V_{SS}
CL2 Low Level Width	t_{WLC2}	150	-	-		PCLK2=V_{DD}
CL2 High Level Width	t_{WHL}	450	-	-		PCLK2=V_{DD}
Data Setup Time	t_{SU}	100	-	-		
Data Hold Time	t_{DH}	100	-	-		
Data Delay Time	t_D	-	-	200		*1
Output Data Hold Time	t_H	10	-	-		
CL2 Rise/Fall Time	t_R/t_F	-	-	30		

***1: Connect load CL=30pF**

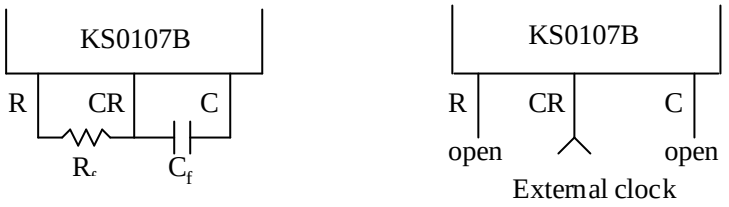


FUNCTIONAL DESCRIPTION

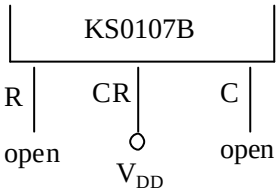
1.RC Oscillator

The RC Oscillator generates CL2, M, FRM, of the KS0107B and CLK1, CLK2 of the KS0107B by the oscillation resister R and capacitor C.
When selecting the master/slave, oscillation circuit is as following:

1) **Master Mode**



2) Slave Mode



2.Timing Generation circuit

It generates CL2, M, FRM, CLK1, and CLK2 by the frequency from oscillation circuit.

1) Selection of Master/Slave (M/S)
   When M/S is "H", it generates CL2, M, FRM, CLK1, and CLK2 internally. When M/S is "L", it operates by receiving M, CLK2 from master device.
2) Frequency Selection (FS)
   To adjust FRM by 70Hz, the oscillation frequency should be as following:

FS	OSCILLATION FREQUENCY
H	f_{OSC}=430KHz
L	f_{OSC}=215KHz

In the slave mode, it is connected to $V_{DD.}$

3) **Duty Selection (DS1, DS2)**
It provides various duty selection according to DS1, DS2.

DS1	DS2	DUTY
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

3. Data shift & Phase Select Control

1) Phase Selection
It is a circuit to shift data on synchronization or rising edge or falling edge of the CL2 according to PCLK2.

PCLK2	PHASE SELECTION
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

2) Data shift Direction Selection
When M/S is connected to VDD, DIO1 and DIO2 terminal is only output.
When M/S is connected to VSS, it depends on the SHL.

MS	SHL	DIO1	DIO2	DIRECTION OF DATA
H	H	Output	Output	C1~C64
	L	Output	Output	C64~C1
L	H	Input	Output	DIO1~C1~C64~DIO2
	L	Output	Input	DIO2~C64~C1~DIO1

CHAPTER 3

Driver IC Function Description

KS0108 Driver IC
64 SEG graphic driver for dot matrix LCD

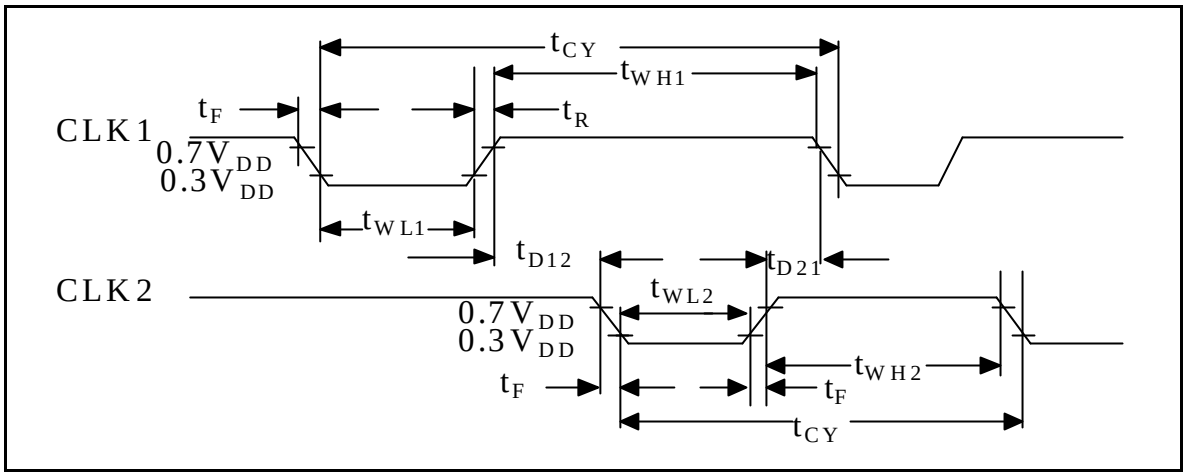
Introduction

The KS0108B is an LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64 bit data latch 64 bit drivers and decoder logics. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The KS0108B composed of the liquid crystal display system in combination with the KS0107B(64 common driver).

AC Characteristics (V_{DD}=4.5~5.5V ,V_{SS}=0V, Ta=-30℃~+85℃)

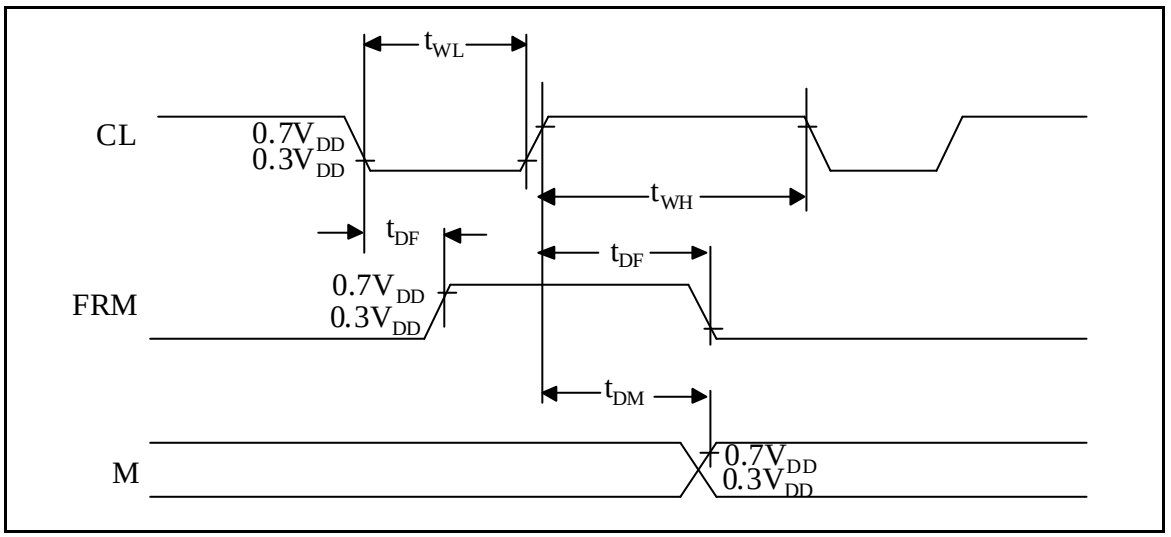
(1) Clock Timing

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
CLK1, CLK2 Cycle Time	t_{CY}	2.5	-	20	μs
CLK1 ' LOW ' Level Width	t_{WL1}	625	-	-	ns
CLK2 ' LOW ' Level Width	t_{WL2}	625	-	-	
CLK1 ' HIGH ' Level Width	t_{WH1}	1875	-	-	
CLK2 ' HIGH ' Level Width	t_{WH2}	1875	-	-	
CLK1-CLK2 Phase Difference	t_{D12}	625	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	625	-	-	
CLK1, CLK2 Rise Time	t_R	-	-	150	
CLK1, CLK2 Fall Time	t_F	-	-	150	



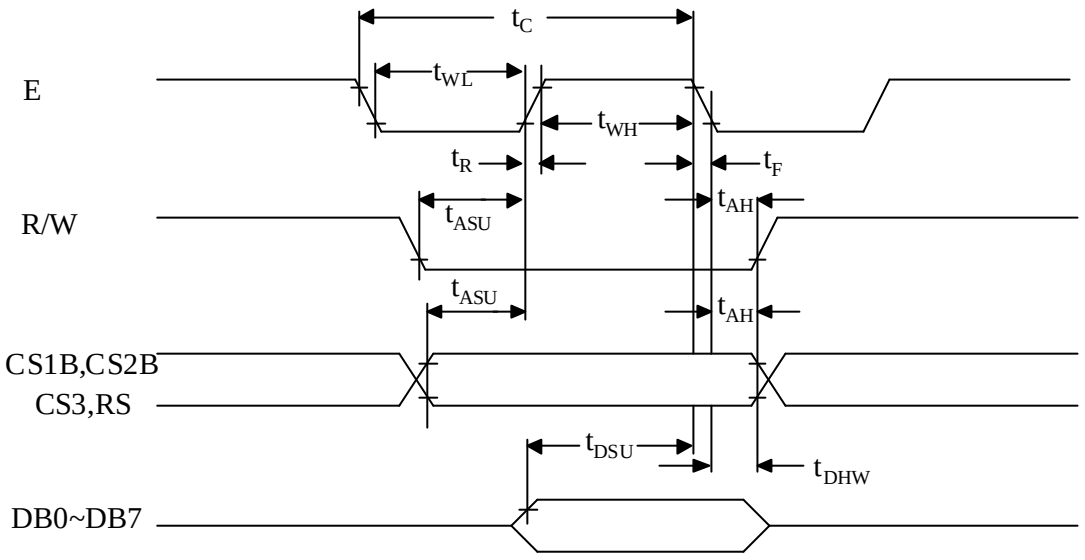
（2）.Display Control Timing

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
FRM Delay Time	t_{DF}	-2	-	2	us
M Delay Time	t_{DM}	-2	-	2	
CL ‘ LOW ’ Level Width	t_{WL}	35	-	-	
CL ‘ HIGH ’ Level Width	t_{WH}	35	-	-	

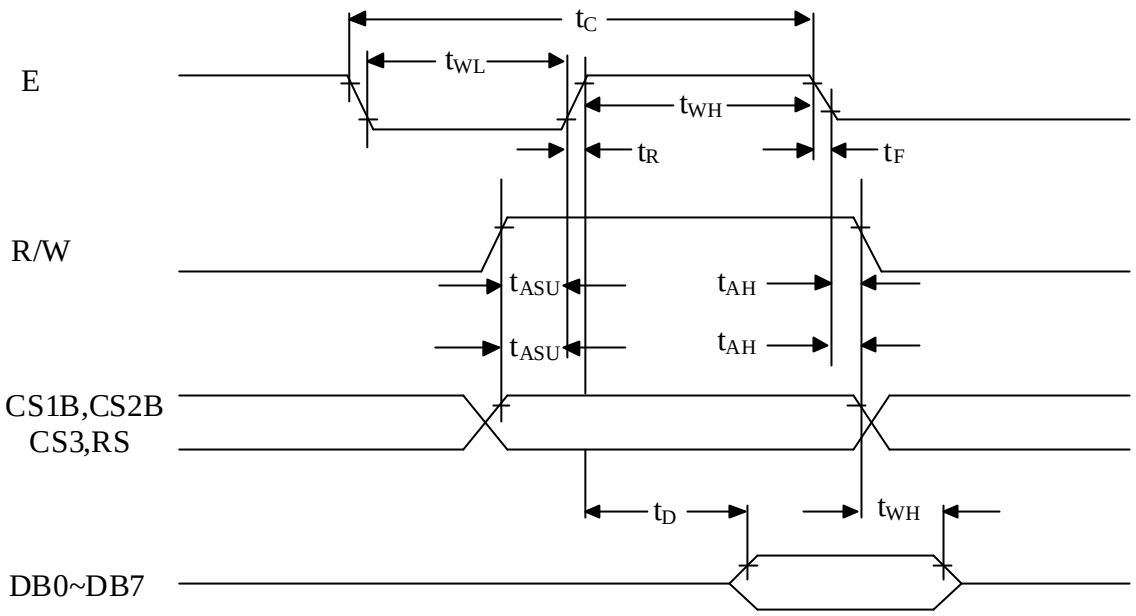


(3) . MPU Interface

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	
E Low Level Width	t_{WL}	450	-	-	
E Rise Time	t_R	-	-	25	
E Fall Time	t_F	-	-	25	
Address Set-Up Time	t_{ASU}	140	-	-	
Address Hold Time	t_{AH}	10	-	-	
Data Set-Up Time	t_{SU}	200	-	-	
Data Delay Time	t_D	-	-	320	
Data Hold Time (Write)	t_{DHW}	10	-	-	
Data Hold Time (Read)	t_{DHR}	20	-	-	



MPU Write timing



MPU Read timing

OPERATING PRINCIPLES & METHODS

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS!B-CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.
When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H , RS=L, status data (busy check) can read out.
To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	FUNCTION
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

4. Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

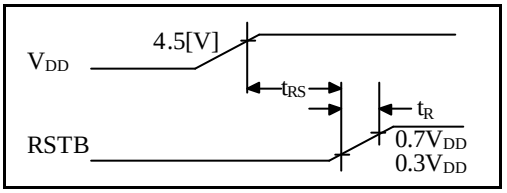
1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can by accepted. Therefore, execute other instructions after making sure that DB4= (clear RSTB) and DB7=0 (ready) by status read instruction.

The conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns

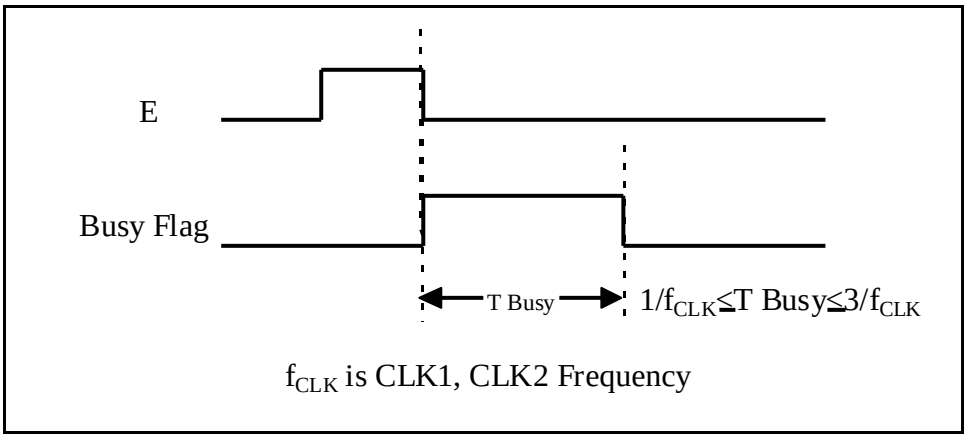


5. Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating .

When busy flag is low, KS0108B can accept the data or instruction.

DB7indicates busy flag of the KS0108B.



6. Display On/Off Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data.
The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.
The status of the flip-flop is output to DB5 by status read instruction.
The display on/off flip-flop synchronized by CL signal.

7. X Page Register

X page register designates pages of the internal display data RAM.
Count function is not available. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9. Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display , write datra1. The other way , off state, writes 0.
Display data RAM address and segment output can be controlled by ADC signal.
ADC=H => Y-address 0: S1~Y address 63: S64
ADC=L => Y-address 0: S64~Yaddress 63: S1
ADC terminal connect the V_{DD} or V_{SS}.

10. Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.
Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.
It is used for scrolling of the liquid crystal display screen.

Display Control Instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

INSTRUCTION	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	FUNCTION
Read Display Date	1	1	Read data								Reads data (DB[7:0]) from display data RAM to the data bus.
Write Display Date	1	0	Write data								Writes data (DB[7:0]) into the DDRAM. After writing instruction, Y address is incriminated by 1 automatically
Status Read	0	1	Busy	0	ON/OFF	Re-set	0	0	0	0	Reads the internal status BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Set Address (Y address)	0	0	0	1	Y address (0~63)						Sets the Y address at the column address counter
Set Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the Display Data RAM displayed at the top of the screen.
Set Address (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display On/off	0	0	0	0	1	1	1	1	1	0/1	Controls the display ON or OFF. The internal status and the DDRAM data is not affected. 0: OFF, 1: ON

1. Display On/Off

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

2. Set Address (Y Address)

Y address (AC0~AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

3. Set Page (X Address)

X address (AC0~AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

4. Display Start Line (Z Address)

Z address (AC0~AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others (1/32~1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.
  When ON/OFF is 0, the display is off.
- RESET
  When RESET is 1, the system is being initialized.
  In this condition, no instructions except status read can be accepted.
  When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

Writes data (D0~D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

7. Read Display Data

Reads data (D0~D7) from the display data RAM.
After reading instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0