

Full-bridge FET Driver

DESCRIPTION

The TS61001 is a high-voltage FET driver that can be used to drive N-channel devices in full or half bridge configurations. The TS61001 can support various power converter applications, multiple standard and proprietary wireless power applications, and motor driver systems.

APPLICATIONS

- Multi-standard compliant and non-compliant wireless chargers for:
 - Cell Phones and Smartphones
 - GPS Devices
 - Digital Cameras
 - Tablets and eReaders
 - Portable Lighting
- Full and half-bridge power converters
- Motor drive applications

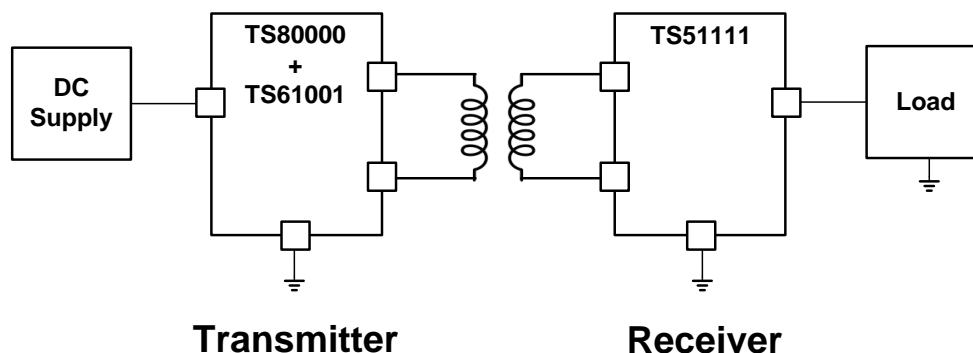
FEATURES

- Supports Qi®, PMA, A4WP and proprietary wireless power applications
- Power outputs scalable based on FET size
- Support for half and full-bridge power sections
- Integrated comparator
- Low external component count
- Available in 28 pin 5x5 QFN

SPECIFICATIONS

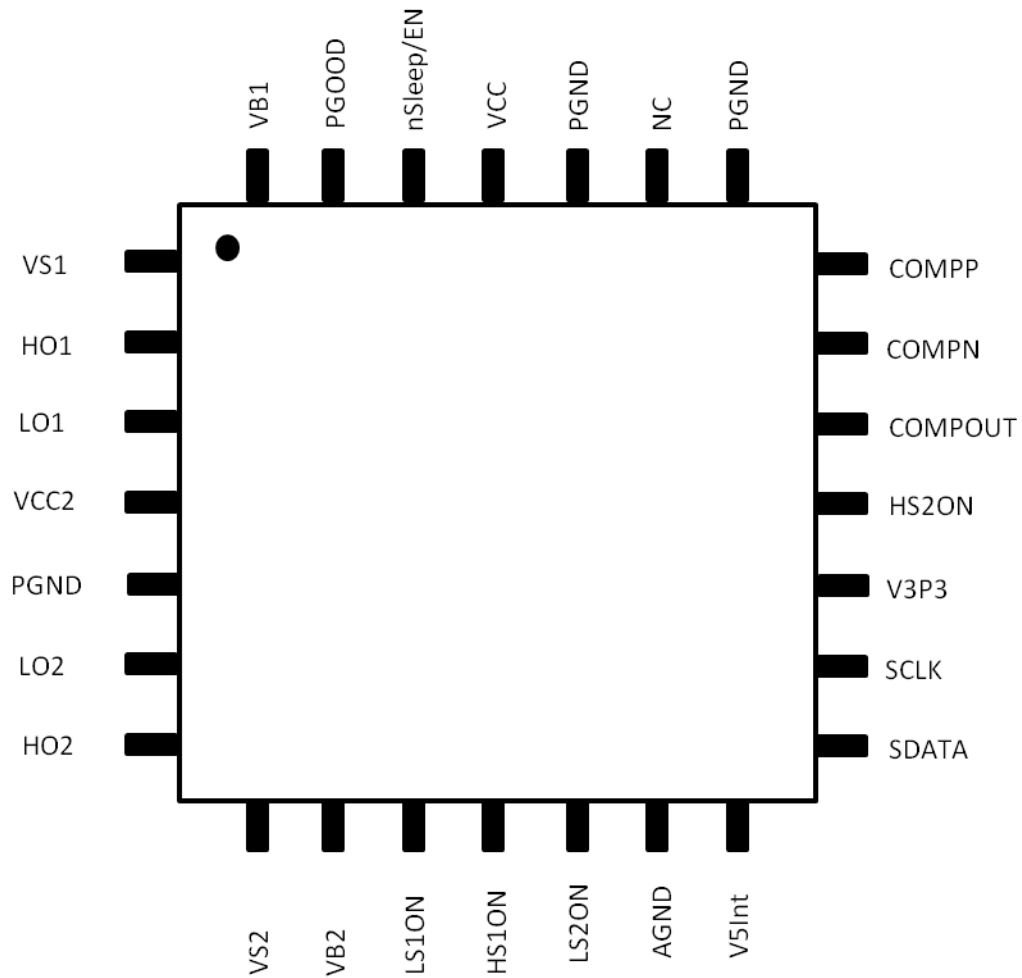
- Drives both low side and high side N-channel MOSFETS
- 6Ω pull-up, 2Ω pull-down gate drivers
- Independent TTL compatible inputs
- Floating gate drive and bootstrap circuits for driving high side devices – up to 85V for the bootstrap supply voltage
- 5 - 12V gate drive capability allows compatibility with a wide range of FETs
- Fast propagation delays (<50nS typical)
- Matched channel to channel delays (<25nS mismatch)
- Fast rise and fall times
- Optional break before make detection to set minimum dead time protection
- Available comparator, amplifier and 3.3V linear regulator (10mA capability) for supporting circuitry
- Under voltage lock out protection
- Over temperature shut down (TSD) protection

TYPICAL APPLICATION



PINOUT

(Top View)



PIN DESCRIPTION

QFN Pin #	Pin Symbol	Function	Description
1	VS1	FET drive	High side MOSFET source #1
2	HO1	FET drive	High side MOSFET gate drive #1
3	LO1	FET drive	Low side MOSFET gate drive #1
4	VCCG	Input power	Input power supply (gate driver supply)
5	PGND	Power GND	Power GND for drivers
6	LO2	FET drive	Low side MOSFET gate drive #2
7	HO2	FET drive	High side MOSFET gate drive #2
8	VS2	FET drive	High side MOSFET source #2
9	VB2	Bootstrap	Bootstrap for gate drive #2
10	LS1ON	PWM1_L	Low-side gate control #1
11	HS1ON	PWM1_H	High-side gate control #1
12	LS2ON	PWM2_L	Low-side gate control #2
13	AGND	Analog GND	Analog GND
14	V5INT	Decoupling	Internal 5V regulator decoupling
15	SDATA	I2C Data	I2C data
16	SCLK	I2C Clock	I2C clock
17	V3P3	Decoupling	Internal 3.3V regulator decoupling
18	HS2ON	PWM2_H	High-side gate control #2
19	COMPOUT	Comparator	Comparator output
20	COMP_N	Comparator	Comparator input (-)
21	COMPP	Comparator	Comparator input (+)
22	PGND	Power GND	Power GND
23	NC	No Connect	No Connect
24	PGND	Power GND	Power GND
25	VCC	Input power	Input power supply (main supply)
26	/SLEEP	Disable	Disable Pin (active low)
27	PGOOD	Output Signal	Power Good Status
28	VB1	Bootstrap	Bootstrap for gate drive #1

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted^(1,2)

Parameter	Value	Unit
VCC, VCCG	13.2	V
VB1, VB2	13.2 (relative to VS1,2)	V
SDATA, SCLK	3.6	V
LS10N, LS20N, HS10N, HS20N	3.6	V
COMP1, COMPP, AMP1, AMP2, COMOUT, AMPOUT	3.6	V
Electrostatic Discharge – Human Body Model	+/-2k	V
Electrostatic Discharge – Charge Device Model	+/-500	V
Lead Temperature (soldering, 10 seconds)	260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (Note 1)	34.5	°C/W
θ_{JC}	Thermal Resistance Junction to Case (Note 1)	2.5	°C/W
T _{STG}	Storage Temperature Range	-65 to 150	°C
T _{JMAX}	Maximum Junction Temperature	150	°C
T _J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes 16LD 3x3 QFN with hi-K JEDEC board and 13.5 inch² of 1 oz Cu and 4 thermal vias connected to PAD

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input Operating Voltage	5	12	12.5	V
C _{BST}	Bootstrap Capacitor		100		nF

ELECTRICAL CHARACTERISTICS

 Electrical Characteristics, $T_j = -40C$ to $125C$, $VCC = 12V$ (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC Supply Voltage						
VCC	Input Supply Voltage		5	12	12.5	V
Iq	Input Supply current	/SLEEP = Hi; No loads; Gate drivers off	0.5	1.5	3	mA
Iq	Input Supply current	/SLEEP = Hi; Gate driver Fs = 200KHz (no load)		4	5	mA
Iqq_sleep	Stand by current	/SLEEP = 0V; Inputs driven Low		3	10	uA
Ron Characteristics						
Ron (pulldown)	HS,LS pull down device	12V VCC		1.4	2	Ω
Ron (pullup)	HS, LS pull up device	12V VCC		4.0	6.5	Ω
Under Voltage Lock Out						
UVLO (rise)	UV threshold (VCCG)	Rising threshold measurement	4.1	4.35	4.5	
UVLO (fall)	UV threshold (VCCG)	Falling threshold measurement	3.8	4	4.3	
UVLO (hyst)	UV hysteresis (VCCG)	Hysteresis		0.15	0.25	
UVLO (rise)	UV threshold (VCC)	Rising threshold measurement	4.1	4.35	4.5	
UVLO (fall)	UV threshold (VCC)	Falling threshold measurement	3.8	4	4.3	
UVLO (hyst)	UV hysteresis (VCC)	Hysteresis		0.15	0.25	
Input Pins VIH & VIL						
VIH	Digital Input Pins	Gate driver inputs, I2C		1.5	2.2	
VIL	Digital Input Pins	Gate driver inputs, I2C	0.8	1.3		
Hyst	Digital Input Pins	Gate driver inputs, I2C	0.1	0.2		
Propagation Delays & Rise/Fall times						
T _{PLShl}	Prop delay (LS) high to low	LSxON to LO1 (11V)		15	50	nS
T _{PLSh}	Prop delay (LS) low to high	LSxON to LO1(1V)		15	50	nS
T _{PHShl}	Prop delay (HS) high to low	HSxON to HOx (HOx - VSx = 10V)		25	50	nS
T _{PHSh}	Prop delay (HS) low to high	HSxON to HOx (HOx - VSx = 1V)		25	50	nS
T _{PMMishs}	Prop delay mismatch (ls to hs)	LS off to HS on mismatch		10	40	nS
T _{PMMhsls}	Prop delay mismatch (hs to ls)	HS off to LS on mismatch		10	40	nS
TPW _{min}		Minimum pulse width response		80		nS
T _r	Rise time (HS/LS)	1nF load; 20 - 80%			20	nS
T _p	Fall time (HS/LS)	1nF load; 80 - 20%			20	nS
V3P3 Regulator						
Vout	Nominal Output voltage		3.15	3.3	3.45	V
Iout	External loading	Output Current capability	10	15		mA
Comparator						
Voffset	Comparator Offset		-10	0	10	mV
VCMIn	Input Common Mode Range		0.2		1.8	V
Tcomp	Comparator detection time	Input signal of 10mV		40	80	nS
Amplifier						
Voffset	Amplifier Offset		-10	0	10	mV
VCMIn	Input Common Mode Range		0.2		1.8	V
AC gain			40			dB
UGBW	Unity gain bandwidth		5			MHz

APPLICATION SCHEMATIC

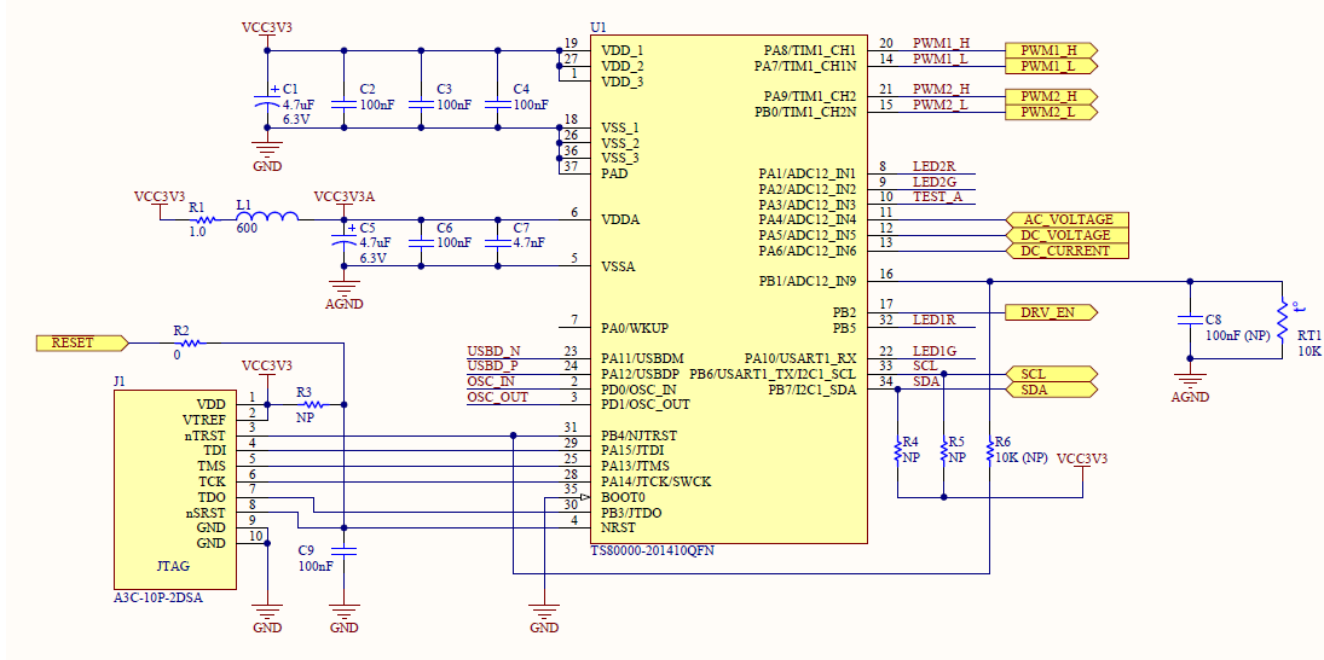


Figure 1: TS61001 Application Schematic (control section)

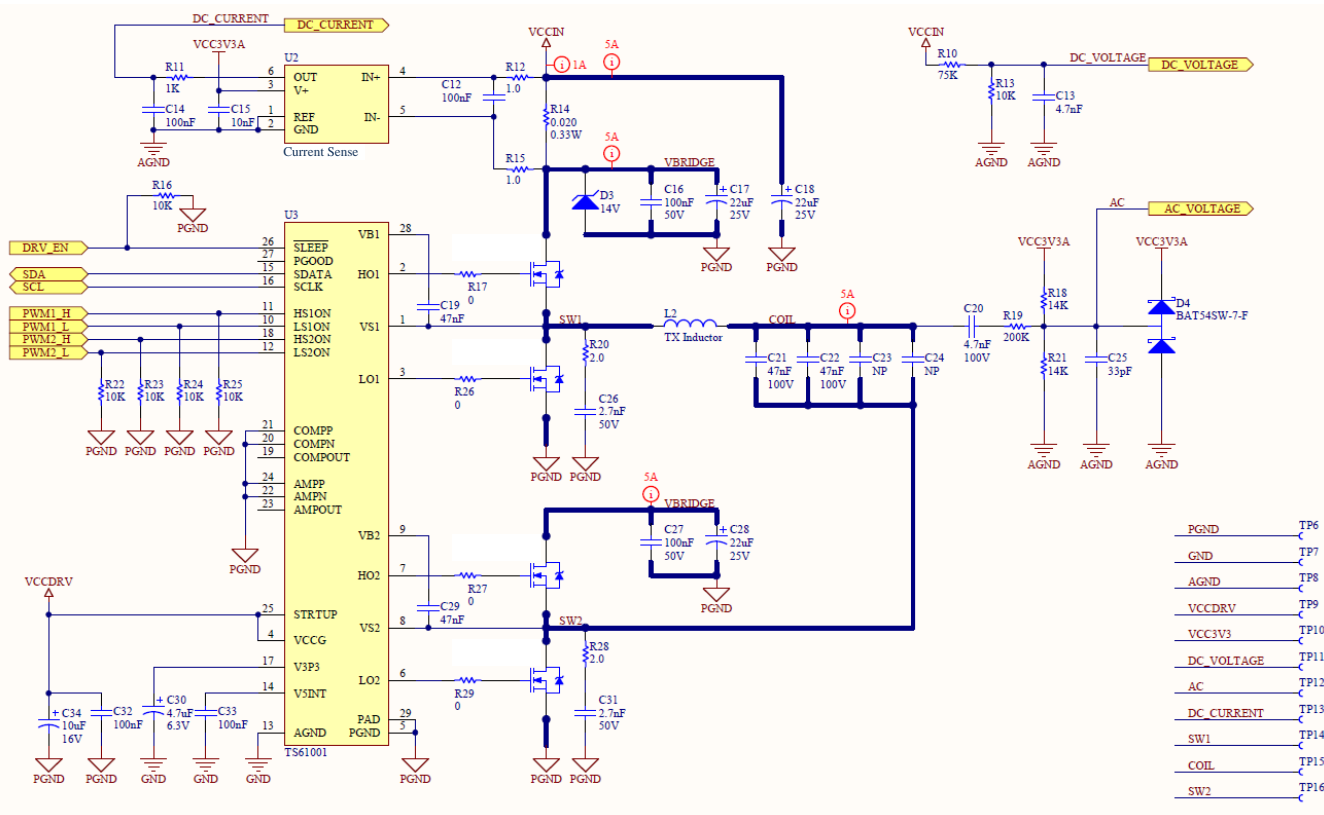
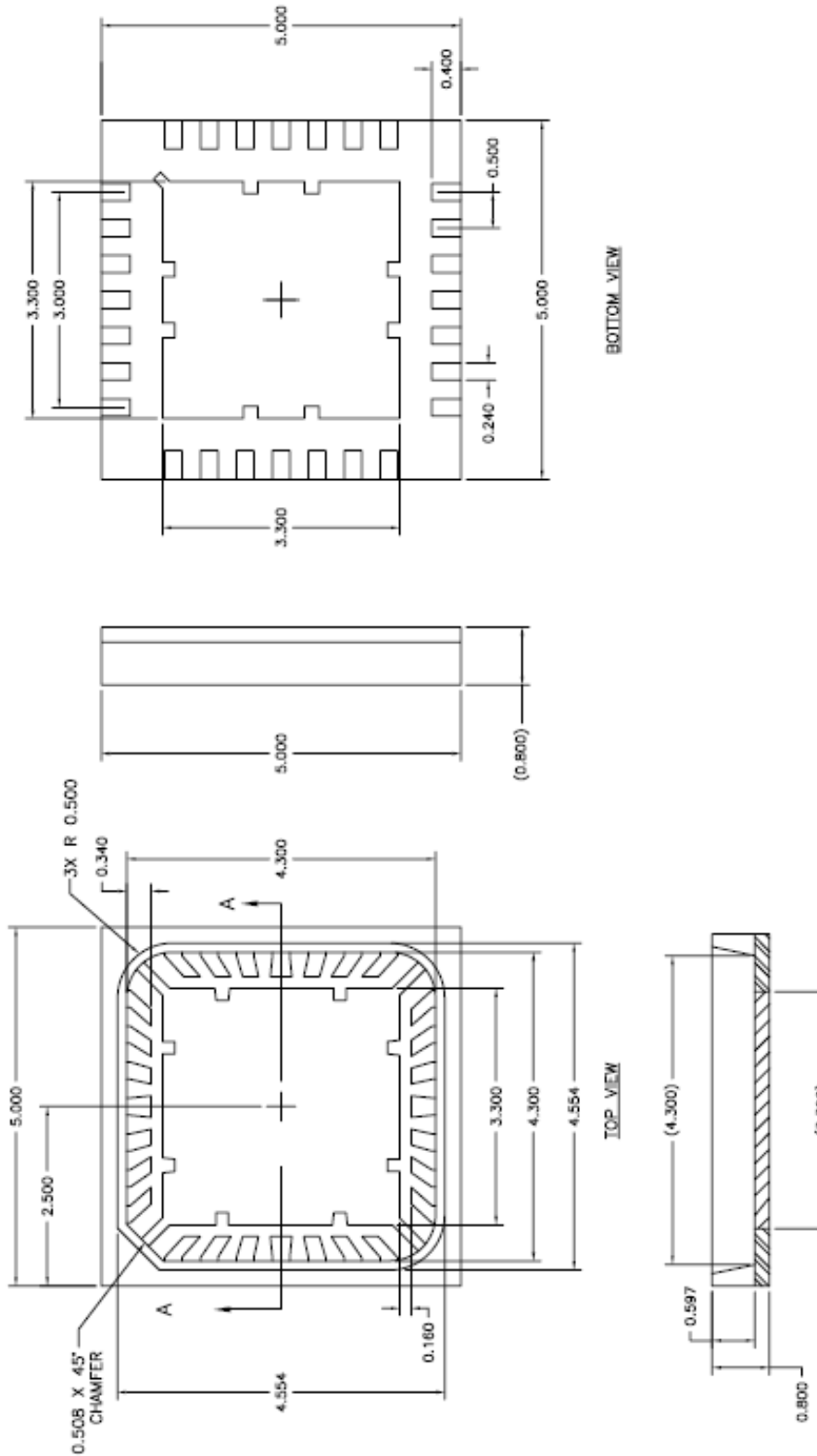


Figure 2: TS61001 Application Schematic (power section)

PACKAGE DIMENSIONS



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