DATA SHEET

OKI GaAs PRODUCTS

10-Gbps GaAs Family High-Speed Optical Communications System

April 1999

Oki Semiconductor

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Oki Semiconductor

10-GHz GaAs Family

High-Speed Optical Communications Systems

INTRODUCTION

Oki's 10-GHz logic devices are manufactured using a 0.2-µm, ion-implanted process, which is similar to Oki's familiar 0.5-µm telecommunications process. However, the 0.2-µm process uses a phase-shifting edge line (PEL) masking method for gate fabrication. Gold-based, three-level metal interconnections are used for high density and shorter wiring paths. Layers 1 and 2 are signal lines. Layer 3, which is formed by electroplating, is used for ground or power supply lines because of its lower resistance. An optional buried "p" channel structure is adopted for reducing short channel effects.

The following table shows the digital GaAs logic processes of the 10-GHz GaAs family.

GaAs Logic Processes

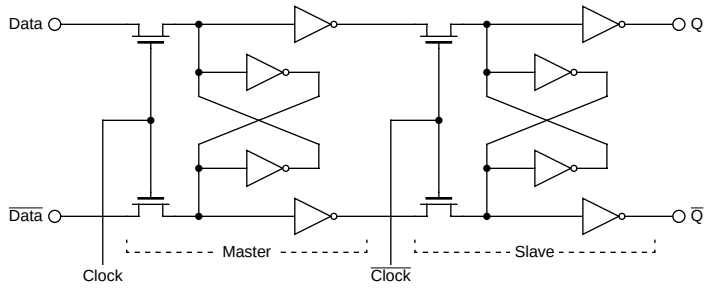
Basic FET Process	Basic Gate Circuit	Photo Masking	Gate Length (µm)	fT (GHz)	Gate Delays (ps)	Application
MESFET	DCFL or SBFL	I-line printing	0.5	30	25	< 2.4 Gbps standard cell
MESFET	DCFL or SBFL	PEL	< 0.2	60	9	>12-Gbps hand-routed logic
Pseudomorphic-inverted HEMT	DCFL or SBFL	PEL	0.2	> 60	7	> 20-Gbps low-density logic
Pseudomorphic BP--MESFET	Analog	Deep UV	0.2	> 60	–	Analog amplifier

The key to operating reliably at 10 Gbps is logic circuitry that can easily manipulate data at over 13 Gbps. The higher frequency overhead is required to meet the different clock skews encountered when designing and routing 10-Gbps data management hardware.

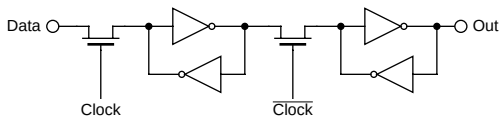
The logic is either direct-coupled FET logic (DCFL) or source-coupled FET logic (SCFL). The low-drive disadvantage of DCFL can be improved by using super-buffer FET logic (SBFL). The basic speed of SBFL is slower than DCFL, but SBFL is faster with higher fanouts and longer metal runs. A designer selects the best performing logic for each logic element application. SBFLs used for clock distribution, output buffers, etc. Typical gate delays of 9 ps and power of 2 mW per gate are achieved. Register logic elements like D-flip flops are assembled using memory cell flip flops (MCFF) as shown in *Figure 1*.The operation speed of a MCFF, which is about twice that of a conventional 6 NOR-gate circuit, operates at very low power. To simplify device interconnections, AC-coupled clock and data input lines are created using the circuit shown in *Figure 2*.

FEATURES

- 10-Gbps operation: highest speed available
- ECL level logic swings: easy interface to other logic
- Inputs internally terminated: reduces noise and phase jitter
- 50-Ω I/Os: easy to interconnect hardware



Master/Slave Flip-Flop



Flip-Flop

Figure 1. Memory Cell Flip-Flops

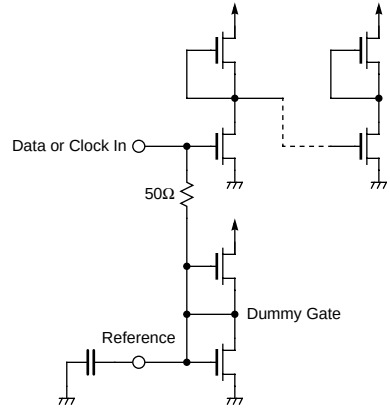


Figure 2. AC-Coupled, Self-Biased Logic Input

Many 10-Gbps inputs are self-biased and 50-Ω terminated, for capacitance coupling. The outputs are DC-coupled to drive 50-Ω ground terminated lines.

DATA SHEETS

This document contains data sheets for the KGL4201, KGL4202, GHDD4411, and GHDD4414 10-Gbps GaAs High-Speed Optical Communication Systems.

Data sheets for other communication devices may be obtained from the Oki Semiconductor WEB site, www.okisemi.com or from the local sales office.

Oki Semiconductor

KGL4201

10-GHz 8:1 Multiplexer

GENERAL DESCRIPTION

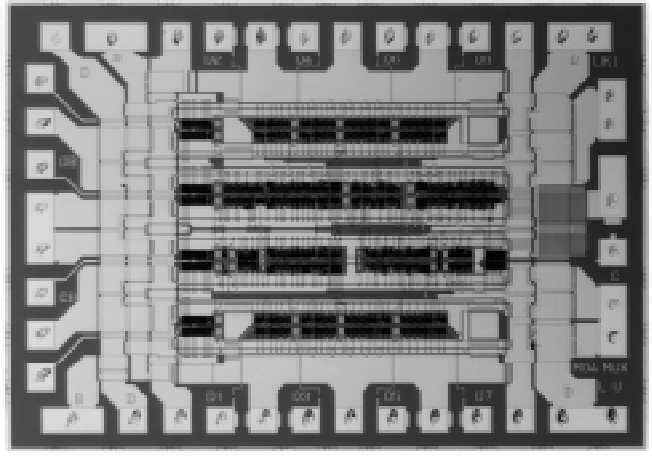
Oki's KGL4201 is a 10-GHz 8:1 multiplexer designed to operate in 10-Gbps communication links. This circuit synchronously merges eight 1.25-Gbps data streams, clocked at low frequency rates into a single 10-Gbps stream, clocked at the higher frequency. In the KGL4201 multiplexer, the 10-GHz master clock is first divided by two, then by four. The lower frequency components are first multiplexed by four, then the two groups are merged into a single data stream using the master 10-Gbps clock. Complementary 1/8 synchronous clock outputs are made available from the KGL4201 for use in synchronizing lower frequency logic.

All signal interfaces are 50-Ω with direct DC coupling on the 1.25-Gbps data inputs and phase-locked 1.25-Gbps clock outputs. The 10-Gbps data output and 10-GHz clock input are AC-capacitively-coupled for ease of interfacing at microwave speeds and reducing ground noise induced phase jitter. All package clock and data pins are separated by either ground or supply voltage pins to control the I/O impedance, maintain signal isolation and reduce phase noise.

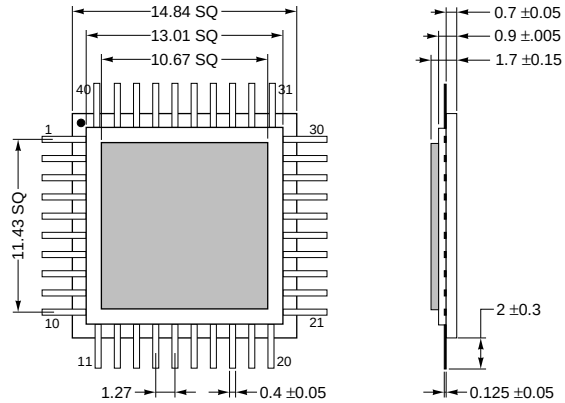
The KGL4201 is shipped in a 40-pin ceramic flat-package with impedance-controlling ground plane and flush mounting bottom heat sink.

FEATURES

- AC-coupled 10 Gbps I/O: eliminates DC coupled phase jitter
- 1/8 clock generated on chip: easy to synchronize downstream logic
- 2 V, 2.4 W
- Isolated I/O pins: minimize noise and impedance variation
- Packaged in 40-pin ceramic flat-package with ground plane and heat sink.



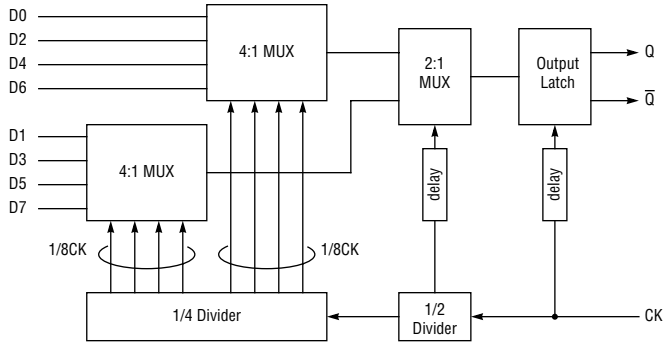
PIN CONFIGURATION



Pin Configuration

Pin	Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	GND	11	GND	21	VDD	31	GND
2	Q	12	VDD	22	GND	32	VDD
3	GND	13	D0	23	GND	33	D7
4	$\overline{Q}$	14	GND	24	CK	34	GND
5	GND	15	D2	25	GND	35	D5
6	GND	16	D4	26	GND	36	D3
7	1/8CK	17	GND	27	RCK	37	GND
8	GND	18	D6	28	GND	38	D1
9	$\overline{1/8CK}$	19	GND	29	GND	39	VB
10	VB	20	GND	30	GND	40	VDD

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage for internal logic	V_{DD}	1.9	2.0	2.1	V
Power supply voltage for output buffer	V_B	1.9	2.0	2.1	V
Operating temperature range at package base	T_S	0	–	70	°C

DC CHARACTERISTICS

V_{DD} = 2V ±0.1V, VB=2V ±0.1V Ts = 0 to 70°C

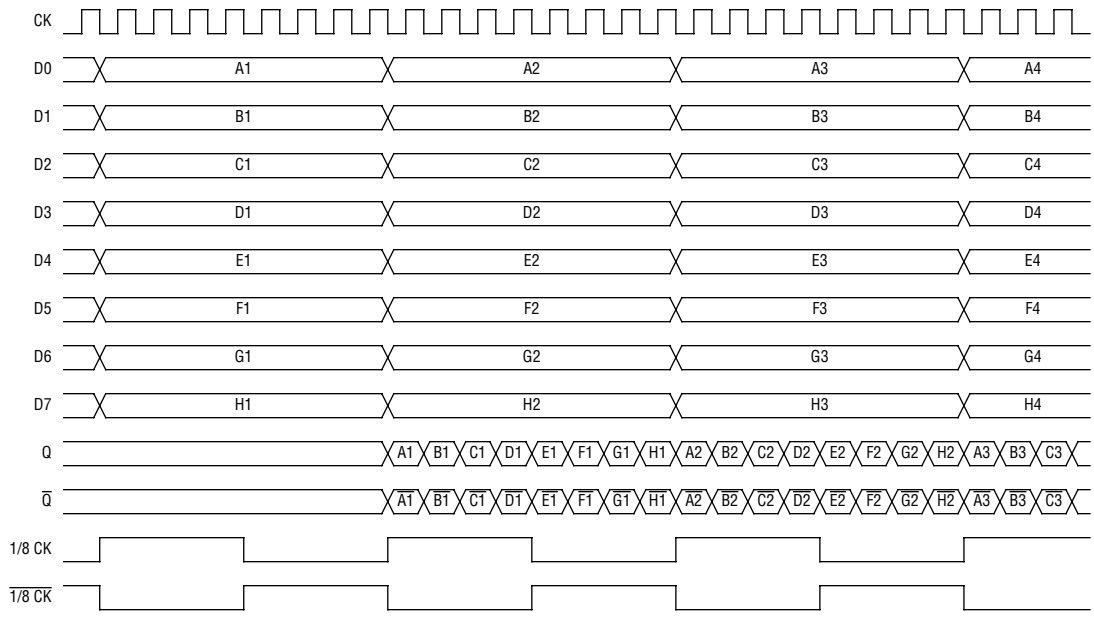
Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Power dissipation	P		–	2.4	3.0	W
High-level 1/8 CK output voltage	V_{OH}		0.85		1.3	V
Low-level 1/8 CK output voltage	V_{OL}		0		0.3	V
Data output voltage swing	V_{OD}	50-Ω load	0.7		1.2	V_{P-P}
Clock input voltage swing	V_{CK}	Capacitive coupling	0.5		0.9	V_{P-P}
High-level data input voltage	V_{IDH}		0.8		1.3	V
Low-level data input voltage	V_{IDL}		0		0.3	V

AC CHARACTERISTICS

V_{DD} = 2V ±0.1V, VB=2V ±0.1V Ts = 0 to 70°C

Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Minimum clock period	Δt_C		–	–	100	ps
Setup time (Data to 1/8 CK ↓)	t_{PS}		450	500	550	ps
Hold time (1/8 CK ↓ to Data)	t_{DH}		-400	-350	-300	ps
CK-D[7:0] phase margin	Δt_M	Input clock period is 100 ps	550	650		ps
Rise time (Q, $\overline{Q}$)	t_R		20	30	40	ps
Fall time (Q, $\overline{Q}$)	t_F		20	30	40	ps

INTERFACE TIMING



Oki Semiconductor

KGL4202

10-GHz 1:8 Demultiplexer

GENERAL DESCRIPTION

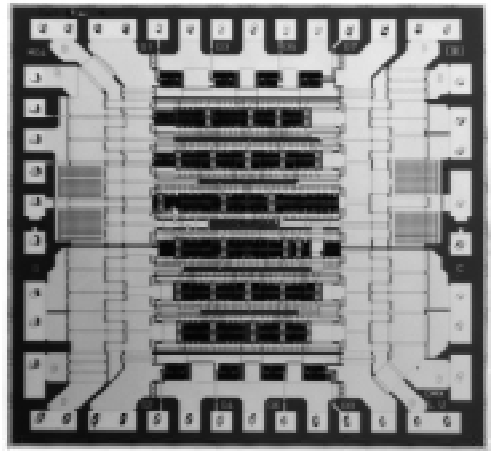
Oki's KGL4202 is a 10-GHz 1:8 demultiplexer designed to operate in 10-Gbps communication links. This circuit synchronously separates a single 10-Gbps data stream, clocked at up to 10 GHz, into eight lower frequency data streams, clocked at lower frequency rates. In the KGL4202 demultiplexer, the 10-GHz master clock is first divided by two, then by four. The 10-Gbps data stream is first divided into two synchronous serial paths, then these two data streams are separated into four each lower speed data streams and brought out to data latched outputs. Complementary 1/8 synchronous clock outputs are made available from the KGL4202 for use in synchronizing lower frequency logic.

All signal interfaces are 50 Ω with all inputs internally terminated in 50 Ω. Direct DC coupling is used on the 10-Gbps data input, the 1.25-Gbps data outputs and phase-locked 1.25-Gbps clock outputs. The 10-GHz clock input is AC-capacitively-coupled for ease of interfacing at microwave speeds and reducing ground noise induced phase jitter. The package 10-GHz clock and 10-Gbps data pins are separated by ground pins to control the I/O impedance, maintain signal isolation and reduce phase noise. The eight data outputs are distributed to opposite sides of the package to facilitate hardware layout and reduce noise. Over one third of the chip power is due to the ten 50-Ω outputs.

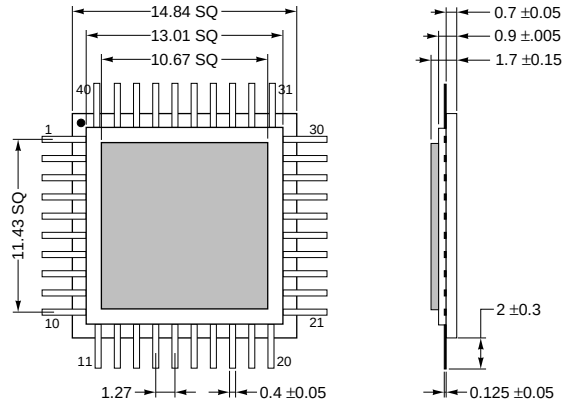
The KGL4202 is shipped in a 40-pin ceramic flat-package with impedance-controlling ground plane and flush-mounting bottom heat sink.

FEATURES

- AC-coupled 10 Gbps I/O: eliminates DC coupled phase jitter
- 1/8 clock generated on chip: easy to synchronize downstream logic
- Isolated I/O pins: minimizes noise and impedance variation
- 2 V, 3.2 W
- Packaged in 40-pin ceramic flat-package with ground plane and heat sink



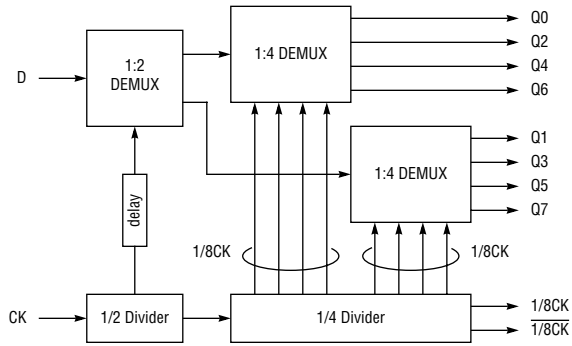
PIN CONFIGURATION



Pin Configuration

Pin	Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	GND	11	GND	21	VDD	31	GND
2	$\overline{1/8CK}$	12	VDD	22	GND	32	VDD
3	GND	13	Q1	23	GND	33	Q6
4	1/8CK	14	GND	24	CKIN	34	GND
5	RD	15	Q3	25	GND	35	Q4
6	GND	16	Q5	26	GND	36	Q2
7	N.C.	17	GND	27	RCK	37	GND
8	GND	18	Q7	28	GND	38	Q0
9	GND	19	VB	29	GND	39	VB
10	VB	20	GND	30	VB	40	VDD

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rated Value		Unit
		Min.	Max.	
Supply voltage for internal logic	V_{DD}	-0.3	2.3	V
Supply voltage for output buffer	V_B	-0.3	2.3	V
Clock input	CK	-0.3	1.5	V
Data inputs	D	-0.3	1.5	V
Temperature at package base under bias	T_S	-45	100	°C
Storage temperature	T_{ST}	-45	125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rated Value			Unit
		Min.	Typ.	Max.	
Power supply voltage for internal logic	V_{DD}	1.9	2.0	2.1	V
Power supply voltage for output buffer	V_B	1.9	2.0	2.1	V
Operating temperature range at package base	T_S	0	–	70	°C

DC CHARACTERISTICS

V_{DD} = 2 V ±0.1 V, VB=2 V ±0.1 V T_S = 0 to 70°C

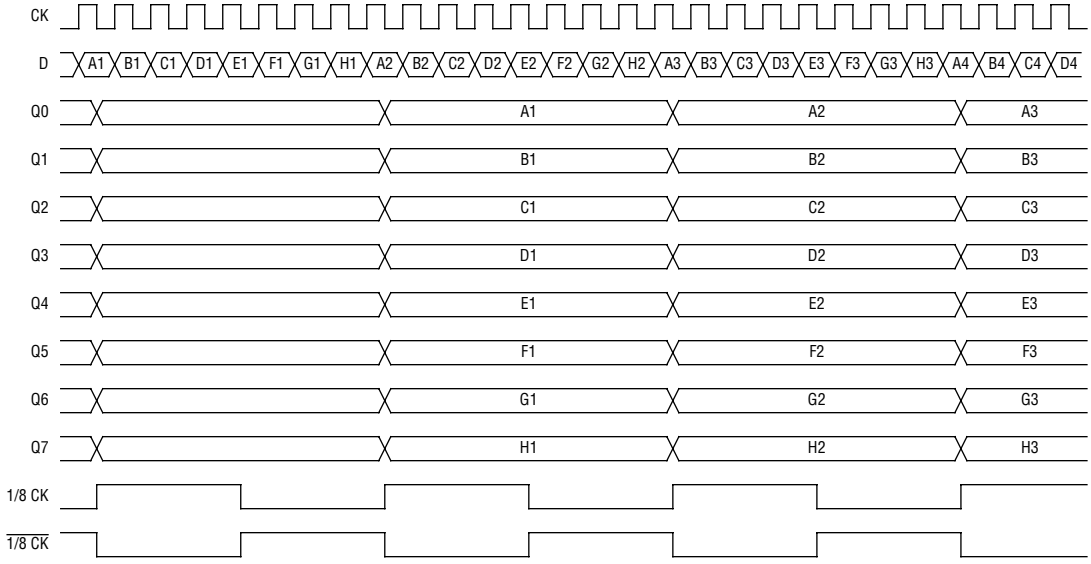
Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Power dissipation	P			3.2	4.0	W
High-level 1/8CK output voltage	V_{OH}	50-Ω load	0.85		1.3	V
Low-level 1/8CK output voltage	V_{OL}	50-Ω load	0		0.3	V
Data input voltage swing	V_{ID}	Capacitive coupling	0.5		0.9	V_{P-P}
Clock input voltage swing	V_{ICK}	Capacitive coupling	0.5		0.9	V_{P-P}

AC CHARACTERISTICS

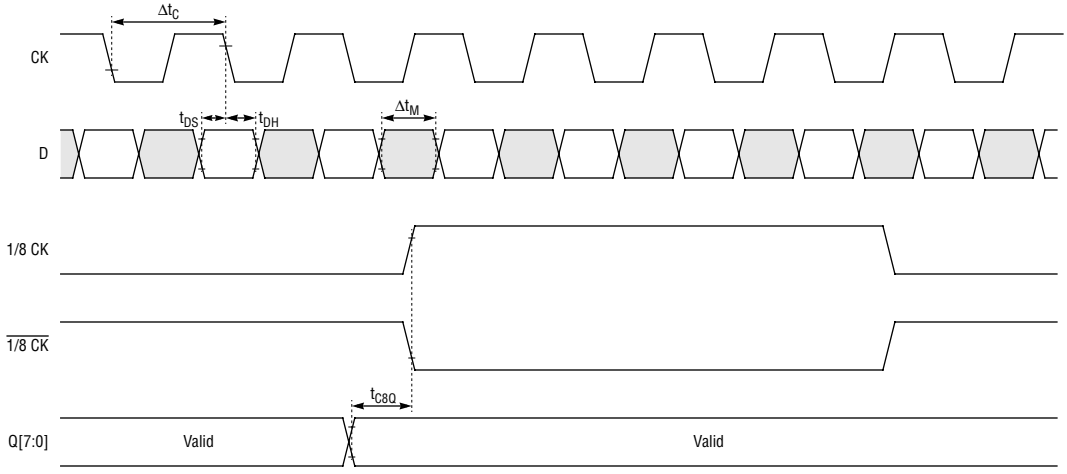
V_{DD} = 2V ±0.1V, VB=2V ±0.1V Ts = 0 to 70°C

Parameter	Symbol	Test Condition	Rated Value			Unit
			Min.	Typ.	Max.	
Minimum clock period	Δt_C				100	ps
Setup time (D to CK ↓)	t_{DS}		-55	-45	-35	ps
Hold time (CK ↓ to D)	t_{DH}		70	80	90	ps
CK-D phase margin	Δt_M	Input clock period is 100 ps	50	65		ps
1/8CK ↑ to valid data delay	t_{C8Q}		-40	-10	20	ps

INTERFACE TIMING



TIMING



Oki Semiconductor

GHDD4411

EX-OR Circuit

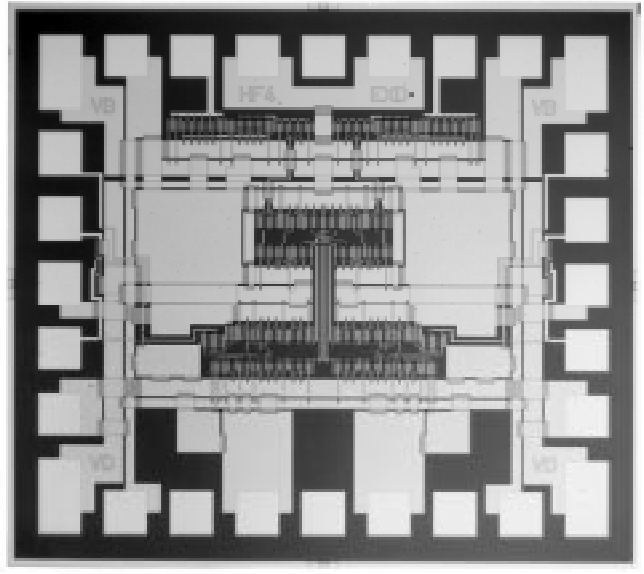
GENERAL DESCRIPTION

Oki's GHDD4411 is a 10-GHz exclusive-OR/NOR circuit designed to function in 10-Gbps high-speed communication serial bit streams. The EX-OR must operate from both rising and falling edges at an equivalent speed of 20-Gbps non-return-to-zero (NRZ) signal to extract a 10-Gbps clock from a 10-Gbps signal. Using closely matched Gilbert cell circuitry, this device operates at over 10 Gbps using DCFL and SBFL logic from inverted HEMT technology. Internal input 50-Ω terminations and a self-referencing bias voltage allow capacitive coupling, simplifying interconnections.

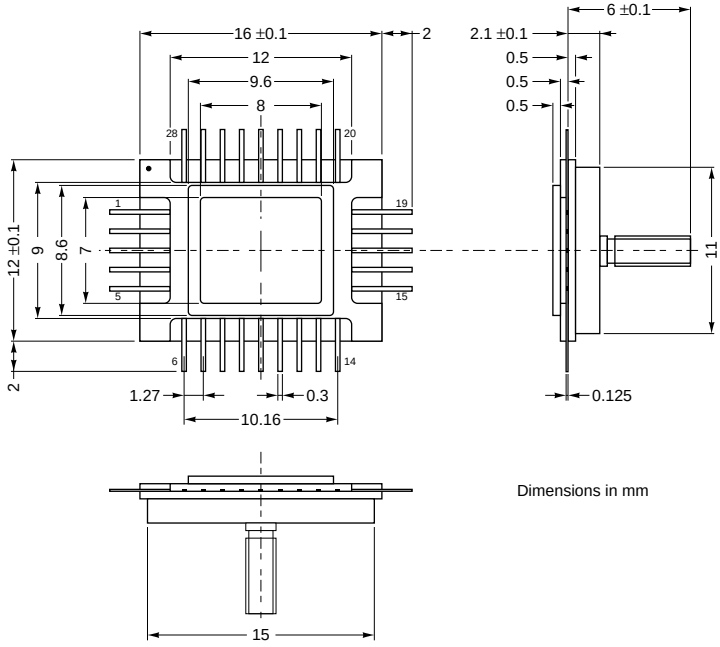
The GHDD4411 EX-OR circuit is high-speed in a 28-pin ceramic flat package with impedance-controlling ground plane and flush-mounting bottom heat sink.

FEATURES

- EX-OR and EX-NOR: outputs optimized for performance
- 1.5 V, 0.6 W: lowest power with 50-Ω interfaces
- Packaged in 28-pin ceramic flat package with ground plane and heat sink



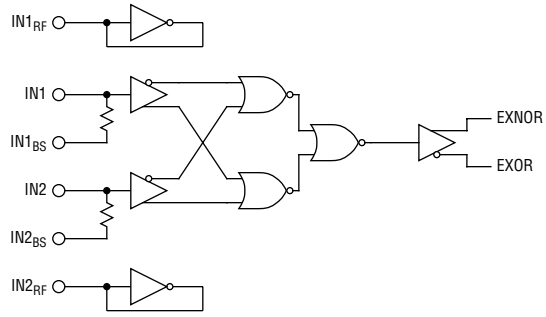
PIN CONFIGURATION



Dimensions in mm

Pin	Signal	Function	Pin	Signal	Function
1	IN1BS	Input 1 bias input	15	VB	Power supply (buffer)
2	N.C.	No Connect	16	N.C.	No Connect
3	IN1RF	Input 1 bias reference output	17	IN2RF	Input 2 bias reference output
4	N.C.	No Connect	18	N.C.	No Connect
5	VB	Power supply (buffer)	19	IN2BS	Input 2 bias input
6	GND	Ground	20	GND	Ground
7	EXOR	EX-OR output	21	IN2	Data input 2
8	GND	Ground	22	GND	Ground
9	N.C.	No Connect	23	VD	Power supply (logic circuit)
10	N.C.	No Connect	24	N.C.	No Connect
11	N.C.	No Connect	25	VD	Power supply (logic circuit)
12	GND	Ground	26	GND	Ground
13	EXNOR	EX-NOR output	27	IN1	Data input 1
14	GND	Ground	28	GND	Ground

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Suuply voltage for internal logic	V_{DD}	-0.3	2.3	V
Supply voltage for outpu buffer	V_B	-0.3	2.3	V
Clock input	CK	-0.3	1.0	V
Data input	D	-0.3	1.0	V
Temperature at package base under bias	T_S	-45	100	℃
Storage temperature	T_{ST}	-45	125	℃

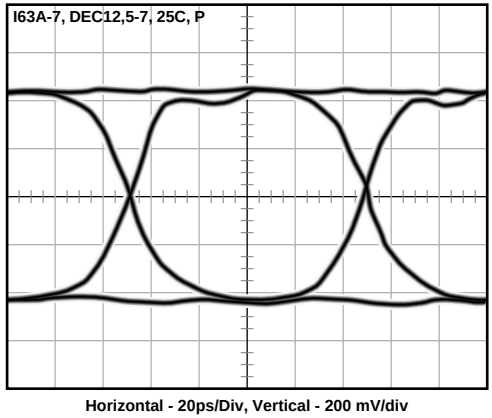
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Suuply voltage for internal logic	V_{DD}	1.4	1.5	1.6	V
Supply voltage for output buffer	V_B	1.4	1.5	1.6	V
Operating temperature range at package base	T_S	0		70	℃

V_{DD} = 1.5 V ±0.1, V_B = 1.5 V ± 0.1, T_S = 0 to 70 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power dissipation	P			0.6		W
Input bit rate	B			10		Gb/s
Data input voltage amplitude	V_{ID}	Capacitive coupling	0.2		0.8	V_{P-P}
Data output voltage amplitude	V_{OD}	50-Ω load, Capacitive coupling		0.7		V_{P-P}
Data output rise/fall time	τ			20		ps

OUTPUT WAVEFORM



Horizontal - 20ps/Div, Vertical - 200 mV/div

Oki Semiconductor

GHDD4414

Decision Circuit with Phase Detectors

GENERAL DESCRIPTION

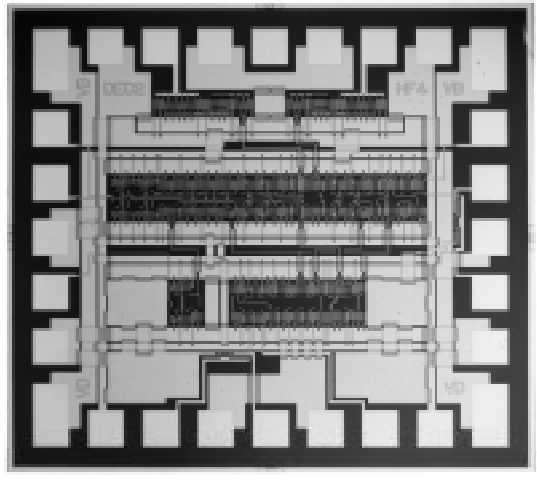
Oki's GHDD4414 is a 10-GHz decision circuit designed to strip data from high-speed serial bit streams in 10-Gbps communication links. Using a clock input at up to 10 GHz and using D-flip-flops, EX-ORs, and phase detectors, this circuit separates a 10-Gbps data stream into: clock output, data output, "phase" variation output, and data density output.

A 10-GHz master clock drives two D-flip-flops in this circuit. Buffered input data is clocked through the first flip-flop, then the second, "data out" is taken from the first flip-flop. The data input buffer is composed of a series of inverters to delay the signal and obtain a small decision ambiguity. A phase comparison is made of the buffered data and data from flip-flop one; a second phase comparison is made of the output of flip-flops one and two. The phase detectors are modified EX-OR circuits with resistor summing of the logic gates to permit analog measurement of their outputs. Any change in the timing relationships between the clock and data is seen at the output of the first phase detector. The second flip-flop operates as a 1-bit shift register with fixed 360-deg phase shift. The second phase detector output depends only upon the transition density (speed of rise and fall transitions) of the input data signal.

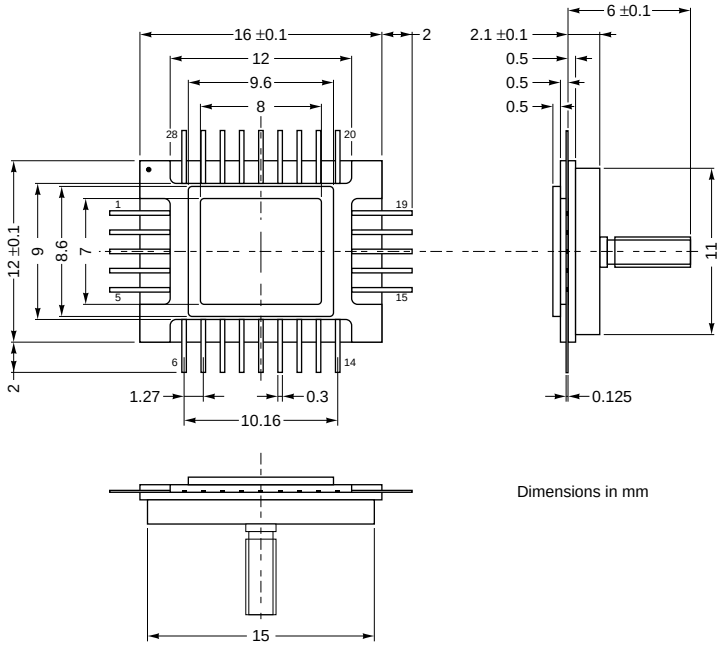
All signal interfaces are 50-Ω with all inputs internally terminated in 50 Ω. The 10-GHz clock and data inputs are AC capacitively-coupled for ease of interfacing at microwave speeds and reducing ground noise induced phase jitter. Data and phase outputs are DC-coupled.

FEATURES

- Phase detectors on chip: verifies data integrity
- Isolated 10-Gbps input pins: minimizes noise and impedance variation
- 1.5 V, 1 W: lowest power with 50-Ω interfaces
- 28-pin ceramic flat package with impedance controlling ground plane and flush mount heat sink



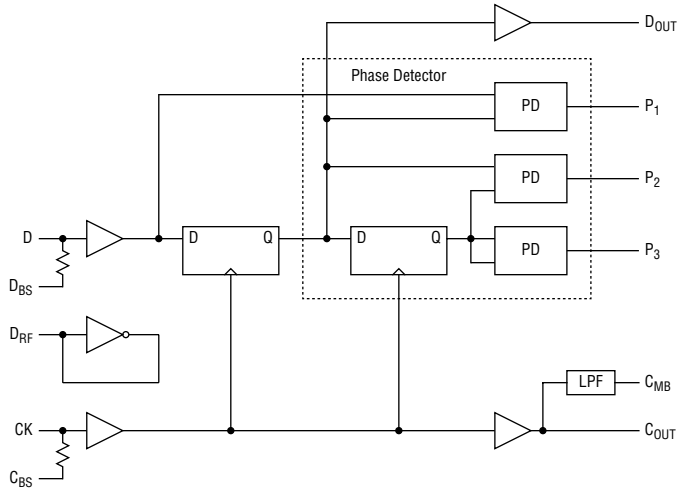
PIN CONFIGURATION



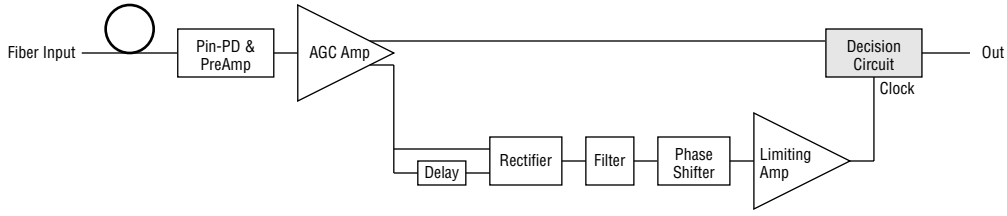
Dimensions in mm

Pin	Signal	Function	Pin	Signal	Function
1	C_{BS}	Clock bias input	15	V_B	Power supply (buffer)
2	NC		16	P1	Phase detector output
3	C_{MB}	Clock output duty monitor	17	P2	Phase detector ref. output 1
4	NC		18	P3	Phase detector ref. output 2
5	V_B	Powr supply (buffer)	19	V_D	Power supply (logic circuit)
6	GND		20	GND	
7	D_{OUT}	Data output	21	D_{IN}	Data input
8	GND		22	GND	
9	NC		23	D_{BS}	Data bias input
10	NC		24	D_{RF}	Data bias reference output
11	NC		25	V_D	Power supply (logic circuit)
12	GND		26	GND	
13	C_{OUT}	Clock output	27	CK	Clock input
14	GND		28	GND	

BLOCK DIAGRAM



APPLICATION BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

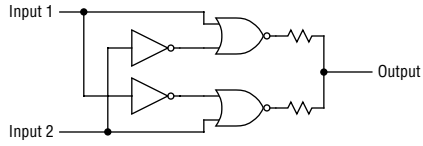
V_{DD} = 1.5 V ±0.1 V, V_B = 1.5 V ±0.1 V, T_S = 0° to 70°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Power dissipation	P			1	W
Decision ambiguity	V_{IDEC}	10 Gbps PRBS: 2^{15} -1		0.05	V_{P-P}
Phase margin	$\Delta\theta$		250		degree
Data input voltage amplitude	V_{ID}	Capacitive coupling		0.8	V_{P-P}
Clock input voltage amplitude	V_{IC}		0.4	0.8	V_{P-P}
Data output voltage amplitude	V_{OD}	50Ω load capacitive coupling	0.7		V_{P-P}
Clock output voltage amplitude	V_{OC}		0.7		V_{P-P}
Clock output duty cycle	D_{TYC}		40	60	%
Clock to data delay	τ_{CD}		25	45	ps
Phase detection sensitivity	$\Delta V\theta$	10 Gbps PRBS: 2^{15} -1	0.28		mV/degree

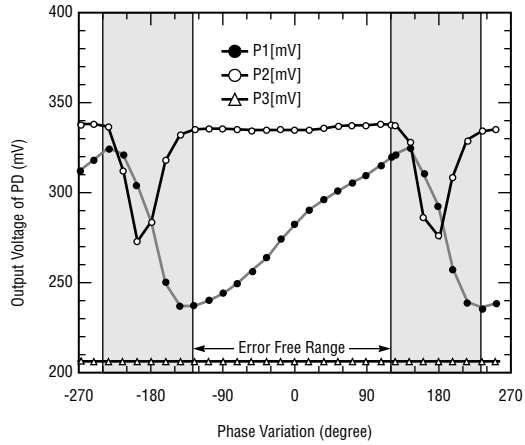
Phase Detection Characteristics (D_{IN} Amplitude = 0.7-V_{P-P})

CIN Delay (ps)	P1 (V)	P2 (V)	P3 (V)	Comments
+29	0.350	0.343	0.443	Maximum delay for ER <10^{-10}
0	0.383	0.340	0.443	Center of phase margin
-29	0.424	0.342	0.443	Minimum delay for ER <10^{-10}

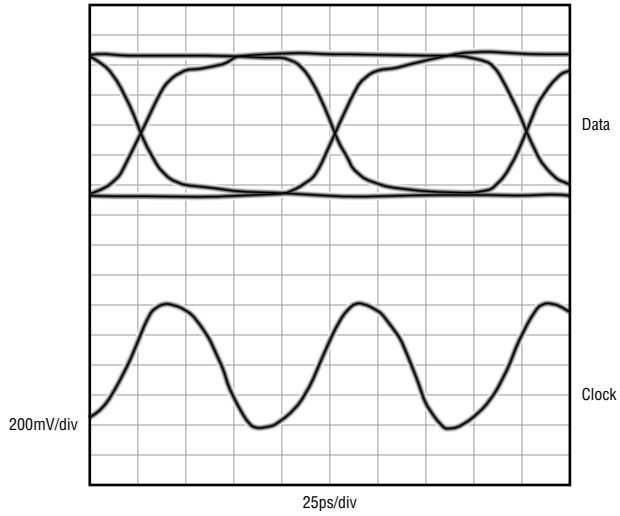
PHASE DETECTOR CIRCUIT



PHASE DETECTION BETWEEN SIGNAL AND CLOCK AT 10 Gbps



TIMING



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