

**Enhanced Multi-touch Capacitive Touch Screen Controller**

**AP389X**

**General Description**

The AP389X is a low-cost high-resolution single chip solution for APA capacitive touch screen. It is an 8-bit single cycle 8051 microcontroller with I<sup>2</sup>C Interface. The chip includes 8-bit successive approximation analog-to-digital converters with an I<sup>2</sup>C interface and multiplexer-switcher circuits for flexible measurement of analog signal from APA panel. An accurate switched-capacitor integrator is built-in and it can auto calibrate the pixel parameters for a wide range of capacitance on the touch screen (0.1pF to 4pF). On-chip capacitor can replace external component. This touch screen controller (TSC) with CMOS integration circuit provides an ideal choice for APA touch panel. The AP389X is specified over the temperature range of -40°C to 95°C.

The AP389X is available in QFN-7×7-56 (for AP3890) and QFN-8×8-68 (for AP3891 and AP3892) packages.

**Features**

- Mutual Capacitive Touch Sensing
- Dual Power Supply: 2.8V to 3.6V Operation Voltage; 1.6V to 2.0V Operation Voltage
- Up to 30/38/36 Drive Lines and 17/22/23 Sense Lines
- Dedicated Internal Two-wire Serial Control Bus I<sup>2</sup>C and UART between AP389X and Host
- Single-end Integrator with Programmable Gain Control and Offset Control
- Multiplexed Analog Digitization with Two 8-bit Resolution Odd/Even Scan SAR ADCs and Its Dedicated 2X to 8X Accumulator XSRAM Buffers

**Features (Continued)**

- Single Cycle 8051 CPU Core, Maximum Operating Clock up to 24MHz from IOSC (Zero Wait State); 48MHz from IOSC(With Wait State) 4MHz to 48MHz Internal Oscillator (IOSC) 64K-byte Flash ROM 256-byte Internal SRAM and 12032-byte XSRAM
- Extra XSRAMs for AFE:
  - ◆ 896×12-bit×2 XSRAM for 8-bit SAR ADC
  - ◆ 896×8-bit XSRAM for 8-bit Parasitital Capacitor Compensator
- Two 16-bit Timers T0/T1 and One 16-bit ECT Timer T2
- One I<sup>2</sup>C Slave Controller and One I<sup>2</sup>C Master Controller Shared with the Same Port
  - ◆ With Asynchronous I<sup>2</sup>C Slave Address Detection Logic Design
- 4 General Purpose GPIO Pins
- One External Interrupt Pin
- One UART Data Transfer Output Pin
- ISP/IAP via I<sup>2</sup>C Port
- Operation Temperature Range: -40°C to 95°C
- Package Types: QFN-7×7-56 and QFN-8×8-68
- RoHS Compliance
- Operating Mode:

Mode	Description
Power-down	No scan with power-down mode
Standard	Higher scan rate when fingers are on panel, IOSC can up to 4MHz to 48MHz

**Applications**

- Mobile Phones
- Personal Digital Assistants
- Smart Hand-held or Gaming Devices

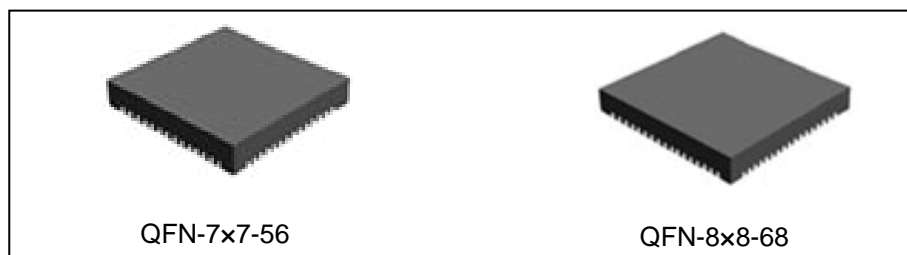


Figure 1. Package Types of AP389X

**Pin Configuration**

FN Package  
(QFN-7x7-56)

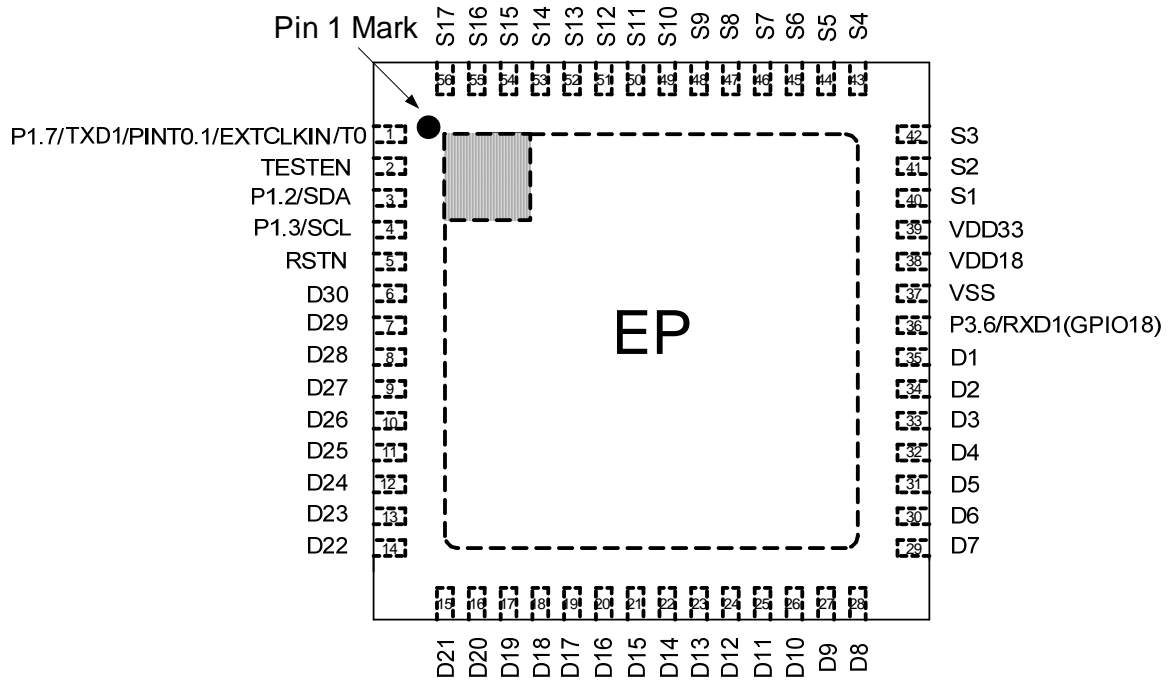


Figure 2. Pin Configuration of AP3890 (Top View)

**Pin Configuration (Continued)**

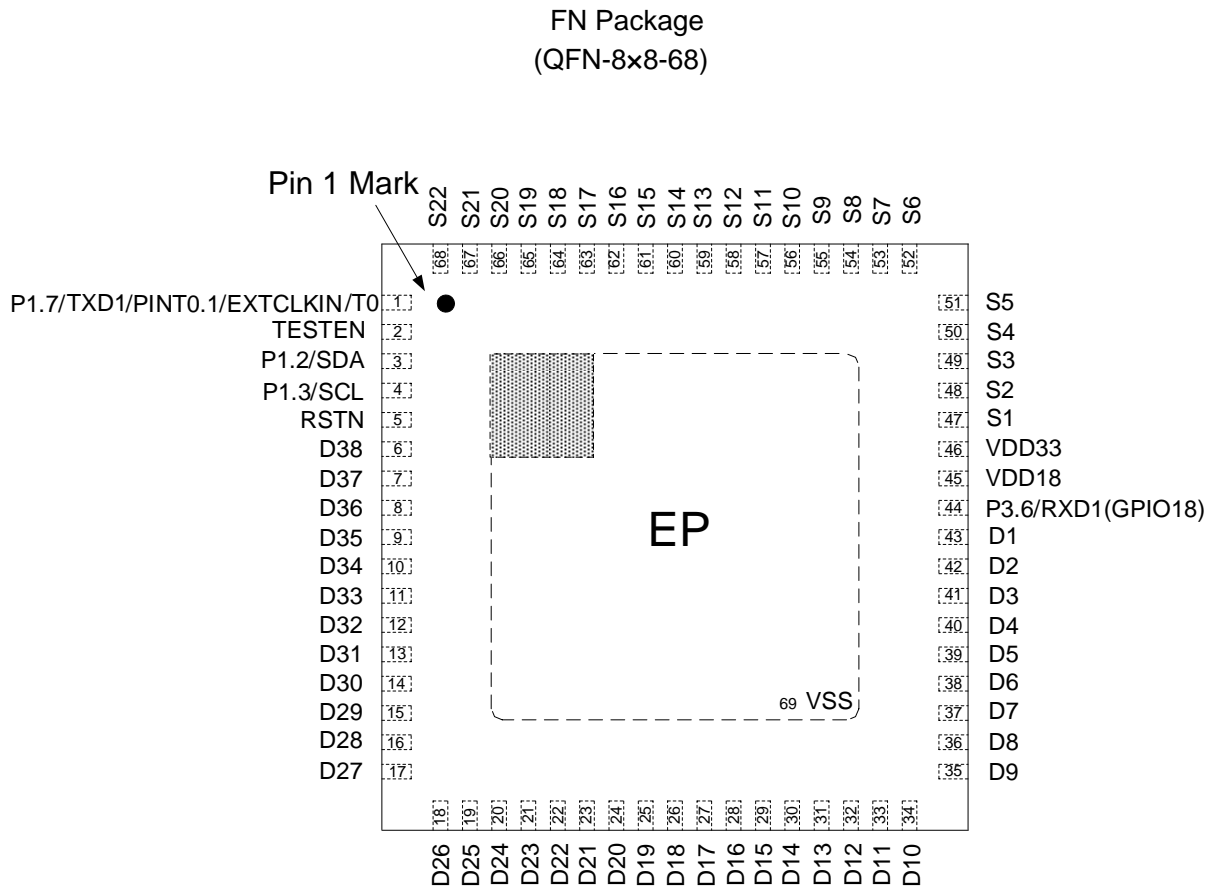


Figure 3. Pin Configuration of AP3891 (Top View)

**Pin Configuration (Continued)**

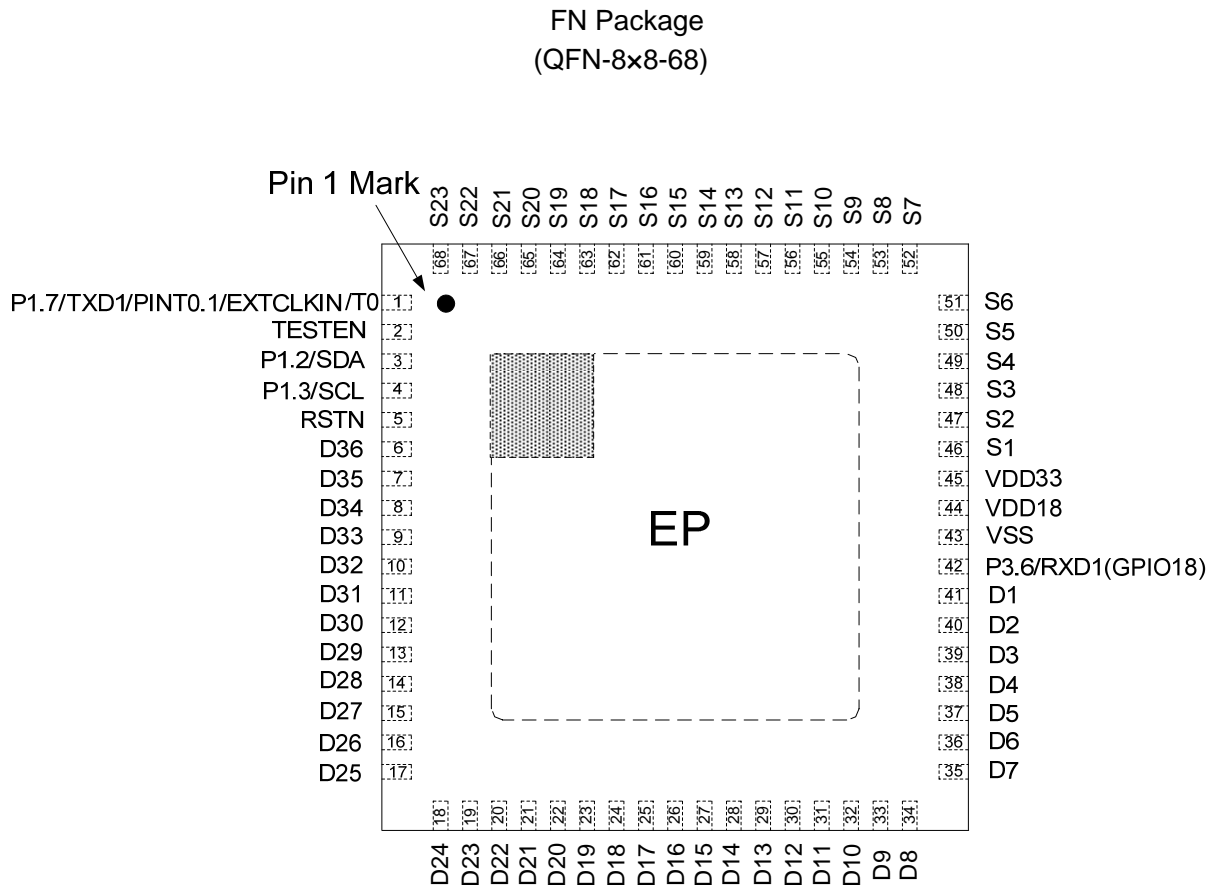


Figure 3. Pin Configuration of AP3892 (Top View)



**Enhanced Multi-touch Capacitive Touch Screen Controller AP389X**

**Pin Description**

Pin Number			Pin Name	Pin Type	Pin Function
QFN-56 AP3890	QFN-68				
	AP3891	AP3892			
1	1	1	P1.7/ TXD1/ PINT0.1/ EXTCLKIN/ T0	I/O	<b>Port 1.7 GPIO</b>
					8051 P1.7 GPIO
					<b>TXD1</b>
					This pin also can be configured as TXD of UART 1
					<b>PINT0.1</b>
					This pin also can be configured as the expanded INTO interrupt
					<b>External Clock Input</b>
					External clock input source.
					<b>T0 Timer 0 Input</b>
This pin also can be configured as Timer 0 input					
2	2	2	TESTEN	I	<b>Test Mode Enable High Active</b>
					This pin has an internal weakly pull low resistor connected. If it is connected high, the chip enters into Test Mode condition
3	3	3	P1.2/SDA (open-drain)	I/O	<b>Port 1.2 GPIO</b>
					8051 P1.2 GPIO
					<b>SDA</b>
					This pin also can be configured as the SDA signal of the I <sup>2</sup> C master or I <sup>2</sup> C slave controller. In this operation mode, this pin should also be configured as bi-directional I/O with open-drain output
4	4	4	P1.3/SCL (open-drain)	I/O	<b>Port 1.3 GPIO</b>
					8051 P1.3 GPIO
					<b>SCL</b>
					This pin also can be configured as the SCL signal of the I <sup>2</sup> C master or I <sup>2</sup> C slave controller. In I <sup>2</sup> C master mode, this pin should be configured as open-drain output. In I <sup>2</sup> C slave, this pin should be configured as input only
5	5	5	RSTN	I	<b>Reset Low Active</b>
					Typically connect a resistor to VDD18 and a capacitor to VSS
					Low asserted and threshold at $0.5 \times V_{DD18}$ . When forced low, the chip enters into reset condition
					This pin should not be connected to any level above $V_{DD18}$



**Enhanced Multi-touch Capacitive Touch Screen Controller**

**AP389X**

**Pin Description (Continued)**

Pin Number			Pin Name	Pin Type	Pin Function
QFN-56 AP3890	QFN-68				
	AP3891	AP3892			
-	6, 7	-	D38, D37	O, A	<b>D38, D37</b> Driving line 38 to line 37
-	8 to 13	6 to 11	D36 to D31	O, A	<b>D36, D35, D34, D33, D32, D31</b> Driving line 36 to line 31
6 to 35	14 to 43	12 to 41	D30 to D1	O, A	<b>D30, D29, D28, D27, D26, D25, D24, D23, D22, D21, D20, D19, D18, D17, D16, D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1</b> Driving line 30 to line 1
36	44	42	P3.6/ RXD1 (open- drain)	I/O	<b>Port 3.6 GPIO</b> 8051 P3.6 GPIO This pin should be configured as open-drain output and the input range can be 1.8V to 3.3V <b>RXD1</b> This pin also can be configured as RXD of UART 1
37	69	43	VSS	Power	<b>Ground Voltage. 0V</b>
38	45	44	VDD18	Power	<b>Internal Regulator Output. 1.6V to 2.0V</b> Typical decoupling capacitors of 0.1μF and 10μF should be connected between VDD18 and VSS
39	46	45	VDD33	Power	<b>Supply Voltage. 2.8V to 3.6V</b> A good decoupling capacitor between VDD33 and VSS is critical for good performance
40 to 56	47 to 63	46 to 62	S1 to S17	I, A	<b>S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, S16, S17</b> Sensing line 1 to line 17
-	64 to 68	63 to 67	S18 to S22	I, A	<b>S18, S19, S20, S21, S22</b> Sensing line 18 to line 22
-	-	68	S23	I, A	<b>S23</b> Sensing line 23

**Functional Block Diagram**

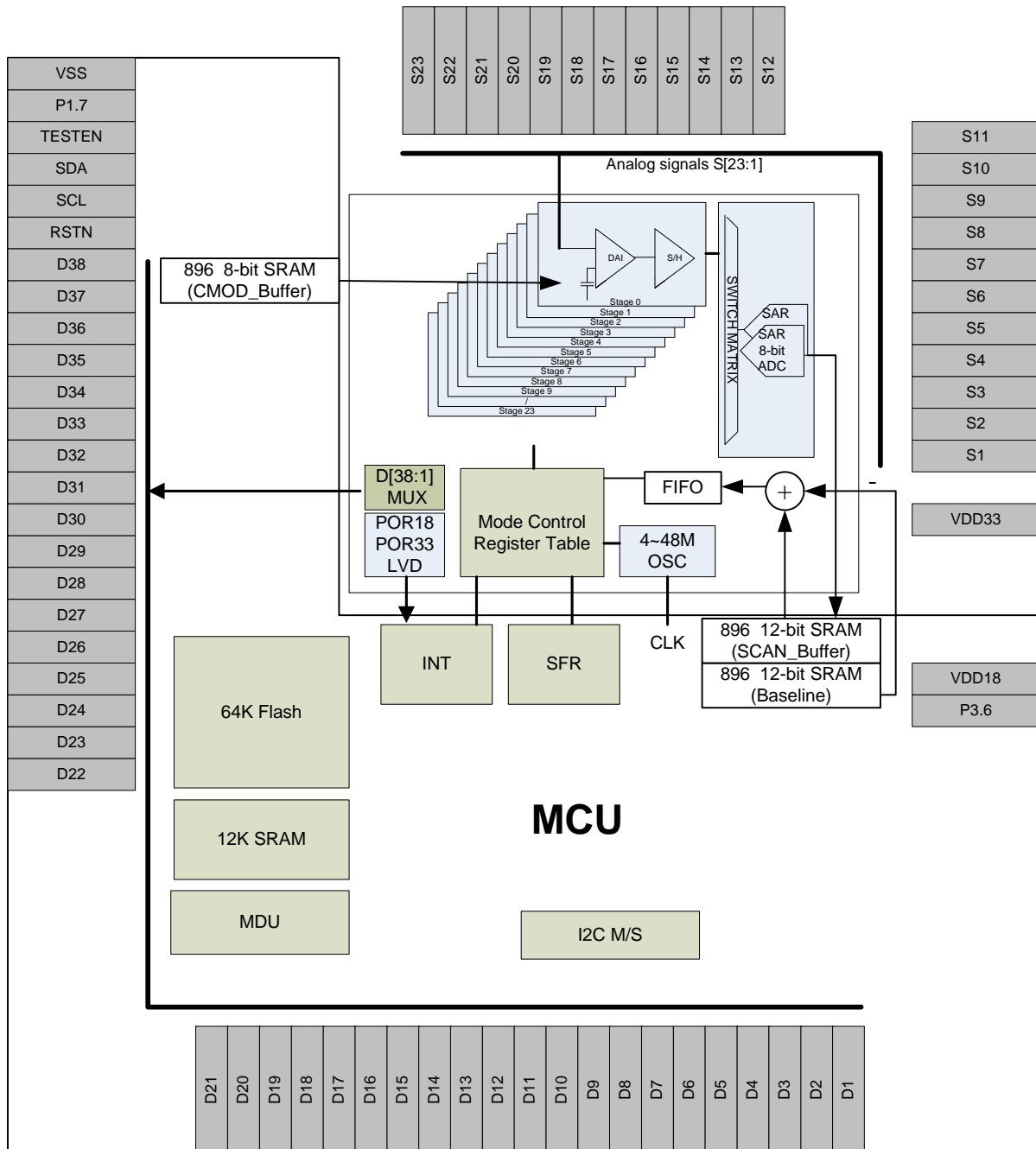
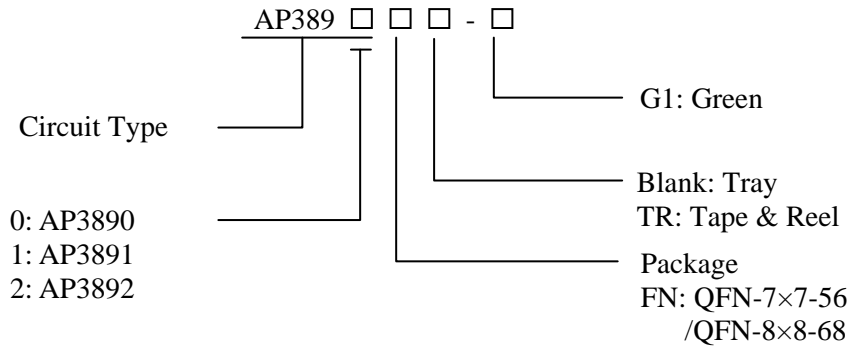


Figure 4. Main AFE I/O Pin Assignment and Whole Chip's Functional Block Diagram

**Enhanced Multi-touch Capacitive Touch Screen Controller**

**AP389X**

**Ordering Information**



Package	Temperature Range	Part Number	Marking ID	Packing Type
QFN-7x7-56	-40 to 95°C	AP3890FN-G1	AP3890FN-G1	Tray
		AP3890FNTR-G1	AP3890FN-G1	Tape & Reel
QFN-8x8-68		AP3891FN-G1	AP3891FN-G1	Tray
		AP3891FNTR-G1	AP3891FN-G1	Tape & Reel
QFN-8x8-68		AP3892FN-G1	AP3892FN-G1	Tray
		AP3892FNTR-G1	AP3892FN-G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" in the part number, are RoHS compliant and green.



**Enhanced Multi-touch Capacitive Touch Screen Controller****AP389X****AP389X Support 7” to 13” Touch Panel, Listed Below:**

PN	TX/ RX	Multi - Touch	Package	Panel size
AP3890	30/17	10 point 100HZ	QFN-7x7-56	7” to 10”
AP3891	38/22	10 point 100HZ	QFN-8x8-68	8” to 13”
AP3892	36/23	10 point 100HZ	QFN-8x8-68	8” to 13”

**Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value	Unit
Supply Voltage 1	$V_{DD}$	2.8 to 3.6	V
Supply Voltage 2	$V_{DD18}$	1.6 to 2.0	V
Analog Input Voltage (Other pins)	$V_{DDA}$	-0.3 to $V_{DD}+0.3$	V
Logic Input Voltage	$V_{DDD}$	-0.3 to $V_{DD}+0.3$	V
Power Dissipation	$P_D$	250	mW
Maximum Junction Temperature	$T_J$	100	°C
Operating Temperature	$T_{OP}$	-40 to 95	°C
Storage Temperature	$T_{STG}$	-65 to 150	°C

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.



**Enhanced Multi-touch Capacitive Touch Screen Controller**

**AP389X**

**Electrical Characteristics**

**DA/AC Characteristics for AFE**

T<sub>A</sub>=-40°C to 95°C, V<sub>DD</sub>=3.3V, I<sup>2</sup>C bus frequency=400kHz, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>ADC DC Accuracy</b>						
Resolution					8	Bits
No Missing Codes		Standard/Fast	6	8		Bits
Integral Linearity Error	INL	Standard/Fast		±2		LSB
Differential Linearity Error	DNL	External V <sub>REF</sub>		±1	±2	LSB
Offset Error						LSB
Gain Error						LSB
<b>Analog Input</b>						
Full-scale Input Span			0		V <sub>DD</sub>	V
Absolute Input Range			-0.2		V <sub>DD</sub> +0.2	V
<b>ADC Sampling Dynamics</b>						
Throughput Rate				500		ksps
<b>Reference Input</b>						
Input Voltage Range			1.8		V <sub>DD</sub>	V
<b>Switched-capacitor Integrator</b>						
Output Voltage Range			0.3		V <sub>DD</sub> -0.3	V
Integrator Capacitor	C <sub>INT</sub>			12		pF
<b>Digital Input/Output</b>						
Logic Family				CMOS		
Input High Voltage	V <sub>IH</sub>		0.7×V <sub>DD</sub>		V <sub>DD</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>		-0.3		0.3×V <sub>DD</sub>	V
Output High Voltage	V <sub>OH</sub>		0.8×V <sub>DD</sub>			V
Output Low Voltage	V <sub>OL</sub>				0.4	V
Input High Voltage for P3.6 (GPIO18)	V <sub>IH18</sub>		0.7×V <sub>DD18</sub>		V <sub>DD18</sub> +0.3	V
Input Low Voltage for P3.6 (GPIO18)	V <sub>IL18</sub>		-0.3		0.3×V <sub>DD18</sub>	V
Output High Voltage for P3.6 (GPIO18)	V <sub>OH18</sub>		0.8×V <sub>DD18</sub>			V
Output Low Voltage for P3.6 (GPIO18)	V <sub>OL18</sub>				0.2×V <sub>DD18</sub>	V
<b>Power Supply</b>						
Supply Voltage	V <sub>DD</sub>	Operating voltage	2.8		3.6	V
Quiescent Current		Standard mode: IOSC=4MHz to 48MHz		TBD		mA
		Power-down mode		10		µA
<b>Temperature Range</b>						
Specified Performance			-40		95	°C

**Enhanced Multi-touch Capacitive Touch Screen Controller****AP389X****Electrical Characteristics (Continued)****DA/AC Characteristics for AFE** $T_A = -40^{\circ}\text{C}$  to  $95^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V}$ , I<sup>2</sup>C bus frequency = 400kHz, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>3.3V-to-1.8V LDO</b>						
Internal 1.8V Regulator Output	$V_{DD18}$ , 15mA		1.6	1.8	2.0	V
Output Voltage Trimming Level			-2/4/6	0	2/4/6	%
<b>Internal OSC</b>						
Frequency			4		48	MHz
Operating Current		Operating frequency=12MHz		50		$\mu\text{A}$
Frequency Trimming Level			-10/20/30	0	10/20/30	%

**Enhanced Multi-touch Capacitive Touch Screen Controller****AP389X****Electrical Characteristics (Continued)****DA/AC Characteristics for 8051 CPU Core, Digital GPIO pins, Digital Peripherals, and IOSC**T<sub>A</sub>=-40°C to 95°C, V<sub>DD</sub>=2.8V to 3.6V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Note
<b>Power Supply Current</b>						
Normal Mode Supply Current Using IOSC up to 48MHz	I <sub>DD</sub> , normal IOSC1			25	mA	2
Normal Mode Supply Current Using IOSC=4MHz	I <sub>DD</sub> , normal IOSC2		2.9		mA	2
PMM Mode Supply Current Using IOSC up to 48MHz	I <sub>DD</sub> , PMM IOSC1		6		mA	2
PMM Mode Supply Current Using IOSC=4MHz	I <sub>DD</sub> , PMM IOSC2		1.5		mA	2
Idle Mode Supply Current Using IOSC up to 48MHz	I <sub>DD</sub> , idle IOSC1		3		mA	2
Stop Mode Supply Current Using IOSC Keeps Low	I <sub>DD</sub> , stop		3		μA	2
<b>Digital GPIO Characteristics</b>						
Input High Voltage	V <sub>IH</sub>	2		3.6	V	3
Input Low Voltage	V <sub>IL</sub>	-0.3		0.8	V	3
Output High Voltage	V <sub>OH</sub>	2.4			V	3
Output Low Voltage	V <sub>OL</sub>			0.4	V	3
High Level Output Current @V <sub>OH</sub> (min)	I <sub>OH</sub> (2mA)	3.0	7.87	12.9	mA	
	I <sub>OH</sub> (4mA)	7.7	15.6	25.8	mA	
Low Level Output Current @V <sub>OL</sub> (max)	I <sub>OL</sub> (2mA)	3.4	5.4	7.4	mA	
	I <sub>OL</sub> (4mA)	6.7	10.7	14.7	mA	
Input Pull Up Resistance	R <sub>PU</sub>	34		74	kΩ	3
Input Pull Down Resistance	R <sub>PD</sub>	29		86	kΩ	3
Input Low to High Level, RSTN	V <sub>IH</sub> , RSTN	0.85		0.93	V	4
Input High to Low Level, RSTN	V <sub>IL</sub> , RSTN	0.63		0.71	V	4
Output Rise Time	t <sub>RISE</sub>		5		ns	7
Output Fall Time	t <sub>FALL</sub>		5		ns	7
<b>Internal 3.3V-to-1.8V LDO from AFE</b>						
Internal 1.8V Regulator Output	V <sub>DD18</sub> , 15mA	1.6	1.8	2.0	V	5
Power On/Off Reset Level	V <sub>DD18</sub> , Reset	80	85	90	%	6

Note 2: Does not include load current and tested under NOP loop and all peripheral disabled.

Note 3: For Digital I/O only.

Note 4: For RSTN pin only.

Note 5: Supply to internal digital and analog circuit only.

Note 6: This is measured as the percentage of steady state value of V<sub>DD18</sub>.

Note 7: This is measured with 20pF load and 20% to 80% output level.

**Enhanced Multi-touch Capacitive Touch Screen Controller**

**AP389X**

**Typical Application**

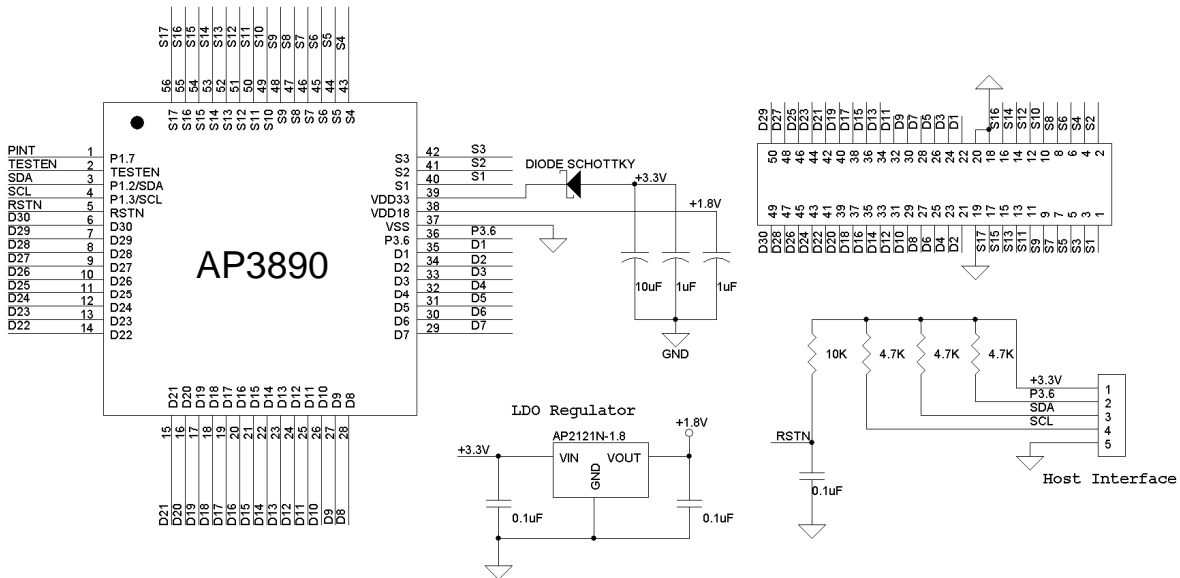


Figure 5. Typical Application Schematic of AP3890 (For QFN-7x7-56 Package)

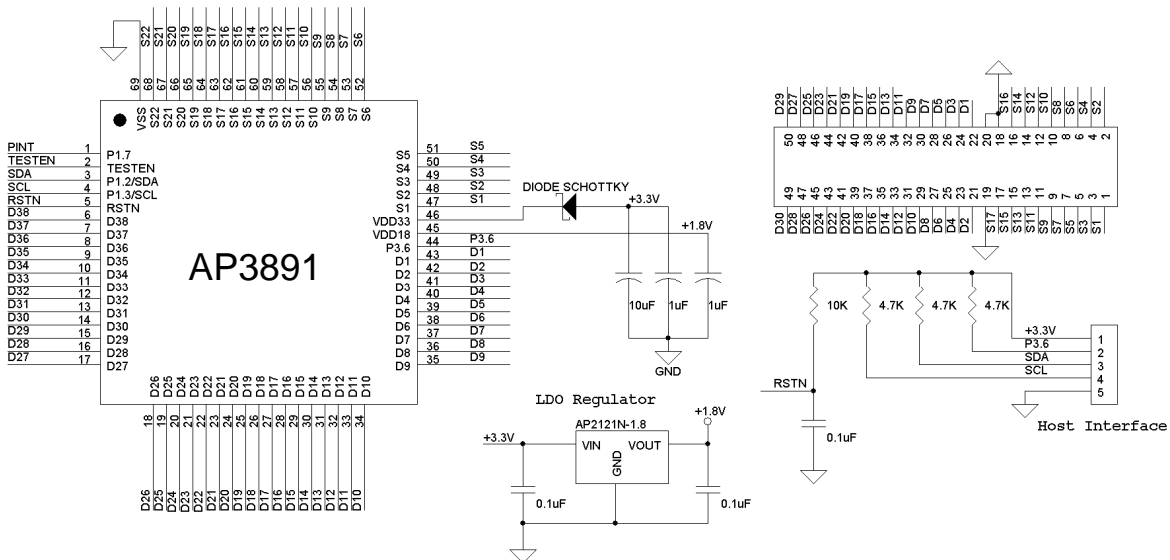


Figure 6. Typical Application Schematic of AP3891 (For QFN-8x8-68 Package)

**Enhanced Multi-touch Capacitive Touch Screen Controller**

**AP389X**

**Typical Application (Continued)**

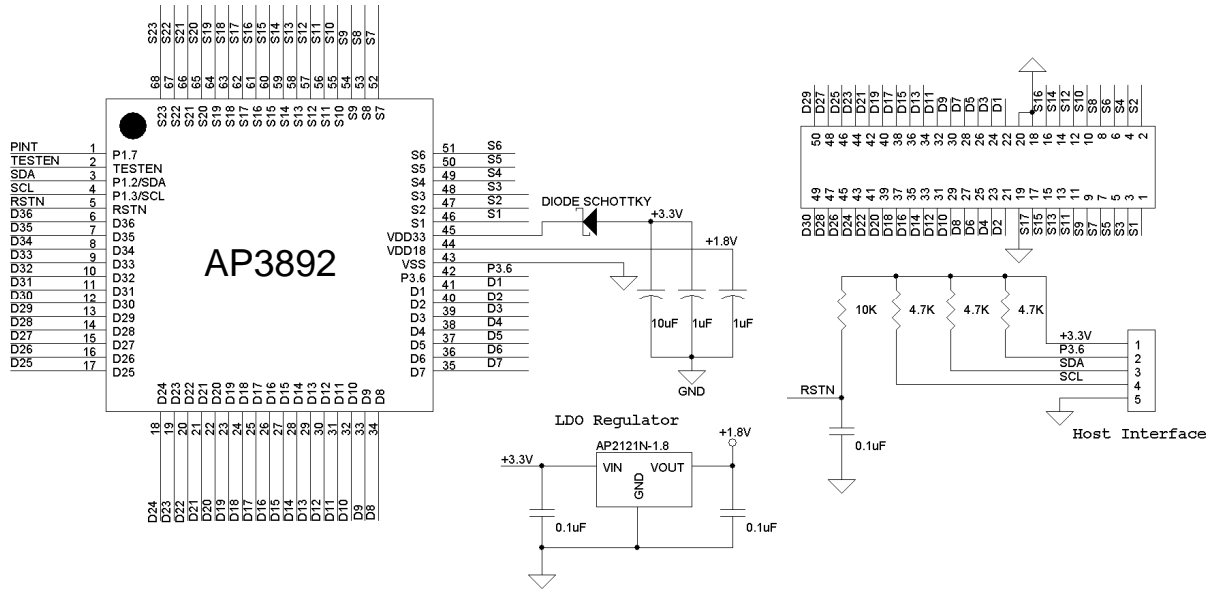


Figure 7. Typical Application Schematic of AP3892 (For QFN-8x8-68 Package)

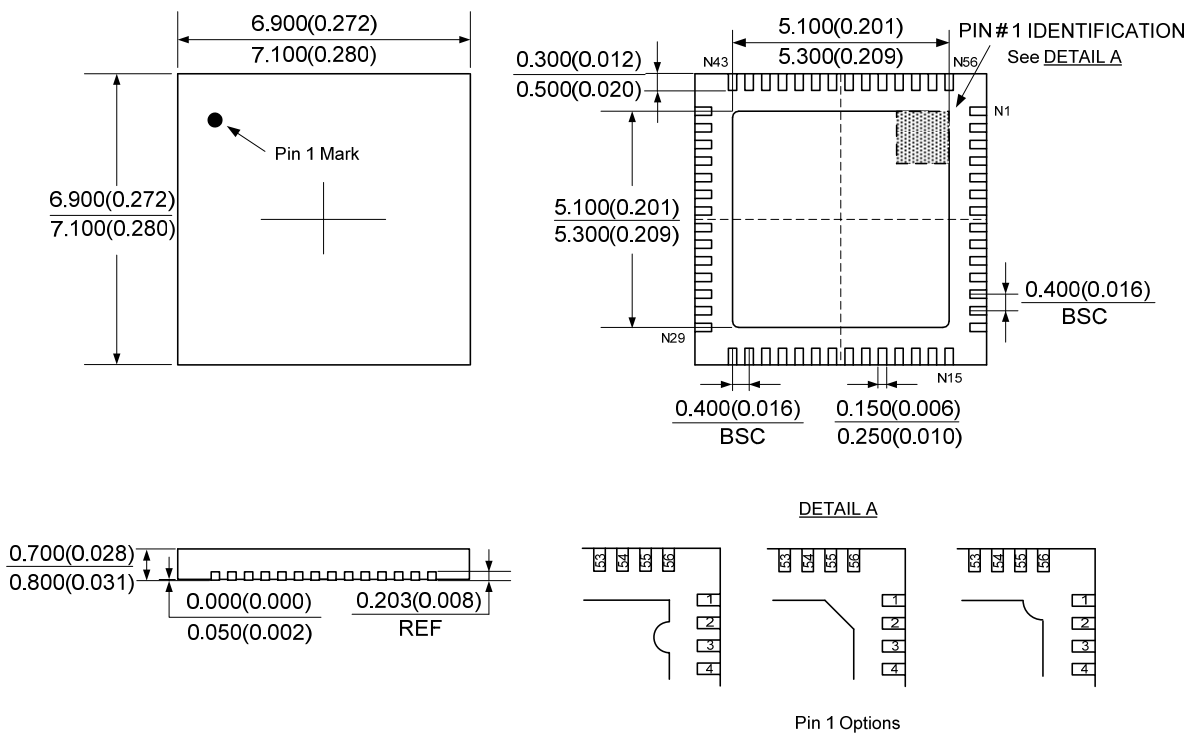
**Enhanced Multi-touch Capacitive Touch Screen Controller**

**AP389X**

**Mechanical Dimensions**

**QFN-7x7-56**

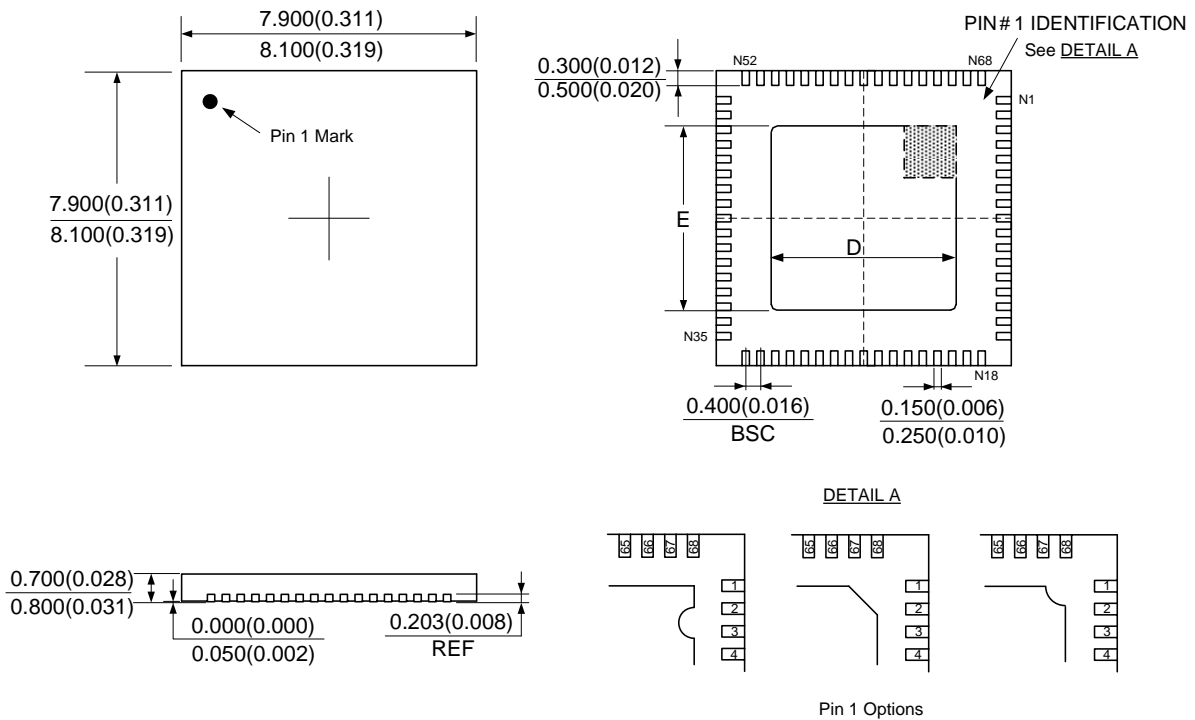
**Unit: mm(inch)**



**Mechanical Dimensions (Continued)**

**QFN-8x8-68**

**Unit: mm(inch)**

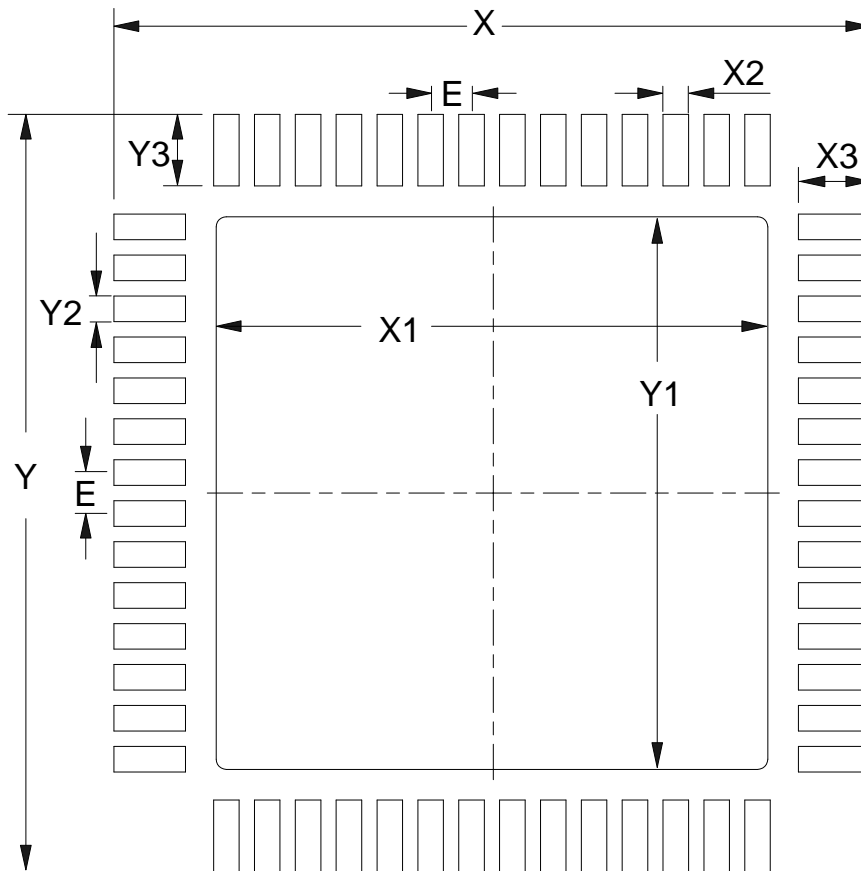


Symbol	D				E			
	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)
Option1	4.300	4.500	0.169	0.177	4.300	4.500	0.169	0.177
Option2	5.400	5.600	0.213	0.220	5.400	5.600	0.213	0.220
Option3	6.100	6.300	0.240	0.248	6.100	6.300	0.240	0.248



**Mounting Pad Layout**

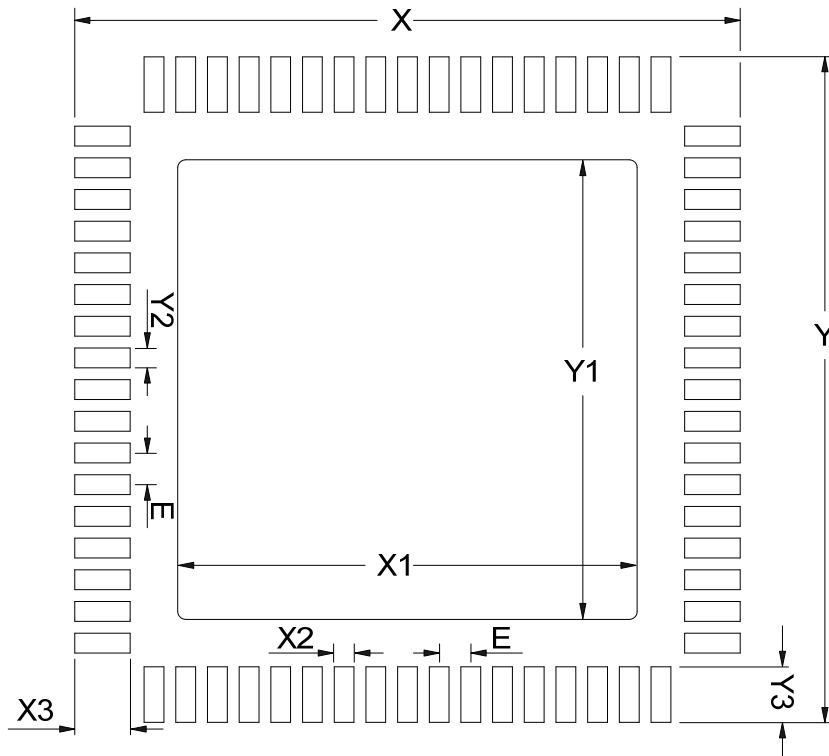
**QFN-7x7-56**



Dimensions	X=Y (mm)/(inch)	X1=Y1 (mm)/(inch)	X2=Y2 (mm)/(inch)	X3=Y3 (mm)/(inch)	E (mm)/(inch)
Value	7.400/0.291	5.400/0.213	0.250/0.010	0.700/0.028	0.400/0.016

**Mounting Pad Layout (Continued)**

**QFN-8x8-68**



Dimensions	X=Y (mm)/(inch)	X1=Y1 (mm)/(inch)	X2=Y2 (mm)/(inch)	E (mm)/(inch)	X3=Y3 (mm)/(inch)
Option1	8.400/0.331	4.700/0.185	0.250/0.010	0.400/0.016	0.700/0.028
Option2	8.400/0.331	5.800/0.228	0.250/0.010	0.400/0.016	0.700/0.028
Option3	8.400/0.331	6.500/0.256	0.250/0.010	0.400/0.016	0.700/0.028



## BCD Semiconductor Manufacturing Limited

<http://www.bcdsemi.com>

### IMPORTANT NOTICE

BCD Semiconductor Manufacturing Limited reserves the right to make changes without further notice to any products or specifications herein. BCD Semiconductor Manufacturing Limited does not assume any responsibility for use of any its products for any particular purpose, nor does BCD Semiconductor Manufacturing Limited assume any liability arising out of the application or use of any its products or circuits. BCD Semiconductor Manufacturing Limited does not convey any license under its patent rights or other rights nor the rights of others.

---

#### MAIN SITE

##### - Headquarters

##### BCD (Shanghai) Micro-electronics Limited

No. 1600, Zi Xing Road, Shanghai ZiZhu Science-based Industrial Park, 200241, P. R. C.  
Tel: +86-021-2416-2266, Fax: +86-021-2416-2277

##### - Wafer Fab

##### Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd.

800 Yishan Road, Shanghai 200233, China  
Tel: +021-6485-1491, Fax: +86-021-5450-0008

#### REGIONAL SALES OFFICE

##### Shenzhen Office

##### Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd., Shenzhen Office

Unit A Room 1203, Skyworth Bldg., Gaoxin Ave.1.S., Nanshan District  
Shenzhen 518057, China

Tel: +86-0755-8660-4900, Fax: +86-0755-8660-4958

##### Taiwan Office (Taipei)

##### BCD Semiconductor (Taiwan) Company Limited

3F, No.17, Lane 171, Sec. 2, Jiu-Zong Rd., Nei-Hu Dist., Taipei(114), Taiwan, R.O.C  
Tel: +886-2-2656-2808

Fax: +886-2-2656-2806/26562950

##### Taiwan Office (Hsinchu)

##### BCD Semiconductor (Taiwan) Company Limited

8F, No.176, Sec. 2, Gong-Dao 5th Road, East District  
HsinChu City 300, Taiwan, R.O.C

Tel: +886-3-5160181, Fax: +886-3-5160181

##### USA Office

##### BCD Semiconductor Corp.

48460 Kato Road, Fremont, CA 94538, USA  
Tel: +1-510-668-1950

Fax: +1-510-668-1990

##### Korea Office

##### BCD Semiconductor Limited Korea office.

Room 101-1112, Digital-Empire II, 486 Sin-dong,  
Yeongtong-Gu, Suwon-city, Gyeonggi-do, Korea

Tel: +82-31-695-8430