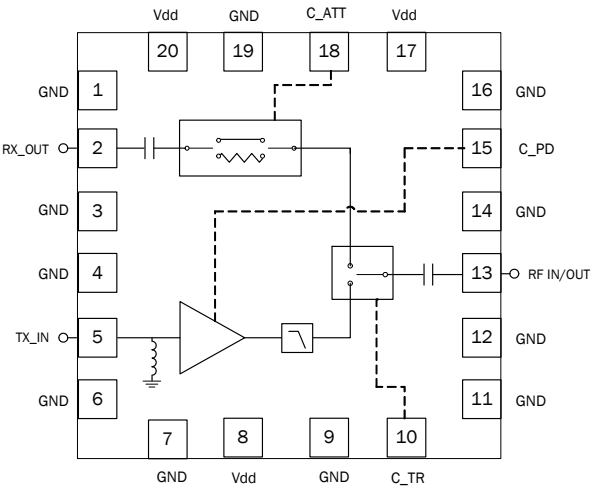
RF5604

5V, 475MHZ TO 625MHZ FEM

Package: 20-Pin, 4.5mmx4.5mmx0.975mm



Functional Block Diagram

Features

- Integrated 50Ω Input/Output Match
- Power Down Control
- TX OIP3 39dBm
- OP1dB 25dB
- 15dB RX Step Attenuator

Applications

- MoCA
- Satellite Set Top Boxes

Product Description

The RF5604 is a 475MHz to 625MHz Front-End Module (FEM) for the distribution of digital video within the home through existing coaxial cable. The FEM contains a linear GaAs Heterojunction Bipolar Transistor (HBT) Power Amplifier (PA) with a pHEMT Single-pole Double-throw (SPDT) switch, and a 1 bit step attenuator. The device is fully integrated with 50Ω input and output terminals with no external matching components required. The RF5604 is assembled in a small footprint 4.5mmx4.5mm RoHS package.

Ordering Information

RF5604	5V, 475MHz to 625MHz FEM, Standard 25-Piece Bag
RF5604SB	5-Piece Bag
RF5604SR	Standard 100-Piece Reel
RF5604TR13	Standard 2500-Piece Reel
RF5604PCK-410	Fully Assembled Evaluation Board and 5-Piece Bag

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+5.5	V_{DC}
Power Control Voltage (C_PD)	+5.5	V_{DC}
DC Supply Current	260	mA
PA Input RF Power	+20*	dBm
Operating Ambient Temperature	0 to +70	°C
Reduced Performance Temperatures	-40 to 0 and +70 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	MSL3	

*Maximum PA Input RF Power with a 50Ω load.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Conditions					T=25 °C, V_{CC}=5.0V_{DC}, C_PD=2.9V_{DC}, Freq=550MHz, circuit per evaluation board schematic.
Supply Voltage (V_{DD})	4.75	5.0	5.25	V	
Operating Ambient Temperature Range (T_{AMB})	0		70	°C	
DC Electrical Specifications					
Supply Current (I_{DD})			200	mA	V_{DD}=5.0V
Input Logic High (V_{IH})	2.8		V_{DD}	V	For C_PD; I≤3mA (sink current)
	1.7		V_{DD}	V	For C_TR and C_ATT; I≤100uA (sink current)
Input Logic Low (V_{IL})	-0.5		+0.4	V	For C_PD
	-0.5		+0.05	V	For C_TR and C_ATT I≤100uA (source current)
Shutdown Current		0.6	1.0	mA	C_PD=0V
		0.4	0.8	mA	C_PD=0V, C_ATT=C_TR=0V
RX Chain					
Frequency Range	475		625	MHz	
Input Power Range	-80		0	dBm	Receive Signal BW≤50MHz
Receive Gain 1 (G_{R1})	-0.7	-1.0		dB	C_ATT=L
Receive Gain 2 (G_{R2})	-14.5	-15.7	-16.5	dB	C_ATT=H
Receive Gain Step Difference (ΔG_R)	14.5	15.0	15.5	dB	G_{R1} to G_{R2} at any (single) Frequency
Pass Band Ripple			0.2	dB	Over any 50MHz
Switch Time			500	ns	G_{R2} to G_{R1}; G_{R1} to G_{R2}; 50% CTL to 10/90% RF
Impedance (Z_{IN}/Z_{OUT})			50	Ω	Single Ended
Input Return Loss (S_{11})	11	15		dB	
Output Return Loss (S_{22})	11	15		dB	
Input Third Order Intercept Point (IIP3)	28	30		dBm	GR_1
	28	33		dBm	GR_2
Input P1dB (IP1dB)	18			dBm	GR_1
	18			dBm	GR_2

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RX Chain, cont.					
Noise Figure (NF)	0.7	1.0		dB	GR_1; Exclusive of PA contribution
	14.5	15.7	16.5	dB	GR_2; Exclusive of PA contribution
TX/RX Switch Time			500	ns	50% CTL to 10/90% RF; Receive mode C_TR=L; Transmit mode C_TR=H
RX (added) Noise			-177	dBm/Hz	Noise contribution of PA output to RX_OUT in RX Mode G_{R1}
TX Chain					
Frequency Range	475		625	MHz	
Pass Band Ripple			0.5	dB	
Transmit Gain (G_T)	16.0	17.5	19.0	dB	Temp Range 0°C to +70°C over any 50MHz
Maximum Transmit Power			9.5	dBm	
Minimum Transmit Power			-33	dBm	
Input Third Order Intercept Point (IIP3)		14	19		Temp Range 0°C to +70°C; TX Power +1>+9dBm
Input 1dB Compression Point (IP1dB)	5.5	8.5		dBm	Temp Range 0°C to +70°C; TX Power +1>+9dBm
Noise Figure (NF)			5	dB	G_T
Input Impedance (Z_{IN})			50	Ω	
Input Return Loss (S_{11})	10	15		dB	
Output Impedance (Z_{OUT})			50	Ω	
Output Return Loss (S_{22})	10	15		dB	
TX/RX Switch Time			500	ns	50% CTL to 10/90% RF; Receive mode C_TR=L; Transmit mode C_TR=H
Transmit Gain Drift versus Temperature			0.015	dB/°C	
PA Output to RX Output Isolation	24	38		dB	TX Mode (C_TR=H; C_ATT=L)
Spurious (2nd Harmonic)			-30	dBm	TX Power=9dBm; TX Mode
Spurious (All Others)			-50	dBm	TX Power=9dBm; TX Mode

Truth Table

Mode	C_TR	C_PD	C_ATT
TX	H	H	L/H
RX	L	H	L
RX_ATTEN	L	H	H
Shut Down	L/H	L	L/H

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Pin	Function	Description
1	GND	Ground connection.
2	RX OUT	RF output, internally matched to 50Ω and DC blocked.
3	GND	Ground connection.
4	GND	Ground connection.
5	TX IN	RF input, internally matched to 50Ω.
6	GND	Ground connection.
7	GND	Ground connection.
8	VDD3	Voltage supply for PA.
9	GND	Ground connection.
10	C_TR	Control voltage for 1-bit switch between transmit and receive RF paths.
11	GND	Ground connection.
12	GND	Ground connection.
13	RF I/O	RF INPUT/OUTPUT, matched to 50Ω and DC blocked.
14	GND	Ground connection.
15	C_PD	Bias voltage for PA regulator.
16	GND	Ground connection.
17	VDD2	Voltage supply for switch/regulator.
18	C_ATT	Control voltage for 1-bit attenuator between receive modes 1 and 2.
19	GND	Ground connection.
20	VDD1	Voltage supply for attenuator.
21	GND	Ground connection. The back side of the package should be connected to the ground plane through as short a connection as possible, e.g., PCB vias under the device are recommended.

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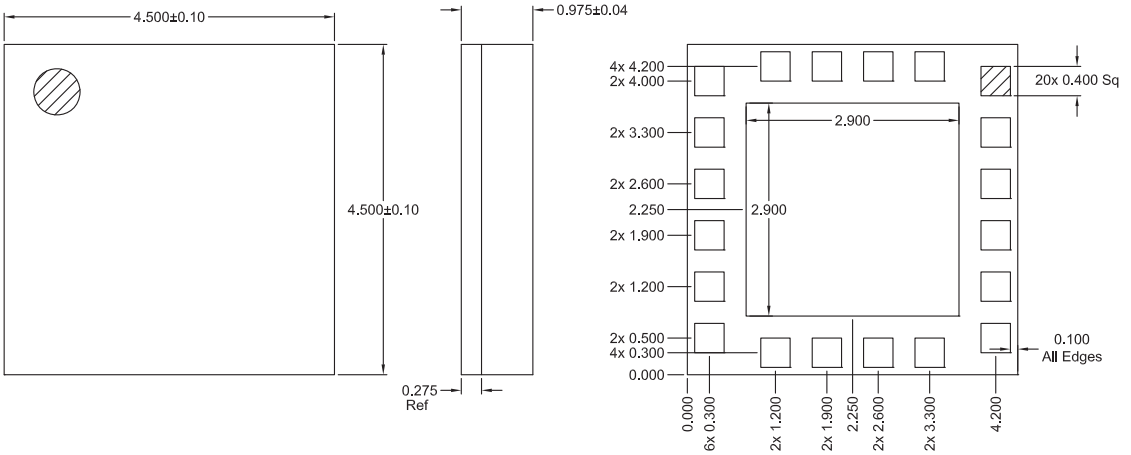
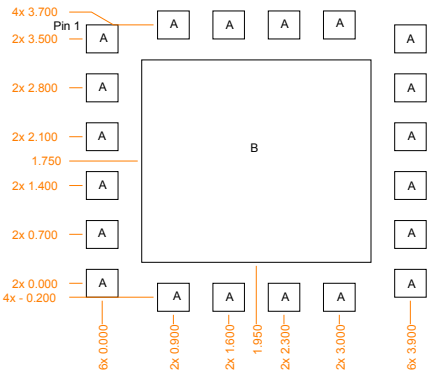
Package Drawing
20-pin, 4.5mm x 4.5mm x 0.975mm



Notes:
1. Shaded area represents Pin 1 location
2. Defining I/O Pad Center:
   To define center of the I/O pad opening, draw a right triangle in one corner of the I/O pad
   Then take the center of the hypotenuse to determine center of I/O pad

PCB Metal Land Pattern

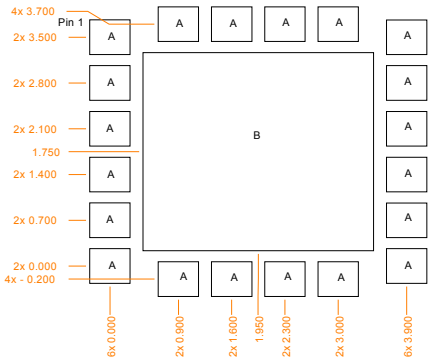
(Top View)



A = 0.400 mm Sq Typ
B = 2.900 mm Sq

PCB Solder Mask Pattern

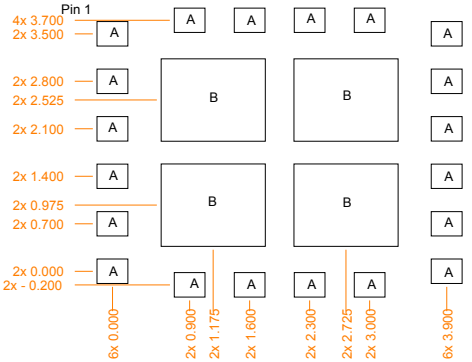
(Top View)



A = 0.530 mm Sq Typ
B = 3.030 mm Sq

PCB Stencil Pattern

(Top View)



A = 0.360 mm Sq Typ
B = 1.215 mm Sq Typ

Note: Thermal vias for center slug “B” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application. Example of the number and size of vias can be found on the RFMD evaluation board layout.

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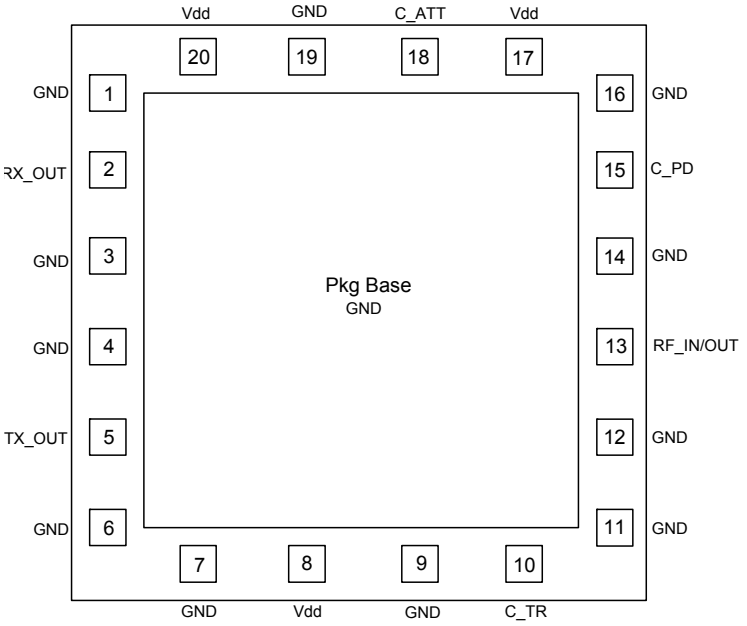
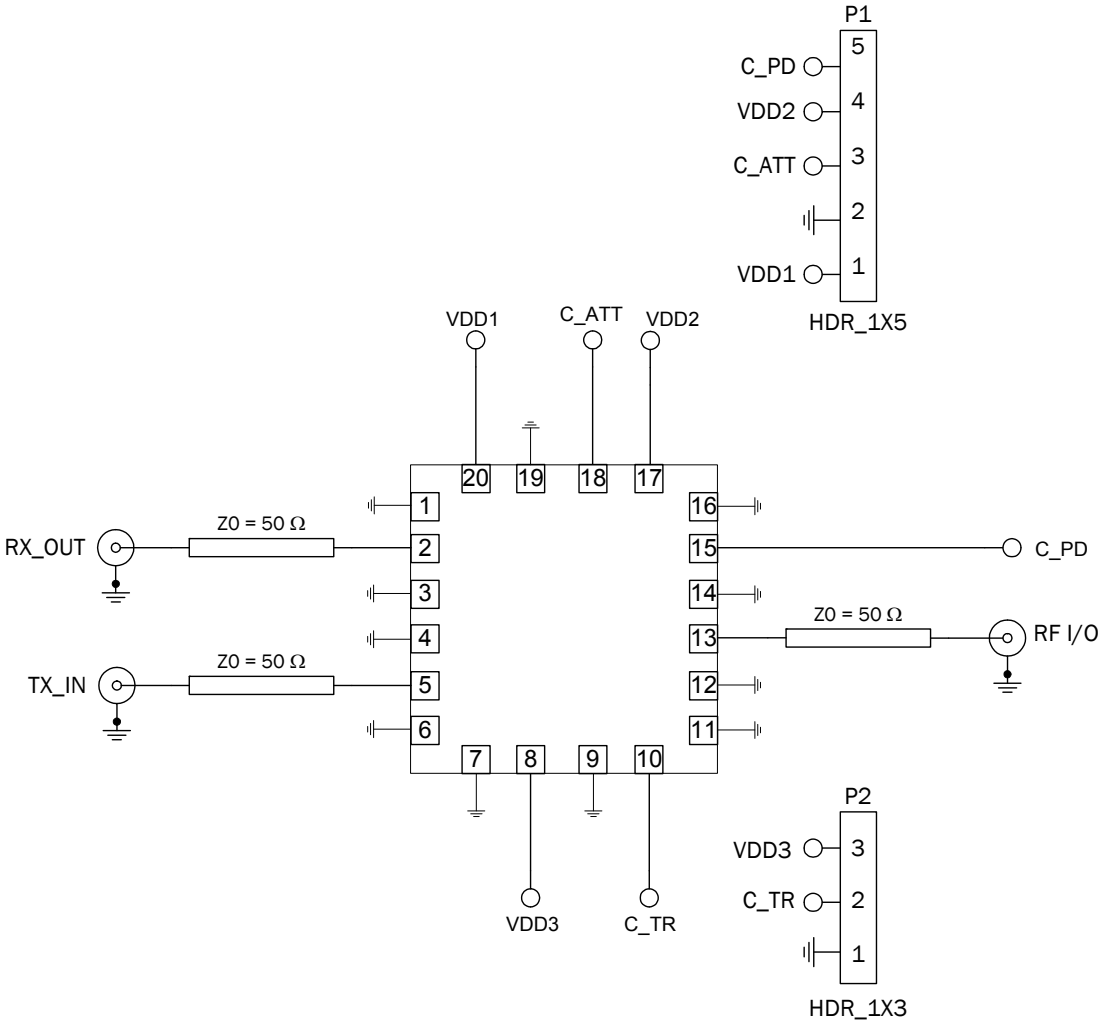
Pin Out


Vdd
GND
C_ATT
Vdd
20
19
18
17
GND
1
16
GND
RX_OUT
2
15
C_PD
GND
3
14
GND
Pkg Base
GND
GND
4
13
RF_IN/OUT
TX_OUT
5
12
GND
GND
6
11
GND
7
8
9
10
GND
Vdd
GND
C_TR

Evaluation Board Schematic



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Evaluation Board Layout