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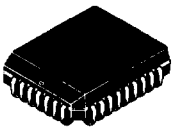
M29F010

Advance Information

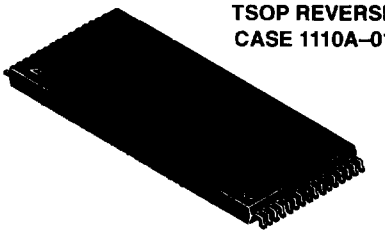
1M CMOS Sector Erase Flash Memory



PLCC
CASE 989A–01

TSOP
CASE 1110–01

TSOP REVERSE
CASE 1110A–01



The M29F010 is a 1M, 5 V–only, sector erase flash memory organized as 128K bytes of 8 bits each. The M29F010 is offered in JEDEC–standard 32–pin packages.

- 5.0 V ± 10% Read, Write and Erase Minimizes System Level Power Requirements
- JEDEC Industry Standard Pin–Out and Architecture
- Compatible with JEDEC–Standard (E^2PROM) Commands
- Minimum 100,000 Write/Erase Cycles
- Sector Erase Architecture:
  - Eight Equal Size Sectors of 16K Bytes Each
  - Any Combination of Sectors can be Concurrently Erased
  - Supports Full Chip Erase
- Embedded Erase™ Algorithms Allow Automatic Preprogram and Erase at any Sector
- Embedded Program™ Algorithms Allow Automatic Write and Verify of Data at a Specified Address
- $\overline{\text{Data}}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion
- Sector Protection Allows Hardware Disable of Sectors from Write or Erase Operations
- Low V_{CC} Write Inhibit ≤ 3.2 V
- Fast Access Time: M29F010–70 = 70 ns (Max)
  M29F010–90 = 90 ns (Max)
  M29F010–12 = 120 (Max)
- Low Active Power Dissipation: M29F010–70 = 275 mW
  M29F010–90 = 275 mW
  M29F010–12 = 275 mW
- Low Standby Power Dissipation:
  - TTL Levels: M29F010–70 = 5.5 mW
    M29F010–90 = 5.5 mW
    M29F010–12 = 5.5 mW
  - CMOS Levels: M29F010–70 = 0.55 mW
    M29F010–90 = 0.55 mW
    M29F010–12 = 0.55 mW

PIN NAMES	
A0 – A16	Address Input
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

M010S253

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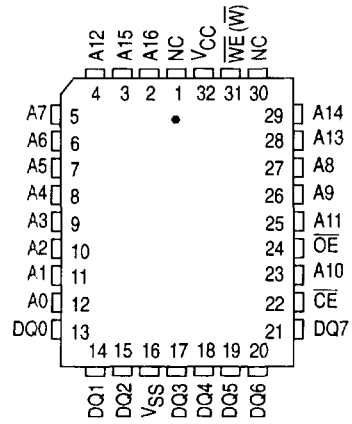
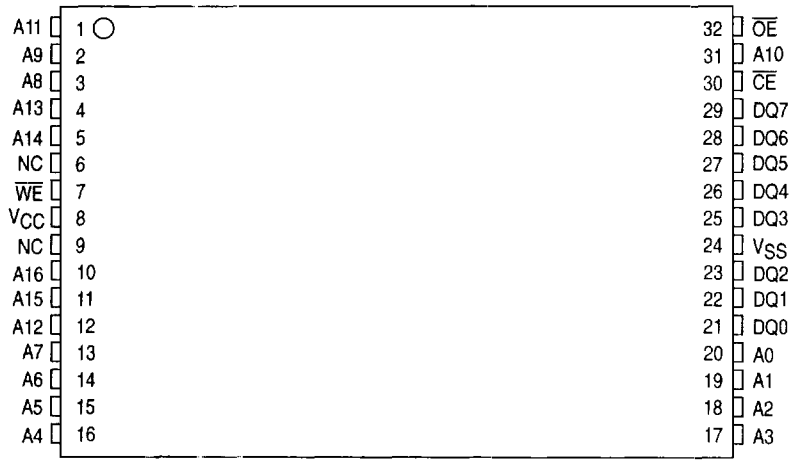
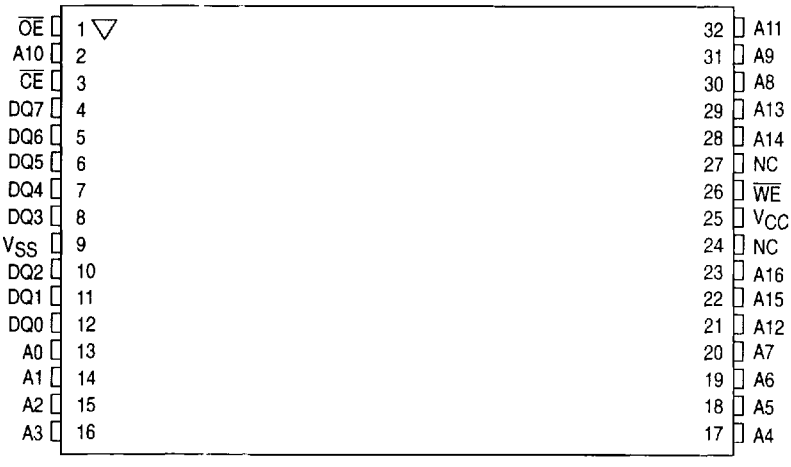
PIN ASSIGNMENTS
PLCC



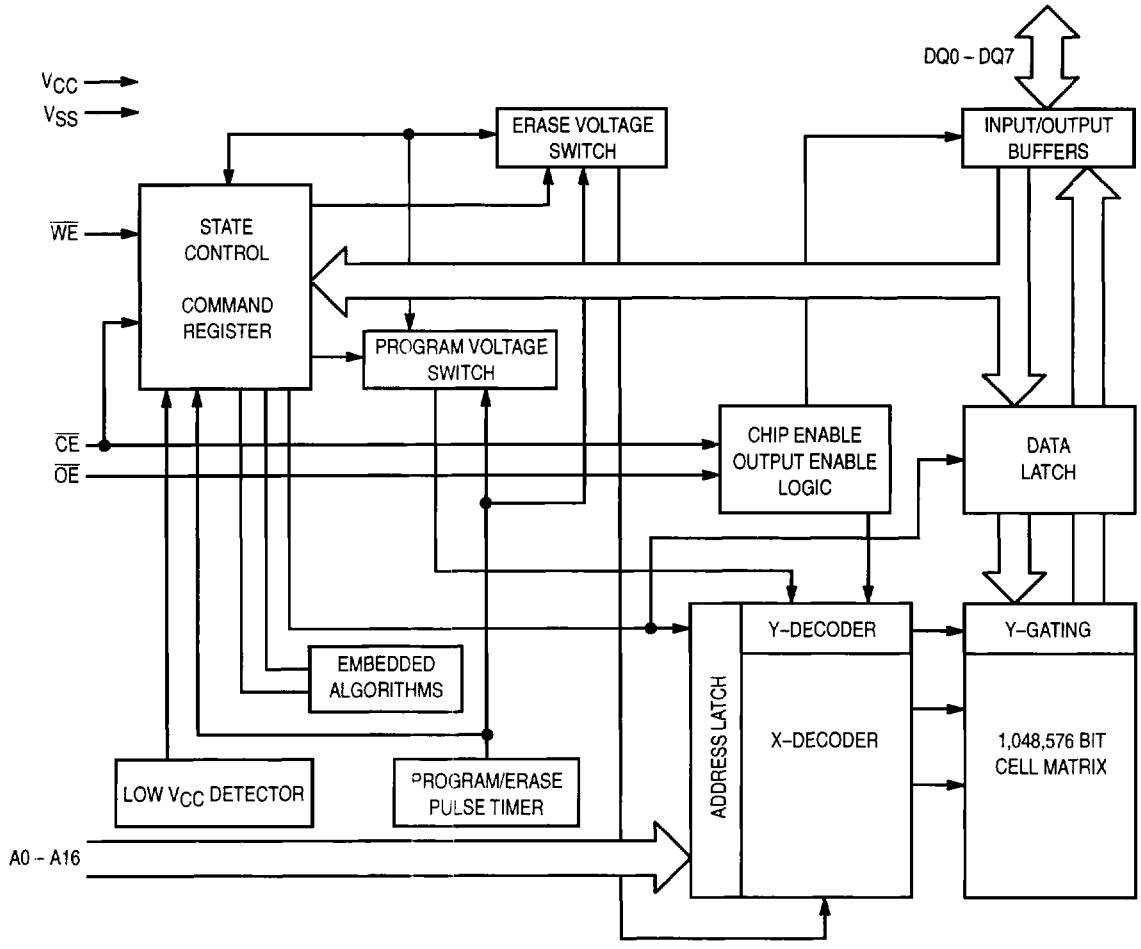
TSOP
STANDARD PINOUT



TSOP
REVERSE PINOUT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Notes 1 through 4)

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 1)	V_{CC}	– 2.0 to + 7	V
Voltage Relative to V_{SS}: All Pins Except A9, $\overline{CE}$, and $\overline{OE}$ (Note 1) A9, $\overline{CE}$, and $\overline{OE}$	V_{in}, V_{out}	 – 2.0 to + 7 – 2.0 to + 14	V
Output Short Circuit Current (Note 3)	I_{out}	200	mA
Power Dissipation	P_D	350	mW
Ambient Temperature with Power Applied	T_A	– 55 to + 125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 – 65 to + 150 – 65 to + 125	°C

NOTES:

1. Minimum dc voltage on input or I/O pins is – 0.5 V. During voltage transitions, inputs may undershoot V_{SS} to – 2.0 V for periods of up to 20 ns. Maximum dc voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.
2. Minimum dc voltage on pin A9, $\overline{CE}$, and $\overline{OE}$ is – 0.5 V. During voltage transitions, A9, $\overline{CE}$, and $\overline{OE}$ may undershoot V to – 2.0 V for periods of up to 20 ns. Maximum dc input voltage on A9, $\overline{CE}$, and $\overline{OE}$ is + 13.5 V which may overshoot to 14.0 V_{SS} for periods up to 20 ns.
3. No more than one output shorted at a time. Duration of the short circuit should not be longer than one second.
4. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

OPERATING RANGES (See Note)

Rating	Symbol	Value	Unit
Supply Voltages M29F010–70 = 70 ns, M29F010–90 = 90 ns, M29F010–12 = 120 ns	V_{CC}	 + 4.50 to + 5.50	V
Operating Temperature Range Commercial Industrial	T_C	 0 to + 70 – 40 to + 85	°C

NOTE: Operating ranges define those limits between which the functionality of the device is guaranteed.

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9)	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC OPERATING CONDITIONS AND CHARACTERISTICS

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{CC1}	—	30	mA	1
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{CC2}	—	50	mA	2, 3
V_{CC} Standby Current TTL/NMOS Levels (V_{CC} = V_{CC} max, $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}) CMOS Levels (V_{CC} = V_{CC} max, $\overline{CE}$ = V_{CC} ± 0.5 V)	I_{CC3}	 — —	 1.0 100	 mA µA	
Input Load Current (V_{in} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max)	I_{LI}	—	± 1.0	µA	
A9, $\overline{CE}$, and $\overline{OE}$ Input Load Current (V_{CC} = V_{CC} max, A9, $\overline{CE}$, and $\overline{OE}$ = 12.5 V)	I_{LIT}	—	50	µA	
Output Leakage Current (V_{out} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max)	I_{LO}	—	± 1.0	µA	
Input Low Level	V_{IL}	−0.5	0.8	V	
Input High Voltage TTL/NMOS Levels CMOS Levels	V_{IH}	 2 0.7 x V_{CC}	 V_{CC} + 0.5 V_{CC} + 0.5	V	
Voltage for Autoselect and Sector Protect (V_{CC} = 5.0 V)	V_{ID}	11.5	12.5	V	
Output High Level TTL/NMOS Levels (I_{OH} = −2.5 mA, V_{CC} = V_{CC} min)	V_{OH}	2.4	—	V	
Output High Voltage CMOS Levels (I_{OH} = −2.5 mA, V_{CC} = V_{CC} min) CMOS Levels (I_{OH} = −100 µA, V_{CC} = V_{CC} min)	 V_{OH1} V_{OH2}	 0.85 V_{CC} V_{CC} − 0.4	 — —	V	
Low V_{CC} Lock–Out Voltage	V_{LKO}	3.2	—	V	

NOTES:
1. The I_{CC} current listed includes both the dc operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Not 100% tested.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

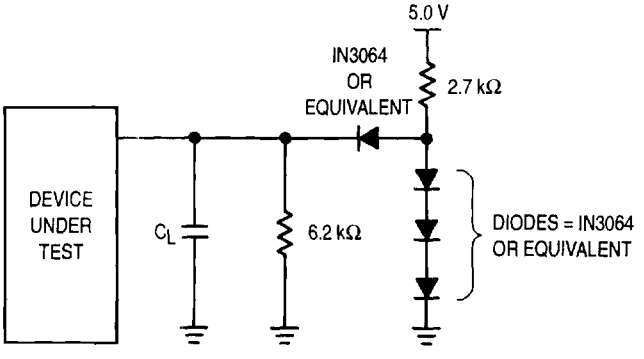
Parameter		Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0)	TSOP PLCC	C_{in}	6 4	7.5 6	pF
Control Pin Capacitance (V_{in} = 0)	TSOP PLCC	C_{in2}	7.5 8	9 12	pF
Output Capacitance (V_{out} = 0)	TSOP PLCC	C_{out}	8.5 8	12 12	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

READ ONLY OPERATIONS CYCLE (See Note 1)

Parameter	Symbol		M29F010–70 (Note 1)		M29F010–90 (Note 2)		M29F010–12 (Note 2)		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	70	—	90	—	120	—	ns	4
Address to Output Delay, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	t_{AVQV}	t_{ACC}	—	70	—	90	—	120	ns	
Chip Enable to Output Delay, $\overline{OE}$ = V_{IL}	t_{ELQV}	t_{CE}	—	70	—	90	—	120	ns	
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	30	—	35	—	50	ns	
Chip Enable to Output High–Z	t_{EHQZ}	t_{DF}	—	20	—	20	—	30	ns	3, 4
Output Enable to Output High–Z	t_{GHQZ}	t_{DF}	—	20	—	20	—	30	ns	3, 4
Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	0	—	0	—	0	—	ns	

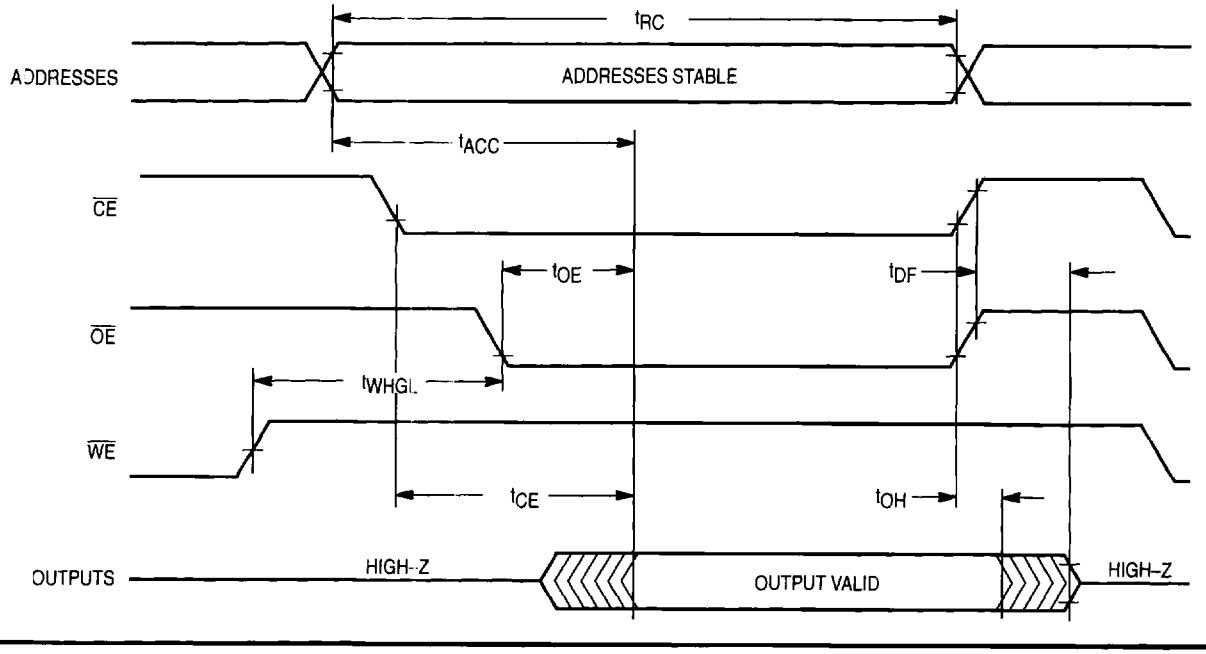
NOTES:
1. Test conditions — output load: one TTL gate and 30 pF; input rise and fall times: 5 ns; input pulse levels: 0 to 3 V; timing measurement reference level: input, 1.5 V; output, 1.5 V.
2. Test conditions — output load: one TTL gate and 100 pF; input rise and fall times: 20 ns; input pulse levels: 0.45 to 2.4 V; timing measurement reference level: input, 0.8 and 2.0 V; output, 0.8 and 2.0 V.
3. Output driver disable time.
4. Not 100% tested.



NOTE: C_L = 100 pF including jig capacitance.

Figure 1. Test Conditions

READ CYCLE



WRITE/ERASE/PROGRAM OPERATIONS

Parameter	Symbol		M29F010–70		M29F010–90		M29F010–12		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	90	—	120	—	ns	1
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{WLAX}	t_{AH}	45	—	45	—	50	—	ns	
Data Setup Time	t_{DVWH}	t_{DS}	30		45		50		ns	
Data Hold Time	t_{WHQX}	t_{DH}	0	—	0	—	0	—	ns	
Output Enable Setup Time		t_{OES}	0	—	0	—	0	—	ns	
Output Enable Hold Time — Read Toggle and $\overline{\text{Data}}$ Polling		t_{OEH}	0 10	— —	0 10	— —	0 10	— —	ns	1
Read Recovery Time Before Write	t_{GHWL}		0	—	0	—	0	—	ns	
$\overline{\text{CE}}$ Setup Time	t_{ELWL}	t_{CS}	0	—	0	—	0	—	ns	
$\overline{\text{CE}}$ Hold Time	t_{WHEH}	t_{CH}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	35	—	45	—	50	—	ns	
Write Pulse Width High	t_{WHWL}	t_{WPH}	20	—	20	—	20	—	ns	
Byte Programming Operation	t_{WHWH1}		14	—	14	—	14	—	µs	
Erase Operation	t_{WHWH2}		2.2	—	2.2	—	2.2	—	s	2
V_{CC} Setup Time		t_{VCS}	50	—	50	—	50	—	µs	1
Voltage Transition Time		t_{VLHT}	4	—	4	—	4	—	µs	1, 3
Write Pulse Width		t_{WPP}	10	—	10	—	10	—	ms	3
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active		t_{OESP}	4	—	4	—	4	—	µs	1, 3
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active		t_{CSP}	4	—	4	—	4	—	µs	1, 4

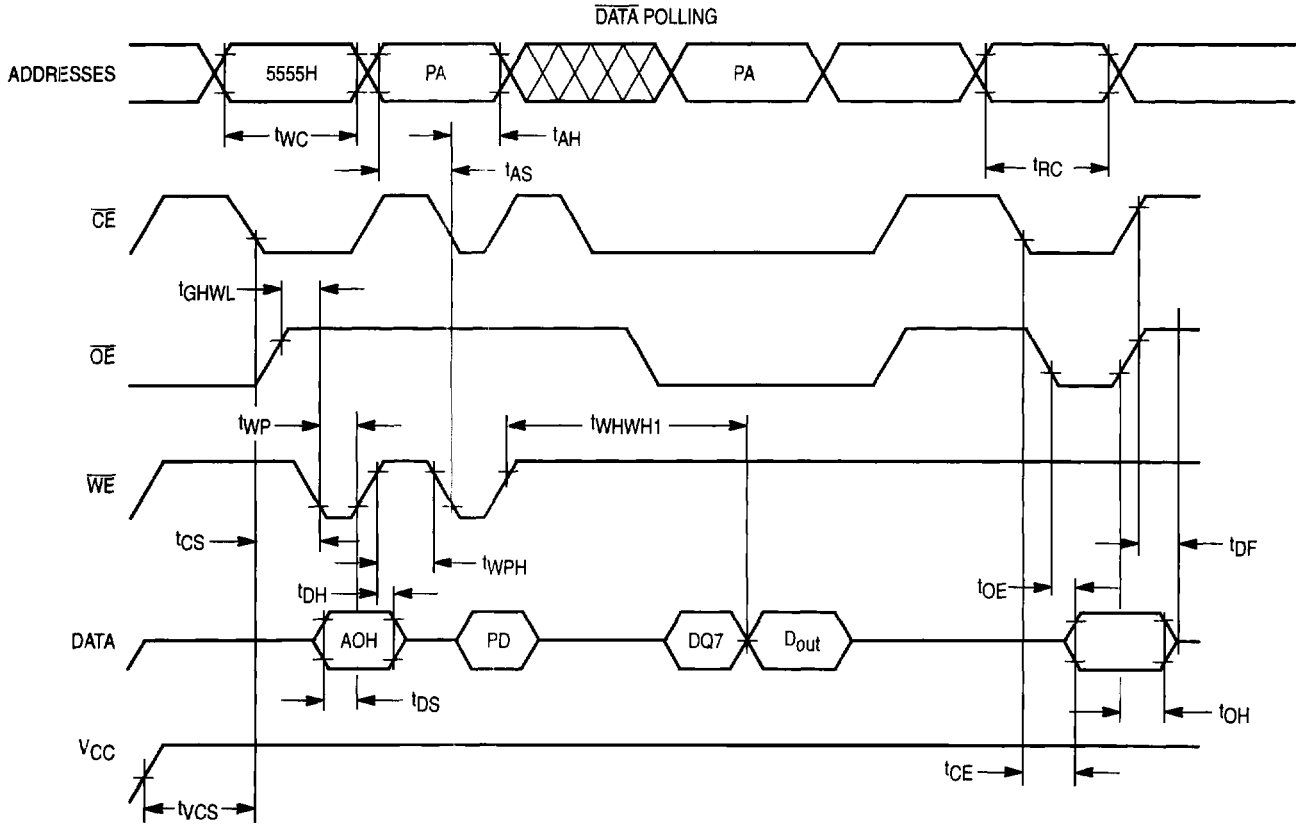
NOTES:
1. Not 100% tested.
2. This includes the preprogramming time.
3. These timings are for Sector Protect/Unprotect operations.
4. This timing is only for Sector Unprotect.

ERASE AND PROGRAMMING PERFORMANCE (See Note 2)

Parameter	Limits			Unit	Comments	Notes
	Min	Typ	Max			
Chip/Sector Erase Time		1	10	sec	Excludes 00H programming prior to erasure	1
Sector Programming Time		0.3		sec		
Chip Programming Time		2	12.5	sec	Excludes system–level overhead	
Erase Program Cycles	100,000	1,000,000		Cycles		
Byte Program Time		14		µs		
			60	ms		3, 4

NOTES:
1. The Embedded Algorithm allows for 60 second erase time for military temperature range operations.
2. The Embedded Algorithms allow for a longer chip program and erase time. However, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.
3. DQ5 = "1" only after a byte takes longer than 60 ms to program.
4. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum Chip Programming Times listed above.

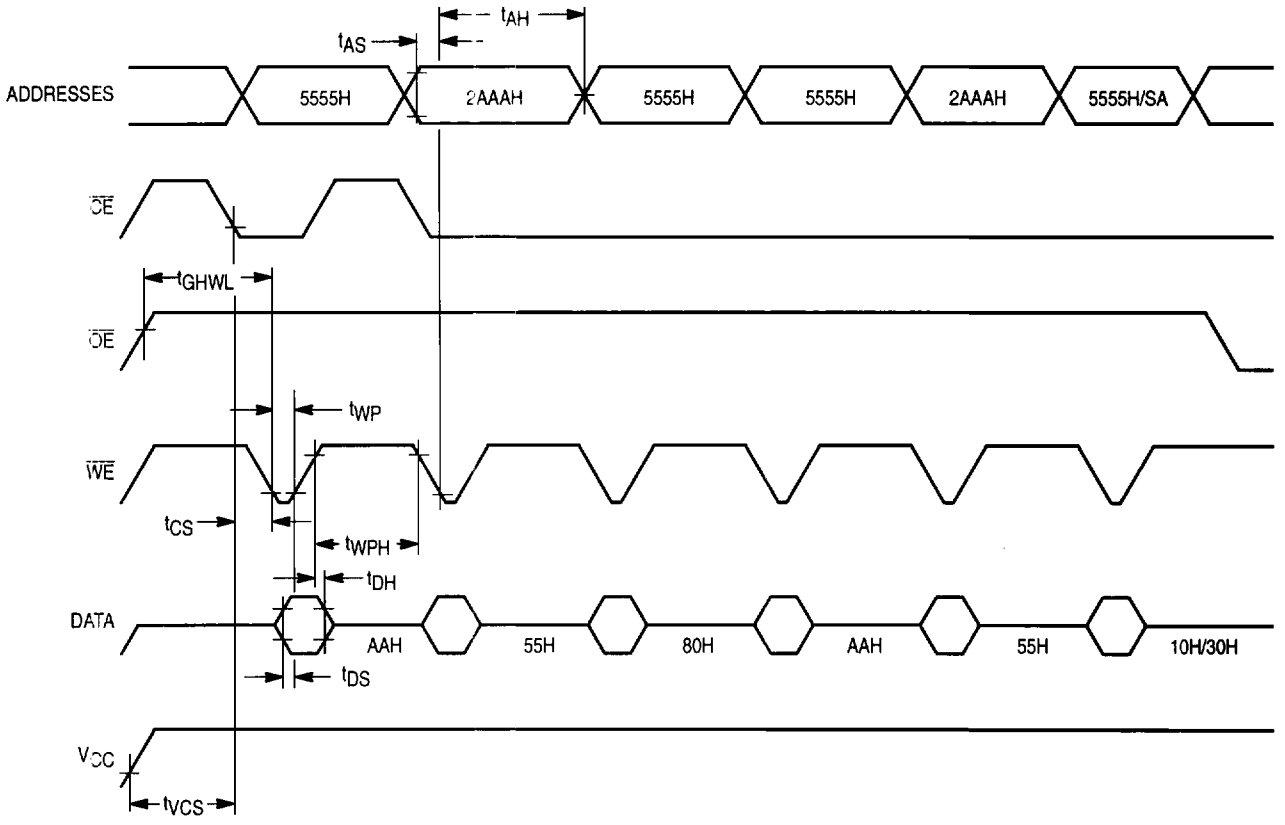
PROGRAM OPERATIONS



NOTES:

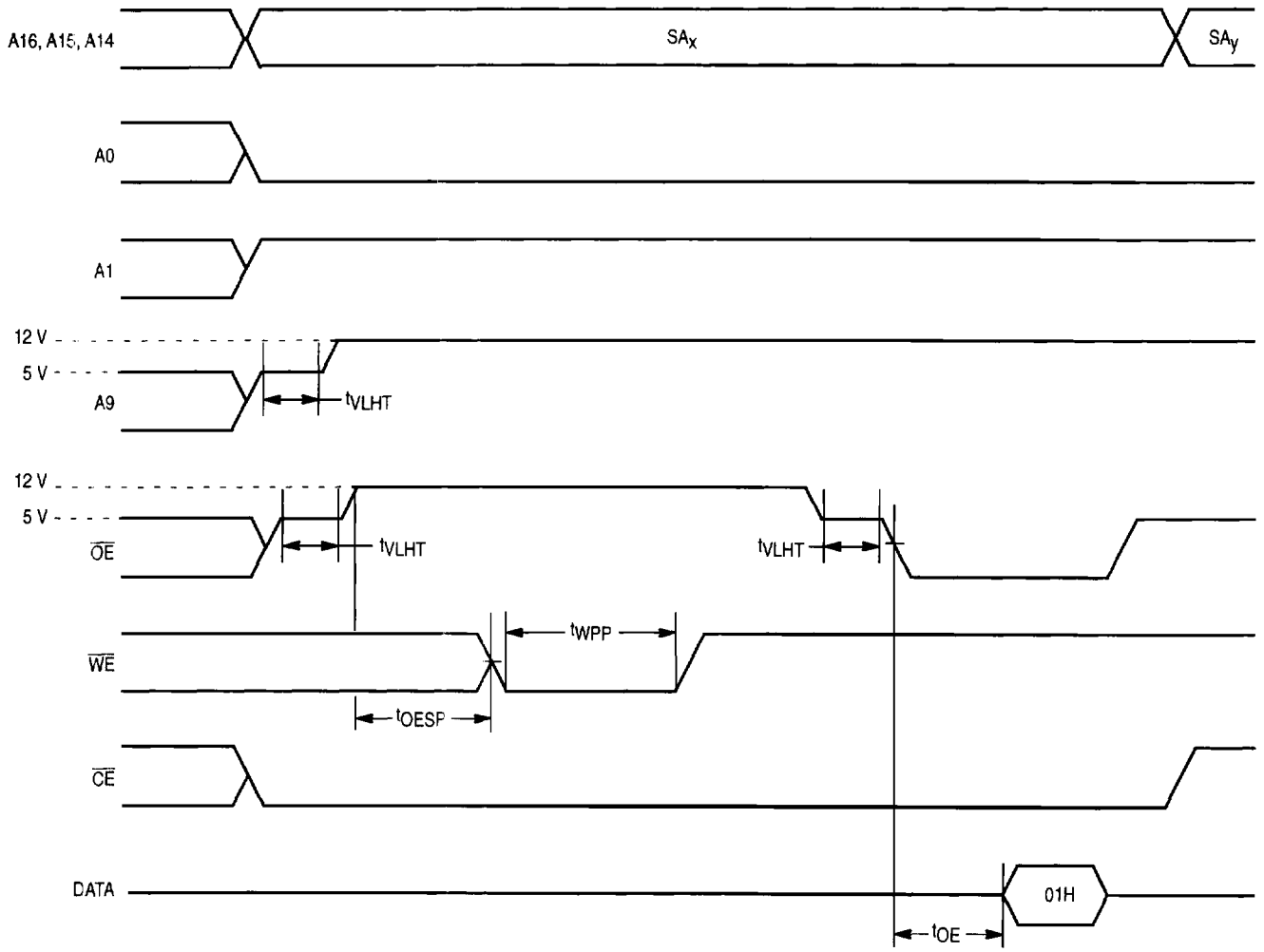
1. Figure indicates last two bus cycles of four bus cycle sequence.
2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. $\overline{DQ7}$ is the output of the complement of the data written to the device.
5. D_{out} is the output of the data written to the device.

CHIP/SECTOR ERASE OPERATIONS



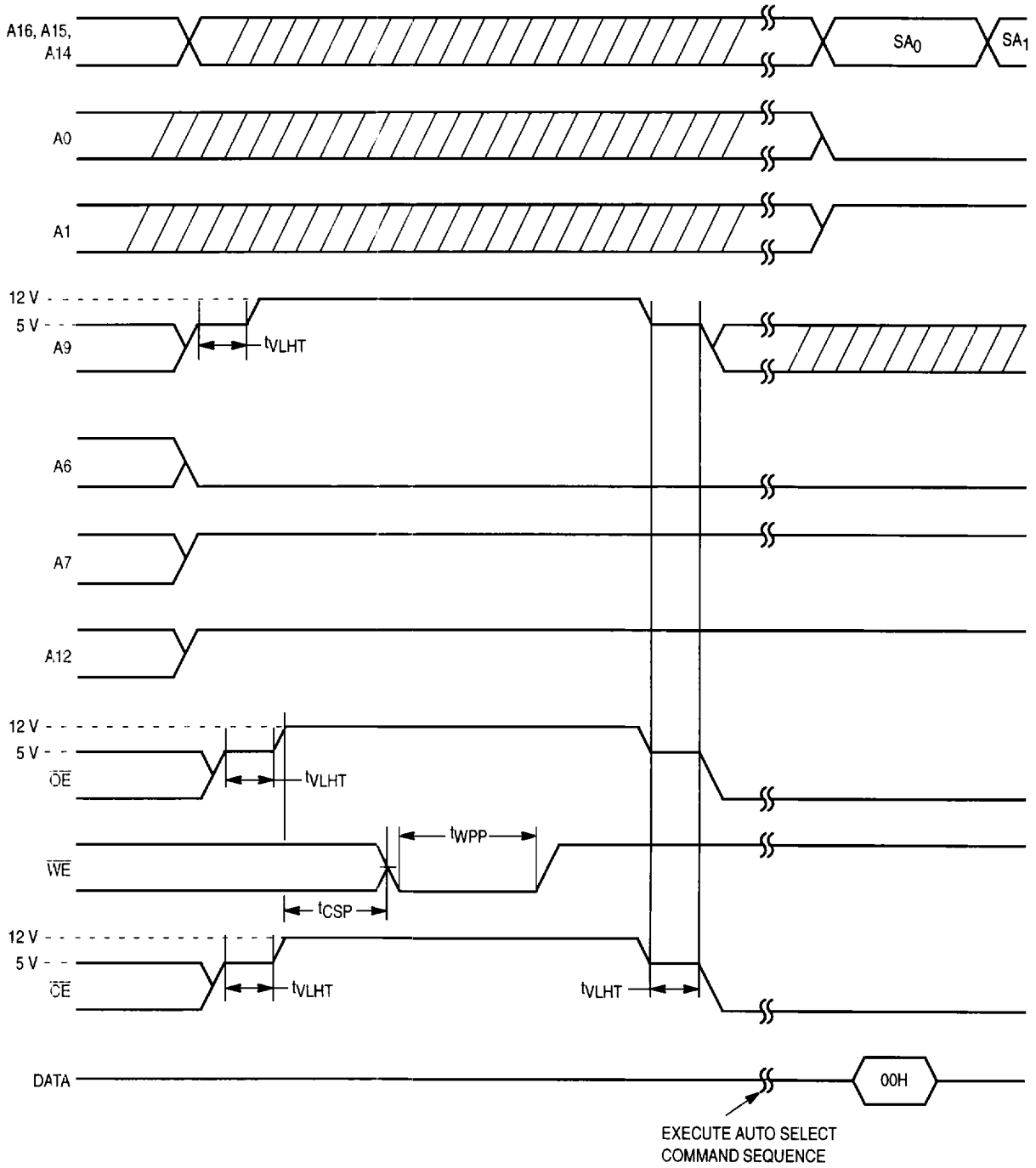
NOTE: SA is the sector address for Sector Erase

SECTOR PROTECT CYCLE



SA_X = Sector Address for initial sector
SA_Y = Sector Address for next sector

SECTOR UNPROTECT CYCLE

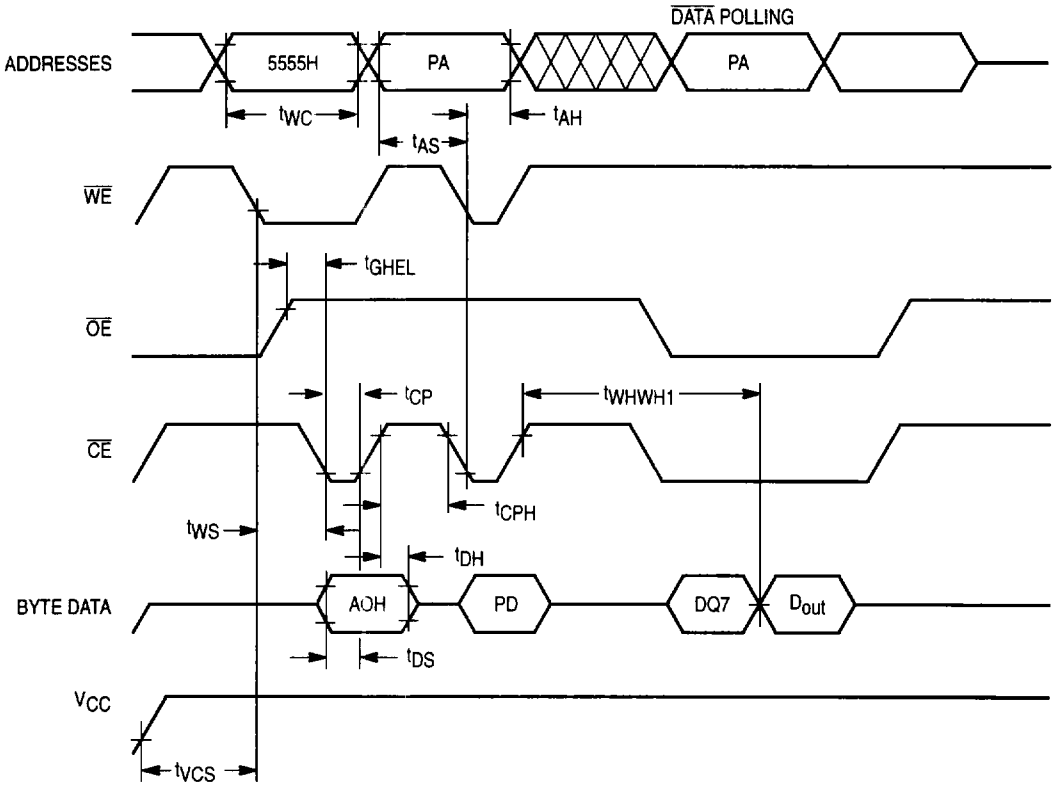


ALTERNATE $\overline{CE}$ CONTROLLED WRITE CYCLES

Parameter	Symbol		M29F010–70		M29F010–90		M29F010–12		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	90	—	120	—	ns	1
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{ELAX}	t_{AH}	45	—	45	—	50	—	ns	
Data Setup Time	t_{DVEH}	t_{DS}	30		45		50		ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Output Enable Setup Time		t_{OES}	0	—	0	—	0	—	ns	
Output Enable Hold Time Read Toggle and $\overline{Data}$ Polling		t_{OEH}	0 10	— —	0 10	— —	0 10	— —	ns	1
Read Recover Time before Write		t_{GHEL}	0	—	0	—	0	—	ns	
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ Hold Time	t_{EHWH}	t_{WH}	0		0		0		ns	
$\overline{CE}$ Pulse Width	t_{ELEH}	t_{CP}	35	—	45	—	50	—	ns	
$\overline{CE}$ Pulse Width High	t_{EHEL}	t_{CPH}	20	—	20	—	20	—	ns	
Byte Programming Operation	t_{WHWH1}	t_{WHWH1}	14	—	14	—	14	—	µs	
Erase Operation	t_{WHWH2}	t_{WHWH2}	2.2	—	2.2	—	2.2	—	s	2
V_{CC} Setup Time		t_{VCS}	2	—	2	—	2	—	µs	1

NOTES:
1. Not 100% tested.
2. This also includes the preprogramming time

ALTERNATE $\overline{CE}$ CONTROLLED WRITE CYCLE



NOTES:

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2. PA is address of the memory location to be programmed.
3. PD is data to be programmed at byte address.
4. $\overline{DQ7}$ is the output of the complement of the data written to the device.
5. D_{out} is the output of the data written to the device.

GENERAL DESCRIPTION

The Motorola M29F010 is a 1M Flash Memory device designed to be programmed in–system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase options. The device can also be reprogrammed in standard EPROM programmers.

The M29F010 offers access times between 70 and 120 nanoseconds, allowing operation of high–speed microprocessors without wait states. To eliminate bus contention, the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

This device is entirely pin and command set compatible with JEDEC standard 1M E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state–machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The M29F010 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This entire chip or any individual sector is typically erased and verified in 3.0 seconds (including preprogramming). Any individual sector is typically erased and verified in 1.3 seconds (including preprogramming).

This device also features a sector erase architecture. The sector mode allows for 16K byte blocks of memory to be erased and reprogrammed without affecting other blocks.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ7 or by the toggle bit feature on DQ6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Flash Technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The M29F010 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler–Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

FLEXIBLE SECTOR–ERASE ARCHITECTURE

- 16K Bytes per sector
- Individual–sector, multiple–sector, or bulk–erase capability
- Individual or multiple–sector protection is user definable

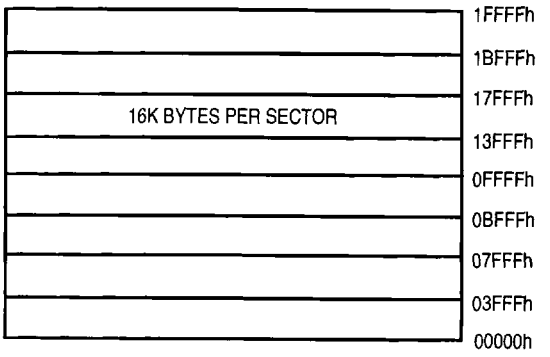


Table 1. User Bus Operations (see Note 1)

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A9	I/O
Auto–Select Manufacturer Code (Note 2)	L	L	H	L	L	V_{ID}	Code
Auto–Select Device Code (Note 2)	L	L	H	H	L	V_{ID}	Code
Read	L	L	H	A0	A1	A9	D_{out}
Standby	H	X	X	X	X	X	High Z
Output Disable	L	H	H	X	X	X	High Z
Write	L	H	L	A0	A1	A9	D_{in} (Note 3)
Enable Sector Protect	L	V_{ID}	L	X	X	V_{ID}	X
Verify Sector Protect (Note 4)	L	L	H	L	H	V_{ID}	Code

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 2 and 3.
3. Refer to Table 4 for valid D_{in} during a write operation.
4. Refer to Sector Protection section.

READ MODE

The M29F010 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC} - t_{OE}$ time).

STANDBY MODE

The device has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), when the current consumed is 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

OUTPUT DISABLE

With the $\overline{OE}$ input at a logic high level (V_{IH}) output from the device is disabled. This will cause the output pins to be in a high impedance state.

AUTOSELECT

The autoselect mode allows the reading out of a binary code from the device and will identify the Flash component manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 4 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (for example, AMD = 01H) and byte 1 (A0 = V_{IH}) the device identifier code (for example, M29F010 = 20H). These two bytes are given in the table below. All identifiers for manufacturers and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (seeTable 2).

Table 2. Autoselect and Sector Protection Verify Codes

Type	A16	A15	A14	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	X	X	X	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Device Code	X	X	X	V_{IL}	V_{IH}	20H	0	0	1	0	0	0	0	0
Sector Protection Verify	Sector Addresses			V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

*Outputs 01H at protected sector addresses. Outputs 00H at unprotected sector addresses.

Table 3. Sector Address Tables

	A16	A15	A14	Address Range
SA0	0	0	0	00000h–03FFFh
SA1	0	0	1	04000h–07FFFh
SA2	0	1	0	08000h–0BFFFh
SA3	0	1	1	0C000h–0FFFFh
SA4	1	0	0	10000h–13FFFh
SA5	1	0	1	14000h–17FFFh
SA6	1	1	0	18000h–1BFFFh
SA7	1	1	1	1C000h–1FFFFh

WRITE

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs tc the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

SECTOR PROTECTION

The M29F010 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 7). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$. The sector addresses (A16, A15, and A14) should be set to the sector to be protected. Table 3 defines the sector address for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Reading the device at a particular sector address (A16, A15, and A14) will produce 01H at data outputs (DQ0 – DQ7) for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A0, and A1 are don't care. Address location 02H is reserved to verify sector protection of the device. Address pin A1 must be held at V_{IH} and A0 at V_{IL} (please refer to Table 2). Address locations 00H and 01H are reserved for autoselect codes. If a verify of the sector protection circuitry were done at these addresses, the device would ouptut the manufacturer and device codes respectively.

It is also possible to determine if a sector is protected in the system by writing an autoselect command. Performing a read operation at particular sector addresses (A16, A15, and A14)and with A1 = VIH and A) = VIL (other addresses are a don't care) will produce 01H data if those sectors are protected. (See Table 2 for autoselect codes.) Otherwise the device will read 00H for an unprotected sector.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register.Table 3 defines the valid register command sequences.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power–up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

AUTOSELECT COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XXX0H retrieves the manufacturer code of 01H. A read cycle from address XXX1H returns the device code 20H (see Table 2). A read cycle from address XXX2H returns information as to which sectors are protected. All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Table 4. Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H	00H/01H	01H/20H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

NOTES:
1. Address bits A15 = X = don't care. Write Sequences may be initiated with A15 in either state.
2. Address bits A16 = X = don't care for all address commands except for program address (PA) and sector address (SA).
3. Bus operations are defined in Table 1.
4. RA = Address of the memory location to be read
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, A14 will uniquely select any sector.
5. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.

BYTE PROGRAMMING

The Flash chip is programmed on a byte–by–byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set–up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The Flash chip will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data 0 cannot be programmed back to a 1. Attempting to do so will probably hang up the device (exceed timing limits), or perhaps result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still 0. Only erase operations can convert 0s to 1s.

Figure 2 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

CHIP ERASE

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set–up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. A Reset command will terminate the Erase but the data in the chip will be undefined. In that case, perform the Erase operation again and allow it to complete.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 of each byte is 1 (see Write Operation Status section) at which time the device returns to read the mode.

Figure 3 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

SECTOR ERASE

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set–up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time–out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

CAUTION

Do not attempt to write an invalid command sequence during the sector erase timeout. Otherwise, it will terminate the sector erase operation and the device will reset back into the read mode.

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re–enabled after the last Sector Erase command is written. A time–out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time–out window the timer is reset. (Monitor DQ3 to determine if the sector erase window is still open, see section DQ3, Sector Erase Timer). Any command other than Sector Erase or Erase Suspend during this period will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution will result in the data of the operated sectors being undefined. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations. A Reset command will terminate the Sector Erase but the data in the sector will be undefined. In that case, perform the Sector Erase operation again and allow it to complete

The automatic sector erase begins after the 100 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 of each byte is 1 (see Write Operation Status section) at which time the device returns to read mode. $\overline{Data}$ polling must be performed at an address within any of the sectors being erased.

Figure 3 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

WRITE OPERATION STATUS

DQ7
$\overline{Data}$ Polling

The device features $\overline{Data}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed.

During the Embedded Program Algorithm an attempt to read the device will produce the complement data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. $\overline{Data}$ polling is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four srite pulse sequence.

During the Embedded Erase Algorithm, an attempt to read the device will produce a 0 at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a 1 at the DQ7 output.

For chip erase, the $\overline{Data}$ Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the $\overline{Data}$ Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. $\overline{Data}$ Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the data pins (DQ7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0 – DQ6 of each byte may be still invalid. The valid data on DQ0 – DQ7 will be read on the successive read attempts.

The $\overline{Data}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time–out (see Table 5).

See Figure 5 for the $\overline{Data}$ Polling timing specifications and diagrams.

DQ6
Toggle Bit

The device also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ6 to toggle.

See Figure 6 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a 1. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The device

must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused). The device must be reset to use the other sectors.

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a 1. Please note that this is not a device failure condition since the device was incorrectly used. The device must be reset to continue using the device.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time–out will begin. DQ3 will remain low until the time–out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high (1) the internally controlled erase cycle has begun; attempts to write subsequent sector erase commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low (0), the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 5: Hardware Sequence Flags.

Table 5. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2 – DQ0
In Progress	Auto–Programming	$\overline{\text{DQ7}}$	Toggle	0	0	Reserved for Future Use
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto–Programming	$\overline{\text{DQ7}}$	Toggle	1	0	Reserved for Future Use
	Program/Erase in Auto Erase	0	Toggle	1	1	

NOTE: DQ4 is for Motorola internal use only.

DATA PROTECTION

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi–bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power–up and power–down transitions or system noise.

LOW V_{CC} WRITE INHIBIT

To avoid initiation of a write cycle during V_{CC} power–up and power–down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

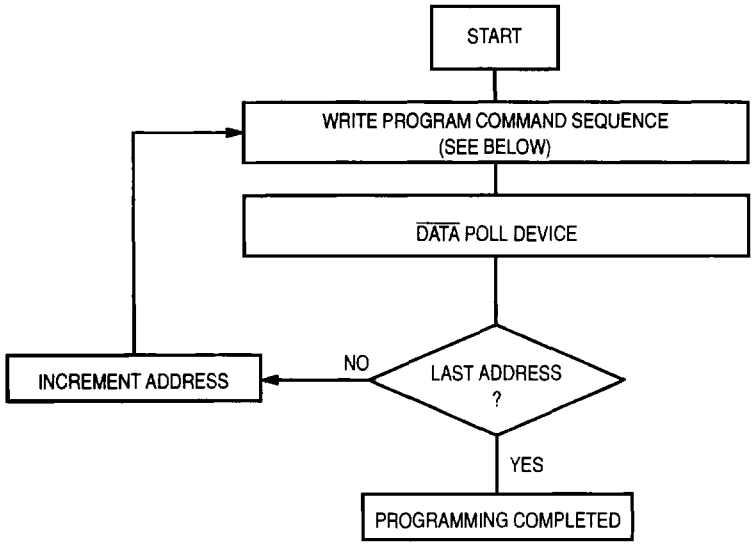
Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER–UP WRITE INHIBIT

Power–up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power–up.

SECTOR PROTECT

Sectors of the device may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.



Program Command Sequence (Address/Command):

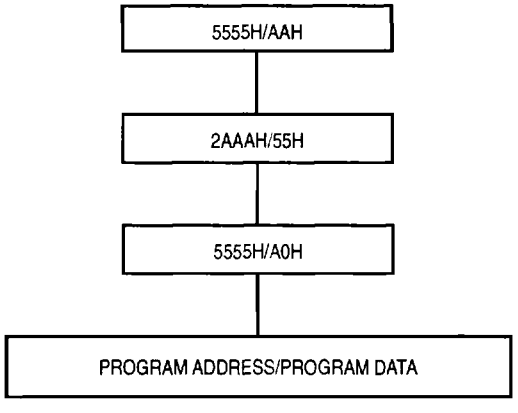


Figure 2. Embedded Programming Algorithm

Table 6. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Embedded Program Algorithm	Valid Address/Data Sequence
Read		Data Polling to Verify Programming

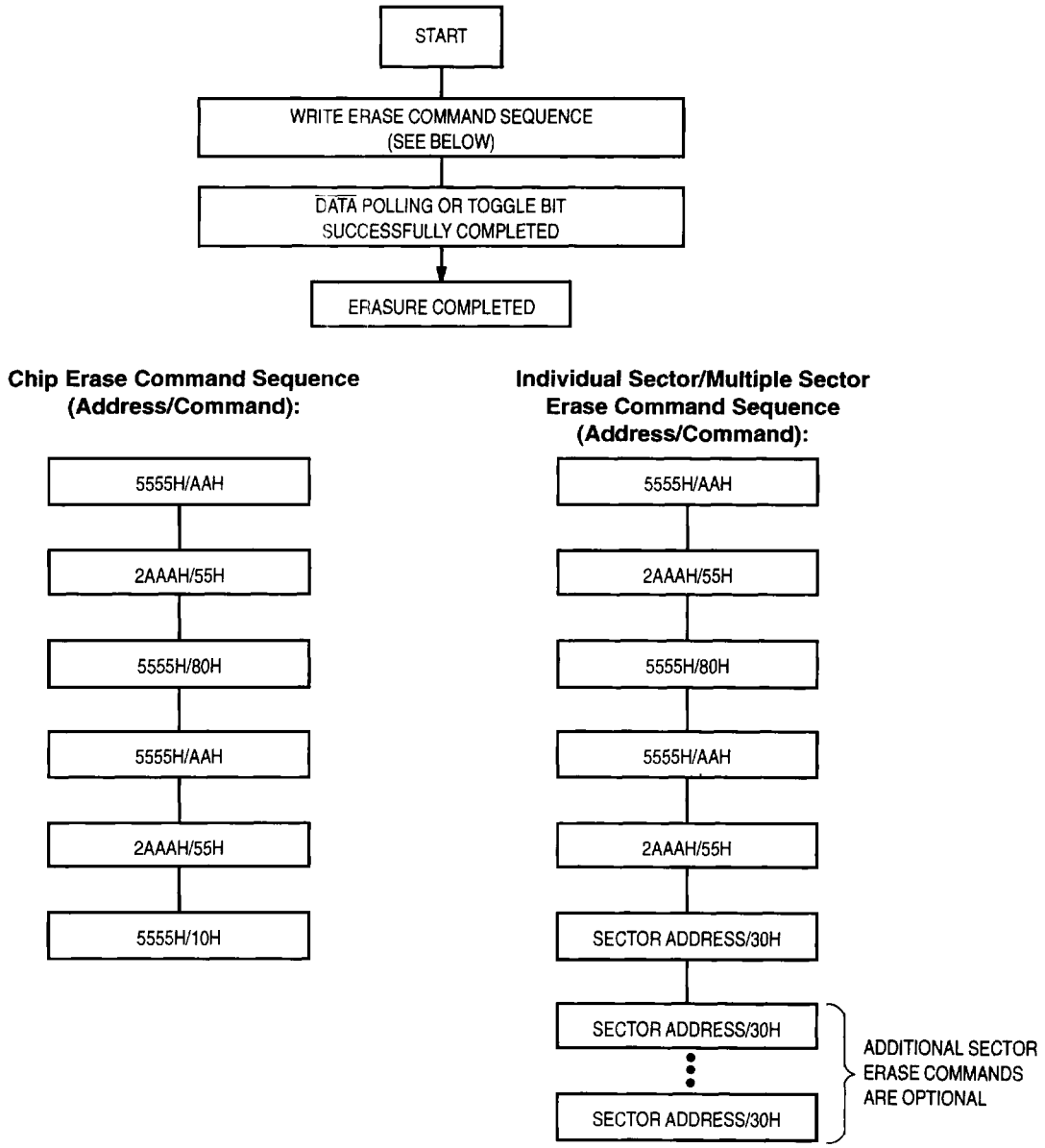
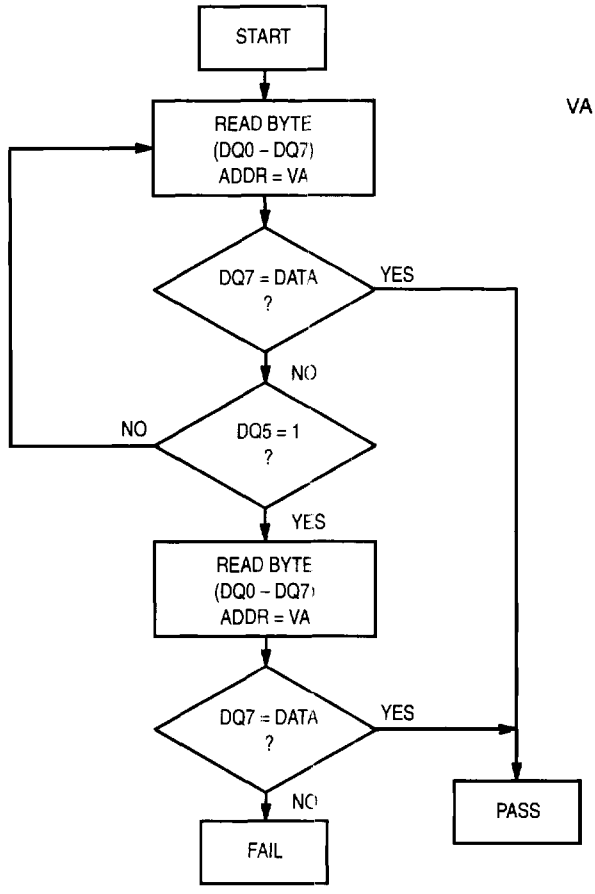


Figure 3. Embedded Erase Algorithm

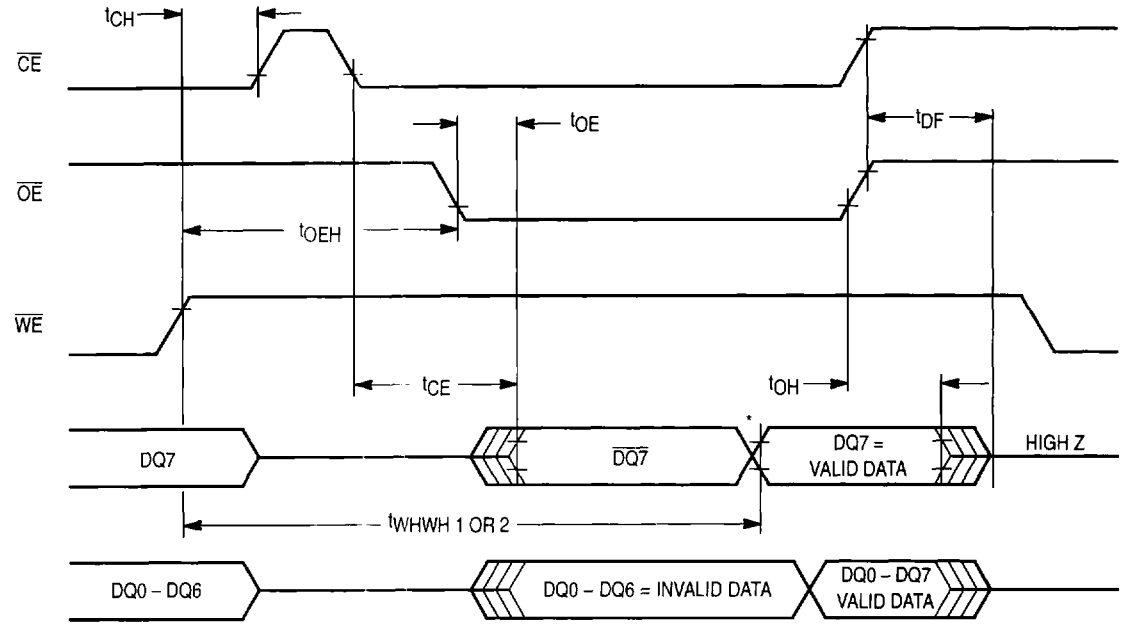
Table 7. Embedded Erase Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Embedded Erase Algorithm	
Read		Data Polling to Verify Erasure



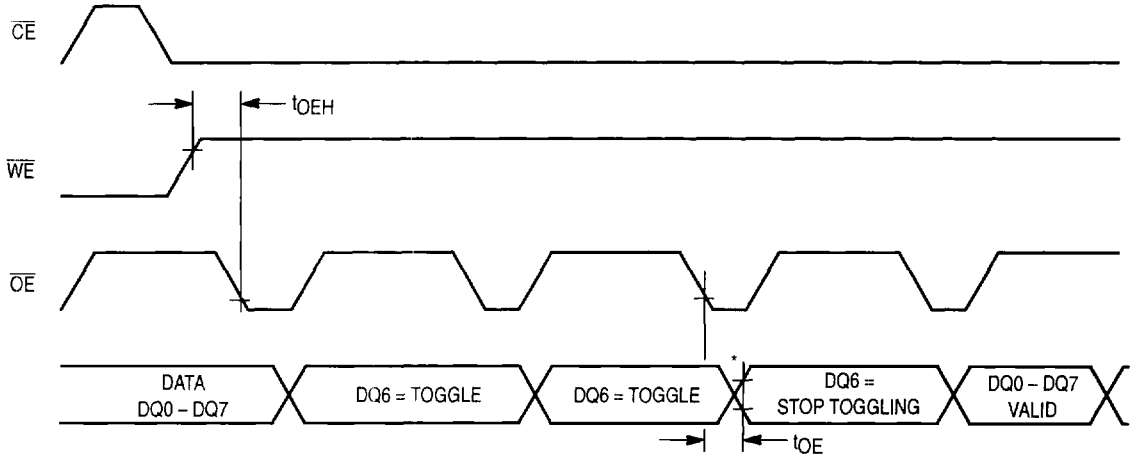
NOTE: DQ7 is rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

Figure 4. $\overline{\text{Data}}$ Polling Algorithm



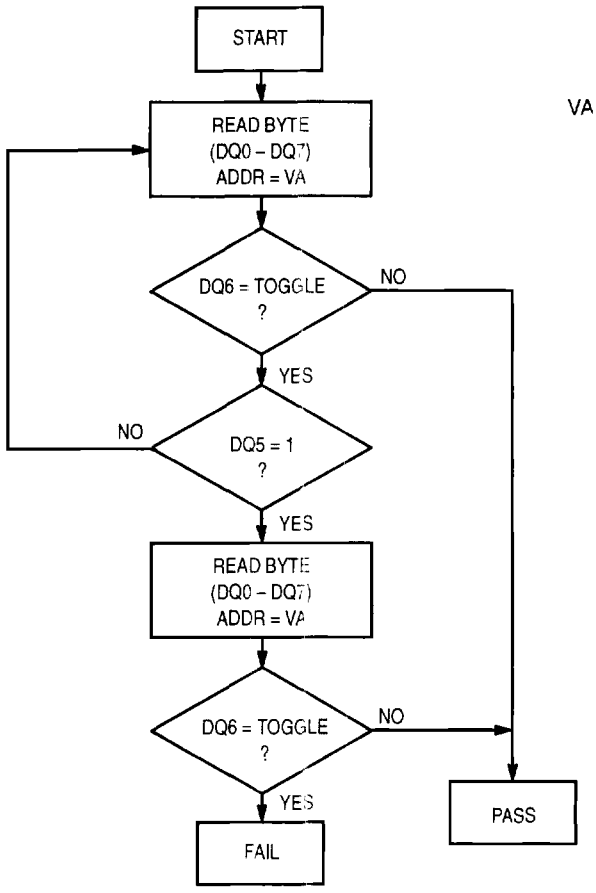
*DQ7 = Valid Data (the device has completed the embedded operation).

Figure 5. AC Waveforms for Data Polling During Embedded Algorithm Operations



*DQ6 Stops Toggling (the device has completed the embedded operation).

Figure 6. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase

NOTE: DQ6 is rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time as DQ5 changing to 1.

Figure 7. Toggle Bit Algorithm

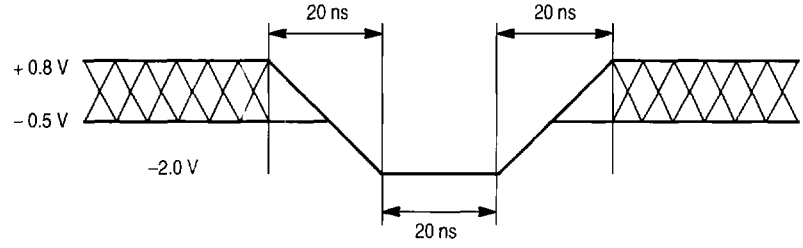


Figure 8. Maximum Undershoot Waveform

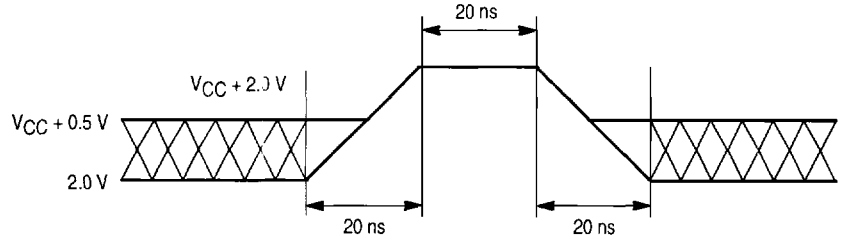


Figure 9. Maximum Overshoot Waveform

SECTOR PROTECTION ALGORITHMS

SECTOR PROTECTION

The device features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A16, A15, and A14. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A16, A15, and A14) define a particular sector, will produce 01H at data outputs (DQ0 – DQ7) for a protected sector.

SECTOR UNPROTECT

The device also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A9. The address pins A6, A7, and A12 should be set to A7 = A12 = V_{IH}, and A6 = V_{IL}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IH}. Performing a read operation at address location XXX2H, where the higher order addresses (A16, A15, and A14) define a particular sector address, will produce 00H at data outputs (DQ0 – DQ7) for an unprotected sector.

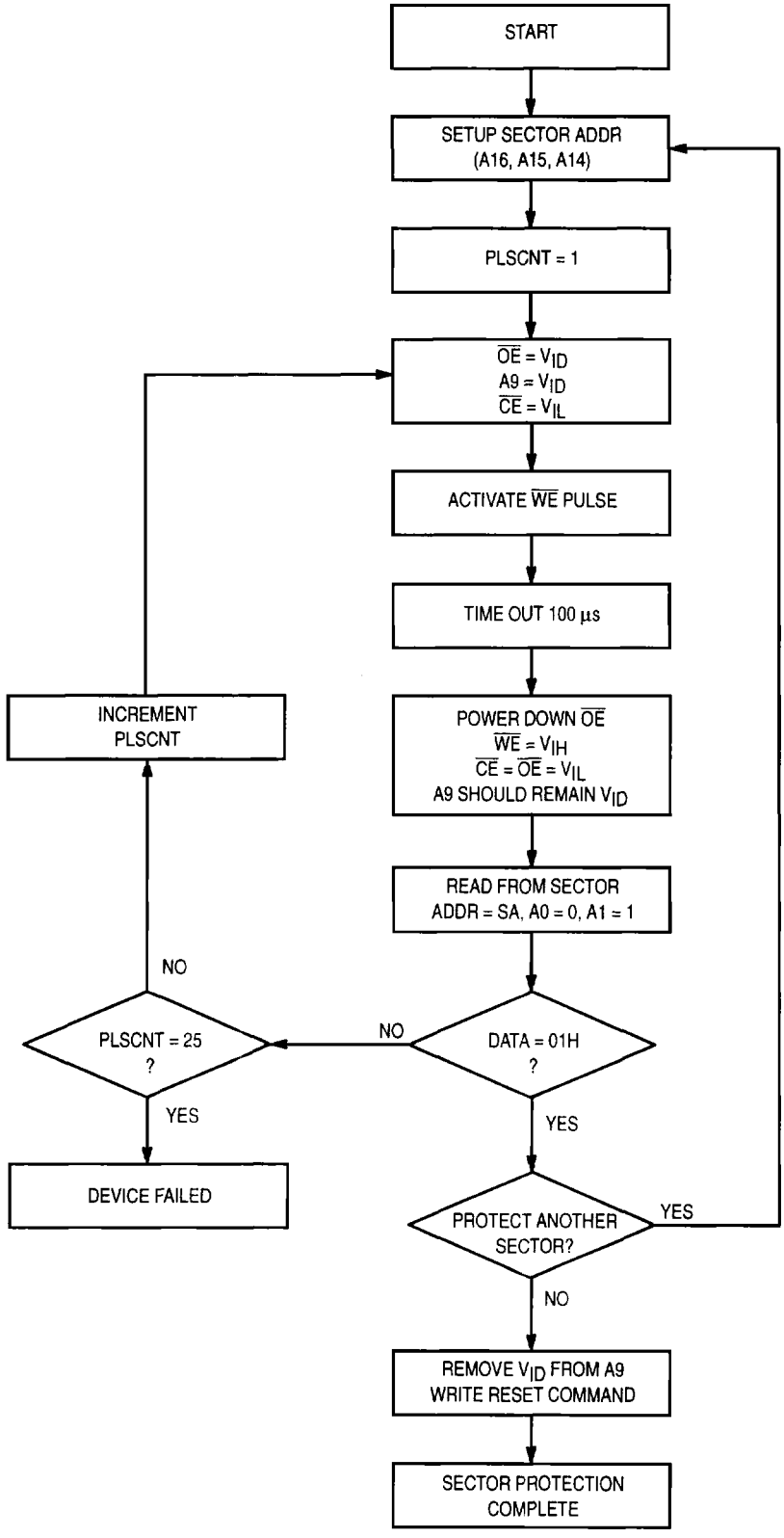


Figure 10. Sector Protection Algorithm

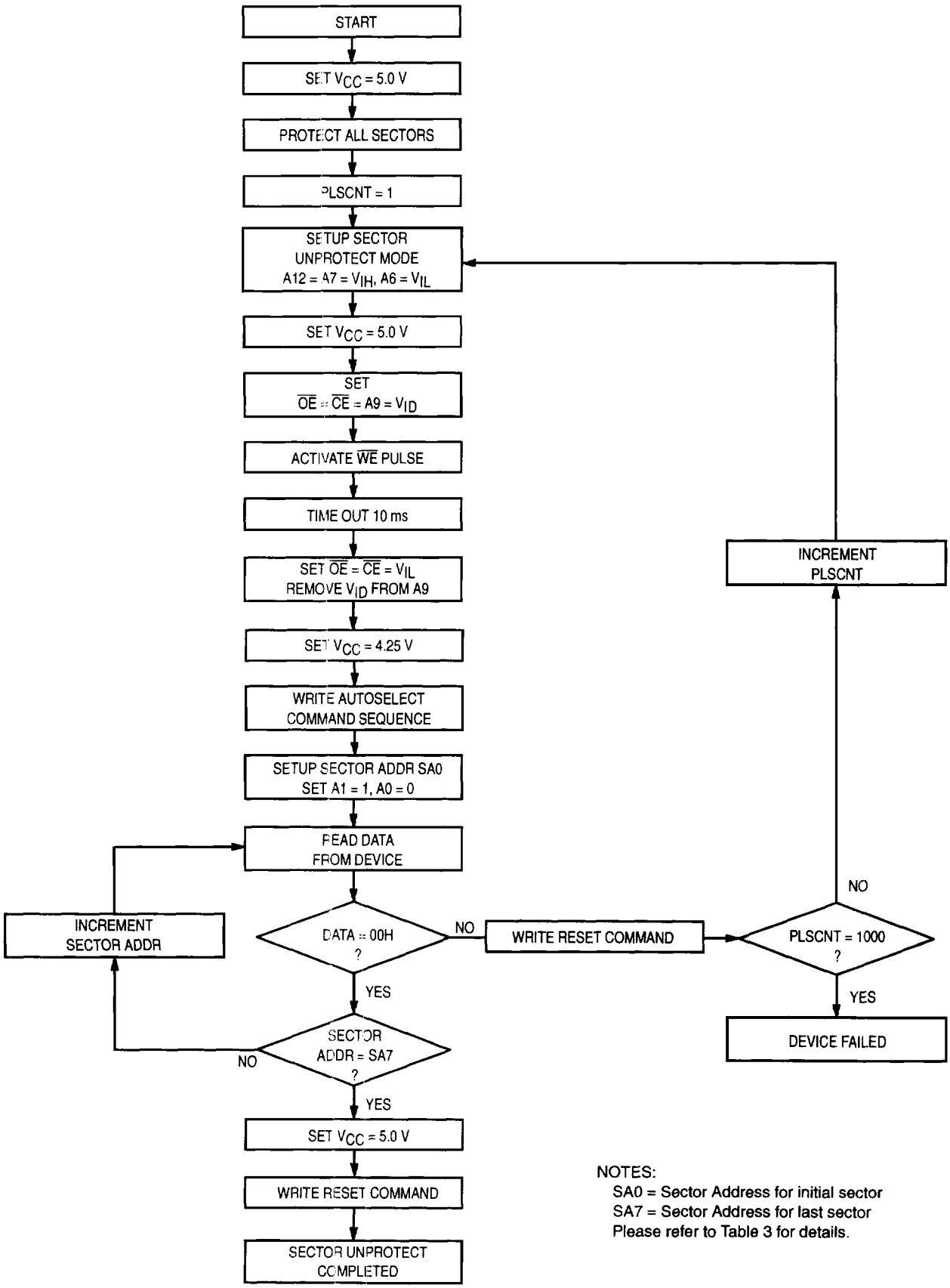
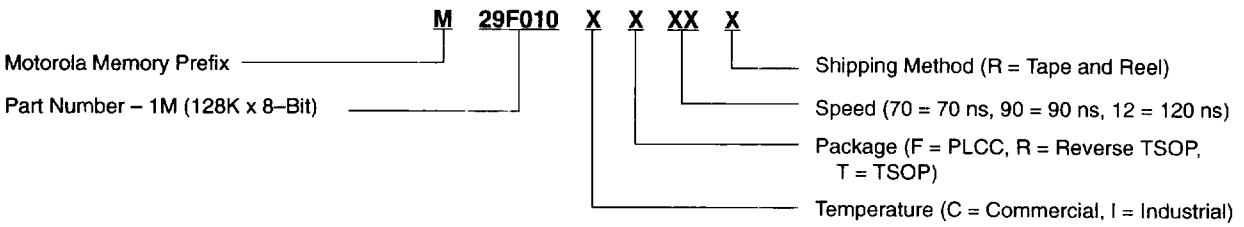


Figure 11. Sector Unprotect Algorithm

ORDERING INFORMATION
(Order by Full Part Number)

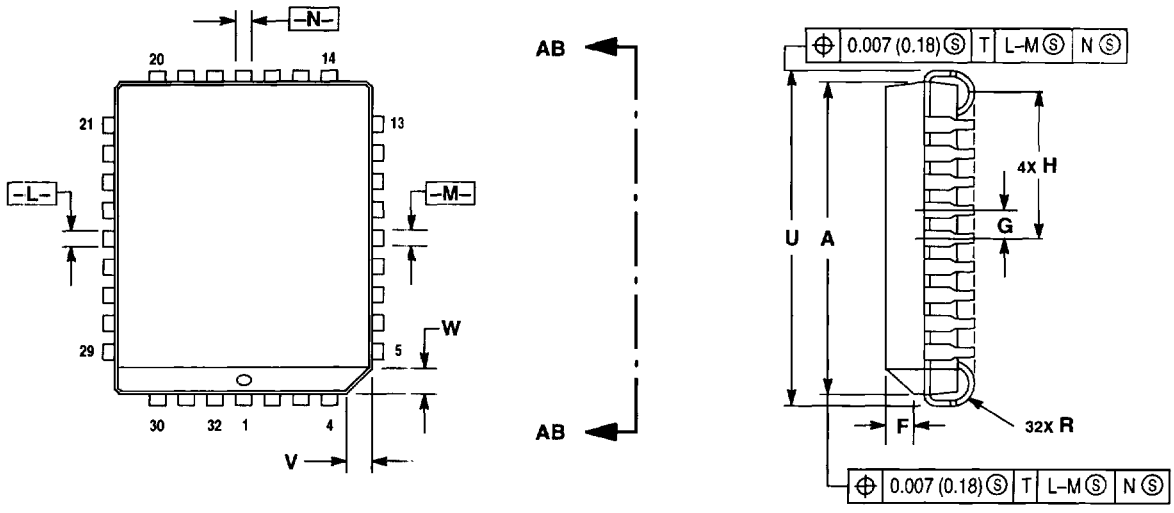


Full Part Numbers —

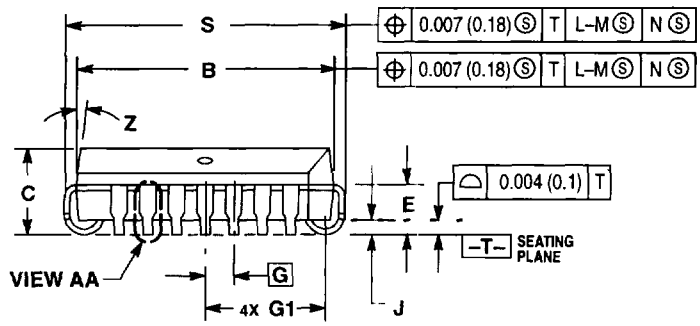
M29F010CT70	M29F010CT90	M29F010CT12
M29F010CR70	M29F010CR90	M29F010CR12
M29F010CF70	M29F010CF90	M29F010CF12
M29F010CT70R	M29F010CT90R	M29F010CT12R
M29F010CR70R	M29F010CR90R	M29F010CR12R
M29F010CF70R	M29F010CF90R	M29F010CF12R
M29F010IT70	M29F010IT90	M29F010IT12
M29F010IR70	M29F010IR90	M29F010IR12
M29F010IF70	M29F010IF90	M29F010IF12
M29F010IT70R	M29F010IT90R	M29F010IT12R
M29F010IR70R	M29F010IR90R	M29F010IR12R
M29F010IF70R	M29F010IF90R	M29F010IF12R

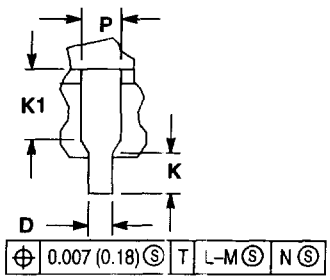
PACKAGE DIMENSIONS

F PACKAGE
32–PIN PLCC
CASE 989A–01



VIEW AB–AB



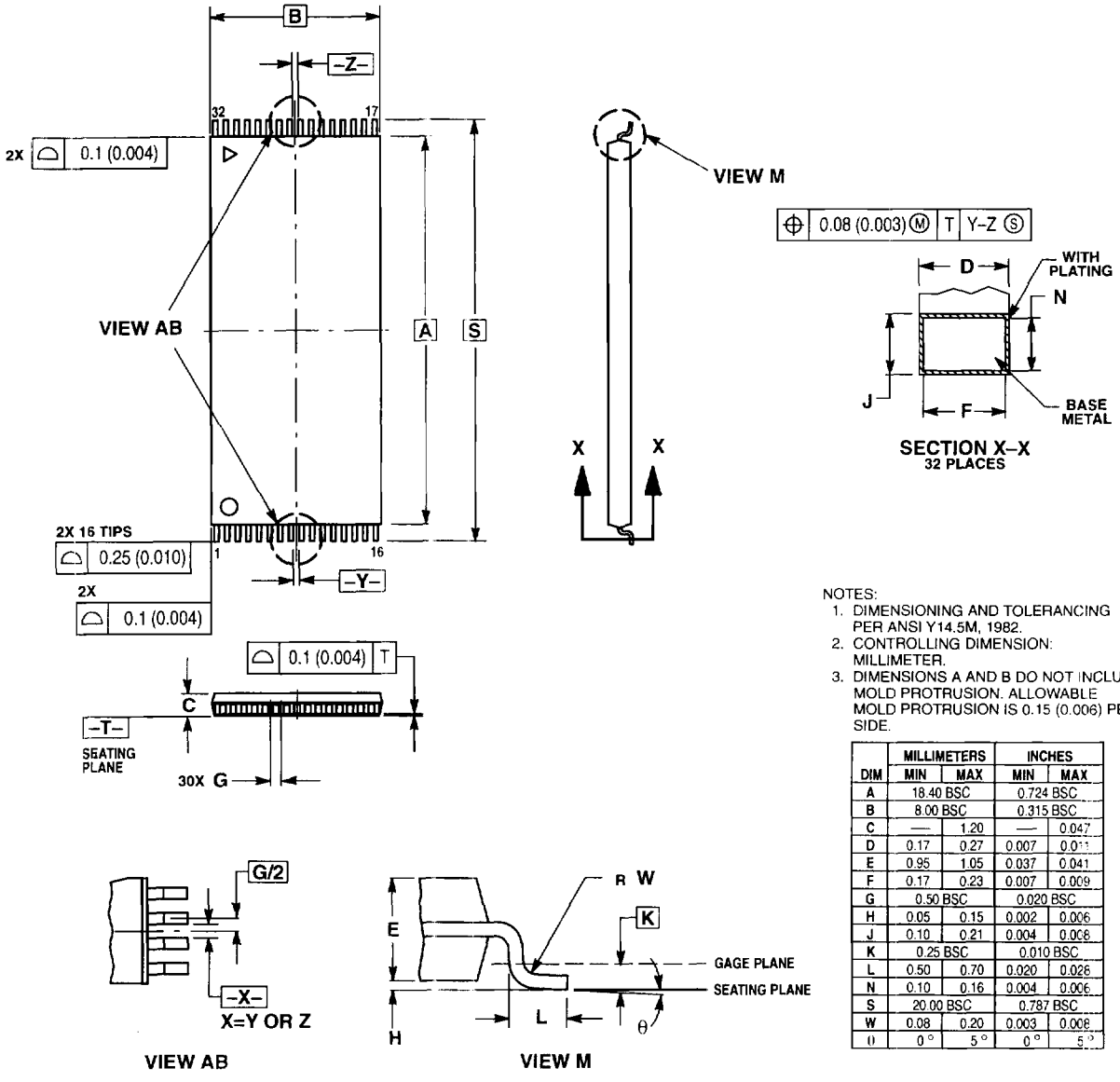


VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DATUMS L, M, AND N DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSIONS G1 AND H MEASURED AT CLOSEST APPROACH OF RADIUS TO SEATING PLANE.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.3). DIMENSIONS S AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION P DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSIONS(S) SHALL NOT CAUSE THE P DIMENSIONTO BE SMALLER THAN 0.025 (0.64).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.447	0.453	11.35	11.51
B	0.547	0.553	13.89	14.05
C	0.125	0.140	3.18	3.56
D	0.013	0.021	0.33	0.53
E	0.080	0.095	2.03	2.41
F	0.042	0.056	1.07	1.42
G	0.050 BSC		1.27 BSC	
G1	0.188	0.223	4.78	5.66
H	0.238	0.273	6.05	6.93
J	0.020	—	0.51	—
K	0.025	—	0.64	—
K1	0.025	—	0.64	—
P	0.026	0.032	0.66	0.81
R	0.025	0.045	0.64	1.14
S	0.585	0.595	14.86	15.11
U	0.485	0.495	12.32	12.57
V	0.042	0.048	1.07	1.22
W	0.042	0.048	1.07	1.22
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°

T PACKAGE
32–PIN TSOP
CASE 1110–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.40 BSC		0.724 BSC	
B	8.00 BSC		0.315 BSC	
C	—	1.20	—	0.047
D	0.17	0.27	0.007	0.011
E	0.95	1.05	0.037	0.041
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	0.25 BSC		0.010 BSC	
L	0.50	0.70	0.020	0.028
N	0.10	0.16	0.004	0.006
S	20.00 BSC		0.787 BSC	
W	0.08	0.20	0.003	0.008
θ	0°	5°	0°	5°

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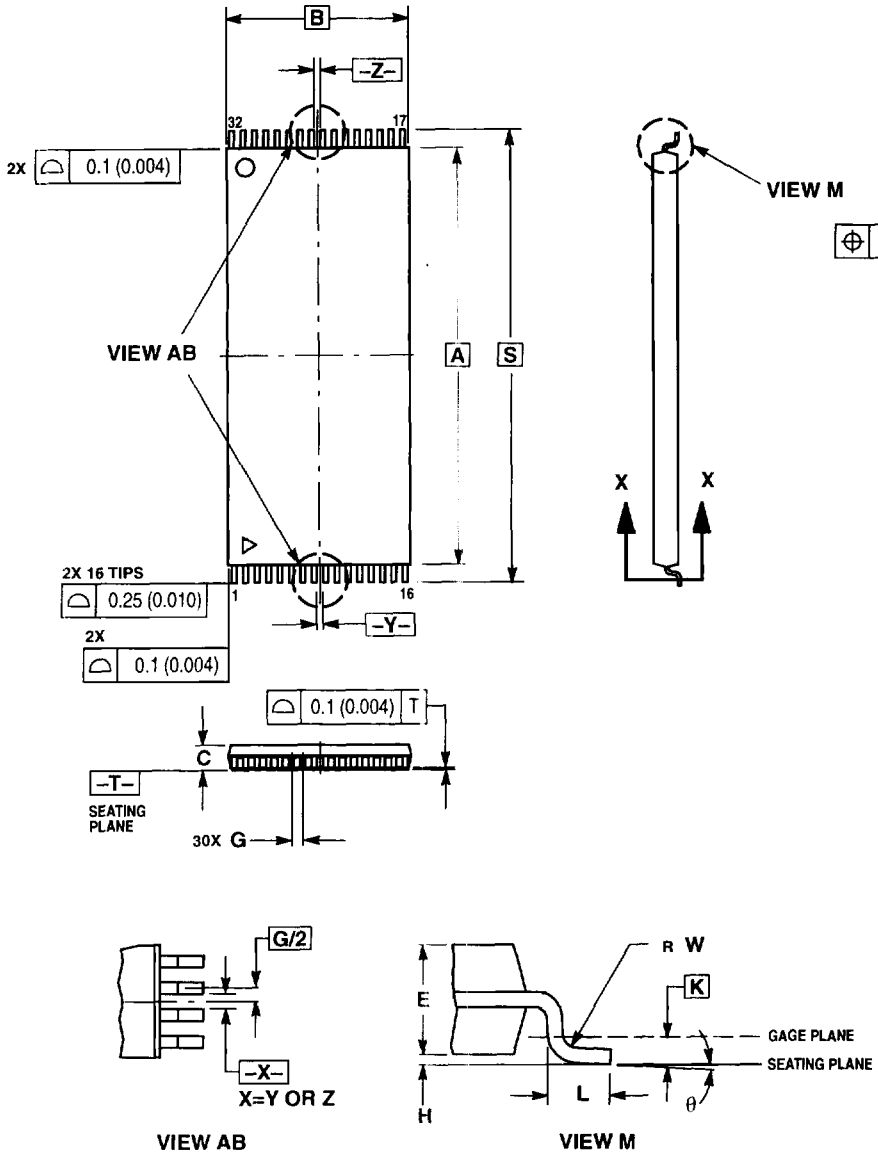
R PACKAGE
32–PIN REVERSE TSOP
CASE 1110A–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.40 BSC		0.724 BSC	
B	8.00 BSC		0.315 BSC	
C	—	1.20	—	0.047
D	0.17	0.27	0.007	0.011
E	0.95	1.05	0.037	0.041
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	0.25 BSC		0.010 BSC	
L	0.50	0.70	0.020	0.028
N	0.10	0.16	0.004	0.006
S	20.00 BSC		0.787 BSC	
W	0.08	0.20	0.003	0.008
θ	0°	5°	0°	5°

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