ANALOG DEVICES

Low Distortion 750 MHz Closed-Loop Buffer Amp

AD9630*

T-79-25

FEATURES
Excellent Gain Accuracy: 0.99 V/V
Wide Bandwidth: 750 MHz
Slew Rate: 1200 V/µs
Low Distortion
    −66 dBc @ 20 MHz
    −80 dBc @ 4.3 MHz
Settling Time
    5 ns to 0.1%
    8 ns to 0.02%
Low Noise: 2.4 nV/√Hz
Improved Source for CLC-110

APPLICATIONS
IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

General Description
The AD9630 is a monolithic buffer amplifier that utilizes innovative (patent pending) closed-loop design techniques to achieve exceptional gain accuracy, wide bandwidth, and low distortion. Slew rate limiting has been overcome as indicated by the 1200 V/µs slew rate; this improvement allows the user greater flexibility in wideband and pulse applications. The second harmonic distortion terms for an analog input tone of 4.3 MHz and 20 MHz are −80 dBc and −66 dBc, respectively. Clearly, the AD9630 establishes a new standard by combining in one part outstanding dc and dynamic performance.

The large signal bandwidth, low distortion over frequency, and drive capabilities of the AD9630 make the buffer an ideal flash ADC driver. The AD9630 provides better signal fidelity than many of the flash ADCs that it has been designed to drive. Other applications which require increased current drive at unity voltage gain such as cable driving benefit from the AD9630's performance.

The AD9630 is available in four 8-pin package styles including Plastic DIP (N), Ceramic DIP (Q), SOIC (R), and Ceramic SOIC (Z). Both Ceramic packages are processed to MIL-STD-883; consult with the factory concerning availability. The "A" grades are guaranteed for −40°C to +85°C; "S" grades are guaranteed from −55°C to +125°C. Die are dc tested at 25°C.

*Patent(s) Pending
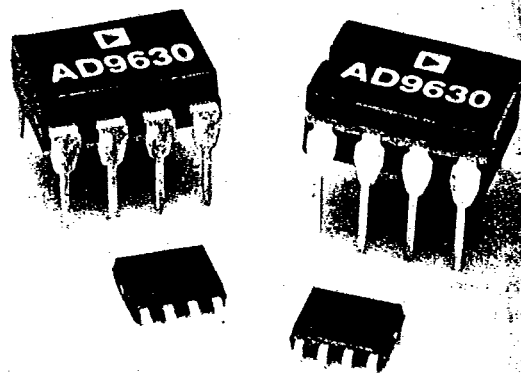
ORDERING INFORMATION

Part Number	Temperature Range	Package	
AD9630AN	−40°C to +85°C	8-Pin Plastic	
AD9630AR	−40°C to +85°C	8-Pin SOIC	
AD9630AQ	−40°C to +85°C	8-Pin Cerdip	
AD9630SZ†	−55°C to +125°C	8-Pin Ceramic SOIC	
AD9630SQ†	−55°C to +125°C	8-Pin Cerdip	
AD9630 Chips	+25°C	Dice	

NOTE
†Consult factory about MIL-STD-883 compliant devices.

AD9630 PIN CONFIGURATION

```
        +Vₛ [1]  •      [8] OUTPUT
         •• [2]         [7] NC
         NC [3]         [6] •••
      INPUT [4] AD9630  [5] −Vₛ
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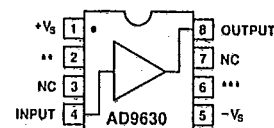
**OPTIONAL +Vₛ ***OPTIONAL −Vₛ NC = NO CONNECT

NOTE: FOR BEST SETTLING TIME PERFORMANCE USE OPTIONAL POWER SUPPLIES. ALL SPECIFICATIONS ARE BASED ON USING SINGLE ±Vₛ CONNECTIONS EXCEPT FOR SETTLING TIME TO 0.02% AND SMALL SIGNAL S21. CONSULT THE FACTORY FOR VERSIONS WITH OPTIONAL POWER SUPPLY PINS DISCONNECTED INTERNAL TO THE PACKAGE.

AD9630 DIE LAYOUT
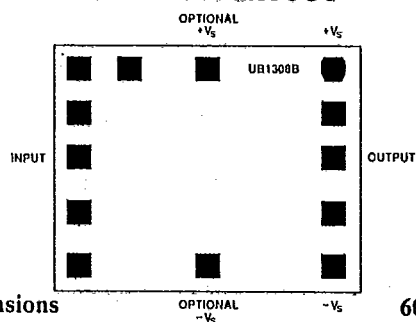
Die Dimensions   60×50×15 mils

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . ±7 V
Continuous Output Current[2] . . . . 70 mA
Temperature Range over Which Specifications Apply
    AD9630AN/AR/AQ . . . . −40°C to +85°C
    AD9630SZ/SQ . . . . −55°C to +125°C
Lead Soldering Temperature (10 sec) . . . . +300°C

Storage Temperature
    AD9630AN/AR . . . . −65°C to +150°C
    AD9630SZ/SQ/AQ . . . . −65°C to +150°C
Junction Temperature[3]
    AD9630AN/AR . . . . +150°C
    AD9630SZ/SQ/AQ . . . . +175°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50$ Ω, $R_{LOAD} = 100$ Ω)

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9630A/N/R/Q Min	Typ	Max	AD9630S/Q/Z Min	Typ	Max	Units
DC SPECIFICATIONS											
Output Offset Voltage		+25°C	I	1	−8	±3	+8	−8	±3	+8	mV
Offset Voltage TC		Full	IV		−25	±8	+25	−25	±8	+25	µV/°C
Input Bias Current		+25°C	I	1	−25	±2	+25	−25	±2	+25	µA
Bias Current TC		Full	IV		−100	±20	+100	−100	±20	+100	nA/°C
Input Resistance		+25 to T_{max}	II	1, 2	300	450		300	450		kΩ
Input Resistance		T_{min}	VI	3	150	250		150	250		kΩ
Input Capacitance		+25°C	V			1.0			1.0		pF
Gain	$V_{OUT} = 2$ V p-p	+25 to T_{max}	II	1, 2	0.983	0.990		0.983	0.990		V/V
Gain	$V_{OUT} = 2$ V p-p	T_{min}	VI	3	0.980	0.985		0.980	0.985		V/V
Output Voltage Range		Full	VI	1, 2, 3	+3.2	±3.6	−3.2	+3.2	±3.6	−3.2	V
Output Current (50 Ω Load)		+25 to T_{max}	II	1, 2	50			50			mA
Output Current (50 Ω Load)		T_{min}	VI	3	40			40			mA
Output Impedance	At dc	+25°C	V			0.6			0.6		Ω
PSRR	$\Delta V_S = \pm5\%$	Full	VI	4, 5, 6	44	55		44	55		dB
DC Nonlinearity	±2 V Full Scale	+25°C	V			0.03			0.03		%
FREQUENCY DOMAIN											
Bandwidth (−3 dB)											
Small Signal	$V_O \leq 0.7$ V p-p	T_{min} to 25	II	4, 6	400	750		400	750		MHz
Small Signal	$V_O \leq 0.7$ V p-p	T_{max}	II	5	330	550		330	550		MHz
Large Signal	$V_O = 5$ V p-p	T_{min} to 25	IV		80	120		80	120		MHz
Large Signal	$V_O = 5$ V p-p	T_{max}	IV		70	105		70	105		MHz
Output Peaking	≤200 MHz	Full	II	4, 5, 6		0.4	1.2		0.4	1.2	dB
Output Rolloff	≤200 MHz	Full	II	4, 5, 6		0	0.3		0	0.3	dB
Group Delay	dc to 150 MHz	+25°C	V			0.7			0.7		ns
Linear Phase Deviation	dc to 150 MHz	+25°C	V			0.7			0.7		Degrees
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV			−80	−74		−80	−74	dBc
	2 V p-p; 20 MHz	Full	IV			−66	−59		−66	−59	dBc
	2 V p-p; 60 MHz	Full	II	4, 5, 6		−52	−43		−52	−43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV			−86	−79		−86	−79	dBc
	2 V p-p; 20 MHz	Full	IV			−75	−68		−75	−68	dBc
	2 V p-p; 60 MHz	T_{min} to +25	II	4, 6		−50	−43		−50	−43	dBc
	2 V p-p; 60 MHz	T_{max}	II	5		−46	−40		−46	−40	dBc
Spectral Input Noise Voltage	10 MHz	+25°C	V			2.4			2.4		nV/$\sqrt{Hz}$
Integrated Output Noise	100 kHz – 200 MHz	+25°C	V			32			32		µV
TIME DOMAIN											
Slew Rate	$V_{OUT} = 5$ V Step	+25°C	IV		800	1200		800	1200		V/µs
Rise/Fall Time	$V_{OUT} = 1$ V Step	T_{min} to +25	IV			0.9	1.3		0.9	1.3	ns
	$V_{OUT} = 1$ V Step	T_{max}	IV			1.1	1.6		1.1	1.6	ns
	$V_{OUT} = 5$ V Step	T_{min} to +25	IV			3.9	5.4		3.9	5.4	ns
	$V_{OUT} = 5$ V Step	T_{max}	IV			4.5	6.1		4.5	6.1	ns
Overshoot Amplitude	$V_{OUT} = 2$ V Step	Full	IV			2	12		2	12	%
Settling Time											
To 0.1%	$V_{OUT} = 2$ V Step	T_{min} to +25	IV			5	8		5	8	ns
To 0.1%	$V_{OUT} = 2$ V Step	T_{max}	IV			7	12		7	12	ns
To 0.02%	$V_{OUT} = 2$ V Step	T_{min} to +25	IV			8	13		8	13	ns
To 0.02%	$V_{OUT} = 2$ V Step	T_{max}	IV			12	18		12	18	ns
Differential Gain	4.4 MHz	+25°C	V			0.015			0.015		%
Differential Phase	4.4 MHz	+25°C	V			0.025			0.025		Degree
SUPPLY CURRENTS											
V_{CC} (+I_S)	$V_{CC} = +5$ V	Full	II	1, 2, 3		19	26		19	26	mA
V_{EE} (−I_S)	$V_{EE} = −5$ V	Full	II	1, 2, 3		19	26		19	26	mA

NOTES
[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2] Output is short-circuit protected to ground, but not to supplies. Prolonged short circuit to ground may affect device reliability.

[3] Typical thermal impedances (part soldered onto board):

Mini-DIP (N):	$\theta_{JA} = 110°C/W$; $\theta_{JC} = 30°C/W$.	SOIC (R):	$\theta_{JA} = 150°C/W$; $\theta_{JC} = 50°C/W$.
Cerdip (Q):	$\theta_{JA} = 110°C/W$; $\theta_{JC} = 20°C/W$.	Ceramic Gull Wing (Z):	$\theta_{JA} = 100°C/W$; $\theta_{JC} = 20°C/W$.

[4] Military subgroups apply only to military qualified devices.

EXPLANATION OF TEST LEVELS

Test Level

I   100% Production tested.

II   100% Production tested at +25°C and sample tested at specified temperatures. AC testing of AN and AR grades done on sample basis only.

III   Sample tested only.

IV   Parameter is guaranteed by design and characterization testing.

V   Typical value.

VI   S versions are 100% production tested at temperature extremes. Other grades are sample tested at extremes.

EXPLANATION OF MILITARY SUBGROUPS

Subgroup   1   Static tests at +25°C.
(5% PDA calculated against Subgroup 1 for high-rel versions)

Subgroup   2   Static tests at maximum rated operating temperature.

Subgroup   3   Static tests at minimum rated operating temperature.

Subgroup   4   Dynamic tests at +25°C.

Subgroup   5   Dynamic tests at maximum rated operating temperature.

Subgroup   6   Dynamic tests at minimum rated operating temperature.

Subgroup   7   Functional tests at +25°C.

Subgroup   8   Functional tests at maximum and minimum rated temperatures.

Subgroup   9   Switching tests at +25°C.

Subgroup   10   Switching tests at maximum rated operating temperature.

Subgroup   11   Switching tests at minimum rated operating temperature.
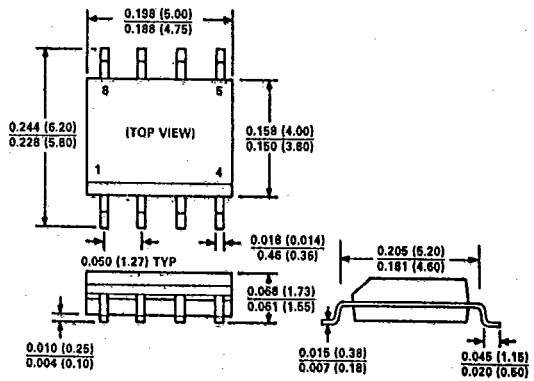
Subgroup   12   Periodically sample tested.

OUTLINE DIMENSIONS
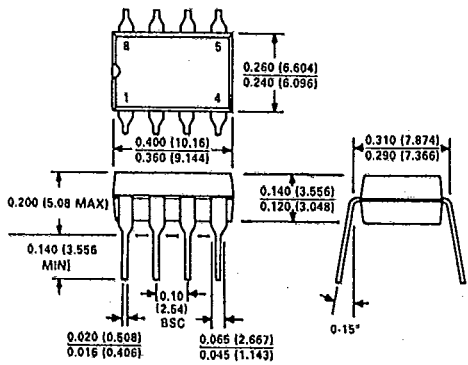Dimensions shown in inches and (mm).
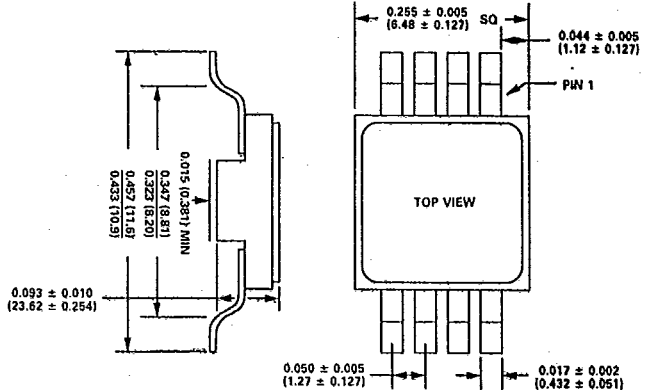
Cerdip (Q) Package Drawing
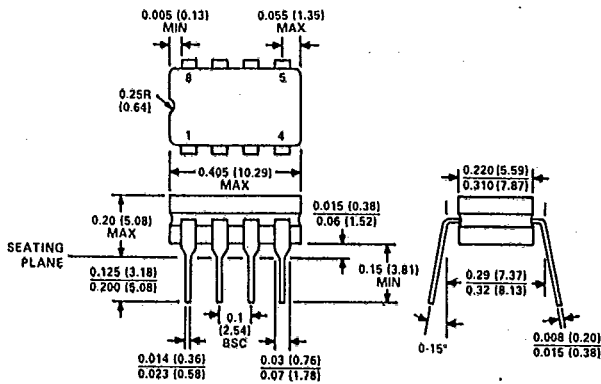
SOIC (R) Package Drawing

Plastic DIP (N) Package Drawing

Ceramic Gull-Wing (Z) Package Drawing

AD9630 Burn-In Circuit

Figure 2. Frequency Response vs. C_L
with Recommended R_S
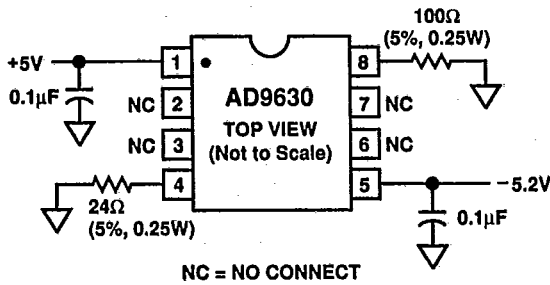
THEORY OF OPERATION

The AD9630 is a wide-bandwidth, closed-loop, unity-gain buffer which makes use of a new voltage-feedback architecture (Patent Pending). This architecture brings together wide bandwidth and high slew rate along with exceptional dc linearity. Most previous wide bandwidth buffers achieved their bandwidth by utilizing an open-loop topology which sacrificed both dc linearity and frequency distortion when driven into low load impedances. The design's high loop correction factor radically improves dc linearity and distortion characteristics without diminishing bandwidth. This, in combination with high slew rate, results in exceptionally low distortion over a wide frequency range.

The AD9630 is an excellent choice to drive high speed and high resolution analog-to-digital Converters. Its output stage is designed to drive high speed flash converters with minimal or no series resistance. A current booster built into the output driver helps to maintain low distortion.

Parasitic or load capacitance (>7 pF) connected directly to the AD9630 output will result in frequency peaking. A small series resistor (R_S) connected between the buffer output and capacitive load will negate this effect. Figure 1 shows the optimal value of R_S as a function of C_L to obtain the flattest frequency response. Figure 2 illustrates frequency response for various capacitive loads utilizing the recommended R_S.

In pulse mode applications, with R_S equal to approximately 12 ohms, capacitive loads of up to 50 pF can be driven with minimal settling time degradation.

The output stage has short circuit protection to ground. The output driver will shut down if more than approximately 130 mA of instantaneous sink or source current is reached. This level of current ensures that output clipping will not result when driving heavy capacitive loads during high slew conditions. Though average load currents above 70 mA may reduce device reliability.

LAYOUT CONSIDERATIONS

Due to the high frequency operation of the AD9630 attention to board layout is necessary to achieve optimum dynamic performance. A two ounce copper ground plane on the top side of the board is recommended; it should cover as much of the board as possible with appropriate openings for supply decoupling capacitors as well as for load and source termination resistors. (See Figure 3.)

Figure 1. Recommended R_S vs. C_L
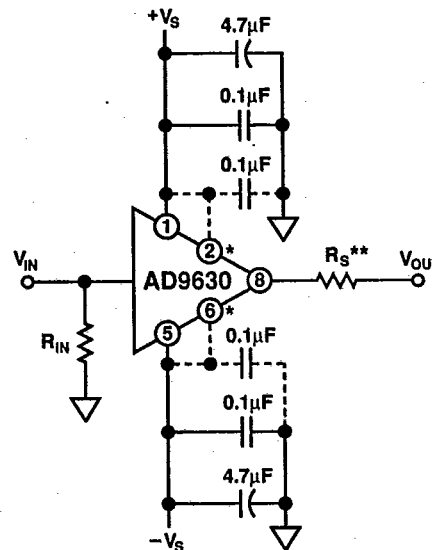
*SEE PINOUTS **SEE FIGURE 1

Figure 3. AD9630 Application Circuit

Optimum settling time and ac performance results will be achieved with surface mount 0.1 μF supply decoupling ceramic chip capacitors mounted within 50 mils of the corresponding device pins with the other side soldered directly to the ground plane. For best high resolution (<0.02%) settling times, the optional power supply pins should be decoupled as shown above. If the optional power supply pins are not used, they should be left open.

If surface mount capacitors cannot be used, radial lead ceramic capacitors with leads less than 30 mils long are recommended. Low frequency power supply decoupling is necessary and can be accomplished with 4.7 μF tantalum capacitors mounted within 0.5 inches of the supply pins. Due to the series inductance of these capacitors interacting with the 0.1 μF capacitors and power supply leads, high frequency oscillations might appear on the device output. To avoid this occurrence, the power supply leads should be tightly twisted (if appropriate). Ferrite beads mounted between the tantalum and ceramic capacitors will serve the same purpose.

All unused pins (except the optional power supply pins) should be connected to ground to reduce pin-to-pin capacitive coupling and prevent external RF interference. If the source and drive electronics require "remote" operation (> 1 inch from the AD9630), the PC board line impedances should be matched with the buffer input and output resistances. Basic micro strip techniques should be observed. R_{IN} and R_S should be connected as close to the AD9630 as possible.

With only minimal pulse overshoot and ringing, the AD9630 can drive terminated cables directly without the use of an output termination resistor (R_S). Termination resistors (R_S and R_{IN}) can be either standard carbon composition or microwave type. For matching characteristic impedances, precision microwave resistor of 1% or better tolerance are preferred.

The AD9630 should be soldered directly to the PC board with as little vertical clearance as possible. The use of zero insertion sockets is strongly discouraged because of the high effective pin inductances. Use of this type socket will result in peaking and possibly induce oscillation. Consult the factory about the availability of an evaluation board, AD9630/PCB.
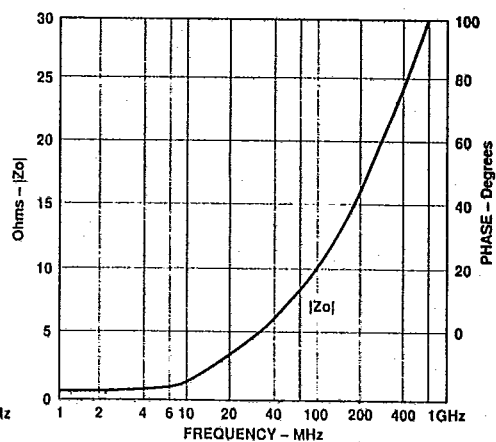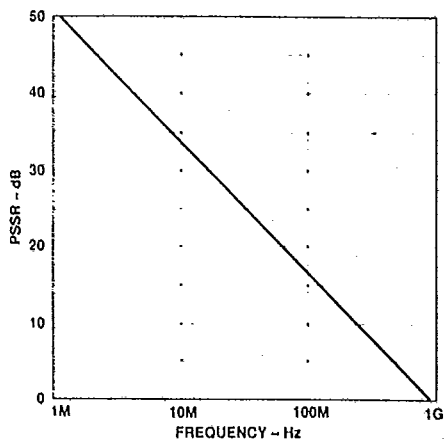
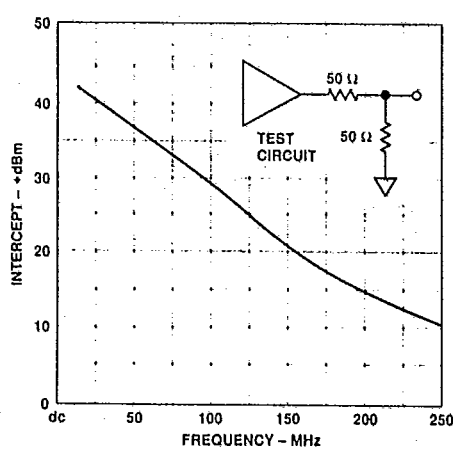# Typical Performance Curves
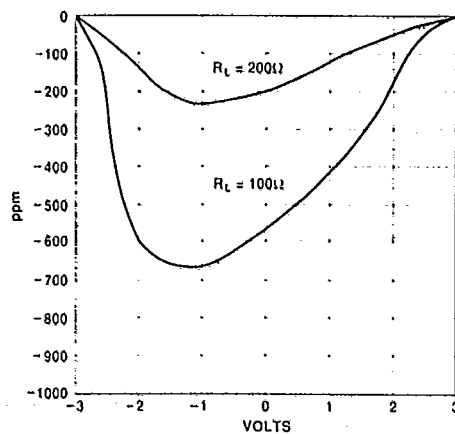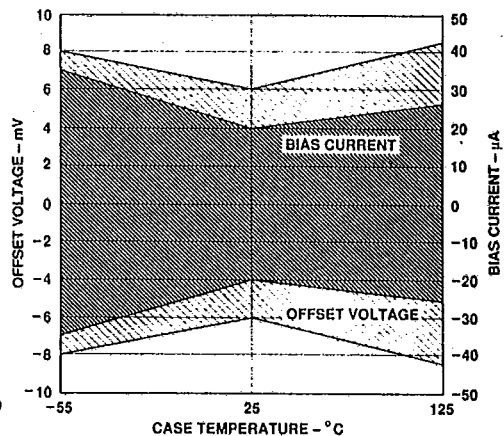

Endpoint DC Linearity Error
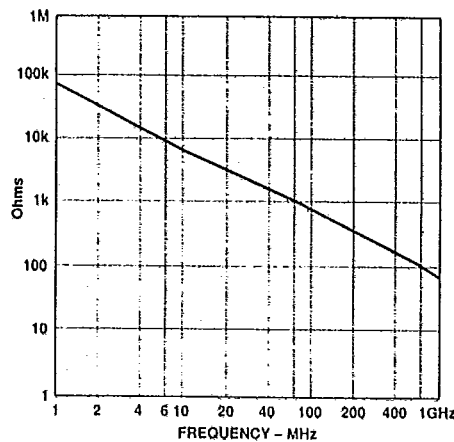
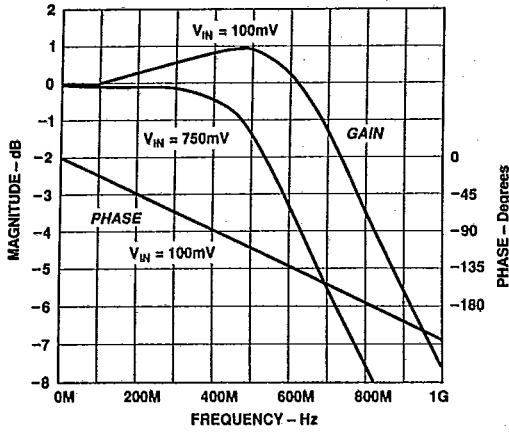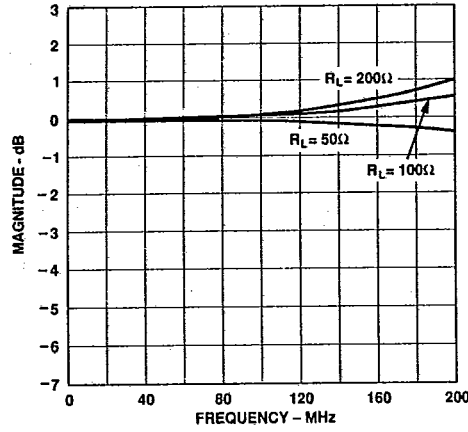Input Impedance

Output Impedance
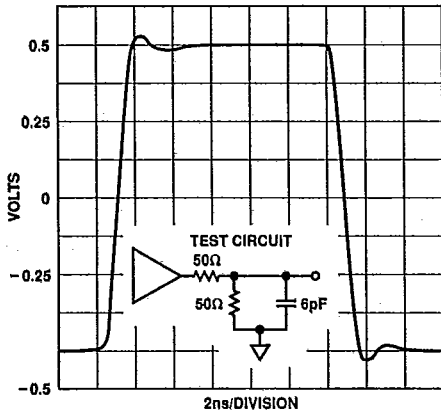

PSRR vs. Frequency

2-Tone Intermodulation Distortion

Offset Voltage and Bias Current vs. Temperature
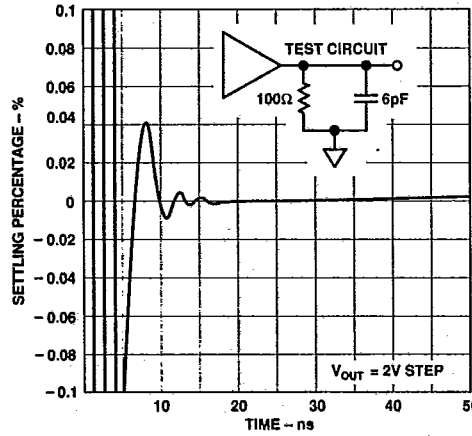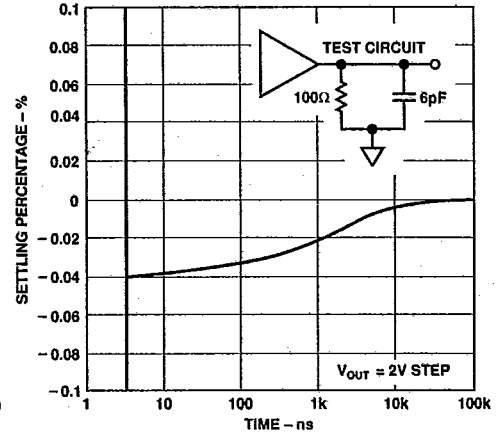
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Forward Gain and Phase

Frequency Response vs. R_{LOAD}
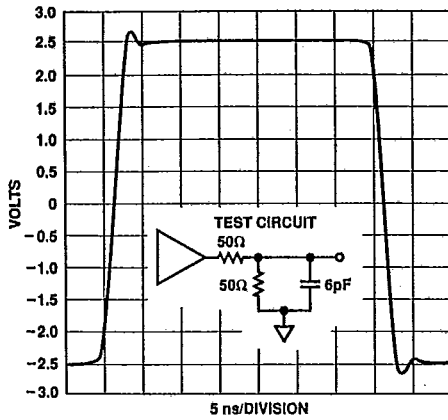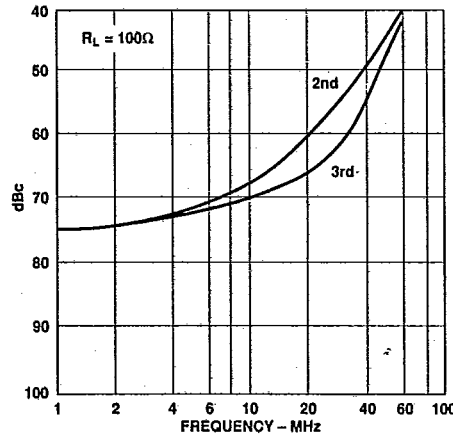
Small-Signal Pulse Response
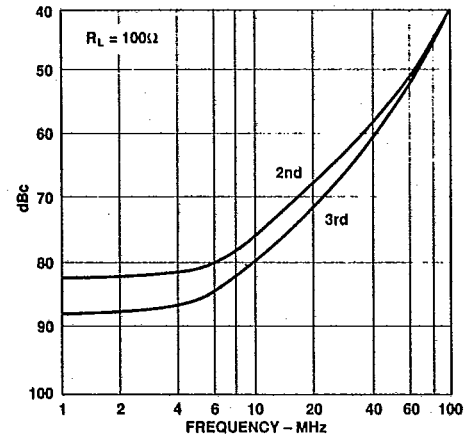
Short-Term Settling Time

Long-Term Settling Time

Large-Signal Pulse Response

Harmonic Distortion $V_{OUT} = 4\,V\,p\text{-}p$

Harmonic Distortion $V_{OUT} = 2\,V\,p\text{-}p$