

# RJK03N3DPA

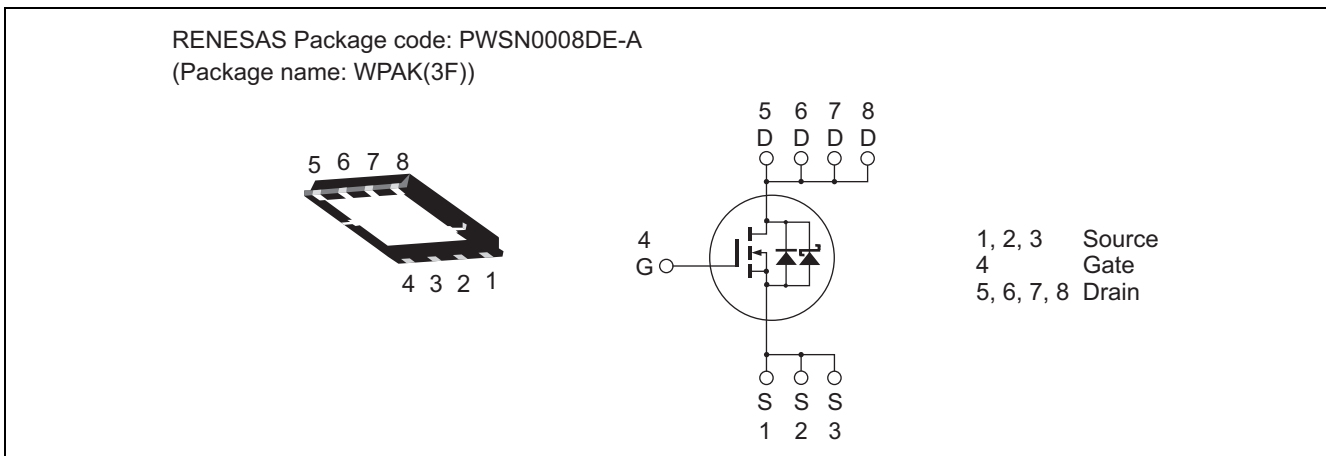
30V, 35A, 4.7mΩmax.  
 Built in SBD N Channel Power MOS FET  
 High Speed Power Switching

R07DS0784EJ0200  
 Rev.2.00  
 Feb 12, 2013

## Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
- Pb-free
- Halogen-free

## Outline



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	30	V
Gate to source voltage	V <sub>GSS</sub>	±12	V
Drain current	I <sub>D</sub>	35	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	140	A
Body-drain diode reverse drain current	I <sub>DR</sub>	35	A
Avalanche current	I <sub>AP</sub> <sup>Note 2</sup>	13	A
Avalanche energy	E <sub>AS</sub> <sup>Note 2</sup>	16.9	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	35	W
Channel to case thermal impedance	θ <sub>ch-c</sub> <sup>Note3</sup>	3.57	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
 2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω  
 3. T<sub>c</sub> = 25°C

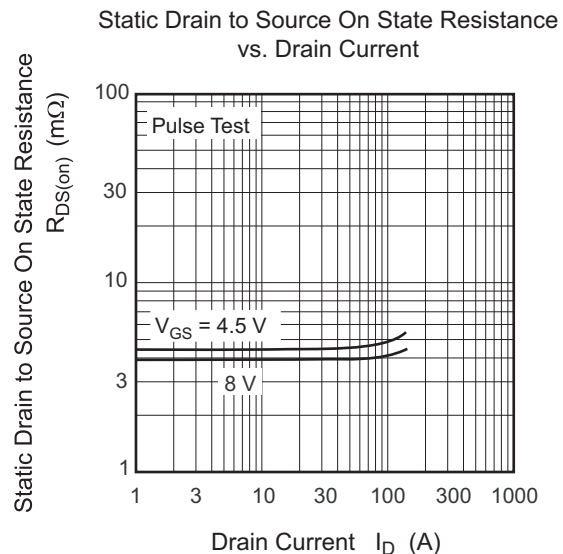
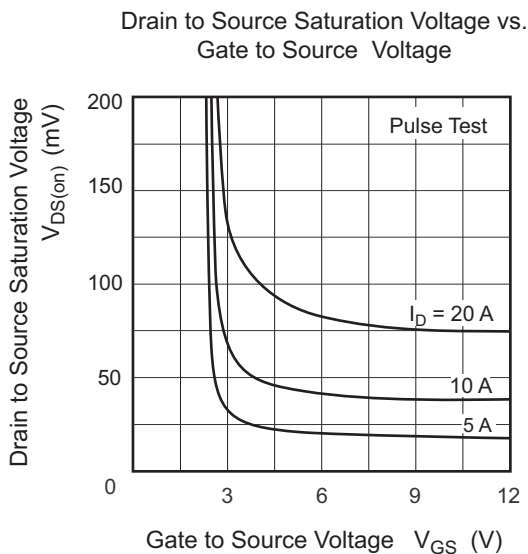
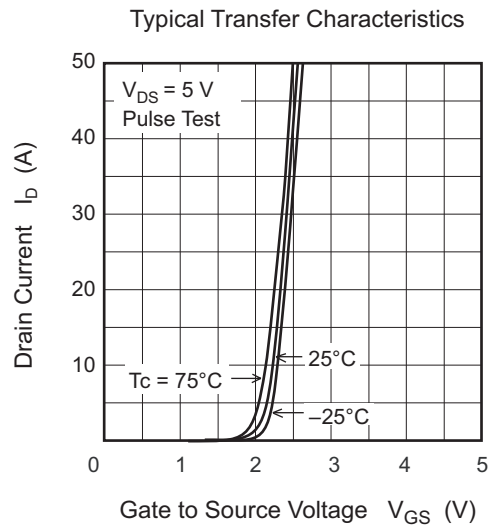
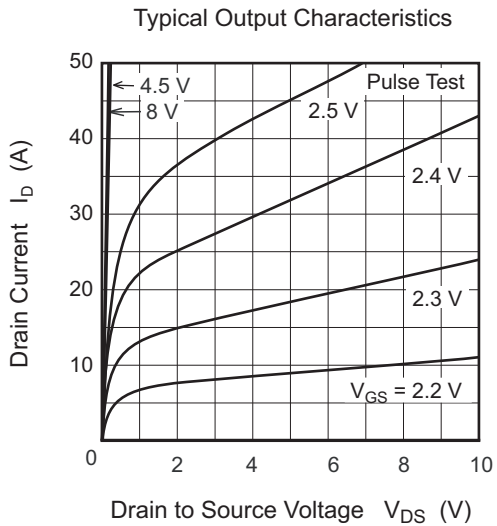
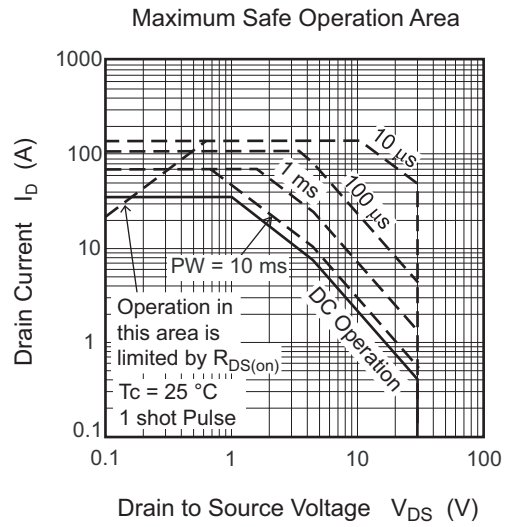
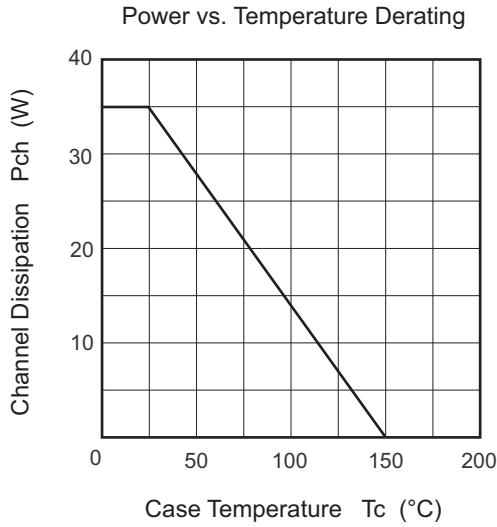
## Electrical Characteristics

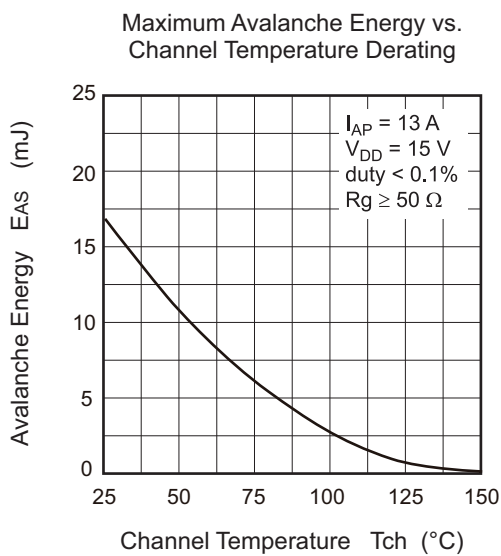
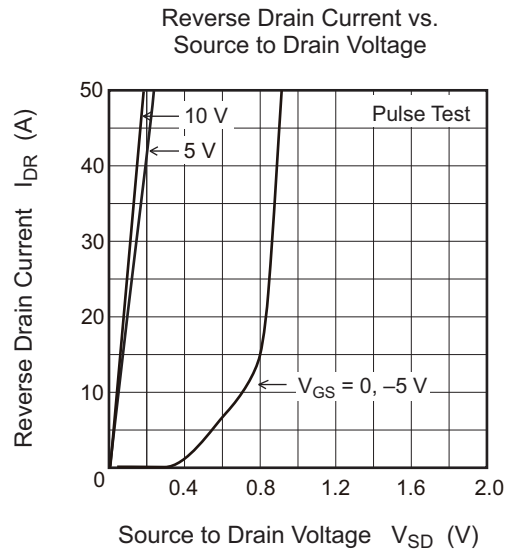
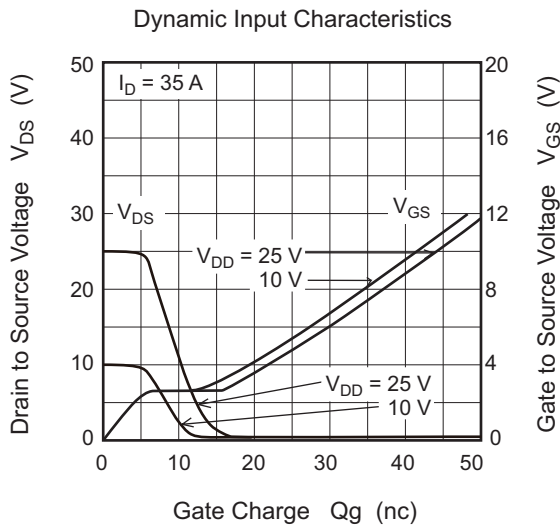
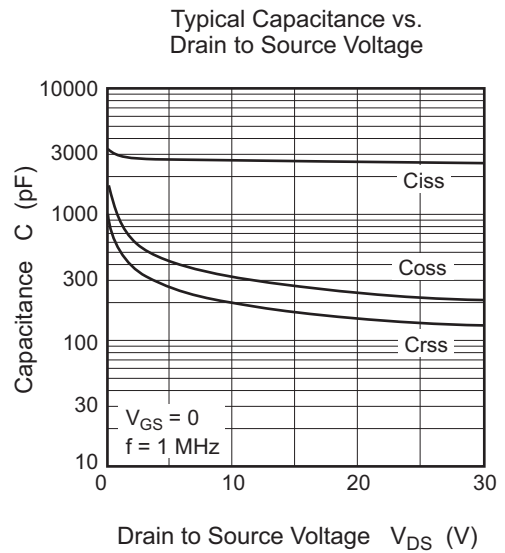
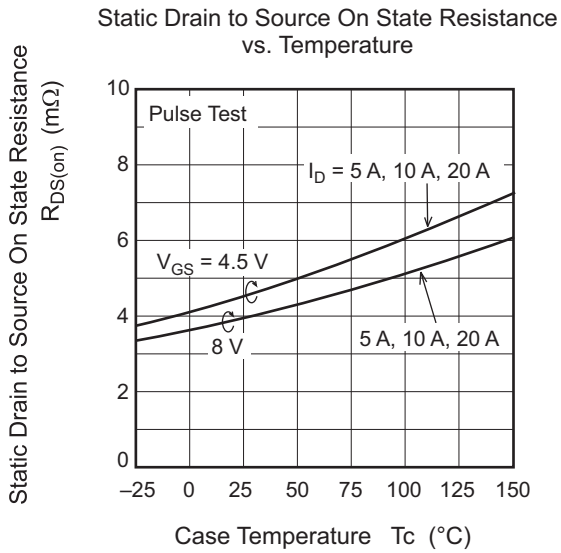
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.5$	$\mu\text{A}$	$V_{GS} = \pm 12 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	mA	$V_{DS} = 24 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.9	4.7	m $\Omega$	$I_D = 17.5\text{A}$ , $V_{GS} = 8.0 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	4.5	5.7	m $\Omega$	$I_D = 17.5\text{A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	92	—	S	$I_D = 17.5\text{A}$ , $V_{DS} = 5 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	2750	3850	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	335	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	205	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	$R_g$	—	2.0	4.0	$\Omega$	
Total gate charge	$Q_g$	—	22.3	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	6.1	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	6.3	—	nC	$I_D = 35 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	5.3	—	ns	$V_{GS} = 8 \text{ V}$ , $I_D = 17.5\text{A}$
Rise time	$t_r$	—	4.0	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	51.2	—	ns	$R_L = 0.57\Omega$
Fall time	$t_f$	—	14.6	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.44	—	V	$I_F = 2 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	7.2	—	ns	$I_F = 35 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

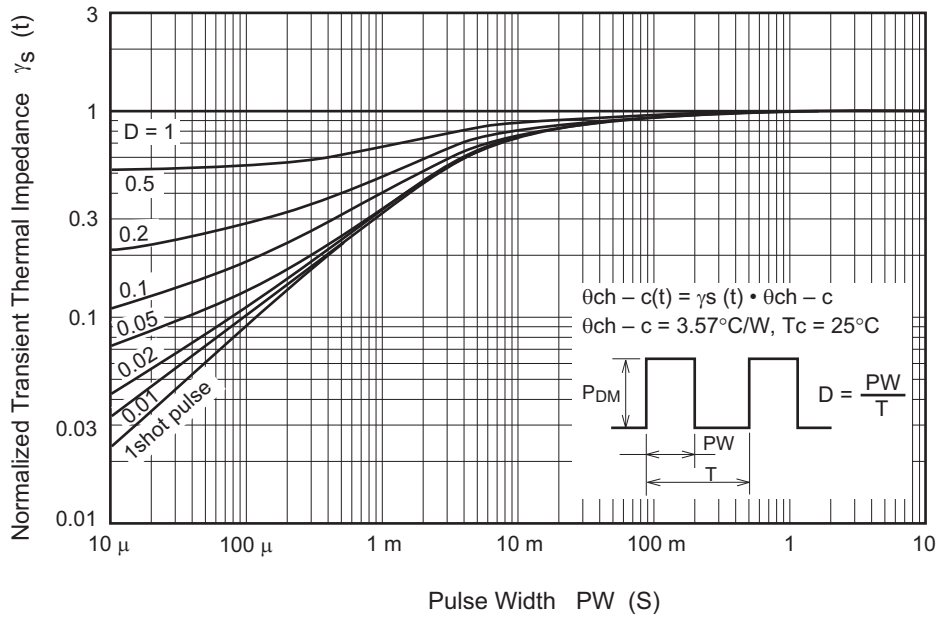
Notes: 4. Pulse test

### Main Characteristics

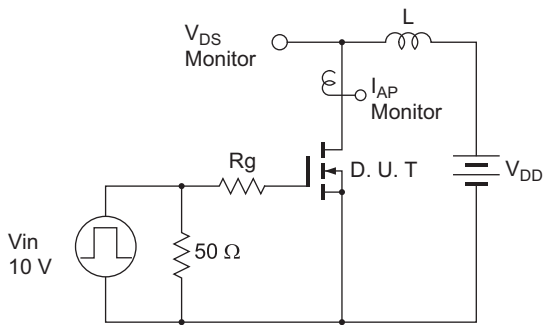




Normalized Transient Thermal Impedance vs. Pulse Width

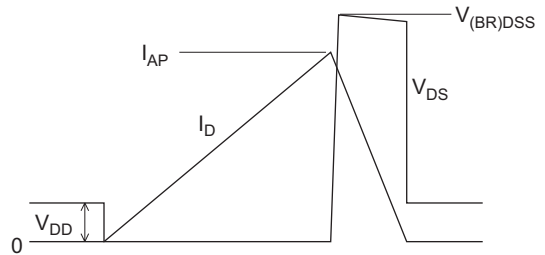


Avalanche Test Circuit

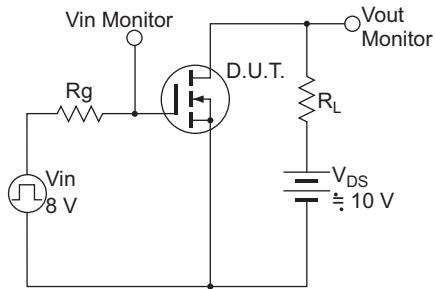


Avalanche Waveform

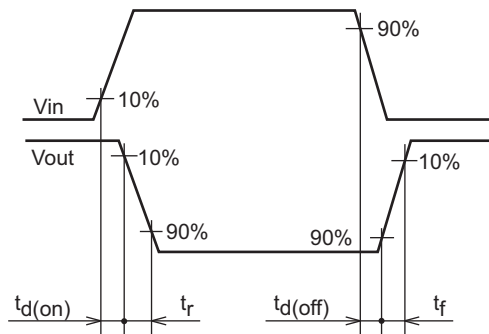
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



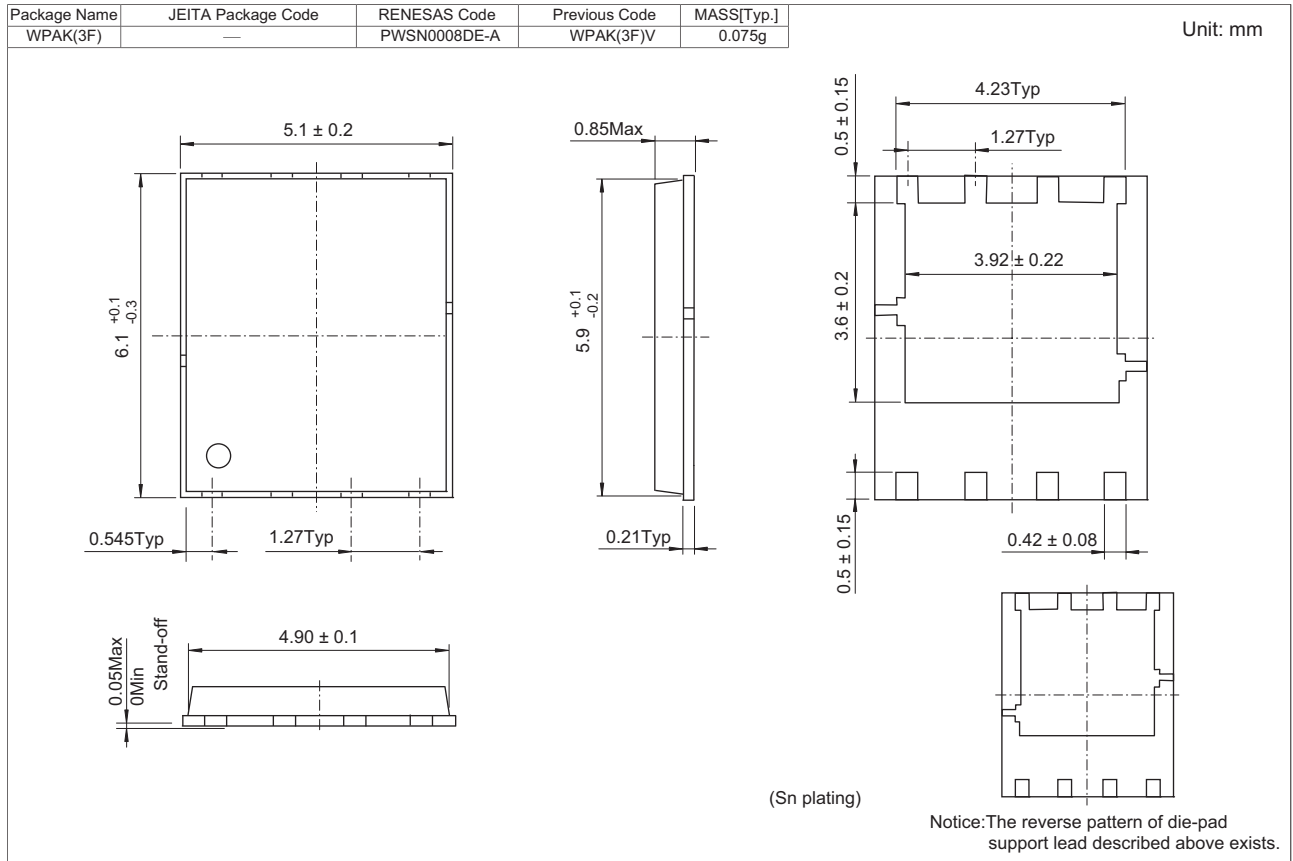
Switching Time Test Circuit



Switching Time Waveform



### Package Dimensions



### Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK03N3DPA-00-J5A	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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