

Small Signal MOSFET

30 Volts

N-Channel SC-88

- We declare that the material of product are Halogen Free and compliance with RoHS requirements.
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

FEATURES

- $R_{DS(ON)} \leq 8\Omega @ V_{GS}=4V$
- $R_{DS(ON)} \leq 13\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding
- ESD Protected:1000V

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch

ORDERING INFORMATION

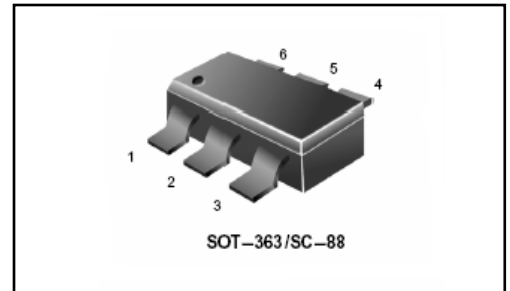
Device	Marking	Shipping
L2N7002FDW1T1G S-L2N7002FDW1T1G	72F	3000 Tape & Reel
L2N7002FDW1T3G S-L2N7002FDW1T3G	72F	10000 Tape & Reel

THERMAL CHARACTERISTICS

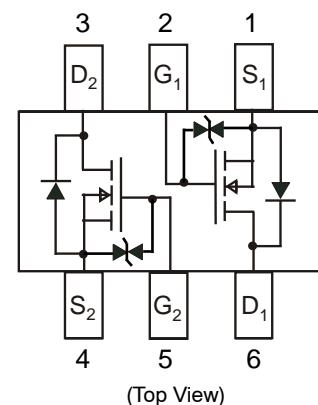
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1.) $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	225 1.8	mW mW/ $^\circ C$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ C/W$
Total Device Dissipation Alumina Substrate,(Note 2.) $T_A = 25^\circ C$ Derate above $25^\circ C$	P_D	300 2.4	mW mW/ $^\circ C$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ C/W$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ C$

1. FR-5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

L2N7002FDW1T1G
S-L2N7002FDW1T1G



Simplified Schematic



L2N7002FDW1T1G,S-L2N7002FDW1T1G

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V

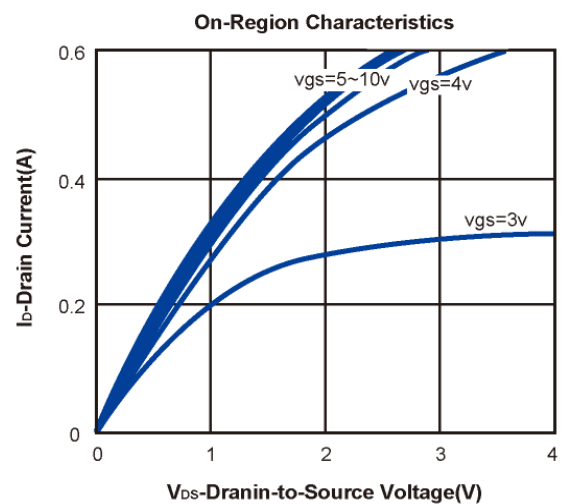
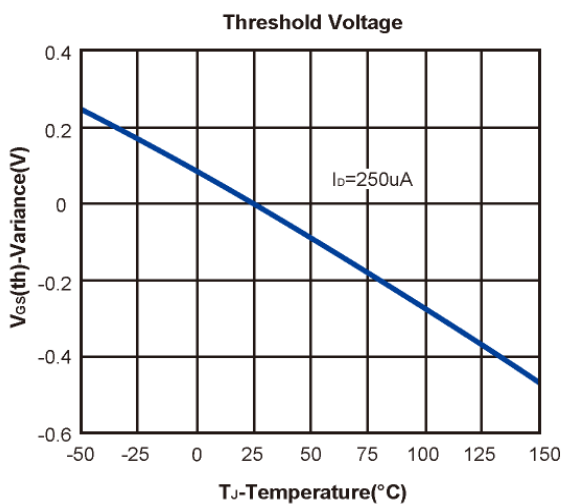
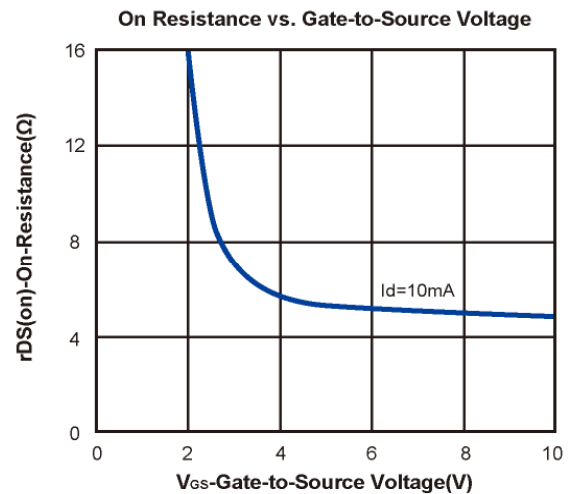
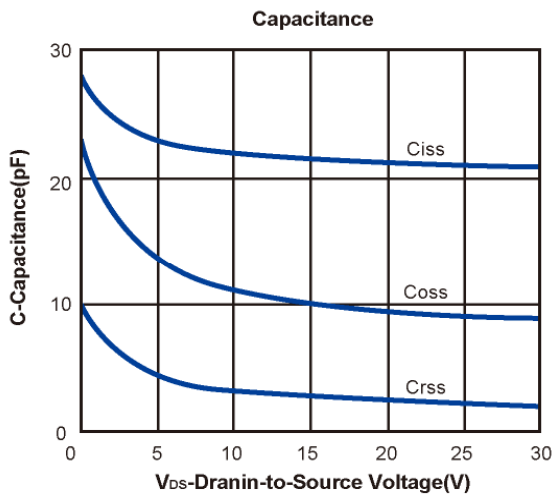
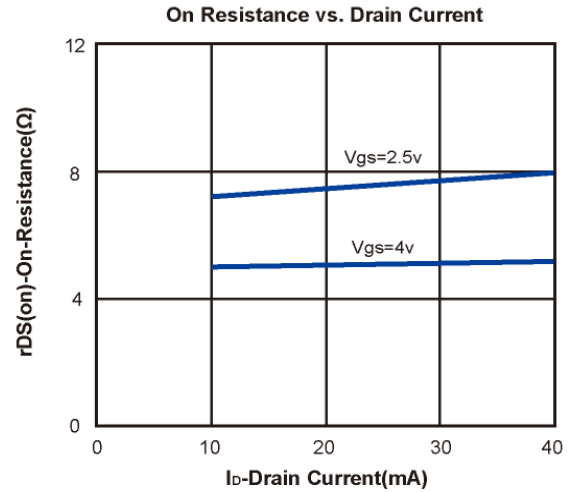
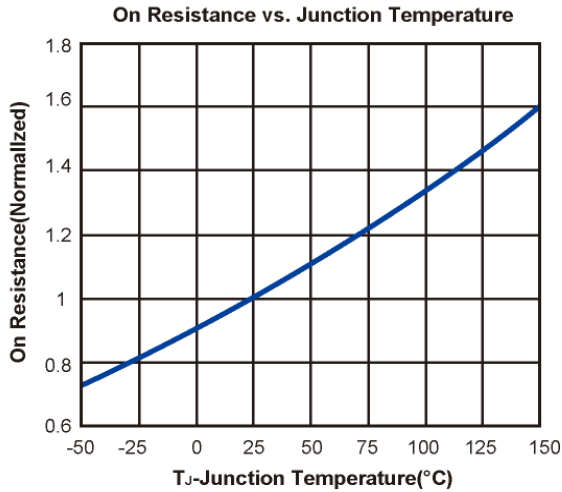
Electrical Characteristics (T_j=25°C Unless Otherwise Specified)

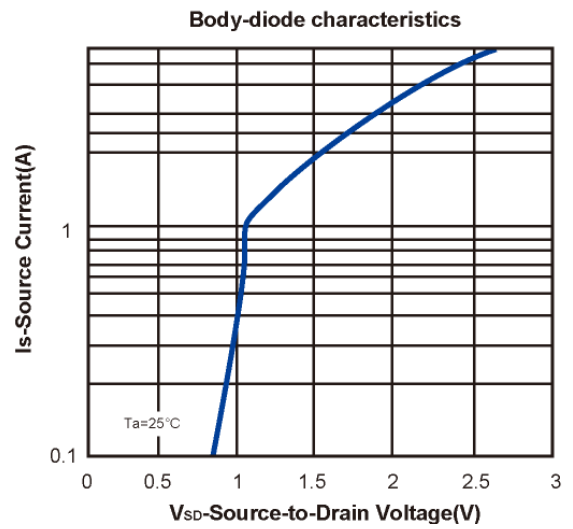
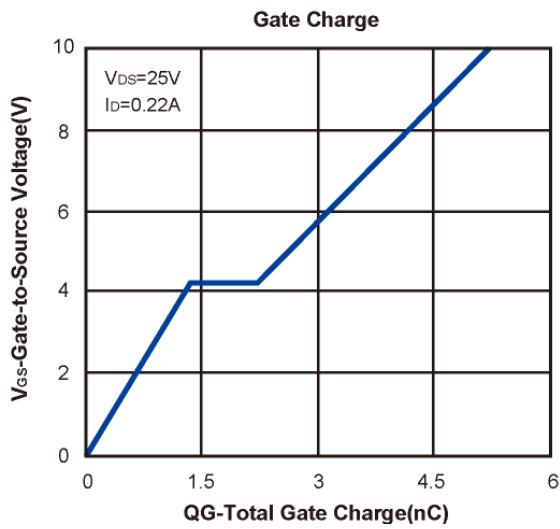
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	0.8		1.5	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} =±20V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =4V, I _D =10mA		5	8	Ω
		V _{GS} =2.5V, I _D =1mA		7	13	
V _{SD}	Diode Forward Voltage *	I _S =200mA, V _{GS} =0V			1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =25V, V _{GS} =10V, I _D =0.22A		4.9		nC
Q _{gs}	Gate-Source Charge			2.1		
Q _{gd}	Gate-Drain Charge			0.6		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		21		pF
C _{oss}	Output Capacitance			10		
C _{rss}	Reverse Transfer Capacitance			2		
t _{d(on)}	Turn-On Delay Time	V _{DD} =5V, R _L =500Ω V _{GES} =5V, R _G =10Ω		10.1		ns
t _r	Turn-On Rise Time			7.3		
t _{d(off)}	Turn-Off Delay Time			31.3		
t _f	Turn-Off Fall Time			28.2		

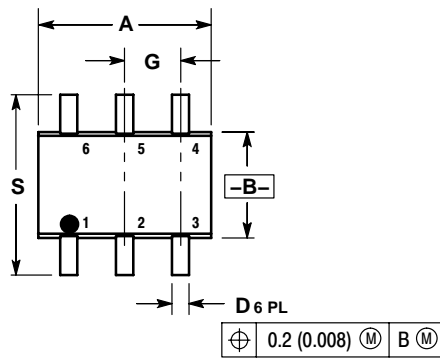
Notes: *. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%.

L2N7002FDW1T1G,S-L2N7002FDW1T1G

Typical Characteristics (T_J =25°C Noted)

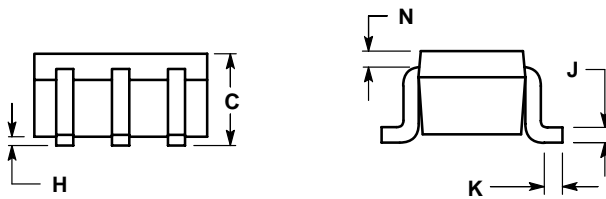


L2N7002FDW1T1G,S-L2N7002FDW1T1G
Typical Characteristics (T_J =25°C Noted)


L2N7002FDW1T1G,S-L2N7002FDW1T1G
SC-88 (SOT-363)
CASE 419B-02

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20


STYLE 1:

- PIN 1. SOURCE 2
2. GATE 2
3. DRAIN 1
4. SOURCE 1
5. GATE 1
6. DRAIN 2

SOLDERING FOOTPRINT*
