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- Please conduct validation and verification of products in actual condition of mounting and operating environment before commercial shipment of the equipment.

- All electronic components or functional modules listed in this catalog are developed, designed and intended for use in general electronics equipment.(for AV, office automation, household, office supply, information service, telecommunications, (such as mobile phone or PC) etc.). Before incorporating the components or devices into any equipment in the field such as transportation,(automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network (telephone exchange, base station) etc. which may have direct influence to harm or injure a human body, please contact TAIYO YUDEN CO., LTD. for more detail in advance.
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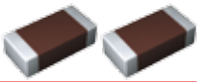
MULTILAYER CERAMIC CAPACITORS



WAVE REFLOW

■PARTS NUMBER

J	M	K	3 1 6	△	B J	1 0 6	M	L	—	T	△
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫

△=Blank space

①Rated voltage

Code	Rated voltage[VDC]
P	2.5
A	4
J	6.3
L	10
E	16
T	25
G	35
U	50
H	100
Q	250
S	630

②Series name

Code	Series name
M	Multilayer ceramic capacitor
V	Multilayer ceramic capacitor for high frequency
W	LW reverse type multilayer capacitor

③End termination

Code	End termination
K	Plated
S	Cu Internal Electrodes

④Dimension(L×W)

Type	Dimensions (L×W)[mm]	EIA(inch)
042	0.4 × 0.2	01005
063	0.6 × 0.3	0201
105	1.0 × 0.5	0402
	0.52× 1.0 ※	0204
107	1.6 × 0.8	0603
	0.8 × 1.6 ※	0306
212	2.0 × 1.25	0805
	1.25× 2.0 ※	0508
316	3.2 × 1.6	1206
325	3.2 × 2.5	1210
432	4.5 × 3.2	1812

Note : ※LW reverse type(□WK) only

⑤Dimension tolerance

Code	Type	L[mm]	W[mm]	T[mm]
△	ALL	Standard	Standard	Standard
A	063	0.6±0.05	0.3±0.05	0.3±0.05
	105	1.0±0.10	0.5±0.10	0.5±0.10
	107	1.6+0.15/−0.05	0.8+0.15/−0.05	0.8+0.15/−0.05
	212	2.0+0.15/−0.05	1.25+0.15/−0.05	0.45±0.05
				0.85±0.10
				1.25+0.15/−0.05
	316	3.2±0.20	1.6±0.20	0.85±0.10
				1.6±0.20
	325	3.2±0.30	2.5±0.30	2.5±0.30
B	105	1.0+0.15/−0.05	0.5+0.15/−0.05	0.5+0.15/−0.05
	107	1.6+0.20/−0	0.8+0.20/−0	0.45±0.05
				0.8+0.20/−0
	212	2.0+0.20/−0	1.25+0.20/−0	0.85±0.10
				1.25+0.20/−0
	316	3.2±0.30	1.6±0.30	1.6±0.30
C	105	1.0+0.20/−0	0.5+0.20/−0	0.5+0.20/−0

Note: P.6 Standard external dimensions △= Blank space

⑥Temperature characteristics code

■High dielectric type(Excluding Super low distortion multilayer ceramic capacitor(CFCAP™))

Code	Applicable standard		Temperature range[℃]	Ref. Temp.[℃]	Capacitance change	Capacitance tolerance	Tolerance code
BJ	JIS	B	−25～+ 85	20	±10%	±10%	K
						±20%	M
	EIA	X5R	−55～+ 85	25	±15%	±10%	K
						±20%	M
B7	EIA	X7R	−55～+125	25	±15%	±10%	K
						±20%	M
C6	EIA	X6S	−55～+105	25	±22%	±10%	K
						±20%	M
C7	EIA	X7S	−55～+125	25	±22%	±10%	K
						±20%	M
LD(※)	EIA	X5R	−55～+ 85	25	±15%	±10%	K
						±20%	M
△F	JIS	F	−25～+ 85	20	+30/−80%	+80/−20%	Z
	EIA	Y5V	−30～+ 85	25	+22/−82%	+80/−20%	Z

Note : ※.LD Low distortion high value multilayer ceramic capacitor △= Blank space

■Temperature compensating type

Code	Applicable standard		Temperature range[℃]	Ref. Temp.[℃]	Capacitance change	Capacitance tolerance	Tolerance code
CG	EIA	C0G	−55～＋125	25	0±60ppm/℃	±0.1pF	B
						±0.25pF	C
						±0.5pF	D
						±1pF	F
						±5%	J
CH	JIS	CH	−55～＋125	20	0±60ppm/℃	±0.1pF	B
						±0.25pF	C
						±0.5pF	D
	EIA	C0H		25		±1pF	F
						±5%	J
						±10%	K
CJ	JIS	CJ	−55～＋125	20	0±120ppm/℃	±0.25pF	C
	EIA	C0J		25			
CK	JIS	CK	−55～＋125	20	0±250ppm/℃	±0.25pF	C
	EIA	C0J		25			
UJ	JIS	UJ	−55～＋125	20	−750±120ppm/℃	±0.25pF	C
	EIA	U2J		25		±0.5pF	D
						±5%	J
UK	JIS	UK	−55～＋125	20	−750±250ppm/℃	±0.5pF	C
	EIA	U2K	−55～＋125	25			
SL	JIS	SL	−55～＋125	20	+350～−1000ppm/℃	±5%	J

⑥Series code

(Super low distortion multilayer ceramic capacitor(CFCAP™)only)

Code	Series code
SD	Standard

⑦Nominal capacitance

Code (example)	Nominal capacitance
0R5	0.5pF
010	1pF
100	10pF
101	100pF
102	1,000pF
103	10,000pF
104	0.1μF
105	1.0μF
106	10μF
107	100μF

Note : R=Decimal point

⑧Capacitance tolerance

Code	Capacitance tolerance
B	±0.1pF
C	±0.25pF
D	±0.5pF
F	±1pF
G	±2%
J	±5%
K	±10%
M	±20%
Z	+80/−20%

⑨Thickness

Code	Thickness[mm]
C	0.2
D	
P	0.3
T	
K	0.45
V	0.5
W	
A	0.8
D	0.85(212type or more)
F	1.15
G	1.25
L	1.6
N	1.9
Y	2.0 max
M	2.5

⑩Special code

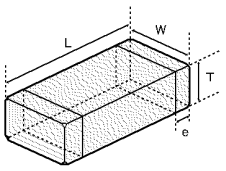
Code	Special code
—	Standard

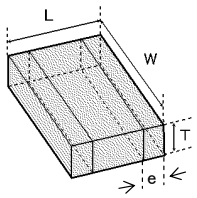
⑪Packaging

Code	Packaging
F	φ178mm Taping (2mm pitch)
T	φ178mm Taping (4mm pitch)
P	φ178mm Taping (4mm pitch, 1000 pcs/reel) 325 type(Thickness code M)
W	φ178mm Taping(1mm pitch)042type only

⑫Internal code

Code	Internal code
△	Standard





※ LW reverse type

Type(EIA)	Dimension [mm]				
	L	W	T	*1	e
□MK042(01005)	0.4±0.02	0.2±0.02	0.2±0.02	C	0.1±0.03
				D	
□VS042(01005)	0.4±0.02	0.2±0.02	0.2±0.02	C	0.1±0.03
□MK063(0201)	0.6±0.03	0.3±0.03	0.3±0.03	P	0.15±0.05
				T	
□MK105(0402)	1.0±0.05	0.5±0.05	0.2±0.02	C	0.25±0.10
			0.3±0.03	P	
			0.5±0.05	V	
□VK105(0402)	1.0±0.05	0.5±0.05	0.5±0.05	W	0.25±0.10
□WK105(0204)※	0.52±0.05	1.0±0.05	0.3±0.05	P	0.18±0.08
□MK107(0603)	1.6±0.10	0.8±0.10	0.45±0.05	K	0.35±0.25
			0.8±0.10	A	
□WK107(0306)※	0.8±0.10	1.6±0.10	0.5±0.05	V	0.25±0.15
□MK212(0805)	2.0±0.10	1.25±0.10	0.45±0.05	K	0.5±0.25
			0.85±0.10	D	
			1.25±0.10	G	
□WK212(0508)※	1.25±0.15	2.0±0.15	0.85±0.1	D	0.3±0.2
□MK316(1206)	3.2±0.15	1.6±0.15	0.85±0.10	D	0.5+0.35/−0.25
			1.15±0.10	F	
			1.25±0.10	G	
			1.6±0.20	L	
□MK325(1210)	3.2±0.30	2.5±0.20	0.85±0.10	D	0.6±0.3
			1.15±0.10	F	
			1.9±0.20	N	
			1.9+0.1/−0.2	Y	
			2.5±0.20	M	
□MK432(1812)	4.5±0.40	3.2±0.30	2.5±0.20	M	0.9±0.6

Note : ※. LW reverse type, *1.Thickness code

■STANDARD QUANTITY

Type	EIA(inch)	Dimension		Standard quantity[pcs]	
		[mm]	Code	Paper tape	Embossed tape
042	01005	0.2	C	—	40000
			D		
063	0201	0.3	P	15000	—
			T		
105	0402	0.2	C	20000	—
		0.3	P	15000	—
		0.5	V	10000	—
			W		
	0204 ※	0.30	P		
107	0603	0.45	K	4000	—
		0.8	A		
	0306 ※	0.50	V	—	4000
212	0805	0.45	K	4000	—
		0.85	D		
		1.25	G	—	3000
	0508 ※	0.85	D	4000	—
316	1206	0.85	D	4000	—
		1.15	F	—	3000
		1.25	G		
		1.6	L	—	2000
325	1210	0.85	D	—	2000
		1.15	F		
		1.9	N		
		2.0 max	Y		
		2.5	M	—	500(T), 1000(P)
432	1812	2.5	M	—	500

Note : ※.LW Reverse type(□WK)

▶ This catalog contains the typical specification only due to the limitation of space. When you consider the purchase of our products, please check our specification. For details of each product (characteristics graph, reliability information, precautions for use, and so on), see our Web site (http://www.ty-top.com/) .

●432TYPE

【Temperature Characteristic BJ : B/X5R】2.5mm thickness(M)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
HMK432 BJ474□M-T		100	B	X5R*1	0.47 μ	±10, ±20	3.5	200	2.5±0.20	R
HMK432 BJ105□M-T			B	X5R*1	1 μ	±10, ±20	3.5	200	2.5±0.20	R
HMK432 BJ155□M-T			B	X5R*1	1.5 μ	±10, ±20	3.5	200	2.5±0.20	R
HMK432 BJ225□M-T			B	X5R*1	2.2 μ	±10, ±20	3.5	200	2.5±0.20	R
QMK432 BJ104□M-T		250	B	X5R*1	0.1 μ	±10, ±20	2.5	150	2.5±0.20	R
QMK432 BJ224□M-T			B	X5R*1	0.22 μ	±10, ±20	2.5	150	2.5±0.20	R
QMK432 BJ334□M-T			B	X5R*1	0.33 μ	±10, ±20	2.5	150	2.5±0.20	R
QMK432 BJ474□M-T			B	X5R*1	0.47 μ	±10, ±20	2.5	150	2.5±0.20	R
SMK432 BJ473□M-T		630	B	X5R*1	47000 p	±10, ±20	2.5	120	2.5±0.20	R
SMK432 BJ683□M-T			B	X5R*1	68000 p	±10, ±20	2.5	120	2.5±0.20	R
SMK432 BJ104□M-T			B	X5R*1	0.1 μ	±10, ±20	2.5	120	2.5±0.20	R

【Temperature Characteristic B7 : X7R】2.5mm thickness(M)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
HMK432 B7474□M-T		100		X7R	0.47 μ	±10, ±20	3.5	200	2.5±0.20	R
HMK432 B7105□M-T				X7R	1 μ	±10, ±20	3.5	200	2.5±0.20	R
HMK432 B7155□M-T				X7R	1.5 μ	±10, ±20	3.5	200	2.5±0.20	R
HMK432 B7225□M-T				X7R	2.2 μ	±10, ±20	3.5	200	2.5±0.20	R
QMK432 B7104□M-T		250		X7R	0.1 μ	±10, ±20	2.5	150	2.5±0.20	R
QMK432 B7224□M-T				X7R	0.22 μ	±10, ±20	2.5	150	2.5±0.20	R
QMK432 B7334□M-T				X7R	0.33 μ	±10, ±20	2.5	150	2.5±0.20	R
QMK432 B7474□M-T				X7R	0.47 μ	±10, ±20	2.5	150	2.5±0.20	R
SMK432 B7473□M-T		630		X7R	47000 p	±10, ±20	2.5	120	2.5±0.20	R
SMK432 B7683□M-T				X7R	68000 p	±10, ±20	2.5	120	2.5±0.20	R
SMK432 B7104□M-T				X7R	0.1 μ	±10, ±20	2.5	120	2.5±0.20	R

LW Reversal Decoupling Capacitors (LWDC™)

●105TYPE

【Temperature Characteristic BJ : X5R】0.3mm thickness(P)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
TWK105 BJ104MP-F		25		X5R	0.1 μ	±20	5	150	0.3±0.05	R
EWK105 BJ224MP-F		16		X5R	0.22 μ	±20	10	150	0.3±0.05	R
LWK105 BJ474MP-F		10		X5R	0.47 μ	±20	10	150	0.3±0.05	R
JWK105 BJ104MP-F		6.3		X5R*1	0.1 μ	±20	5	150	0.3±0.05	R
JWK105 BJ474MP-F				X5R*1	0.47 μ	±20	10	150	0.3±0.05	R
JWK105 BJ105MP-F				X5R	1 μ	±20	10	150	0.3±0.05	R
JWK105 BJ225MP-F				X5R	2.2 μ	±20	10	150	0.3±0.05	R
AWK105 BJ224MP-F		4		X5R	0.22 μ	±20	10	150	0.3±0.05	R

【Temperature Characteristic C6 : X6S , C7 : X7S】0.3mm thickness(P)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
EWK105 C6104MP-F		16		X6S	0.1 μ	±20	5	150	0.3±0.05	R
LWK105 C7104MP-F		10		X7S	0.1 μ	±20	5	150	0.3±0.05	R
LWK105 C6224MP-F				X6S	0.22 μ	±20	10	150	0.3±0.05	R
JWK105 C7104MP-F		6.3		X7S	0.1 μ	±20	5	150	0.3±0.05	R
JWK105 C7224MP-F				X7S	0.22 μ	±20	10	150	0.3±0.05	R
JWK105 C6474MP-F				X6S	0.47 μ	±20	10	150	0.3±0.05	R
AWK105 C6224MP-F		4		X6S	0.22 μ	±20	10	150	0.3±0.05	R
AWK105 C6474MP-F				X6S	0.47 μ	±20	10	150	0.3±0.05	R
AWK105 C6105MP-F				X6S	1 μ	±20	10	150	0.3±0.05	R
AWK105 C6225MP-F				X6S	2.2 μ	±20	10	150	0.3±0.05	R

●107TYPE

【Temperature Characteristic BJ : X5R】0.5mm thickness(V)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
TWK107 BJ104MV-T		25		X5R*1	0.1 μ	±20	5	150	0.5±0.05	R
EWK107 BJ224MV-T		16		X5R*1	0.22 μ	±20	5	150	0.5±0.05	R
EWK107 BJ474MV-T				X5R*1	0.47 μ	±20	5	150	0.5±0.05	R
LWK107 BJ105MV-T		10		X5R	1 μ	±20	10	150	0.5±0.05	R
LWK107 BJ225MV-T				X5R	2.2 μ	±20	10	150	0.5±0.05	R
JWK107 BJ105MV-T		6.3		X5R*1	1 μ	±20	10	150	0.5±0.05	R
JWK107 BJ225MV-T				X5R	2.2 μ	±20	10	150	0.5±0.05	R
JWK107 BJ475MV-T				X5R	4.7 μ	±20	10	150	0.5±0.05	R
AWK107 BJ106MV-T		4		X5R	10 μ	±20	10	150	0.5±0.05	R

【Temperature Characteristic B7 : X7R , C6 : X6S , C7 : X7S】0.5mm thickness(V)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
TWK107 B7104MV-T		25		X7R	0.1 μ	±20	5	150	0.5±0.05	R
EWK107 B7224MV-T		16		X7R	0.22 μ	±20	5	150	0.5±0.05	R
EWK107 B7474MV-T				X7R	0.47 μ	±20	5	150	0.5±0.05	R
JWK107 C7105MV-T		6.3		X7S	1 μ	±20	10	150	0.5±0.05	R
AWK107 C7225MV-T		4		X7S	2.2 μ	±20	10	150	0.5±0.05	R
AWK107 C6475MV-T				X6S	4.7 μ	±20	10	150	0.5±0.05	R
PWK107 C6106MV-T		2.5		X6S	10 μ	±20	10	150	0.5±0.05	R

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■PARTS NUMBER

●212TYPE

【Temperature Characteristic BJ : X5R】0.85mm thickness(D)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
TWK212 BJ475□D-T		25		X5R	4.7 μ	±10, ±20	10	150	0.85±0.10	R
EWK212 BJ106MD-T		16		X5R	10 μ	±20	10	150	0.85±0.10	R
LWK212 BJ475□D-T		10		X5R	4.7 μ	±10, ±20	10	150	0.85±0.10	R
LWK212 BJ106MD-T				X5R	10 μ	±20	10	150	0.85±0.10	R
JWK212 BJ226MD-T		6.3		X5R	22 μ	±20	10	150	0.85±0.10	R

【Temperature Characteristic B7 : X7R , C6 : X6S】0.85mm thickness(D)

Part number 1	Part number 2	Rated voltage [V]	Temperature characteristics		Capacitance [F]	Capacitance tolerance [%]	tan δ [%]	HTLT Rated voltage x %	Thickness*3 [mm]	Soldering R:Reflow W:Wave
TWK212 B7225□D-T		25		X7R	2.2 μ	±10, ±20	5	150	0.85±0.10	R
EWK212 C6475□D-T		16		X6S	4.7 μ	±10, ±20	10	150	0.85±0.10	R
LWK212 C6106MD-T		10		X6S	10 μ	±20	10	150	0.85±0.10	R
AWK212 C6226MD-T		4		X6S	22 μ	±20	10	150	0.85±0.10	R

■PACKAGING

①Minimum Quantity

●Taped package

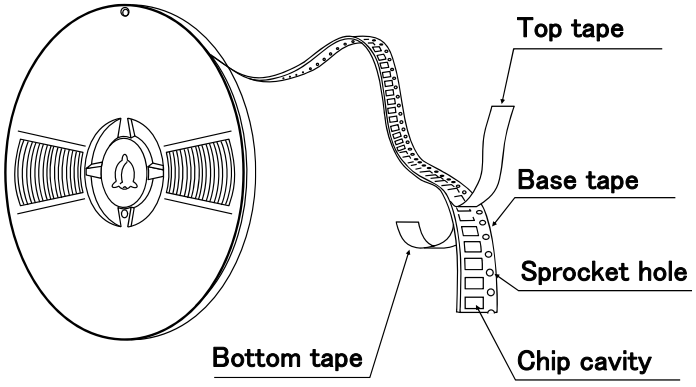
Type(EIA)	Thickness		Standard quantity [pcs]	
	mm	code	Paper tape	Embossed tape
□MK042(01005)	0.2	C, D	—	40000
□VS042(01005)	0.2	C		
□MK063(0201)	0.3	P, T	15000	—
□WK105(0204) ※	0.3	P	10000	
□MK105(0402)	0.2	C	20000	
	0.3	P	15000	
	0.5	V	10000	
□VK105(0402) ※	0.5	W		
□MK107(0603)	0.45	K	4000	
□WK107(0306) ※	0.5	V	—	4000
□MR107(0603)	0.8	A	4000	—
□MK212(0805)	0.45	K		
□WK212(0508) ※	0.85	D		
□MR212(0805)	125	G	—	3000
□MK316(1206) □MR316(1206)	0.85	D	4000	—
	1.15	F	—	3000
	125	G		
	1.6	L	—	2000
□MK325(1210) □MR325(1210)	0.85	D	—	2000
	1.15	F		
	1.9	N		
	2.0max.	Y		
	2.5	M		500(T), 1000(P)
□MK432(1812)	2.5	M	—	500

Note : ※ LW Reverse type.

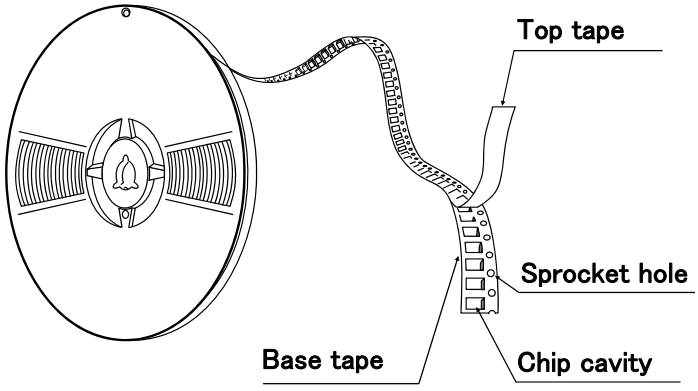
②Taping material

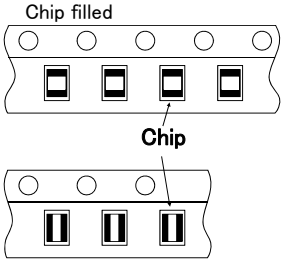
※No bottom tape for pressed carrier tape

●Card board carrier tape



●Embossed tape

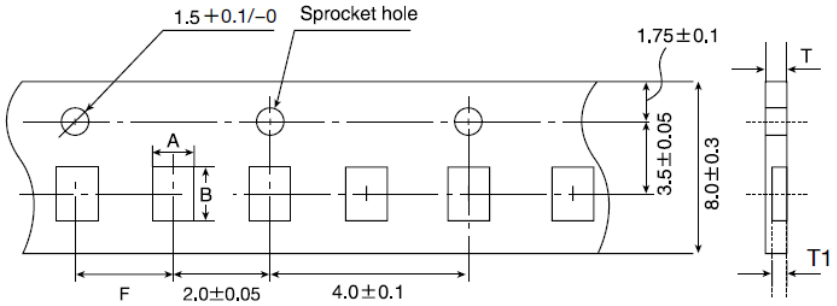




③Representative taping dimensions

Paper Tape(8mm wide)

●Pressed carrier tape(2mm pitch)

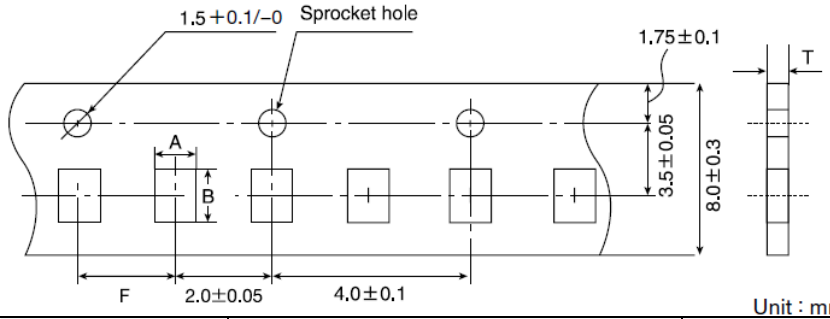


Unit : mm

Type(EIA)	Chip Cavity		Insertion Pitch	Tape Thickness	
	A	B	F	T	T1
□MK063(0201)	0.37	0.67	2.0±0.05	0.45max.	0.42max.
□WK105(0204) ※	0.65	1.15			
□MK105(0402) (*1 C)				0.4max.	0.3max.
□MK105(0402) (*1 P)				0.45max.	0.42max.

Note *1 Thickness, C:0.2mm ,P:0.3mm. ※ LW Reverse type. Unit:mm

●Punched carrier tape (2mm pitch)

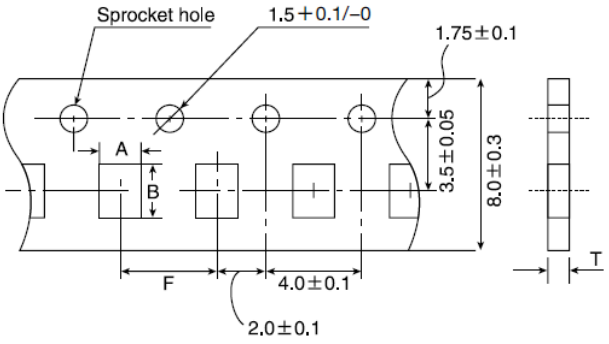


Unit : mm

Type(EIA)	Chip Cavity		Insertion Pitch	Tape Thickness
	A	B	F	T
□MK105 (0402) □VK105 (0402)	0.65	1.15	2.0±0.05	0.8max.

Unit:mm

●Punched carrier tape (4mm pitch)

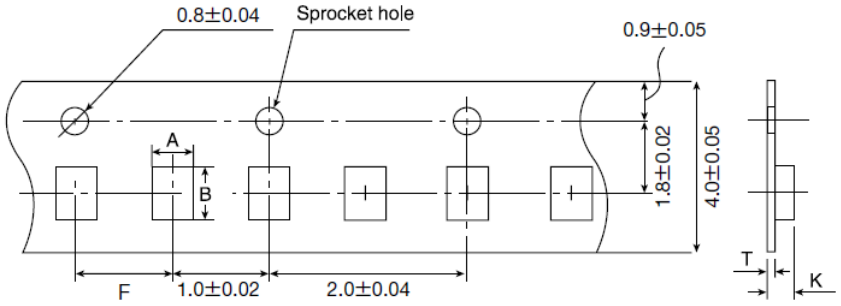


Unit : mm

Type(EIA)	Chip Cavity		Insertion Pitch	Tape Thickness
	A	B	F	T
□MK107(0603) □WK107(0306) ※ □MR107(0603)	1.0	1.8	4.0±0.1	1.1max.
□MK212(0805) □WK212(0508) ※	1.65	2.4		1.1max.
□MK316(1206)	2.0	3.6		

Note:Taping size might be different depending on the size of the product. ※ LW Reverse type. Unit:mm

Embossed tape (4mm wide)

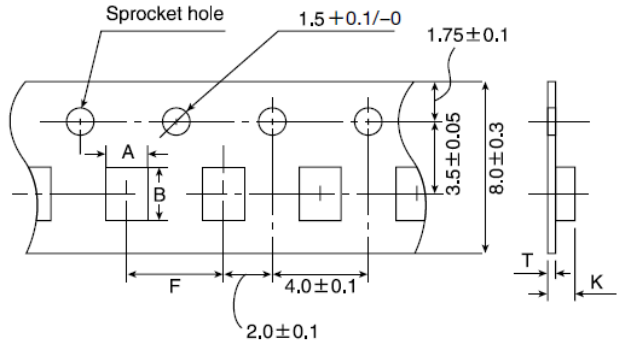


Unit : mm

Type(EIA)	Chip Cavity		Insertion Pitch	Tape Thickness	
	A	B	F	K	T
□MK042(01005) □VS042(01005)	0.23	0.43	1.0±0.02	0.5max.	0.25max.

Unit : mm

Embossed tape (8mm wide)



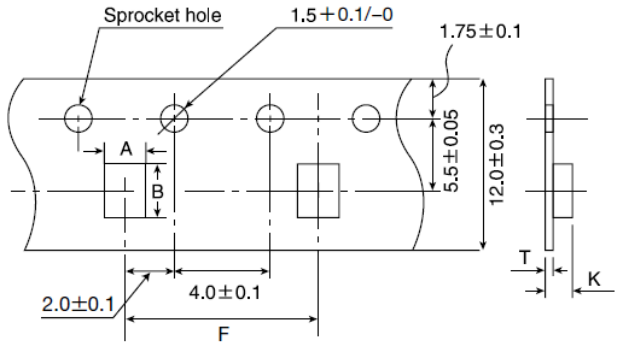
Unit : mm

Type(EIA)	Chip Cavity		Insertion Pitch	Tape Thickness	
	A	B	F	K	T
□WK107(0306) ※	1.0	1.8	4.0±0.1	1.3max.	0.25±0.1
□MK212(0805) □MR212(0805)	1.65	2.4		3.4max.	0.6max.
□MK316(1206) □MR316(1206)	2.0	3.6			
□MK325(1210) □MR325(1210)	2.8	3.6			

Note : ※ LW Reverse type.

Unit : mm

Embossed tape (12mm wide)

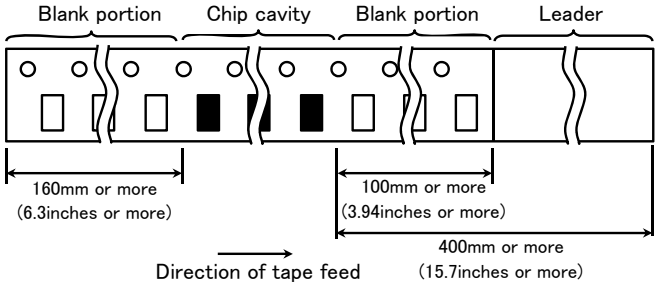


Unit : mm

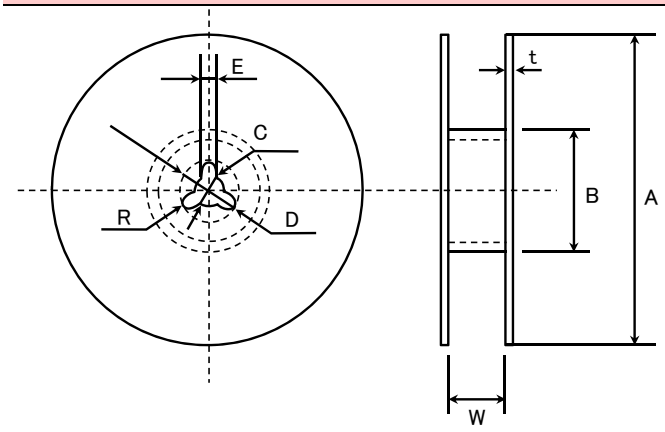
Type(EIA)	Chip Cavity		Insertion Pitch	Tape Thickness	
	A	B	F	K	T
□MK432(1812)	3.7	4.9	8.0±0.1	4.0max.	0.6max.

Unit : mm

④Trailer and Leader



⑤Reel size



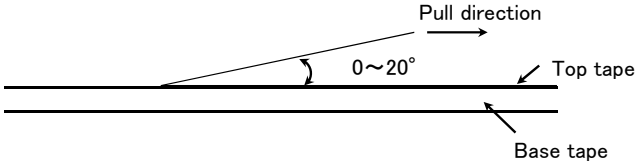
A	B	C	D	E	R
ϕ178±2.0	ϕ50min.	ϕ13.0±0.2	ϕ21.0±0.8	2.0±0.5	1.0

	T	W
4mm wide tape	1.5max.	5±1.0
8mm wide tape	2.5max.	10±1.5
12mm wide tape	2.5max.	14±1.5

Unit : mm

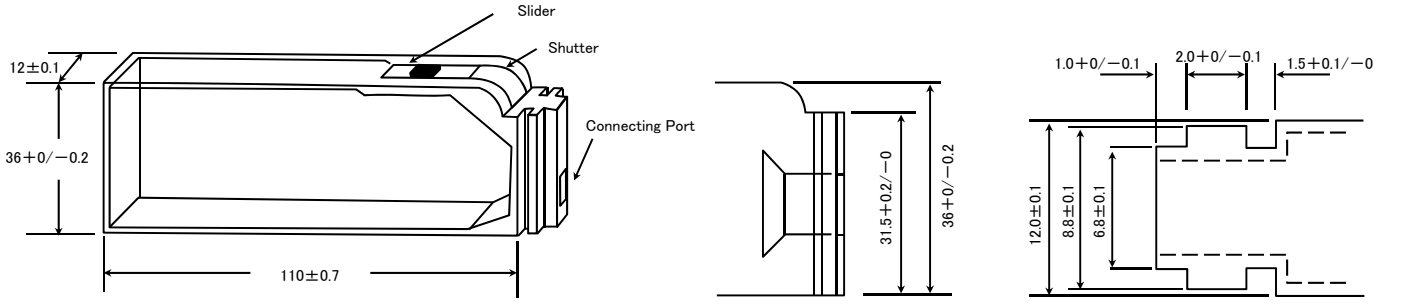
⑥Top Tape Strength

The top tape requires a peel-off force of 0.1 to 0.7N in the direction of the arrow as illustrated below.



⑦Bulk Cassette

The exchange of individual specification is necessary.
Please contact Taiyo Yuden sales channels.



Unit : mm

Multilayer Ceramic Capacitors

■RELIABILITY DATA

1.Operating Temperature Range

Specified Value	Temperature Compensating(Class1)	Standard / High Frequency Type	−55 to +125℃
	High Permittivity (Class2)		See table below

	Specification	Temperature Range
BJ	B	−25 to +85℃
	X5R	−55 to +85℃
B7	X7R	−55 to +125℃
C6	X6S	−55 to +105℃
C7	X7S	−55 to +125℃
LD(※)	X5R	−55 to +85℃
F	F	−25 to +85℃
	Y5V	−30 to +85℃

Note: ※LD Low distortion high value multilayer ceramic capacitor

2. Storage Conditions

Specified Value	Temperature Compensating(Class1)	Standard / High Frequency Type	−55 to +125℃
	High Permittivity (Class2)		See table below

	Specification	Temperature Range
BJ	B	−25 to +85℃
	X5R	−55 to +85℃
B7	X7R	−55 to +125℃
C6	X6S	−55 to +105℃
C7	X7S	−55 to +125℃
LD(※)	X5R	−55 to +85℃
F	F	−25 to +85℃
	Y5V	−30 to +85℃

Note: ※LD Low distortion high value multilayer ceramic capacitor

3. Rated Voltage

Specified Value	Temperature Compensating(Class1)	Standard	50VDC, 25VDC, 16VDC
		High Frequency Type	50VDC, 25VDC, 16VDC
	High Permittivity (Class2)		50VDC, 35VDC, 25VDC, 16VDC, 10VDC, 6.3VDC, 4VDC, 2.5VDC

4. Withstanding Voltage (Between terminals)

Specified Value	Temperature Compensating(Class1)	Standard / High Frequency Type	No breakdown or damage
	High Permittivity (Class2)		

Test Methods and Remarks	Class 1	Class 2
Applied voltage	Rated voltage × 3	Rated voltage × 2.5
Duration	1 to 5 sec.	
Charge/discharge current	50mA max.	

5. Insulation Resistance

Specified Value	Temperature Compensating(Class1)	Standard / High Frequency Type	10000 MΩ min.
	High Permittivity (Class2) Note 1		C≦0.047μF : 10000 MΩ min. C＞0.047μF : 500MΩ・μF
Test Methods and Remarks	Applied voltage : Rated voltage Duration : 60±5 sec. Charge/discharge current : 50mA max.		

6. Capacitance (Tolerance)

Specified Value

Temperature Compensating(Class1)	Standard	C□ 0.2pF≦C≦5pF : ±0.25pF U□ 0.2pF≦C≦10pF : ±0.5pF SL C>10pF : ±5% or ±10%
	High Frequency Type	CH 0.2pF≦C≦2pF : ±0.1pF C>2pF : ±5%
High Permittivity (Class2)		BJ, B7, C6, C7, LD(※) : ±10% or ±20%, F : +80/−20% Note: ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

	Class 1		Class 2	
	Standard	High Frequency Type	C≦10μF	C>10μF
Preconditioning	None		Thermal treatment (at 150℃ for 1hr) Note 2	
Measuring frequency	1MHz±10%		1kHz±10%	120±10Hz
Measuring voltage Note	0.5 to 5Vrms		1±0.2Vrms	0.5±0.1Vrms
Bias application	None			

7. Q or Dissipation Factor

Specified Value

Temperature Compensating(Class1)	Standard	C<30pF : Q≧400+20C C≧30pF : Q≧1000 (C:Nominal capacitance)
	High Frequency Type	Refer to detailed specification
High Permittivity (Class2) Note 1		BJ, B7, C6, C7:2.5% max., F:7% max.

Test Methods and Remarks

	Class 1		Class 2	
	Standard	High Frequency Type	C≦10μF	C>10μF
Preconditioning	None		Thermal treatment (at 150℃ for 1hr) Note 2	
Measuring frequency	1MHz±10%	1GHz	1kHz±10%	120±10Hz
Measuring voltage Note 1	0.5 to 5Vrms		1±0.2Vrms	0.5±0.1Vrms
Bias application	None			

High Frequency Type
Measuring equipment : HP4291A
Measuring jig : HP16192A

8. Temperature Characteristic (Without voltage application)

Specified Value

Temperature Compensating(Class1)	Standard	Temperature Characteristic [ppm/℃] / Tolerance [ppm/℃] C□ : 0 — CG,CH, CJ, CK — G : ±30, H : ±60, J : ±120, K : ±250 U□ : −750 — UJ, UK SL : +350 to −1000
	High Frequency Type	Temperature Characteristic [ppm/℃] / Tolerance [ppm/℃] C□ : 0 — CH — H : ±60
High Permittivity (Class2)		

	Specification	Capacitance change	Reference temperature	Temperature Range
BJ	B	±10%	20℃	−25 to +85℃
	X5R	±15%	25℃	−55 to +85℃
B7	X7R	±15%	25℃	−55 to +125℃
C6	X6S	±22%	25℃	−55 to +105℃
C7	X7S	±22%	25℃	−55 to +125℃
LD(※)	X5R	±15%	25℃	−55 to +85℃
F	F	+30/−80%	20℃	−25 to +85℃
	Y5V	+22/−82%	25℃	−30 to +85℃

Note : ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

Class 1
Capacitance at 20℃ and 85℃ shall be measured in thermal equilibrium, and the temperature characteristic shall be calculated from the following equation.

$$\frac{(C_{85}-C_{20})}{C_{20}\times\Delta T}\times 10^{6}(\text{ppm/℃}) \qquad \Delta T=65$$

Class 2
Capacitance at each step shall be measured in thermal equilibrium, and the temperature characteristic shall be calculated from the following equation.

Step	B、F	X5R、X7R、X6S、X7S、Y5V
1	Minimum operating temperature	
2	20℃	25℃
3	Maximum operating temperature	

$$\frac{(C-C_2)}{C_2} \times 100(\%)$$

C : Capacitance in Step 1 or Step 3
C2 : Capacitance in Step 2

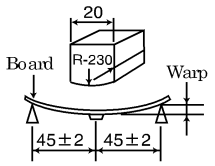
9. Deflection

Specified Value	Temperature Compensating(Class1)	Standard	Appearance : No abnormality Capacitance change : Within ±5% or ±0.5 pF, whichever is larger.
		High Frequency Type	Appearance : No abnormality Capacitance change : Within±0.5 pF
	High Permittivity (Class2)		Appearance : No abnormality Capacitance change : Within ±12.5%(BJ, B7, C6, C7,LD(※)) Within ±30%(F) Note: ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

	Multilayer Ceramic Capacitors	
	042, 063, ※105 Type	The other types
Board	Glass epoxy-resin substrate	
Thickness	0.8mm	1.6mm
Warp	1mm	
Duration	10 sec.	

※105 Type thickness, C: 0.2mm ,P: 0.3mm.



(Unit: mm)

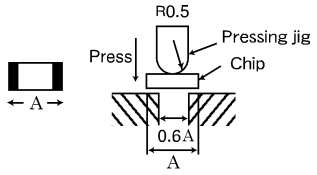
Capacitance measurement shall be conducted with the board bent

10. Body Strength

Specified Value	Temperature Compensating(Class1)	Standard	—
		High Frequency Type	No mechanical damage.
	High Permittivity (Class2)		—

Test Methods and Remarks

High Frequency Type
Applied force : 5N
Duration : 10 sec.

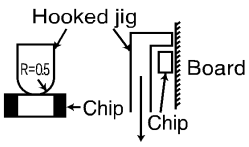


11. Adhesive Strength of Terminal Electrodes

Specified Value	Temperature Compensating(Class1)	Standard	No terminal separation or its indication.
		High Frequency Type	
	High Permittivity (Class2)		

Test Methods and Remarks

	Multilayer Ceramic Capacitors	
	042, 063 Type	105 Type or more
Applied force	2N	5N
Duration	30±5 sec.	



12. Solderability

Specified Value	Temperature Compensating(Class1)	Standard	At least 95% of terminal electrode is covered by new solder.
		High Frequency Type	
	High Permittivity (Class2)		

Test Methods and Remarks

	Eutectic solder	Lead-free solder
Solder type	H60A or H63A	Sn-3.0Ag-0.5Cu
Solder temperature	230±5℃	245±3℃
Duration	4±1 sec.	

13. Resistance to Soldering

Specified Value

Temperature Compensating(Class1)	Standard	Appearance : No abnormality Capacitance change : Within ±2.5% or ±0.25pF, whichever is larger. Q : Initial value Insulation resistance : Initial value Withstanding voltage (between terminals) : No abnormality
	High Frequency Type	Appearance : No abnormality Capacitance change : Within ±2.5% Q : Initial value Insulation resistance : Initial value Withstanding voltage (between terminals) : No abnormality
High Permittivity (Class2) Note 1		Appearance : No abnormality Capacitance change : Within ±7.5%(BJ, B7, C6, C7, LD(※)) Within ±20%(F) Dissipation factor : Initial value Insulation resistance : Initial value Withstanding voltage (between terminals): No abnormality Note: ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

	Class 1	
	042, 063 Type	105 Type
Preconditioning	None	
Preheating	150℃, 1 to 2 min.	80 to 100℃, 2 to 5 min. 150 to 200℃, 2 to 5 min.
Solder temp.	270±5℃	
Duration	3±0.5 sec.	
Recovery	6 to 24 hrs (Standard condition) Note 5	

	Class 2		
	042、063 Type	105, 107, 212 Type	316, 325 Type
Preconditioning	Thermal treatment (at 150℃ for 1 hr) Note 2		
Preheating	150℃, 1 to 2 min.	80 to 100℃, 2 to 5 min. 150 to 200℃, 2 to 5 min.	80 to 100℃, 5 to 10 min. 150 to 200℃, 5 to 10 min.
Solder temp.	270±5℃		
Duration	3±0.5 sec.		
Recovery	24±2 hrs (Standard condition) Note 5		

14. Temperature Cycle (Thermal Shock)

Specified Value

Temperature Compensating(Class1)	Standard	Appearance : No abnormality Capacitance change : Within ±2.5% or ±0.25pF, whichever is larger. Q : Initial value Insulation resistance : Initial value Withstanding voltage (between terminals) : No abnormality
	High Frequency Type	Appearance : No abnormality Capacitance change : Within ±0.25pF Q : Initial value Insulation resistance : Initial value Withstanding voltage (between terminals) : No abnormality
High Permittivity (Class2) Note 1		Appearance : No abnormality Capacitance change : Within ±7.5% (BJ, B7, C6, C7, LD(※)) Within ±20% (F) Dissipation factor : Initial value Insulation resistance : Initial value Withstanding voltage (between terminals) : No abnormality Note: ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

	Class 1	Class 2
Preconditioning	None	Thermal treatment (at 150℃ for 1 hr) Note 2
1 cycle		

Step	Temperature(℃)	Time(min.)
1	Minimum operating temperature	30±3
2	Normal temperature	2 to 3
3	Maximum operating temperature	30±3
4	Normal temperature	2 to 3

Number of cycles	5 times	
Recovery	6 to 24 hrs (Standard condition) Note 5	24±2 hrs (Standard condition) Note 5

15. Humidity (Steady State)

Specified Value

Temperature Compensating(Class1)	Standard	Appearance : No abnormality Capacitance change : Within ±5% or ±0.5pF, whichever is larger. Q : C＜10pF : Q≧200＋10C 10≦C＜30pF : Q≧275＋2.5C C≧30pF:Q≧350(C:Nominal capacitance) Insulation resistance : 1000 MΩ min.
	High Frequency Type	Appearance : No abnormality Capacitance change : Within ±0.5pF, Insulation resistance : 1000 MΩ min.
High Permittivity (Class2) Note 1		Appearance : No abnormality Capacitance change : Within ±12.5% (BJ, B7, C6, C7, LD(※)) Within ±30% (F) Dissipation factor : 5.0% max.(BJ, B7, C6, C7, LD(※)) 11.0% max.(F) Insulation resistance : 50 MΩ μF or 1000 MΩ whichever is smaller. Note: ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

	Class 1		Class 2
	Standard	High Frequency Type	All items
Preconditioning	None		Thermal treatment(at 150℃ for 1 hr) Note 2
Temperature	40±2℃	60±2℃	40±2℃
Humidity	90 to 95%RH		90 to 95%RH
Duration	500＋24/－0 hrs		500＋24/－0 hrs
Recovery	6 to 24 hrs (Standard condition) Note 5		24±2 hrs (Standard condition) Note 5

16. Humidity Loading

Specified Value

Temperature Compensating(Class1)	Standard	Appearance : No abnormality Capacitance change : Within ±7.5% or ±0.75pF, whichever is larger. Q : C＜30pF : Q≧100＋10C/3 C≧30pF : Q≧200 (C : Nominal capacitance) Insulation resistance : 500 MΩ min.
	High Frequency Type	Appearance : No abnormality Capacitance change : C≦2pF : Within ±0.4 pF C＞2pF : Within ±0.75 pF (C : Nominal capacitance) Insulation resistance : 500 MΩ min.
High Permittivity (Class2) Note 1		Appearance : No abnormality Capacitance change : Within ±12.5% (BJ, B7, C6, C7, LD(※)) Within ±30% (F) Dissipation factor : 5.0% max. (BJ, B7, C6, C7, LD(※)) 11.0% max. (F) Insulation resistance : 25 MΩ μF or 500 MΩ, whichever is smaller. Note: ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

	Class 1		Class 2
	Standard	High Frequency Type	All items
Preconditioning	None		Voltage treatment (Rated voltage are applied for 1 hour at 40℃) Note 3
Temperature	40±2℃	60±2℃	40±2℃
Humidity	90 to 95%RH		90 to 95%RH
Duration	500＋24/－0 hrs		500＋24/－0 hrs
Applied voltage	Rated voltage		Rated voltage
Charge/discharge current	50mA max.		50mA max.
Recovery	6 to 24 hrs (Standard condition) Note 5		24±2 hrs(Standard condition) Note 5

17. High Temperature Loading

Specified Value	Temperature Compensating(Class1)	Standard	Appearance : No abnormality Capacitance change : Within ±3% or ±0.3pF, whichever is larger. Q : C＜10pF: Q≧200＋10C 10≦C＜30pF:Q≧275＋2.5C C≧30pF: Q≧350(C:Nominal capacitance) Insulation resistance : 1000 MΩ min.
		High Frequency Type	Appearance : No abnormality Capacitance change : Within ±3% or ±0.3pF, whichever is larger. Insulation resistance : 1000 MΩ min.
	High Permittivity (Class2) Note 1		Appearance : No abnormality Capacitance change : Within ±12.5% (BJ, B7, C6, C7, LD(※)) Within ±30% (F) Dissipation factor : 5.0% max.(BJ, B7, C6, C7, LD(※)) 11.0% max.(F) Insulation resistance : 50 MΩ μF or 1000 MΩ, whichever is smaller. Note: ※LD Low distortion high value multilayer ceramic capacitor

Test Methods and Remarks

	Class 1		Class 2		
	Standard	High Frequency Type	BJ, LD(※), F	C6	B7, C7
Preconditioning	None		Voltage treatment(Twice the rated voltage shall be applied for 1 hour at 85℃, 105℃ or 125℃) Note 3, 4		
Temperature	Maximum operating temperature		Maximum operating temperature		
Duration	1000＋48/－0 hrs		1000＋48/－0 hrs		
Applied voltage	Rated voltage×2		Rated voltage×2 Note 4		
Charge/discharge current	50mA max.		50mA max.		
Recovery	6 to 24hr (Standard condition) Note 5		24±2 hrs (Standard condition) Note 5		

Note: ※LD Low distortion high value multilayer ceramic capacitor

Note 1 The figures indicate typical specifications. Please refer to individual specifications in detail.

Note 2 Thermal treatment : Initial value shall be measured after test sample is heat-treated at 150＋0/－10℃ for an hour and kept at room temperature for 24±2hours.

Note 3 Voltage treatment : Initial value shall be measured after test sample is voltage-treated for an hour at both the temperature and voltage specified in the test conditions, and kept at room temperature for 24±2hours.

Note 4 150% of rated voltage is applicable to some items. Please refer to their specifications for further information.

Note 5 Standard condition: Temperature: 5 to 35℃, Relative humidity: 45 to 85 % RH, Air pressure: 86 to 106kPa When there are questions concerning measurement results, in order to provide correlation data, the test shall be conducted under the following condition.
Temperature: 20±2℃, Relative humidity: 60 to 70 % RH, Air pressure: 86 to 106kPa Unless otherwise specified, all the tests are conducted under the "standard condition".

Precautions on the use of Multilayer Ceramic Capacitors

■PRECAUTIONS

1. Circuit Design

Precautions

◆Verification of operating environment, electrical rating and performance

1. A malfunction of equipment in fields such as medical, aerospace, nuclear control, etc. may cause serious harm to human life or have severe social ramifications.
   Therefore, any capacitors to be used in such equipment may require higher safety and reliability, and shall be clearly differentiated from them used in general purpose applications.

◆Operating Voltage (Verification of Rated voltage)

1. The operating voltage for capacitors must always be their rated voltage or less.
   If an AC voltage is loaded on a DC voltage, the sum of the two peak voltages shall be the rated voltage or less.
   For a circuit where an AC or a pulse voltage may be used, the sum of their peak voltages shall also be the rated voltage or less.
2. Even if an applied voltage is the rated voltage or less reliability of capacitors may be deteriorated in case that either a high frequency AC voltage or a pulse voltage having rapid rise time is used in a circuit.

2. PCB Design

Precautions

◆Pattern configurations (Design of Land-patterns)

1. When capacitors are mounted on PCBs, the amount of solder used (size of fillet) can directly affect the capacitor performance. Therefore, the following items must be carefully considered in the design of land patterns:
   (1) Excessive solder applied can cause mechanical stresses which lead to chip breaking or cracking. Therefore, please consider appropriate land-patterns for proper amount of solder.
   (2) When more than one component are jointly soldered onto the same land, each component's soldering point shall be separated by solder-resist.

◆Pattern configurations (Capacitor layout on PCBs)

After capacitors are mounted on boards, they can be subjected to mechanical stresses in subsequent manufacturing processes (PCB cutting, board inspection, mounting of additional parts, assembly into the chassis, wave soldering of the boards, etc.). For this reason, land pattern configurations and positions of capacitors shall be carefully considered to minimize stresses.

Technical considerations

◆Pattern configurations (Design of Land-patterns)

The following diagrams and tables show some examples of recommended land patterns to prevent excessive solder amounts.

(1) Recommended land dimensions for typical chip capacitors

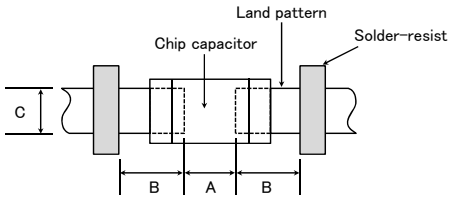
●Multilayer Ceramic Capacitors : Recommended land dimensions

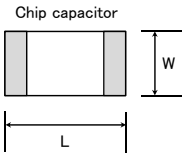
(unit: mm)

Wave-soldering

Type		107	212	316	325
Size	L	1.6	2.0	3.2	3.2
	W	0.8	1.25	1.6	2.5
A		0.8 to 1.0	1.0 to 1.4	1.8 to 2.5	1.8 to 2.5
B		0.5 to 0.8	0.8 to 1.5	0.8 to 1.7	0.8 to 1.7
C		0.6 to 0.8	0.9 to 1.2	1.2 to 1.6	1.8 to 2.5

Land patterns for PCBs





Reflow-soldering

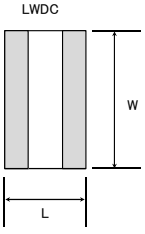
Type		042	063	105	107	212	316	325	432
Size	L	0.4	0.6	1.0	1.6	2.0	3.2	3.2	4.5
	W	0.2	0.3	0.5	0.8	1.25	1.6	2.5	3.2
A		0.15 to 0.25	0.20 to 0.30	0.45 to 0.55	0.8 to 1.0	0.8 to 1.2	1.8 to 2.5	1.8 to 2.5	2.5 to 3.5
B		0.15 to 0.20	0.20 to 0.30	0.40 to 0.50	0.6 to 0.8	0.8 to 1.2	1.0 to 1.5	1.0 to 1.5	1.5 to 1.8
C		0.15 to 0.30	0.25 to 0.40	0.45 to 0.55	0.6 to 0.8	0.9 to 1.6	1.2 to 2.0	1.8 to 3.2	2.3 to 3.5

Note : Recommended land size might be different according to the allowance of the size of the product.

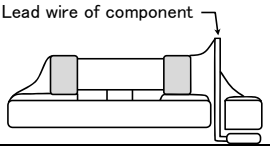
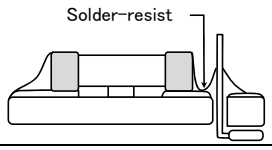
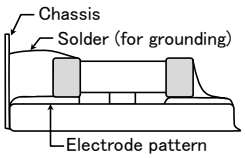
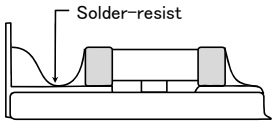
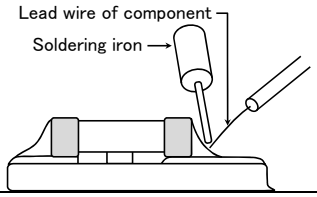
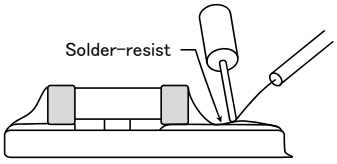
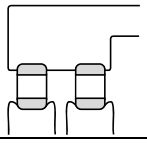
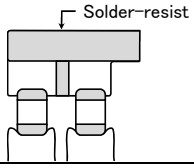
●LWDC: Recommended land dimensions for reflow-soldering

(unit: mm)

Type		105	107	212
Size	L	0.52	0.8	1.25
	W	1.0	1.6	2.0
A		0.18 to 0.22	0.25 to 0.3	0.5 to 0.7
B		0.2 to 0.25	0.3 to 0.4	0.4 to 0.5
C		0.9 to 1.1	1.5 to 1.7	1.9 to 2.1

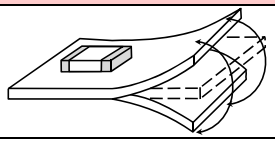
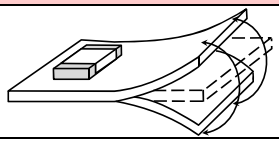


(2)Examples of good and bad solder application

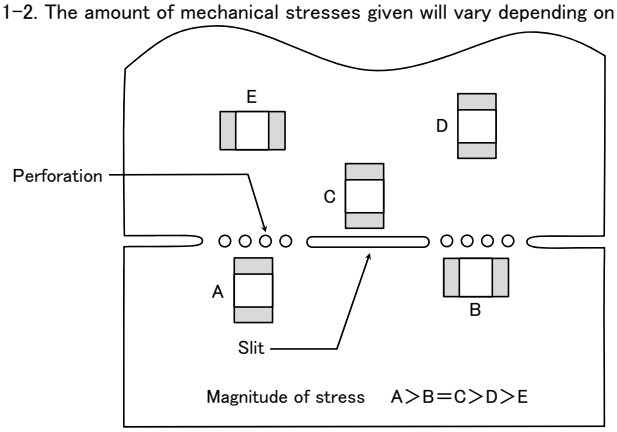
Item	Not recommended	Recommended
Mixed mounting of SMD and leaded components		
Component placement close to the chassis		
Hand–soldering of leaded components near mounted components		
Horizontal component placement		

◆Pattern configurations (Capacitor layout on PCBs)

1–1. The following is examples of good and bad capacitor layouts ; capacitors shall be located to minimize any possible mechanical stresses from board warp or deflection.

Items	Not recommended	Recommended
Deflection of board		 Place the product at a right angle to the direction of the anticipated mechanical stress.

1–2. The amount of mechanical stresses given will vary depending on capacitor layout. Please refer to diagram below.



1–3. When PCB is split, the amount of mechanical stress on the capacitors can vary according to the method used. The following methods are listed in order from least stressful to most stressful: push–back, slit, V–grooving, and perforation. Thus, please consider the PCB, split methods as well as chip location.

3. Mounting

Precautions

◆Adjustment of mounting machine

1. When capacitors are mounted on PCB, excessive impact load shall not be imposed on them.
2. Maintenance and inspection of mounting machines shall be conducted periodically.

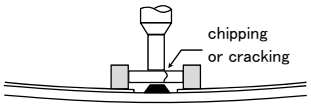
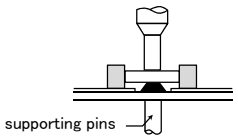
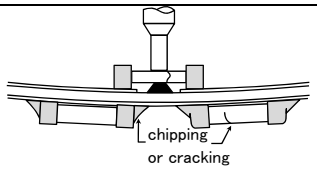
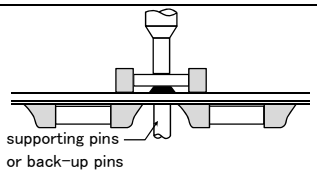
◆Selection of Adhesives

1. When chips are attached on PCBs with adhesives prior to soldering, it may cause capacitor characteristics degradation unless the following factors are appropriately checked : size of land patterns, type of adhesive, amount applied, hardening temperature and hardening period. Therefore, please contact us for further information.

Technical considerations

◆Adjustment of mounting machine

1. When the bottom dead center of a pick-up nozzle is too low, excessive force is imposed on capacitors and causes damages. To avoid this, the following points shall be considerable.
   (1) The bottom dead center of the pick-up nozzle shall be adjusted to the surface level of PCB without the board deflection.
   (2) The pressure of nozzle shall be adjusted between 1 and 3 N static loads.
   (3) To reduce the amount of deflection of the board caused by impact of the pick-up nozzle, supporting pins or back-up pins shall be used on the other side of the PCB. The following diagrams show some typical examples of good and bad pick-up nozzle placement:

Item	Improper method	Proper method
Single-sided mounting		
Double-sided mounting		

2. As the alignment pin is worn out, adjustment of the nozzle height can cause chipping or cracking of capacitors because of mechanical impact on the capacitors.
   To avoid this, the monitoring of the width between the alignment pins in the stopped position, maintenance, check and replacement of the pin shall be conducted periodically.

◆Selection of Adhesives

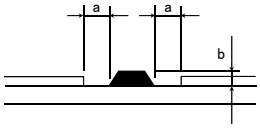
Some adhesives may cause IR deterioration. The different shrinkage percentage of between the adhesive and the capacitors may result in stresses on the capacitors and lead to cracking. Moreover, too little or too much adhesive applied to the board may adversely affect components. Therefore, the following precautions shall be noted in the application of adhesives.

(1) Required adhesive characteristics
   a. The adhesive shall be strong enough to hold parts on the board during the mounting & solder process.
   b. The adhesive shall have sufficient strength at high temperatures.
   c. The adhesive shall have good coating and thickness consistency.
   d. The adhesive shall be used during its prescribed shelf life.
   e. The adhesive shall harden rapidly.
   f. The adhesive shall have corrosion resistance.
   g. The adhesive shall have excellent insulation characteristics.
   h. The adhesive shall have no emission of toxic gasses and no effect on the human body.

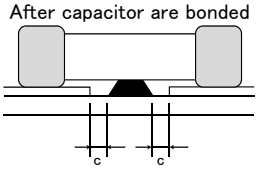
(2) The recommended amount of adhesives is as follows;
   [Recommended condition]

Figure	212/316 case sizes as examples
a	0.3mm min
b	100 to 120 μm
c	Adhesives shall not contact land

Amount adhesive



After capacitor are bonded



4. Soldering

Precautions

◆Selection of Flux

Since flux may have a significant effect on the performance of capacitors, it is necessary to verify the following conditions prior to use;
(1) Flux used shall be less than or equal to 0.1 wt%(in Cl equivalent) of halogenated content. Flux having a strong acidity content shall not be applied.
(2) When shall capacitors are soldered on boards, the amount of flux applied shall be controlled at the optimum level.
(3) When water-soluble flux is used, special care shall be taken to properly clean the boards.

◆Soldering

Temperature, time, amount of solder, etc. shall be set in accordance with their recommended conditions.
Sn-Zn solder paste can adversely affect MLCC reliability.
Please contact us prior to usage of Sn-Zn solder.

Technical considerations

◆Selection of Flux

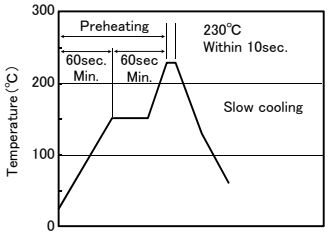
1-1. When too much halogenated substance(Chlorine, etc.) content is used to activate flux, or highly acidic flux is used, it may lead to corrosion of terminal electrodes or degradation of insulation resistance on the surfaces of the capacitors.
1-2. Flux is used to increase solderability in wave soldering. However if too much flux is applied, a large amount of flux gas may be emitted and may adversely affect the solderability. To minimize the amount of flux applied, it is recommended to use a flux-bubbling system.
1-3. Since the residue of water-soluble flux is easily dissolved in moisture in the air, the residues on the surfaces of capacitors in high humidity conditions may cause a degradation of insulation resistance and reliability of the capacitors. Therefore, the cleaning methods and the capability of the machines used shall also be considered carefully when water-soluble flux is used.

◆Soldering

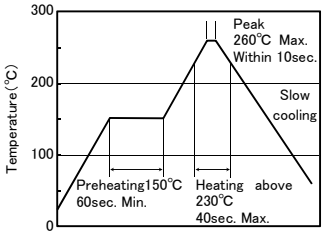
- Ceramic chip capacitors are susceptible to thermal shock when exposed to rapid or concentrated heating or rapid cooling.
- Therefore, the soldering must be conducted with great care so as to prevent malfunction of the components due to excessive thermal shock.
- Preheating : Capacitors shall be preheated sufficiently, and the temperature difference between the capacitors and solder shall be within 100 to 130℃.
- Cooling : The temperature difference between the capacitors and cleaning process shall not be greater than 100℃.

[Reflow soldering]

【Recommended conditions for eutectic soldering】

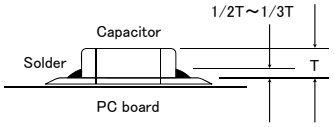


【Recommended condition for Pb-free soldering】



Caution

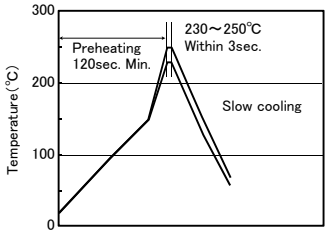
①The ideal condition is to have solder mass (fillet) controlled to 1/2 to 1/3 of the thickness of a capacitor.



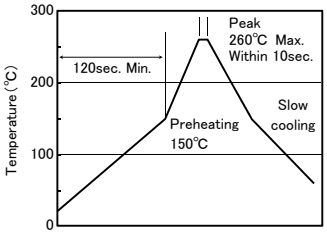
②Because excessive dwell times can adversely affect solderability, soldering duration shall be kept as close to recommended times as possible.

[Wave soldering]

【Recommended conditions for eutectic soldering】



【Recommended condition for Pb-free soldering】

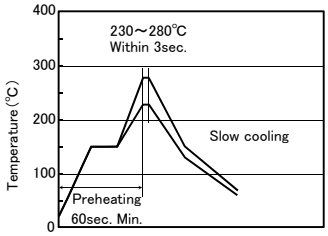


Caution

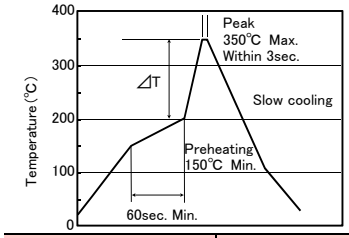
①Wave soldering must not be applied to capacitors designated as for reflow soldering only.

[Hand soldering]

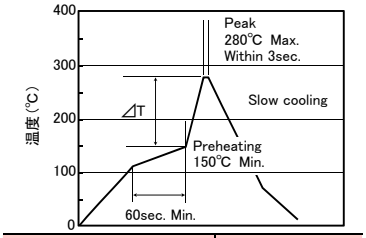
【Recommended conditions for eutectic soldering】



【Recommended condition for Pb-free soldering】



	⊿T
316type or less	⊿T≦150℃



	⊿T
325type or more	⊿T≦130℃

Caution

①Use a 50W soldering iron with a maximum tip diameter of 1.0 mm.

②The soldering iron shall not directly touch capacitors.

5. Cleaning

Precautions

◆Cleaning conditions

1. When PCBs are cleaned after capacitors mounting, please select the appropriate cleaning solution in accordance with the intended use of the cleaning. (e.g. to remove soldering flux or other materials from the production process.)
2. Cleaning condition shall be determined after it is verified by using actual cleaning machine that the cleaning process does not affect capacitor's characteristics.

Technical considerations

1. The use of inappropriate cleaning solutions can cause foreign substances such as flux residue to adhere to capacitors or deteriorate their outer coating, resulting in a degradation of the capacitor's electrical properties (especially insulation resistance).
2. Inappropriate cleaning conditions (insufficient or excessive cleaning) may adversely affect the performance of the capacitors. In the case of ultrasonic cleaning, too much power output can cause excessive vibration of PCBs which may lead to the cracking of capacitors or the soldered portion, or decrease the terminal electrodes' strength. Therefore, the following conditions shall be carefully checked;

   Ultrasonic output : 20 W/ℓ or less

   Ultrasonic frequency : 40 kHz or less

   Ultrasonic washing period : 5 min. or less

6. Resin coating and mold	
Precautions	1. With some type of resins, decomposition gas or chemical reaction vapor may remain inside the resin during the hardening period or while left under normal storage conditions resulting in the deterioration of the capacitor's performance. 2. When a resin's hardening temperature is higher than capacitor's operating temperature, the stresses generated by the excessive heat may lead to damage or destruction of capacitors. The use of such resins, molding materials etc. is not recommended.

7. Handling	
Precautions	◆Splitting of PCB 1. When PCBs are split after components mounting, care shall be taken so as not to give any stresses of deflection or twisting to the board. 2. Board separation shall not be done manually, but by using the appropriate devices. ◆Mechanical considerations Be careful not to subject capacitors to excessive mechanical shocks. (1)If ceramic capacitors are dropped onto a floor or a hard surface, they shall not be used. (2)Please be careful that the mounted components do not come in contact with or bump against other boards or components.

8. Storage conditions	
Precautions	◆Storage 1. To maintain the solderability of terminal electrodes and to keep packaging materials in good condition, care must be taken to control temperature and humidity in the storage area. Humidity should especially be kept as low as possible. ・Recommended conditions Ambient temperature : Below 30℃ Humidity : Below 70% RH The ambient temperature must be kept below 40℃. Even under ideal storage conditions, solderability of capacitor is deteriorated as time passes, so capacitors shall be used within 6 months from the time of delivery. ・Ceramic chip capacitors shall be kept where no chlorine or sulfur exists in the air. 2. The capacitance values of high dielectric constant capacitors will gradually decrease with the passage of time, so care shall be taken to design circuits . Even if capacitance value decreases as time passes, it will get back to the initial value by a heat treatment at 150℃ for 1hour.
Technical considerations	If capacitors are stored in a high temperature and humidity environment, it might rapidly cause poor solderability due to terminal oxidation and quality loss of taping/packaging materials. For this reason, capacitors shall be used within 6 months from the time of delivery. If exceeding the above period, please check solderability before using the capacitors.

※RCR-2335B(Safety Application Guide for fixed ceramic capacitors for use in electronic equipment)is published by JEITA.
Please check the guide regarding precautions for deflection test, soldering by spot heat, and so on.