FEATURES:

- 128KB direct mapped secondary cache module
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write
- Matches all timing and signals of the i486™ processor
- 72 lead FR-4 SIMM (Single-in-Line Memory Module)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

DESCRIPTION:

The IDT7MP6086 is a 128KB direct mapped secondary cache module, using four IDT71589 32K x 9 CacheRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) substrate with gold-plated leads. Extremely high speeds are achieved using IDT's high performance, high reliability CMOS technology. This module is designed to facilitate the implementation of the highest perfor-mance secondary caches for the i486 architecture while using low-speed logic devices and consuming the minimum board space.

The IDT7MP6086 contains a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle. An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

Three program identification pins are provided so that the system can uniquely identify the IDT7MP6086.

Note that individual parity bits are grouped with their respective bytes, not all at the end.

The SIMM package configuration allows 72 leads to be placed on a package 4.25 inches long, 0.55 inches tall and 0.25 inches thick. All inputs and outputs of the IDT7MP6086 are TTL-compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM

2835 drw 01
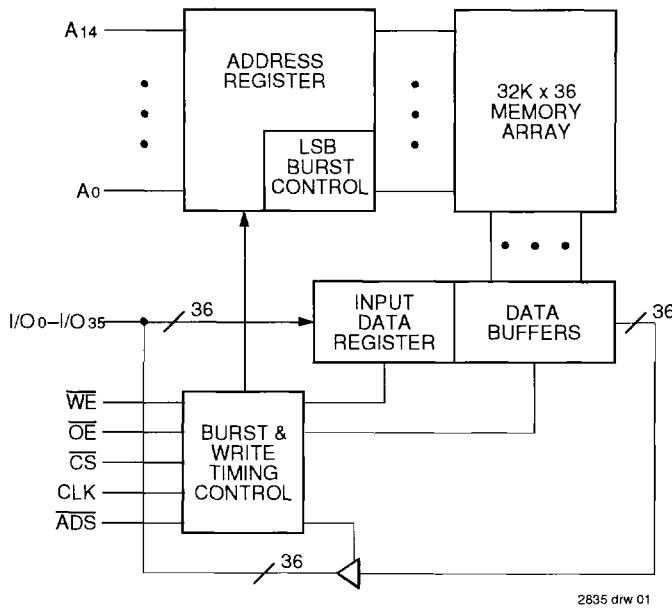
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All others are trademarks of their respective companies.

COMMERCIAL TEMPERATURE RANGE **AUGUST 1993**

DSC-7089/3

PIN CONFIGURATION[1]

```
                1 | GND
  GND   | 2    3 | Vcc
  I/O0  | 4    5 | I/O1
  I/O2  | 6    7 | I/O3
  I/O4  | 8    9 | I/O5
  I/O6  | 10  11 | I/O7
  I/O8  | 12  13 | WE0
  WE1   | 14  15 | I/O9
  I/O10 | 16  17 | I/O11
  GND   | 18  19 | I/O12
  I/O13 | 20  21 | I/O14
  I/O15 | 22  23 | I/O16
  I/O17 | 24  25 | A0
  A1    | 26  27 | A2
  A3    | 28  29 | A4
  A5    | 30  31 | A6
  A7    | 32  33 | A8
  ADS   | 34  35 | CLK
  Vcc   | 36
             37 | GND
  CS    | 38  39 | OE
  A9    | 40  41 | A10
  A11   | 42  43 | A12
  A13   | 44  45 | A14
  I/O18 | 46  47 | I/O19
  I/O20 | 48  49 | I/O21
  I/O22 | 50  51 | I/O23
  I/O24 | 52  53 | I/O25
  I/O26 | 54  55 | GND
  WE2   | 56  57 | WE3
  I/O27 | 58  59 | I/O28
  I/O29 | 60  61 | I/O30
  I/O31 | 62  63 | I/O32
  I/O33 | 64  65 | I/O34
  I/O35 | 66  67 | PD0
  PD1   | 68  69 | PD2
  Vcc   | 70  71 | GND
  GND   | 72
```

2835 drw 02

SIMM
TOP VIEW

NOTES:
1. Please consult the factory regarding program identification pins.

PIN NAMES

A0–A14	Address Inputs
I/O0–I/O35	Data Input/Output
CS	Chip Select/Count Enable
WE0-3	Byte Write Enables
OE	Output Enable
ADS	Address Status
CLK	System Clock
PD0-2	Program Identification
GND	Ground
Vcc	Power

2835 tbl 01

CAPACITANCE (TA = +25°C, F = 1.0 MHZ)

Symbol	Parameter[1]	Condition	Max.	Unit
CIN	Input Capacitance (Data)	VIN = 0V	13	pF
CIN	Input Capacitance (Address & Control)	VIN = 0V	42	pF
CI/O	Output Capacitance	VOUT = 0V	13	pF

NOTE: 2835 tbl 02
1. This parameter is guaranteed by design but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	−10 to +85	°C
TSTG	Storage Temperature	−55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2835 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2835 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	−0.5[1]	—	0.8	V

NOTE: 2835 tbl 05
1. VIL = −3.0V for pulse width less than 5ns.

TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	High-Z	Outputs Disabled
—	—	—	—	H	—	L	DATA$_{OUT}$	Read
↑	X	H	—	L	L	H	DATA$_{IN}$	Write
↑	L	X	—	L	L	H	DATA$_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

2635 tbl 06

NOTE:
H   = HIGH
L   = LOW
X   = Don't Care
–   = Unrelated
Hi-Z = High Impedance

DC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, TA = 0°C TO + 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$|I_{LI}|$	Input Leakage Current (Address & Contol)	Vcc = 5.5V, VIN = 0V to Vcc	—	40	μA
$|I_{LI}|$	Input Leakage Current (Data)	Vcc = 5.5V, VIN = 0V to Vcc	—	10	μA
$|I_{LO}|$	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = 0V to Vcc, Vcc = Max.	—	10	μA
VOL	Output Low Voltage	IOL = 8mA, Vcc = Min.	—	0.4	V
VOH	Output High Voltage	IOH = –4mA, Vcc = Min.	2.4	—	V

DC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, TA = 0°C to +70°C)

Symbol	Parameter	Test Condition	40MHz	33MHz	Unit
ICC1	Operating Power Supply Current	$\overline{CS}$ = VIL Outputs Open Vcc = Max., f = 0[1]	520	520	mA
ICC2	Dynamic Operating Current	$\overline{CS}$ = VIL Outputs Open Vcc = Max., f = fMAX[1]	960	880	mA

2835 tbl 08

NOTE:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency of read cycles of 1/tRC. f = 0 means no input lines change.
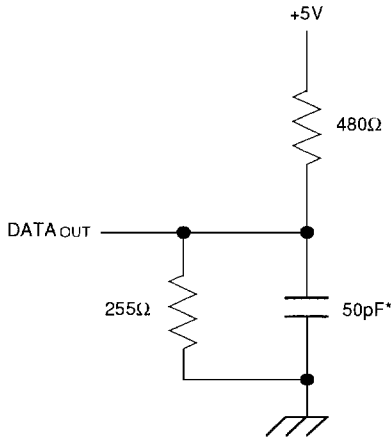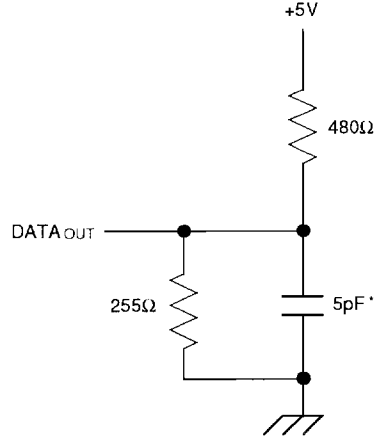
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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2835 tbl 09

Figure 1. Output Load

Figure 1. Output Load
(for tOHZ, tCHZ, tOLZ and tCLZ)

*including scope and jig

## AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, TA = 0° to +70°C)

		7MP6086SxxM				
		40 MHz		33 MHz		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tCYC	Clock Cycle Time	25	—	30	—	ns
tCH	Clock Pulse HIGH	10	—	11	—	ns
tCL	Clock Pulse LOW	10	—	11	—	ns
ts1	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$)	4	—	4	—	ns
ts2	Set-up Time (Address, Input Data)	5	—	5	—	ns
tH1	Hold Time ($\overline{CS}\downarrow$ Input Data)	1	—	1	—	ns
tH2	Hold Time ($\overline{CS}\uparrow$, $\overline{WE}$, Address)	2	—	2	—	ns
tADSH	Hold Time ($\overline{ADS}$)	3	—	3	—	ns
tCD	Clock to Data Valid	—	19	—	24	ns
tDC	Data Valid After Clock	4	—	4	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	ns
tOLZ	Output Enable to Output in Low-Z[1,2]	2	—	2	—	ns
tOHZ	Output Disable to Output in High-Z[1,2]	—	8	—	9	ns

NOTES:
1. Transition is measured ±200mV from low or high-impedance voltage with load (Figure 2).
2. This parameter is guaranteed, but not tested.

2835 tbl 10

TIMING WAVEFORM OF BURST READ CYCLE

2835 drw 05
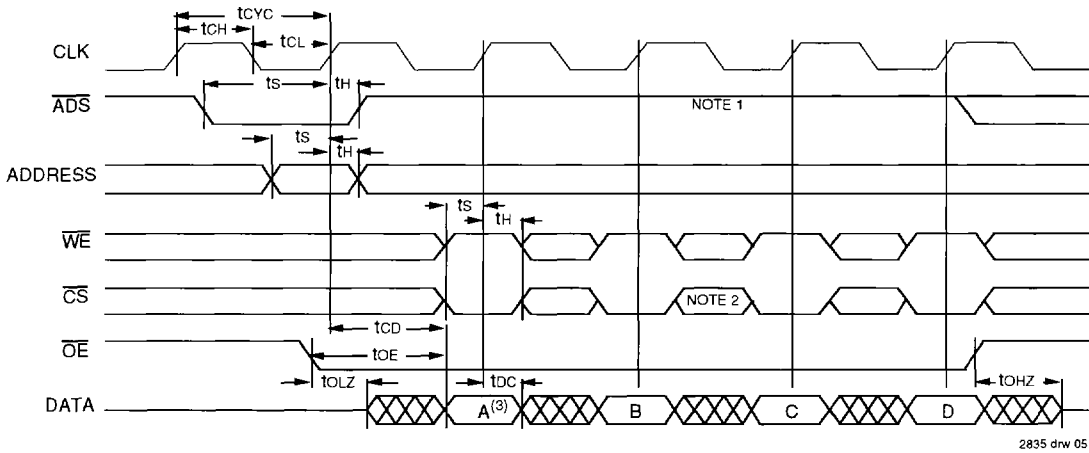
NOTES:
1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_S and t_H.
3. A-Data from input address. B-Data from input address except A_0 is now $\overline{A}_0$. C-Data from input address except A_1 is now $\overline{A}_1$. D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
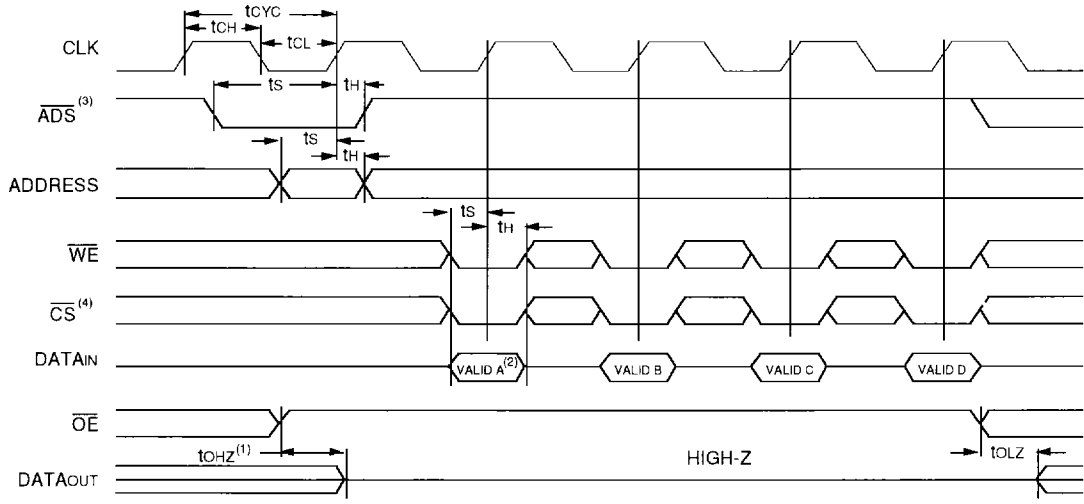
TIMING WAVEFORM OF WRITE CYCLE
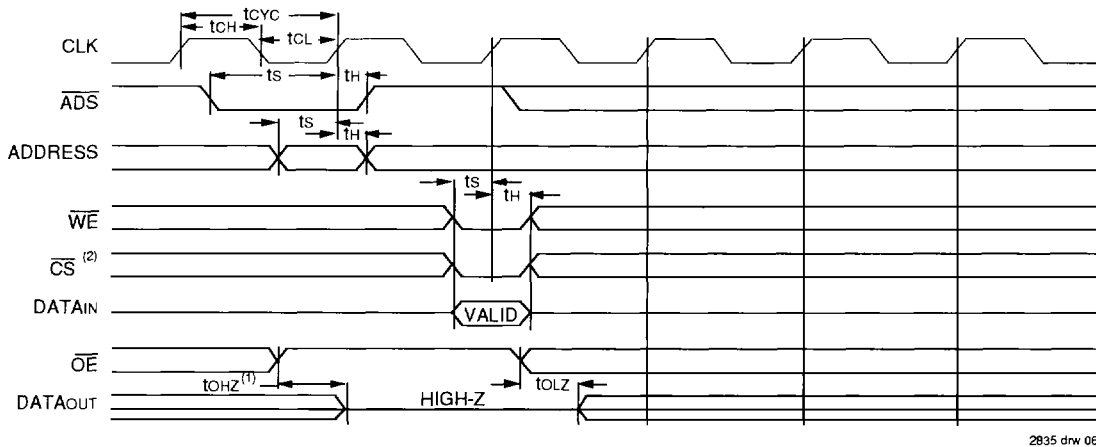
2835 drw 06

NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + t_S before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.
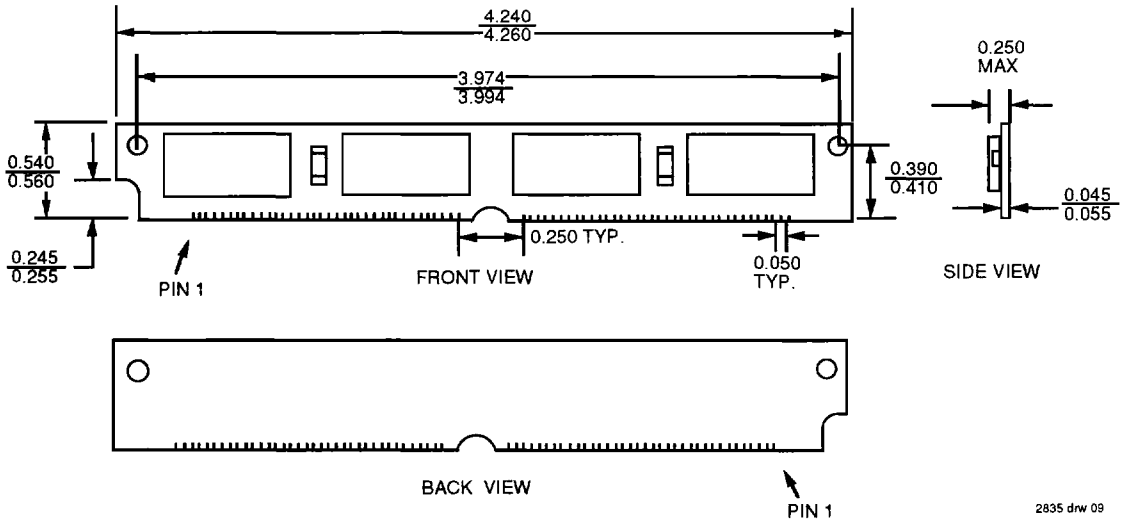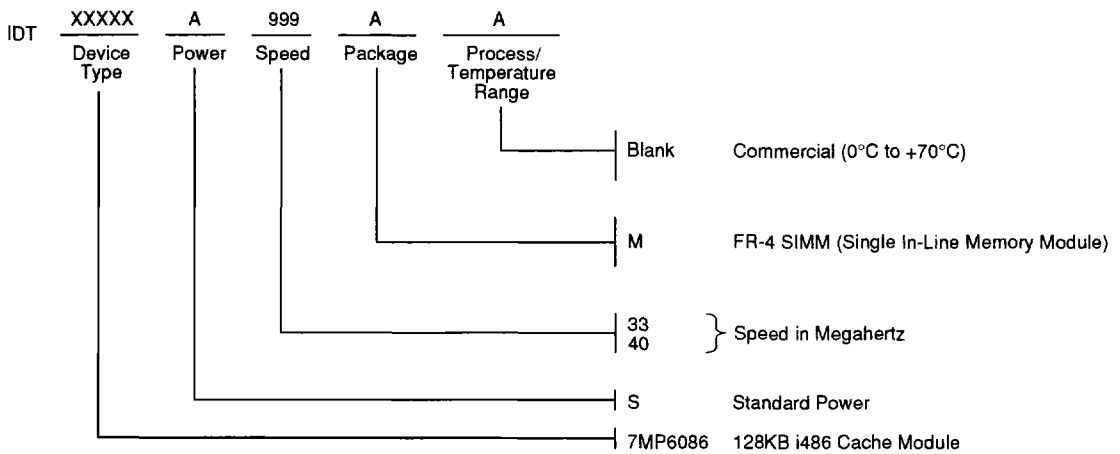
TIMING WAVEFORM OF BURST WRITE CYCLE

2835 drw 07

NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A0 is now $\overline{A}_0$.
   C-Data to be written to original input address except A1 is now $\overline{A}_1$.
   D-Data to be written to original input address except A0 and A1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and tH. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

PACKAGE DIMENSIONS

2835 drw 09

ORDERING INFORMATION

IDT XXXXX A 999 A A

Device Type | Power | Speed | Package | Process/Temperature Range

Blank — Commercial (0°C to +70°C)

M — FR-4 SIMM (Single In-Line Memory Module)

33 / 40 — Speed in Megahertz

S — Standard Power

7MP6086 — 128KB i486 Cache Module

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