AN4138
Application note

HSP061-2 / HSP062-2 high speed line protection on HDMI 1.4 link

Introduction

This application note presents the HSP061-2 and HSP062-2 series and their capability to protect HDMI 1.3 and HDMI 1.4 TMDS lines.

The HDMI interface is used for transmitting digital television audiovisual signals from DVD players, set-top- boxes and other sources to television sets and other video displays.

The HSP series have been developed to be compliant with:

- HDMI version 1.4 standard knowing the key point is the capability to transfer data with a maximum rate of 3.4 Gbps per channel without distortion. This leads the HSP061-2 and HSP062-2 to have a large bandwidth, to pass fast voltage slopes and to contain the 100 Ω line impedance, HSP061-2 and HSP062-2 are used on the TMDS line.
- IEC 61000-4-2 level 4 (8 kV contact discharge)

HSP061-2 and HSP062-2 series are composed of several packages and topologies (see *Chapter 1*) to better fit customer requirements in terms of PCB design.

HSP061-2 has the ground pin in the middle of the package and is proposed in:

- SOT-666: HSP061-2P6
- µQFN-6L: HSP061-2M6
- µQFN-4L: HSP061-2N4

HSP062-2 has the ground pin on the side of the package and is proposed in:

- SOT-666: HSP062-2P6
- µQFN-6L: HSP062-2M6

All these devices are flow-through.

1 HSP061-2 and HSP062-2 topology

HSP061-2 series protects two high speed lines (see *Figure 1*). This is a flow-through package to get an easy layout and to ensure the 100 Ω differential impedance on HDMI (*Figure 2*). As PCB tracks are not cut, this offers the possibility to test a board with or without protection depending on circuit portion to test.

The device is rated V_{BR}min = 6 V @ 1 mA with a low typical leakage current of 0.1 nA @ 25 °C.

Figure 1. HSP061-2 topology

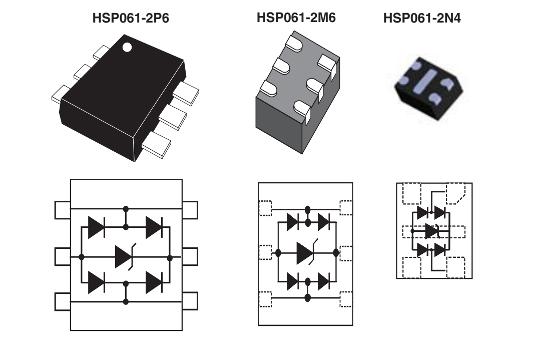
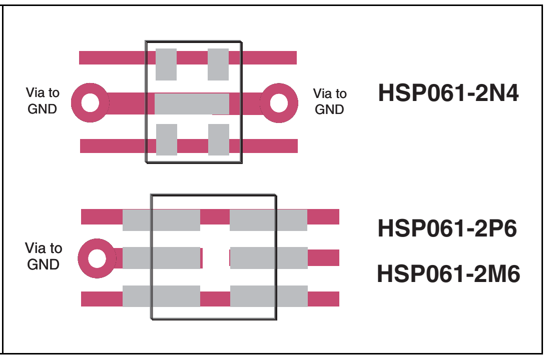


Figure 2. HSP061-2 footprint



For further information refer to the product datasheet for HSP061-2.

HSP062-2 series uses the same technology as the HSP061-2.The only difference is location the ground pin as shown in *Figure 3* and *Figure 4*.

Figure 3. HSP062-2 topology

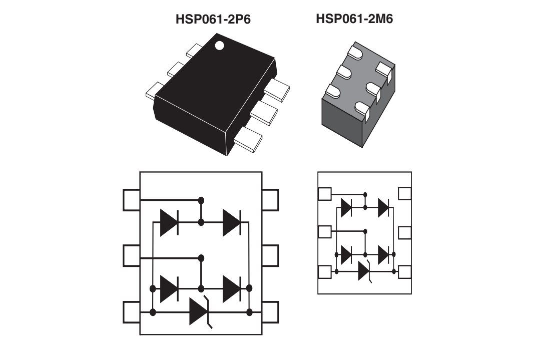
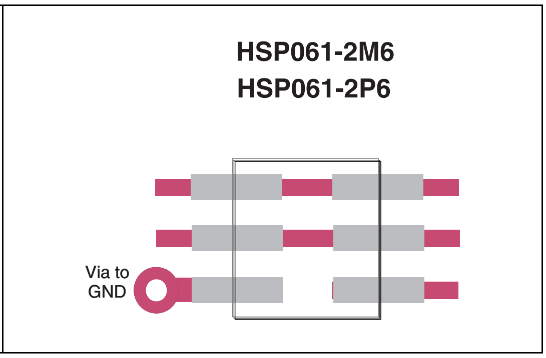


Figure 4. HSP062-2 footprint



For further information refer to the product datasheet for HSP062-2.

2 Characteristics related to HDMI 1.4

Protection bandwidth must be large enough to be transparent when a high bit rate is transferred on the line. The equation below give the relationship between lines, pixels, color depth and bit rate per channel:

$$\text{Lane data rate} = (\text{H\_total\_pixels}) \times (\text{V\_total\_lines}) \times \left(\frac{\text{Color\_depth}}{3}\right) \times (\text{Frame\_rate}) \times \frac{10}{8}$$

Table 1. Sample characteristics

CEA video code	Video format	Horizontal total pixel per line	Vertical total lines per frame	Frame rate (Hz)	Color depth (bits)	HDMI data rate (Gbps)	Lane data rate (Gbps)
16	1920 x 1080p	2200	1125	60	24	4.46	1.49
					30	5.57	1.86
					36	6.68	2.23
					48	8.91	2.97

HDMI standard give a minimum rise time of 75 ps between 20% and 80%. Considering a constant slope, this is equal to 100 ps between 10% and 90%.

In order to be transparent, the ESD protection must have a bandwidth in accordance with a rise time of 100 ps.

Usually, the relations between bandwidth and rise time is defined by the following formula:

$$BW = 1 / (PI \times tr)$$

tr = 100 ps gives a BW = 3.2 GHz.

Figure 5 shows the cut-off frequency of the HSP061-2N4 is 6 GHz which is high enough to correctly manage HDMI signals.

Figure 5. S21 attenuation measurement

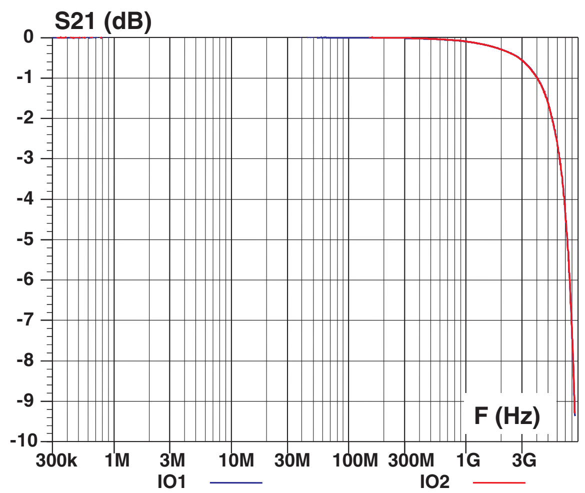


Figure 6. Differential impedance

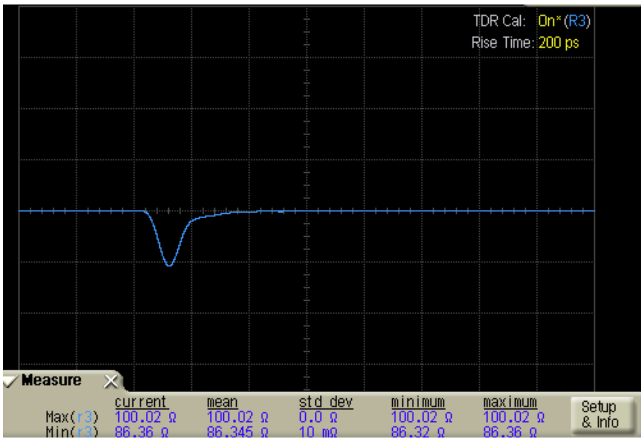
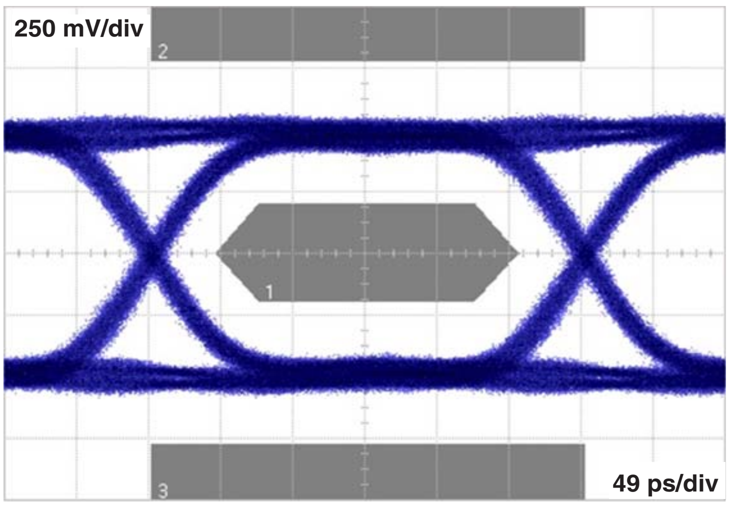


Figure 6 shows the differential impedance measured with the "Time Domain Reflectometry" method. This method consists of sending a pulse with a short rise time (200 ps between 10% and 90% for HDMI) and to measure the reflected pulse. This gives the impedance of the line along the signal path.

The HDMI standard requires 100 Ω ±15% differential impedance (between 85 Ω and 115 Ω). As shown *Figure 6*, TDR measurement on HSP062-2 gives an impedance between 91Ω and 100 Ω. These values are in accordance with the HDMI standard.

The eye diagrams defined in the HDMI standard are related to bit rate of the signal and to location (source or sink). There are more constraints on the source side, this is why we have chosen this one in the datasheet. The duration of the eye corresponds to a bit time. This diagram visualizes signal duration, synchronization, overshoot and capability of the signal to move from one state to another one. The key point for protection is to be sure there is no slow down effect. *Figure 7* shows the eye diagram for a 3.4 Gbps signal. This measurement is done directly on the HSP061-2 to avoid PCB measurement effects. Measurement shows a large safety margin between the eye pattern and the signal.

Figure 7. Eye diagram- HDMI mask at 3.4Gbps per channel (HSP061-2M6)

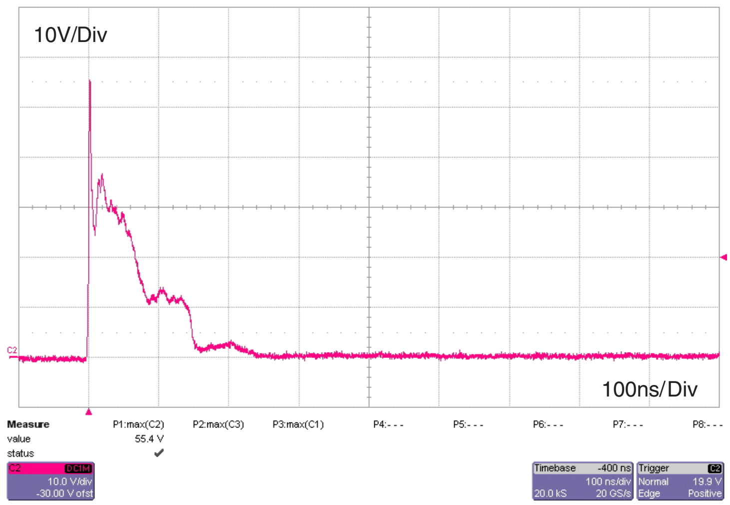


The goal of a protection device is to protect against parasitic disturbances. HDMI 1.4 standard specifies a 8 kV contact discharge requirement according to IEC 61000-4-2. The test must be performed 5 times with 1 second between each shot.

Figure 8 shows the ESD measurement when applied to HSP061-2M6. After a first short spike at around 55 V, the clamping voltage is limited at around 30 V at 30 ns instead of 8 kV.

There is no ageing phenomenon and the protection remains efficient whatever the number of surges. It is important to keep in mind most of the integrated circuits are ESD rated between 500 V and 2 kV (Human body model) thanks to internal protection.It is important to note IEC 61000-4-2 is much more severe than HBM, and for this reason it is mandatory to add an external protection.

Figure 8. IEC 61000-4-2 response



3 Layout considerations

3.1 Location for HSP device

The ESD projection is made by performance of the ESD protection device, but also by the device placement and routing: a wrong placement, or a poor routing can completely cancel the performance of the ESD device.

The layout shown in *Figure 9* may produce parasitic inductances responsible for artificial overvoltages directly applied on the IC to be protected.

Figure 9. Non-optimized location

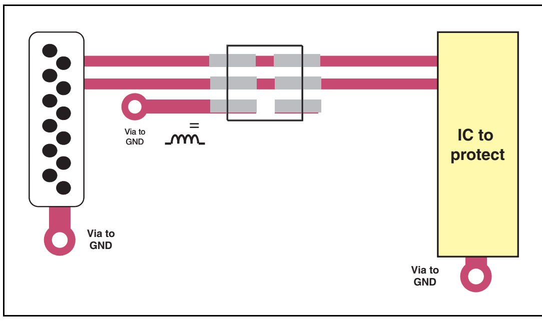
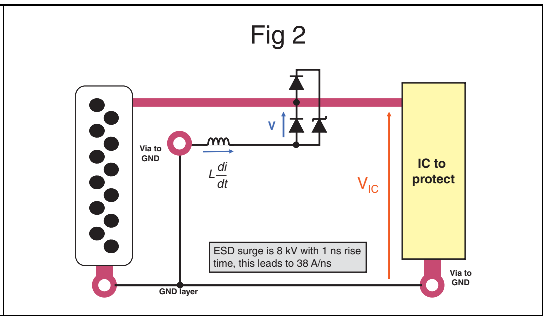


Figure 10. Significant overvoltages due to non-optimal location



A very simple calculation shows that for an 8 kV ESD surge according to IEC61000-4-2, the overvoltage due to parasitic inductances as shown in*Figure 10* may be really significant.With a peak current of 30 A reached in 0.8 ns and an parasitic PCB inductance of 5 nH (corresponds to metal track 5 mm long):

$$\frac{di}{dt} = 38\ \text{A/ns}$$

then the overvoltage seen by the IC is:

$$V_{IC} = V + L\cdot\frac{di}{dt}$$

$$V_{IC} = V + 190\ \text{V}$$

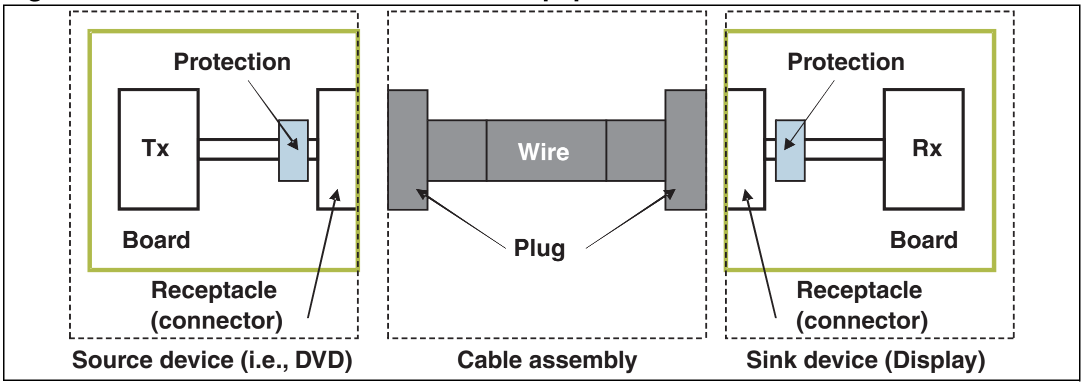
This parasitic inductance must be reduced as much as possible by shortening the ground path return to the GND via.

To avoid ESD propagation on the PCB, the ESD protection must be placed as close as possible to the ESD source with the layout given in the datasheet.

The layout given in the datasheet reduces parasitic inductance. It is important to connect the connector on one side of the HSP and the transceiver on the other side. The GND via on both sides must be used.

As ESD stress can be propagated on both sides of the cable, a protection device on each end of the cable is required.

Figure 11. Protection location on HDMI equipment



PCB layout must be optimized to take advantage of all performances of the HSP products.

For ESD protection efficiency, the HSP products must be located as close as possible to the connector (see *Figure 11*). This will avoid disturbance propagation to other components through the coupling effect.

To avoid the inductance effect of PCB tracks, it is required to go directly from the connector to the HSP and then after to go to the HDMI circuit. Vias to connect the ground pin of HSP to the ground plane must be as many as possible and placed as close as possible to the protection device to reduce parasitic inductance on the ground return path. Vias to connect ground plane and the connector can be located on both sides of the connector.

To be compliant with HDMI requirements, differential pairs must be designed with 100 Ω differential impedance from the connector to the IC. The length of each line in the same differential pair must be equal to minimize intra pair skew. Length of lines in different differential pair must also be as equal as far as possible to minimize inter pair skew. Track width must be calculated depending on PCB characteristics (relative permittivity, spacing, number of layers…).

Figure 12 shows an example of PCB layout with an HDMI type A SMD connector.

Figure 12. Layout for HDMI TMDS type A connector (4x HSP061-2P6)

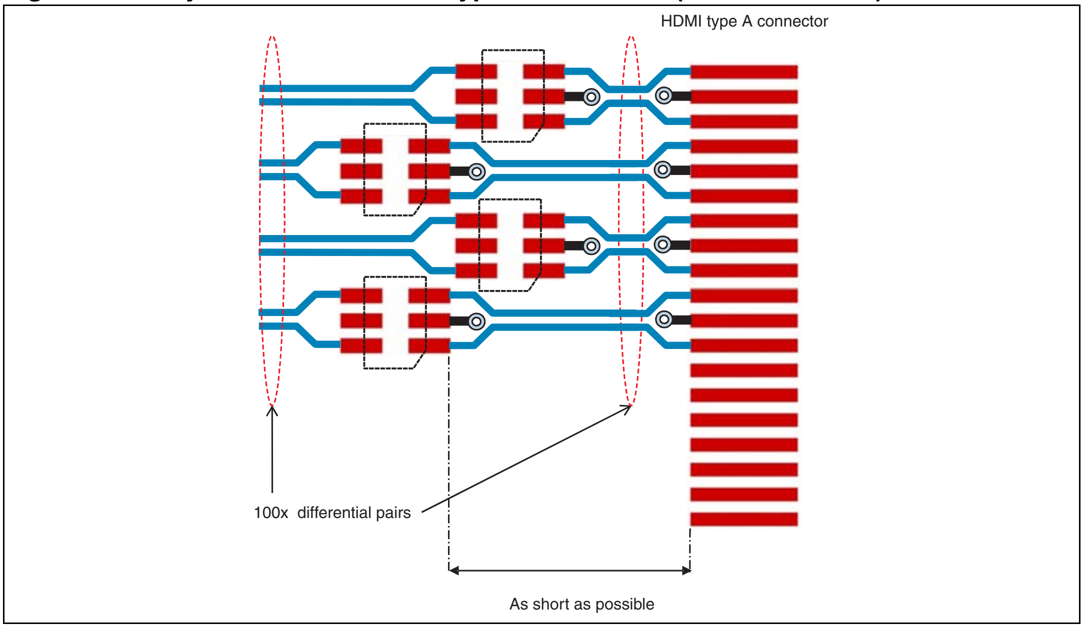


Figure 13. Layout for HDMI TMDS type C connector (4x HSP062-2M6)

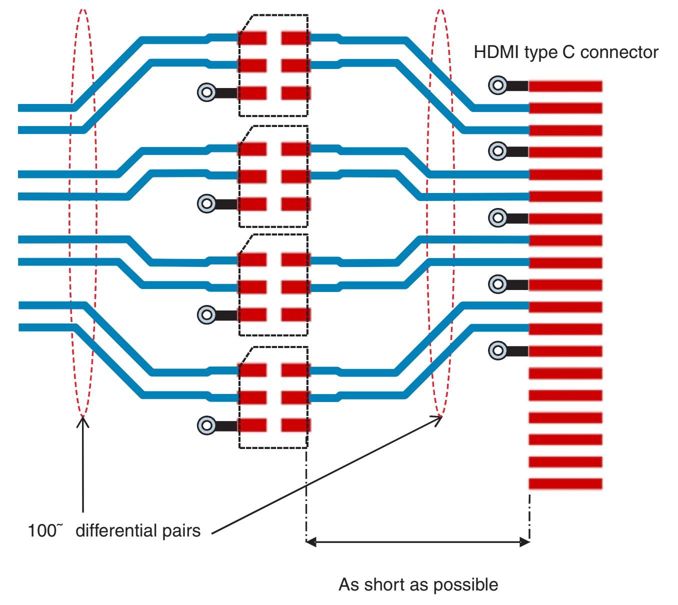


Figure 13 shows an example of PCB layout for an HDMI type C SMD connector

4 Conclusion

Two-lines HSP061-2 and HSP062-2 series complete the existing four- and eight-lines range to better fit customer requirements in terms of PCB design.Their characteristics make them compatible with most of the high speed lines of the market (such as HDMI 1.4, Ethernet, Display Port, USB3.0...).

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
11-Jan-2013	1	Initial release.