Precision Low Noise CMOS Rail-to-Rail Input/Output Operational Amplifiers

# AD8605/AD8606/AD8608*

## FEATURES

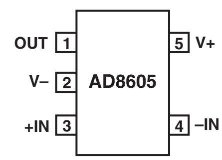
Low Offset Voltage: 65 μV Max
Low Input Bias Currents: 1 pA Max
Low Noise: 8 nV/√Hz
Wide Bandwidth: 10 MHz
High Open-Loop Gain: 120 dB
Unity Gain Stable
Single-Supply Operation: 2.7 V to 5.5 V
MicroCSP™

## APPLICATIONS

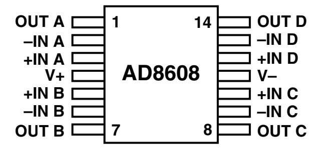
Photodiode Amplification
Battery-Powered Instrumentation
Multipole Filters
Sensors
Barcode Scanners
Audio

## FUNCTIONAL BLOCK DIAGRAMS

5-Lead SOT-23
(RT Suffix)

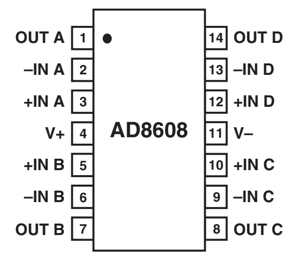



14-Lead TSSOP
(RU Suffix)

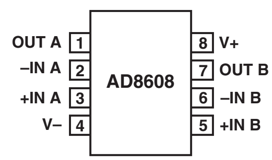



8-Lead MSOP
(RM Suffix)

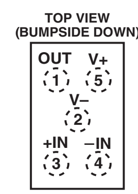

14-Lead SOIC
(R Suffix)




8-Lead SOIC
(R Suffix)




5-Bump MicroCSP
(CB Suffix)




AD8605 ONLY

## GENERAL DESCRIPTION

The AD8605, AD8606, and AD8608 are single, dual, and quad rail-to-rail input and output, single-supply amplifiers that feature very low offset voltage, low input voltage and current noise, and wide signal bandwidth. They use Analog Devices' patented DigiTrim® trimming technique, which achieves superior precision without laser trimming.

The combination of low offsets, low noise, very low input bias currents, and high speed makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. Applications for these amplifiers include optical control loops, portable and loop-powered instrumentation, and audio amplification for portable devices.

The AD8605, AD8606, and AD8608 are specified over the extended industrial (–40°C to +125°C) temperature range. The AD8605 single is available in the 5-lead SOT-23 and 5-bump MicroCSP packages. The 5-bump MicroCSP offers the smallest available footprint for any surface-mount operational amplifier. The AD8606 dual is available in an 8-lead MSOP package and a narrow SOIC surface-mount package. The AD8608 quad is available in a 14-lead TSSOP and a narrow 14-lead SOIC package. MicroCSP, SOT, MSOP, and TSSOP versions are available in tape and reel only.

*Protected by U.S.Patent No. 5,969,657; other patents pending.

REV. C



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# AD8605/AD8606/AD8608–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 5 V, $V_{CM}$ = $V_S$/2, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Offset Voltage | $V_{OS}$ | | | | | |
| AD8605/AD8606 | | $V_S$ = 3.5 V, $V_{CM}$ = 3 V | | 20 | 65 | µV |
| AD8608 | | $V_S$ = 3.5 V, $V_{CM}$ = 2.7 V | | 20 | 75 | µV |
| | | $V_S$ = 5 V, $V_{CM}$ = 0 V to 5 V | | 80 | 300 | µV |
| | | –40°C < $T_A$ < +125°C | | | 750 | µV |
| Input Bias Current | $I_B$ | | | 0.2 | 1 | pA |
| AD8605/AD8606 | | –40°C < $T_A$ < +85°C | | | 50 | pA |
| AD8605/AD8606 | | –40°C < $T_A$ < +125°C | | | 250 | pA |
| AD8608 | | –40°C < $T_A$ < +85°C | | | 100 | pA |
| AD8608 | | –40°C < $T_A$ < +125°C | | | 300 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.1 | 0.5 | pA |
| | | –40°C < $T_A$ < +85°C | | | 20 | pA |
| | | –40°C < $T_A$ < +125°C | | | 75 | pA |
| Input Voltage Range | | | 0 | | 5 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 5 V | 85 | 100 | | dB |
| | | –40°C < $T_A$ < +125°C | 75 | 90 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $V_O$ = 0.5 V to 4.5 V<br>$R_L$ = 2 kΩ, $V_{CM}$ = 0 V | 300 | 1,000 | | V/mV |
| Offset Voltage Drift | | | | | | |
| AD8605/AD8606 | $\Delta V_{OS}/\Delta T$ | | | 1 | 4.5 | µV/°C |
| AD8608 | $\Delta V_{OS}/\Delta T$ | | | 1.5 | 6.0 | µV/°C |
| **INPUT CAPACITANCE** | | | | | | |
| Common-Mode Input Capacitance | | | | 8.8 | | pF |
| Differential Input Capacitance | | | | 2.59 | | pF |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 1 mA | 4.96 | 4.98 | | V |
| | | $I_L$ = 10 mA | 4.7 | 4.79 | | V |
| | | –40°C < $T_A$ < +125°C | 4.6 | | | V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 1 mA | | 20 | 40 | mV |
| | | $I_L$ = 10 mA | | 170 | 210 | mV |
| | | –40°C < $T_A$ < +125°C | | | 290 | mV |
| Output Current | $I_{OUT}$ | | | ±80 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | 10 | | Ω |
| **POWER SUPPLY** | | | | | | |
| Power Supply Rejection Ratio | PSRR | | | | | |
| AD8605/AD8606 | | $V_S$ = 2.7 V to 5.5 V | 80 | 95 | | dB |
| AD8608 | | $V_S$ = 2.7 V to 5.5 V | 77 | 92 | | dB |
| | | –40°C < $T_A$ < +125°C | 70 | 90 | | dB |
| Supply Current/Amplifier | $I_{SY}$ | $V_O$ = 0 V | | 1 | 1.2 | mA |
| | | –40°C < $T_A$ < +125°C | | | 1.4 | mA |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 5 | | V/µs |
| Settling Time | $t_S$ | To 0.01%, 0 V to 2 V step | | < 1 | | µs |
| Full Power Bandwidth | $BW_P$ | < 1% Distortion | | 360 | | kHz |
| Gain Bandwidth Product | GBP | | | 10 | | MHz |
| Phase Margin | $\phi_O$ | | | 65 | | Degrees |
| **NOISE PERFORMANCE** | | | | | | |
| Peak-to-Peak Noise | $e_n$ p-p | f = 0.1 Hz to 10 Hz | | 2.3 | 3.5 | µV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 8 | 12 | nV/$\sqrt{Hz}$ |
| Voltage Noise Density | $e_n$ | f = 10 kHz | | 6.5 | | nV/$\sqrt{Hz}$ |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.01 | | pA/$\sqrt{Hz}$ |

## ELECTRICAL CHARACTERISTICS (@ $V_S$ = 2.7 V, $V_{CM}$ = $V_S$/2, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | | | | | |
| AD8605/AD8606 | | $V_S$ = 3.5 V, $V_{CM}$ = 3 V | | 20 | 65 | µV |
| AD8608 | | $V_S$ = 3.5 V, $V_{CM}$ = 2.7 V | | 20 | 75 | µV |
| | | $V_S$ = 2.7 V, $V_{CM}$ = 0 V to 2.7 V | | 80 | 300 | µV |
| | | –40°C < $T_A$ < +125°C | | | 750 | µV |
| Input Bias Current | $I_B$ | | | 0.2 | 1 | pA |
| AD8605/AD8606 | | –40°C < $T_A$ < +85°C | | | 50 | pA |
| AD8605/AD8606 | | –40°C < $T_A$ < +125°C | | | 250 | pA |
| AD8608 | | –40°C < $T_A$ < +85°C | | | 100 | pA |
| AD8608 | | –40°C < $T_A$ < +125°C | | | 300 | pA |
| Input Offset Current | $I_{OS}$ | | | 0.1 | 0.5 | pA |
| | | –40°C < $T_A$ < +85°C | | | 20 | pA |
| | | –40°C < $T_A$ < +125°C | | | 75 | pA |
| Input Voltage Range | | | 0 | | 2.7 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = 0 V to 2.7 V | 80 | 95 | | dB |
| | | –40°C < $T_A$ < +125°C | 70 | 85 | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ, $V_O$ = 0.5 V to 2.2 V | 110 | 350 | | V/mV |
| Offset Voltage Drift | | | | | | |
| AD8605/AD8606 | $\Delta V_{OS}/\Delta T$ | | | 1 | 4.5 | µV/°C |
| AD8608 | $\Delta V_{OS}/\Delta T$ | | | 1.5 | 6.0 | µV/°C |
| INPUT CAPACITANCE | | | | | | |
| Common-Mode Input Capacitance | | | | 8.8 | | pF |
| Differential Input Capacitance | | | | 2.59 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | $V_{OH}$ | $I_L$ = 1 mA | 2.6 | 2.66 | | V |
| | | –40°C < $T_A$ < +125°C | 2.6 | | | V |
| Output Voltage Low | $V_{OL}$ | $I_L$ = 1 mA | | 25 | 40 | mV |
| | | –40°C < $T_A$ < +125°C | | | 50 | mV |
| Output Current | $I_{OUT}$ | | | ±30 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = 1 | | 12 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | | | | | |
| AD8605/AD8606 | | $V_S$ = 2.7 V to 5.5 V | 80 | 95 | | dB |
| AD8608 | | $V_S$ = 2.7 V to 5.5 V | 77 | 92 | | dB |
| | | –40°C < $T_A$ < +125°C | 70 | 90 | | dB |
| Supply Current/Amplifier | $I_{SY}$ | $V_O$ = 0 V | | 1.15 | 1.4 | mA |
| | | –40°C < $T_A$ < +125°C | | | 1.5 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | | 5 | | V/µs |
| Settling Time | $t_S$ | To 0.01%, 0 V to 1 V step | | < 0.5 | | µs |
| Gain Bandwidth Product | GBP | | | 9 | | MHz |
| Phase Margin | $\phi_O$ | | | 50 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Peak-to-Peak Noise | $e_n$ p-p | f = 0.1 Hz to 10 Hz | | 2.3 | 3.5 | µV p-p |
| Voltage Noise Density | $e_n$ | f = 1 kHz | | 8 | 12 | nV/√Hz |
| Voltage Noise Density | $e_n$ | f = 10 kHz | | 6.5 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.01 | | pA/√Hz |

**ABSOLUTE MAXIMUM RATINGS***

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6 V
Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . GND to $V_S$
Differential Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . 6 V
Output Short-Circuit Duration
  to GND . . . . . . . . . . . . . . . . . . . . . Observe Derating Curves
Storage Temperature Range
  All Packages . . . . . . . . . . . . . . . . . . . . . . . –65°C to +150°C
Operating Temperature Range
  AD8605/AD8606/AD8608 . . . . . . . . . . . . –40°C to +125°C
Junction Temperature Range
  All Packages . . . . . . . . . . . . . . . . . . . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Package Type | $\theta_{JA}$* | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 5-Bump MicroCSP (CB) | 220 | 220 | °C/W |
| 5-Lead SOT-23 (RT) | 230 | 92 | °C/W |
| 8-Lead MSOP (RM) | 210 | 45 | °C/W |
| 8-Lead SOIC (R) | 158 | 43 | °C/W |
| 14-Lead SOIC (R) | 120 | 36 | °C/W |
| 14-Lead TSSOP (RU) | 180 | 35 | °C/W |

*$\theta_{JA}$ is specified for worst-case conditions, i.e., $\theta_{JA}$ is specified for device in socket for PDIP packages; $\theta_{JA}$ is specified for device soldered onto a circuit board for surface-mount packages.

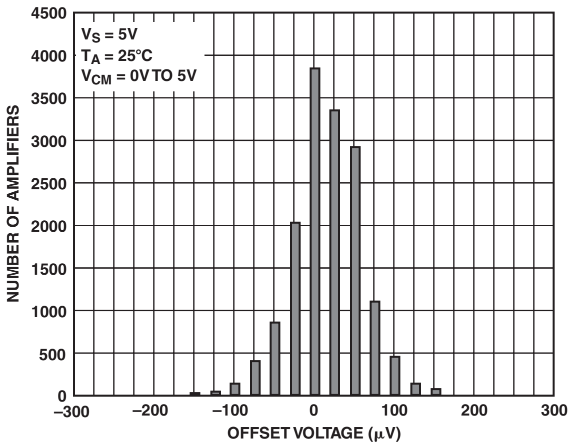
**ORDERING GUIDE**

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| AD8605ACB-R2* | –40°C to +125°C | 5-Bump MicroCSP | CB-5 | B3A |
| AD8605ACB-REEL* | –40°C to +125°C | 5-Bump MicroCSP | CB-5 | B3A |
| AD8605ACB-REEL7* | –40°C to +125°C | 5-Bump MicroCSP | CB-5 | B3A |
| AD8605ART-R2 | –40°C to +125°C | 5-Lead SOT-23 | RT-5 | B3A |
| AD8605ART-REEL | –40°C to +125°C | 5-Lead SOT-23 | RT-5 | B3A |
| AD8605ART-REEL7 | –40°C to +125°C | 5-Lead SOT-23 | RT-5 | B3A |
| AD8606ARM-R2 | –40°C to +125°C | 8-Lead MSOP | RM-8 | B6A |
| AD8606ARM-REEL | –40°C to +125°C | 8-Lead MSOP | RM-8 | B6A |
| AD8606AR | –40°C to +125°C | 8-Lead SOIC | R-8 | |
| AD8606AR-REEL | –40°C to +125°C | 8-Lead SOIC | R-8 | |
| AD8606AR-REEL7 | –40°C to +125°C | 8-Lead SOIC | R-8 | |
| AD8608AR | –40°C to +125°C | 14-Lead SOIC | R-14 | |
| AD8608AR-REEL | –40°C to +125°C | 14-Lead SOIC | R-14 | |
| AD8608AR-REEL7 | –40°C to +125°C | 14-Lead SOIC | R-14 | |
| AD8608ARU | –40°C to +125°C | 14-Lead TSSOP | RU-14 | |
| AD8608ARU-REEL | –40°C to +125°C | 14-Lead TSSOP | RU-14 | |

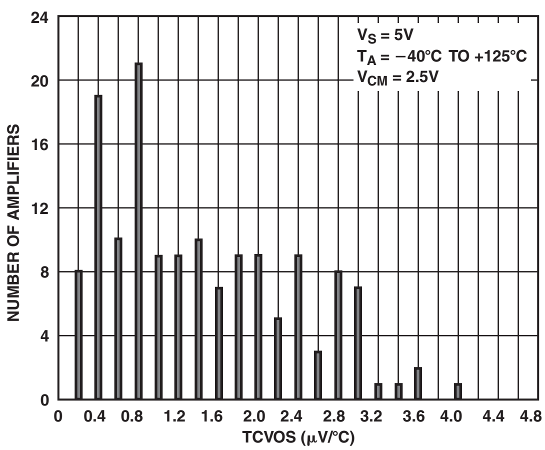
*Consult factory for availability.

**CAUTION**

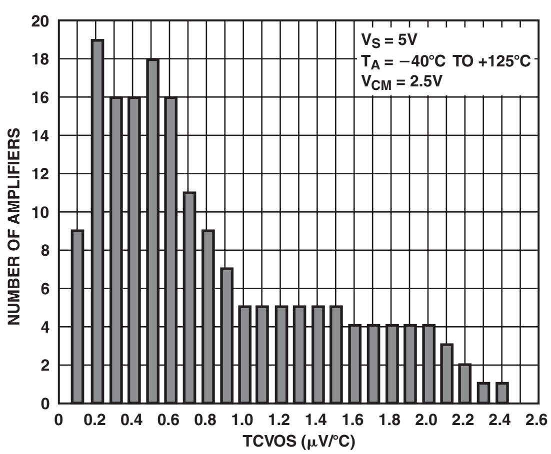
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8605/AD8606/AD8608 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



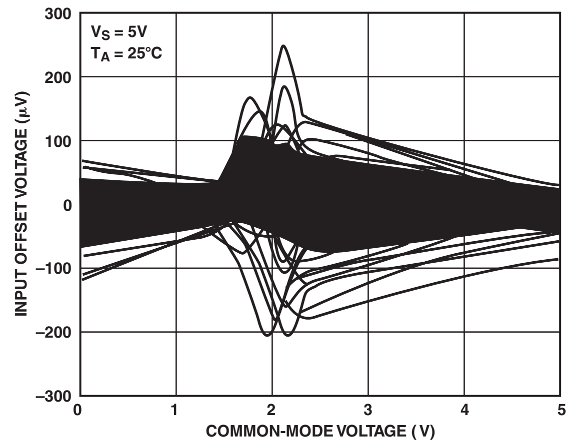

*TPC 1. Input Offset Voltage Distribution*



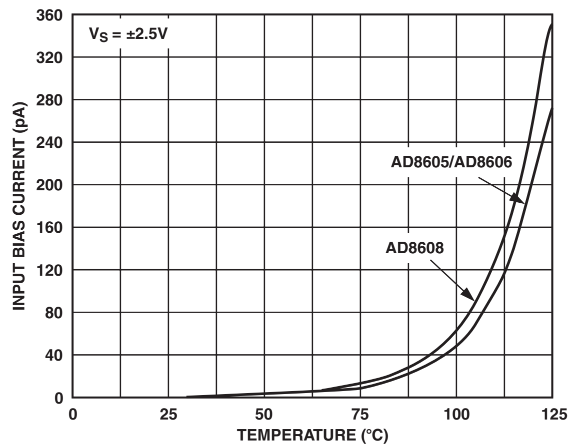

*TPC 2. AD8608 Input Offset Voltage Drift Distribution*



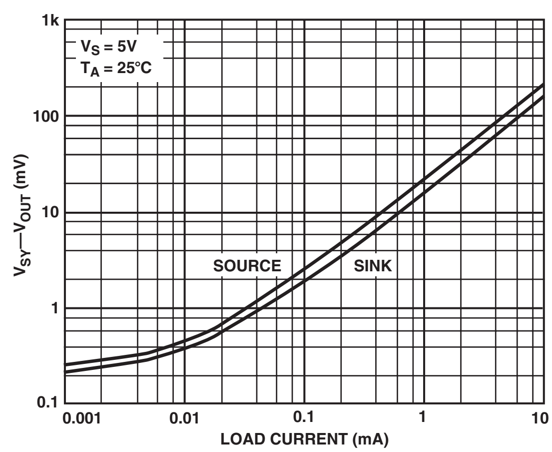

*TPC 3. AD8605/AD8606 Input Offset Voltage Drift Distribution*



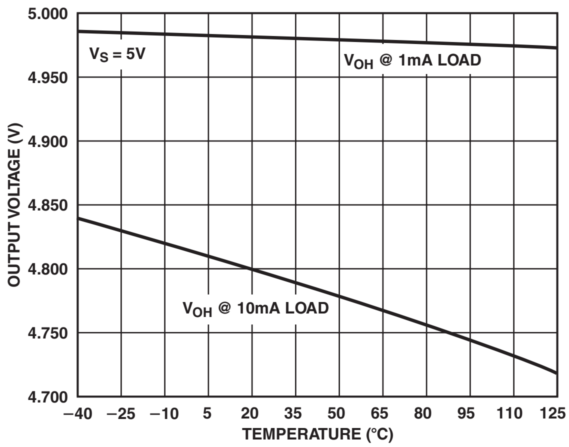

*TPC 4. Input Offset Voltage vs. Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)*



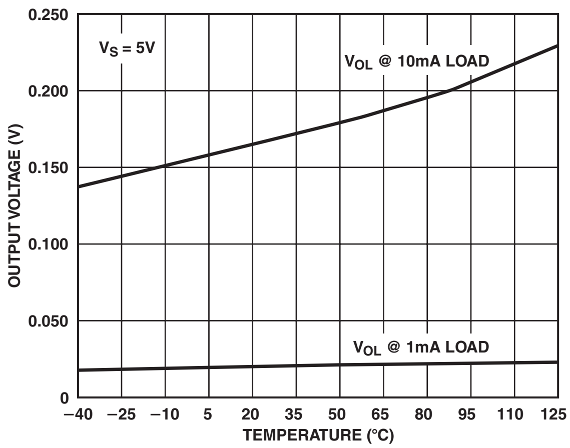

*TPC 5. Input Bias Current vs. Temperature*



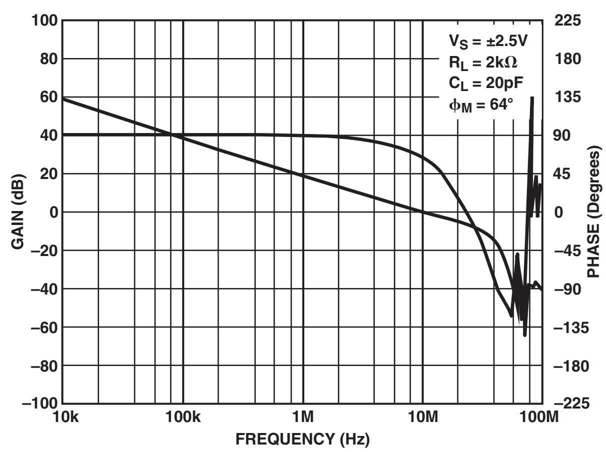

*TPC 6. Output Voltage to Supply Rail vs. Load Current*



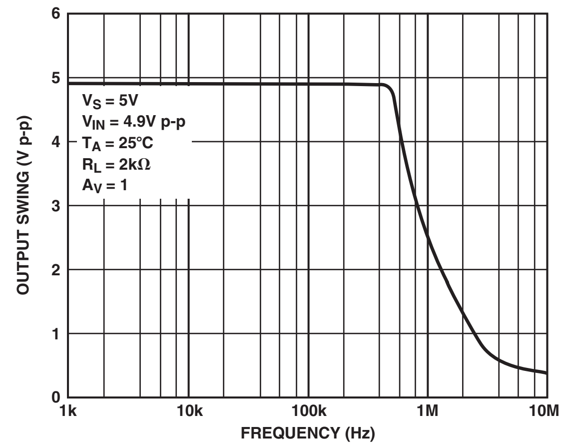

TPC 7. Output Voltage Swing vs. Temperature



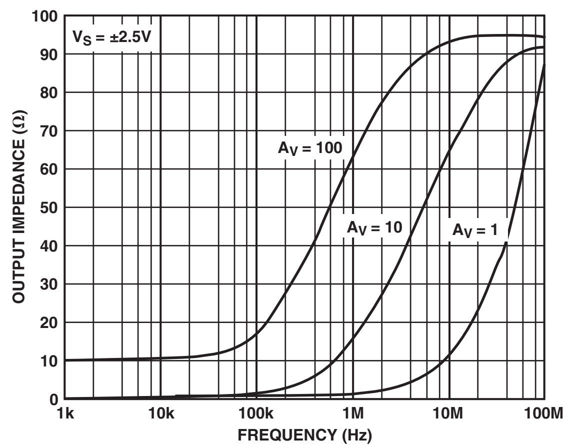

TPC 8. Output Voltage Swing vs. Temperature



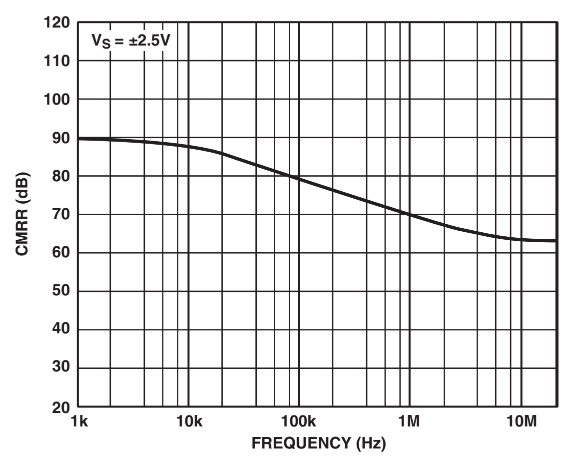

TPC 9. Open-Loop Gain and Phase vs. Frequency



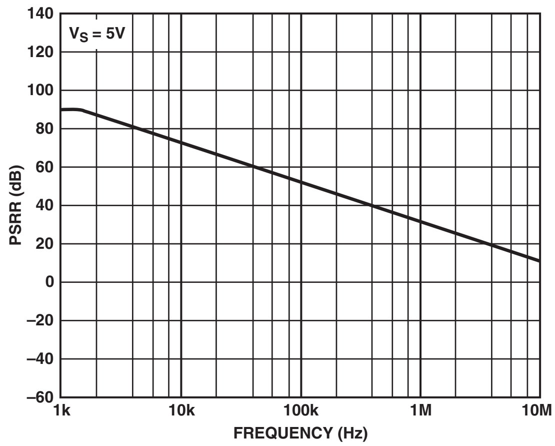

TPC 10. Closed-Loop Output Voltage Swing



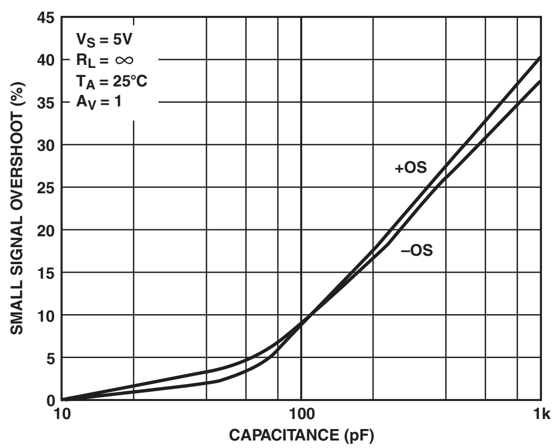

TPC 11. Output Impedance vs. Frequency



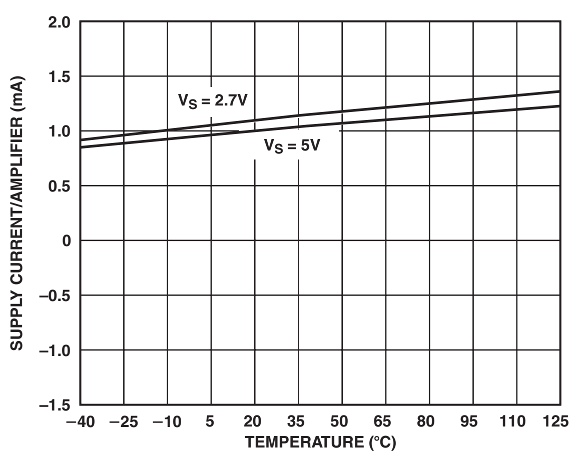

TPC 12. Common-Mode Rejection Ratio vs. Frequency



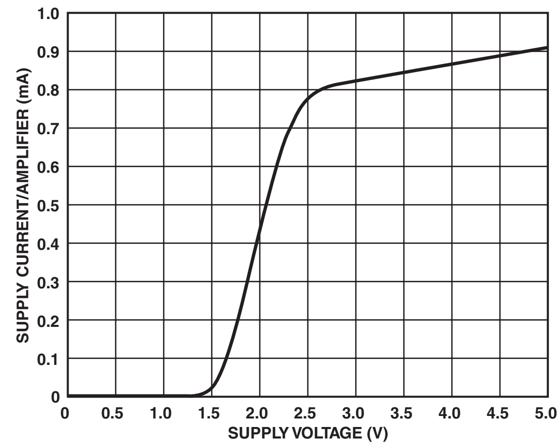

TPC 13. PSRR vs. Frequency



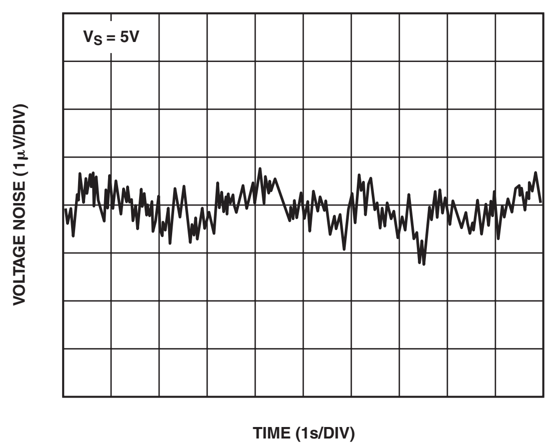

TPC 14. Small Signal Overshoot vs. Load Capacitance



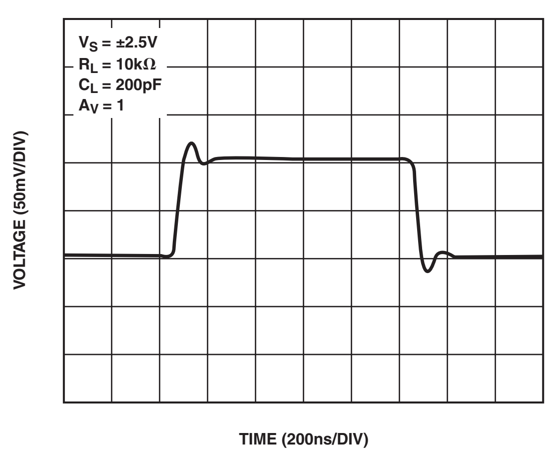

TPC 15. Supply Current vs. Temperature



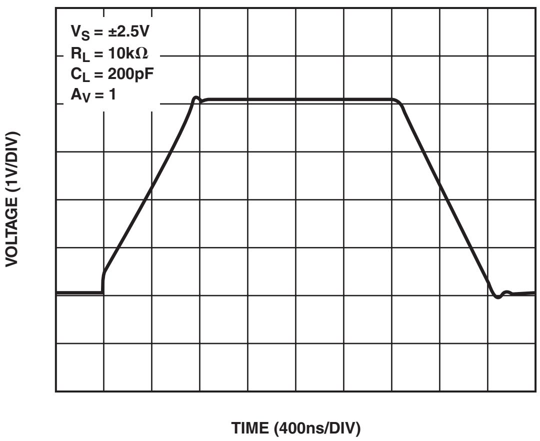

TPC 16. Supply Current vs. Supply Voltage



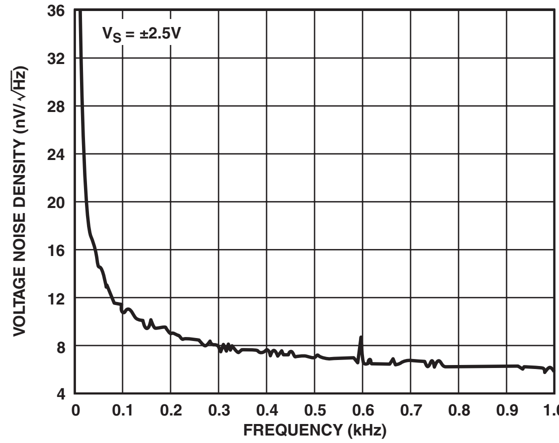

TPC 17. 0.1 Hz to 10 Hz Input Voltage Noise



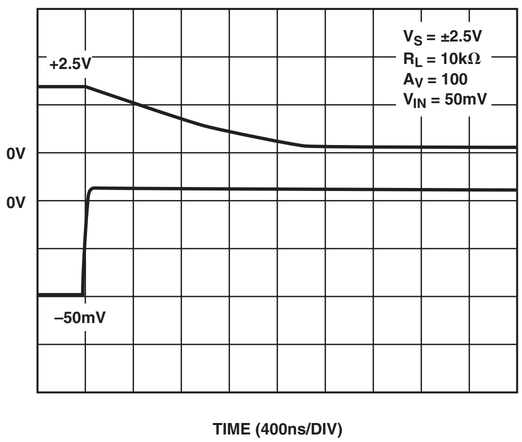

TPC 18. Small Signal Transient Response



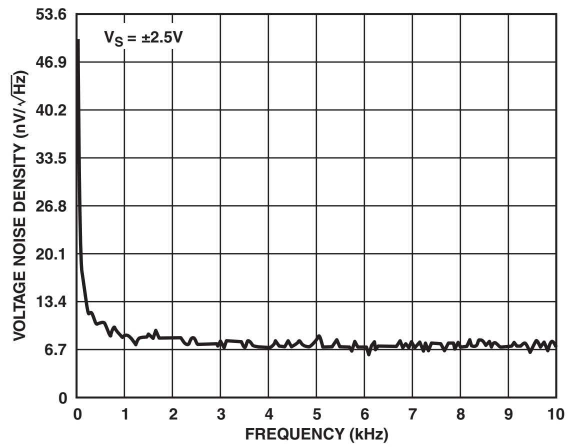

*TPC 19. Large Signal Transient Response*



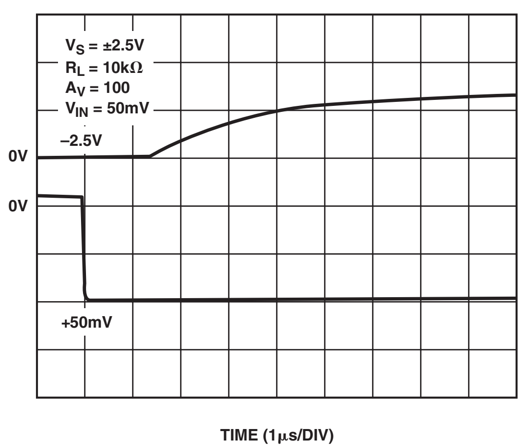

*TPC 22. Voltage Noise Density*



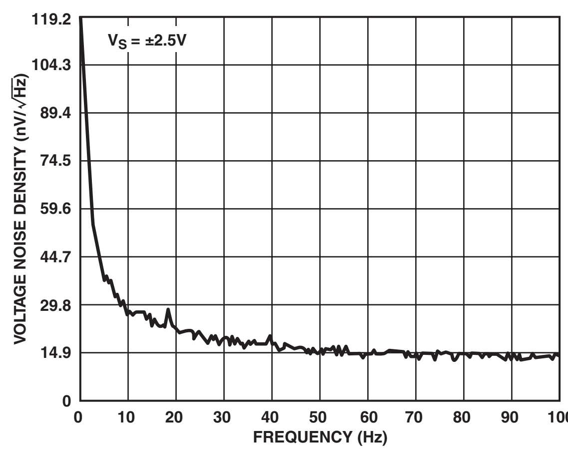

*TPC 20. Negative Overload Recovery*



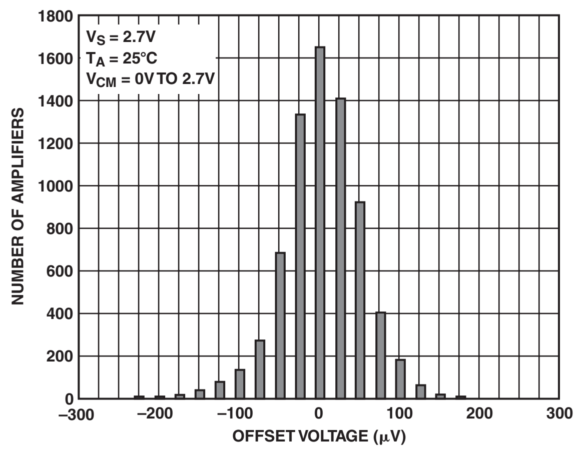

*TPC 23. Voltage Noise Density*



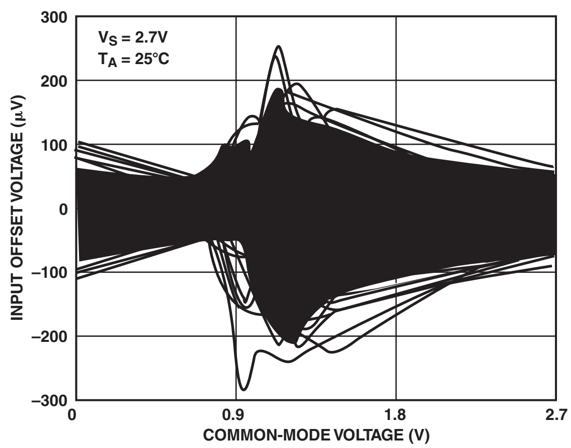

*TPC 21. Positive Overload Recovery*



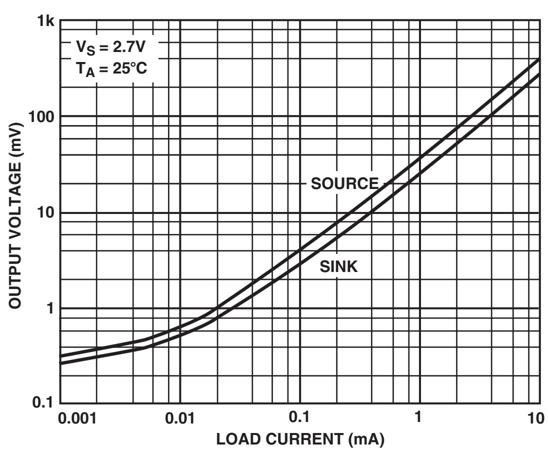

*TPC 24. Voltage Noise Density*



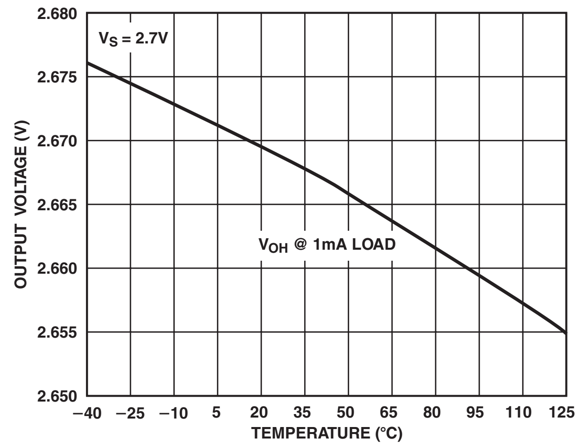

*TPC 25. Input Offset Voltage Distribution*



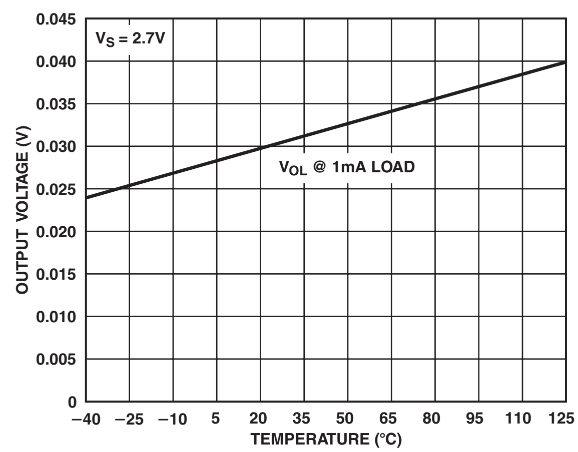

*TPC 26. Input Offset Voltage vs. Common-Mode Voltage (200 Units, 5 Wafer Lots, Including Process Skews)*



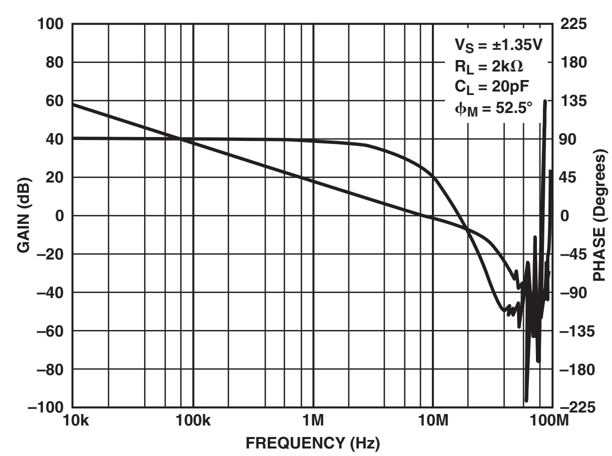

*TPC 27. Output Voltage to Supply Rail vs. Load Current*



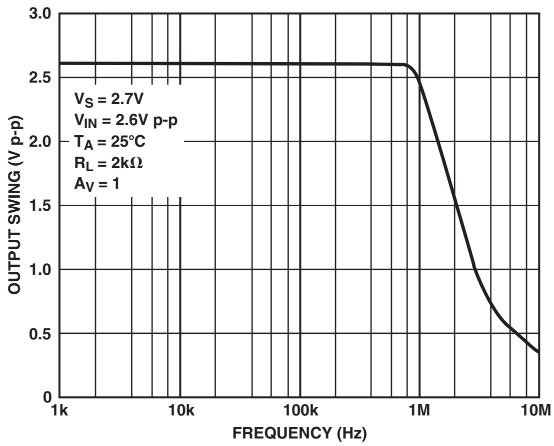

*TPC 28. Output Voltage Swing vs. Temperature*



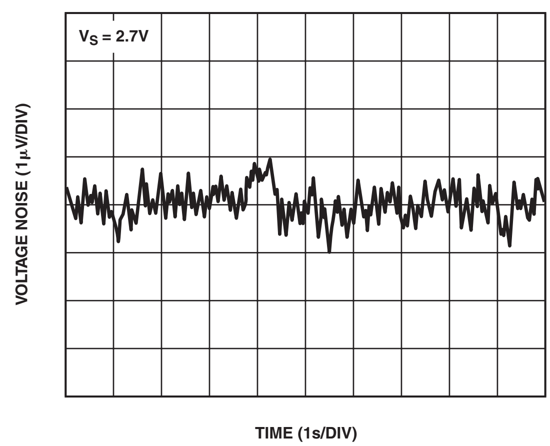

*TPC 29. Output Voltage Swing vs. Temperature*



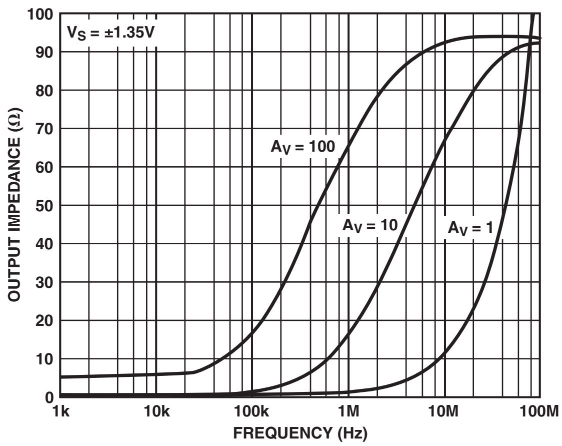

*TPC 30. Open-Loop Gain and Phase vs. Frequency*



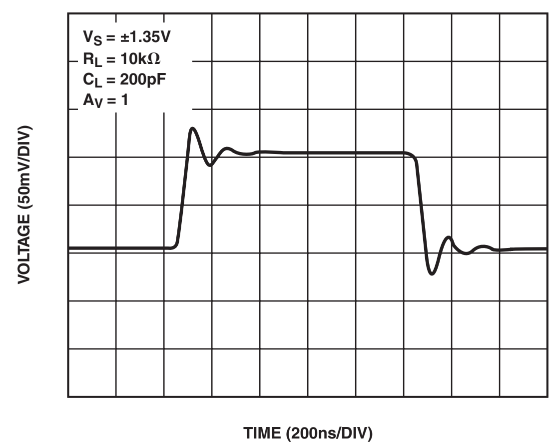

TPC 31. Closed-Loop Output Voltage Swing vs. Frequency



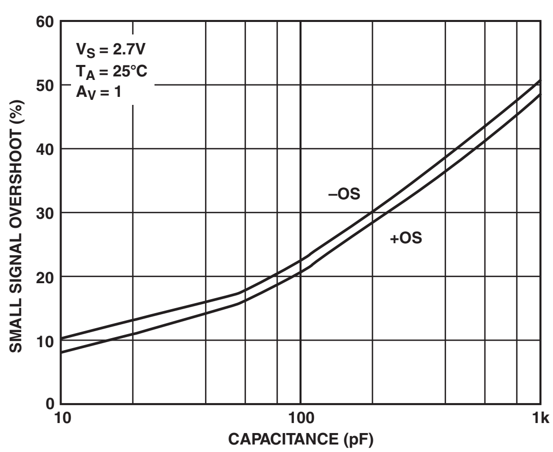

TPC 34. 0.1 Hz to 10 Hz Input Voltage Noise



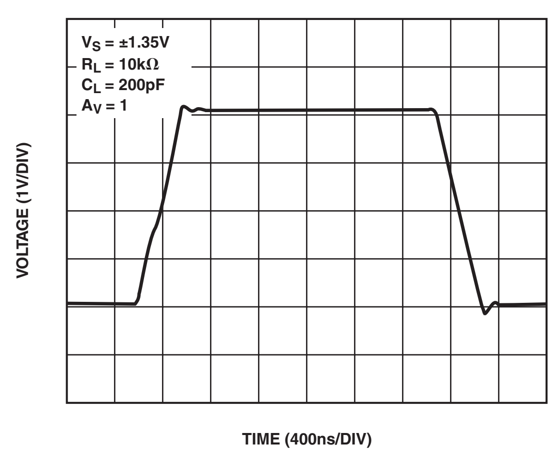

TPC 32. Output Impedance vs. Frequency




TPC 35. Small Signal Transient Response




TPC 33. Small Signal Overshoot vs. Load Capacitance




TPC 36. Large Signal Transient Response

**Output Phase Reversal**

Phase reversal is defined as a change in polarity at the output of the amplifier when a voltage that exceeds the maximum input common-mode voltage drives the input.

Phase reversal can cause permanent damage to the amplifier; it may also cause system lockups in feedback loops. The AD8605 does not exhibit phase reversal even for inputs exceeding the supply voltage by more than 2 V.

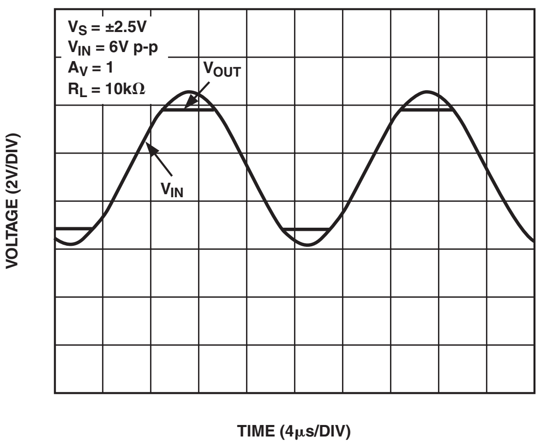



*Figure 1. No Phase Reversal*

**Maximum Power Dissipation**

Power dissipated in an IC will cause the die temperature to increase. This can affect the behavior of the IC and the application circuit performance.

The absolute maximum junction temperature of the AD8605/AD8606/AD8608 is 150°C. Exceeding this temperature could cause damage or destruction of the device.

The maximum power dissipation of the amplifier is calculated according to the following formula:

$$P_{DISS} = \frac{(T_J - T_A)}{\theta_{JA}}$$

where:
$T_J$ = junction temperature
$T_A$ = ambient temperature
$\theta_{JA}$ = junction-to-ambient thermal resistance

Figure 2 compares the maximum power dissipation with temperature for the various packages available for the AD8605 family.

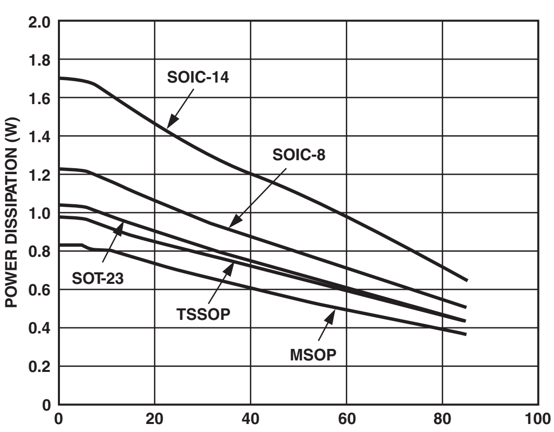



*Figure 2. Maximum Power Dissipation vs. Temperature*

**Input Overvoltage Protection**

The AD8605 has internal protective circuitry. However, if the voltage applied at either input exceeds the supplies by more than 2.5 V, external resistors should be placed in series with the inputs. The resistor values can be determined according to the formula

$$\frac{(V_{IN} - V_S)}{(R_S + 200\Omega)} \le 5\,mA$$

The remarkable low input offset current of the AD8605 (<1 pA) allows the use of larger value resistors. With a 10 kΩ resistor at the input, the output voltage will have less than 10 nV of error voltage. A 10 kΩ resistor has less than 13 nV/$\sqrt{Hz}$ of thermal noise at room temperature.

**THD + Noise**

Total harmonic distortion is the ratio of the input signal in V rms to the total harmonics in V rms throughout the spectrum. Harmonic distortion adds errors to precision measurements and adds unpleasant sonic artifacts to audio systems.

The AD8605 has a low total harmonic distortion. Figure 3 shows that the AD8605 has less than 0.005% or –86 dB of THD + N over the entire audio frequency range. The AD8605 is configured in positive unity gain, which is the worst case, and with a load of 10 kΩ.

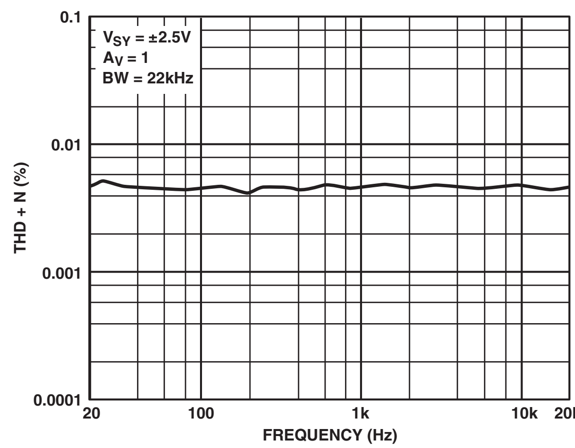



*Figure 3. THD + N*

**Total Noise Including Source Resistors**

The low input current noise and input bias current of the AD8605 make it the ideal amplifier for circuits with substantial input source resistance such as photodiodes. Input offset voltage increases by less than 0.5 nV per 1 kΩ of source resistance at room temperature and increases to 10 nV at 85°C.

The total noise density of the circuit is

$$e_{n,TOTAL} = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S}$$

where:
$e_n$ is the input voltage noise density of the AD8605
$i_n$ is the input current noise density of the AD8605
$R_S$ is the source resistance at the noninverting terminal
$k$ is Boltzmann's constant (1.38 × $10^{-23}$ J/K)
$T$ is the ambient temperature in Kelvin (T = 273 + °C)

For example, with $R_S$ = 10 kΩ, the total voltage noise density is roughly 15 nV/$\sqrt{Hz}$.

For $R_S$ < 3.9 kΩ, $e_n$ dominates and $e_{n,TOTAL} \approx e_n$.

The current noise of the AD8605 is so low that its total density does not become a significant term unless $R_S$ is greater than 6 MΩ.

The total equivalent rms noise over a specific bandwidth is expressed as

$$E_n = \left(e_{n,TOTAL}\right)\sqrt{BW}$$

where *BW* is the bandwidth in hertz.

Note that the analysis above is valid for frequencies greater than 100 Hz and assumes relatively flat noise, above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

**Channel Separation**

Channel separation, or inverse crosstalk, is a measure of the signal feed from one amplifier (channel) to the other on the same IC.

The AD8606 has a channel separation of greater than –160 dB up to frequencies of 1 MHz, allowing the two amplifiers to amplify ac signals independently in most applications.

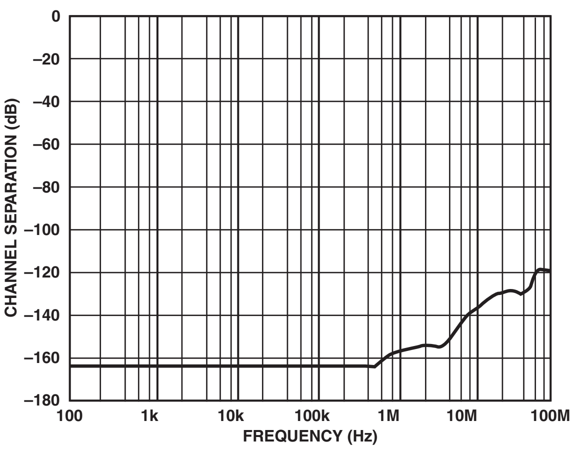



*Figure 4. Channel Separation vs. Frequency*

**Capacitive Load Drive**

The AD8605 is capable of driving large capacitive loads without oscillation.

Figure 5 shows the output of the AD8606 in response to a 200 mV input signal. In this case, the amplifier was configured in positive unity gain, worst case for stability, while driving a 1,000 pF load at its output. Driving larger capacitive loads in unity gain may require the use of additional circuitry.

A snubber network, shown in Figure 7, helps reduce the signal overshoot to a minimum and maintain stability. Although this circuit does not recover the loss of bandwidth induced by large capacitive loads, it greatly reduces the overshoot and ringing. This method does not reduce the maximum output swing of the amplifier.

Figure 6 shows a scope photograph of the output at the snubber circuit. The overshoot is reduced from over 70% to less than 5%, and the ringing is eliminated by the snubber. Optimum values for $R_S$ and $C_S$ are determined experimentally. Table I summarizes a few starting values.

An alternate technique is to insert a series resistor inside the feedback loop at the output of the amplifier. Typically, the value of this resistor is approximately 100 Ω. This method also reduces overshoot and ringing but causes a reduction in the maximum output swing.

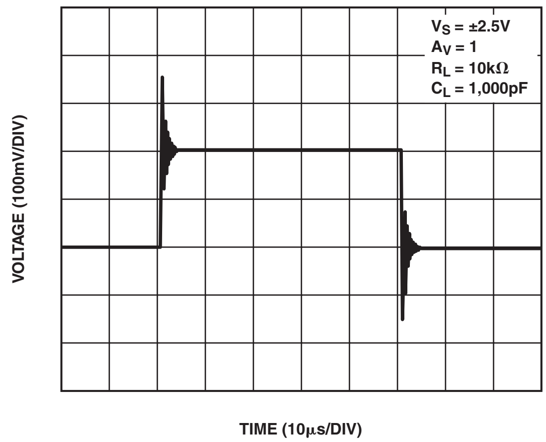



*Figure 5. Capacitive Load Drive without Snubber*

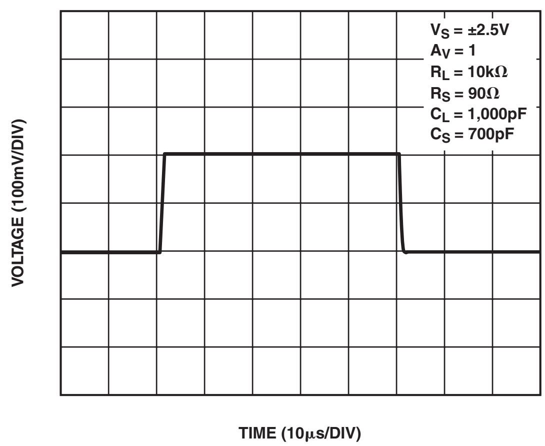



*Figure 6. Capacitive Load Drive with Snubber*

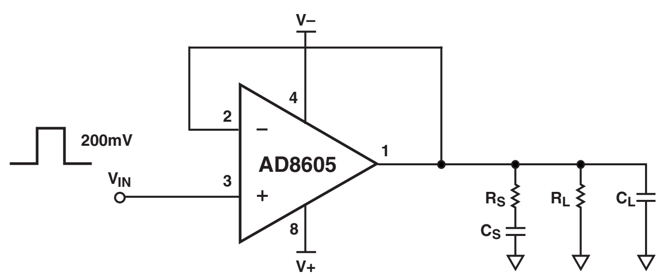



*Figure 7. Snubber Network Configuration*

**Table I. Optimum Values for Capacitive Loads**

| $C_L$ (pF) | $R_S$ (Ω) | $C_S$ (pF) |
|---|---|---|
| 500 | 100 | 1,000 |
| 1,000 | 70 | 1,000 |
| 2,000 | 60 | 800 |

**LIGHT SENSITIVITY**

The AD8605ACB (MicroCSP package option) is essentially a silicon die with additional post fabrication dielectric and inter-metallic processing designed to contact solder bumps on the active side of the chip. With this package type, the die is exposed to ambient light and is subject to photoelectric effects. Light sensitivity analysis of the AD8605ACB mounted on standard PCB material reveals that only the input bias current ($I_B$) parameter is impacted when the package is illuminated directly by high intensity light. No degradation in electrical performance is observed due to illumination by low intensity (0.1 mW/cm$^2$) ambient light. Figure 8 shows that $I_B$ increases with increasing wavelength and intensity of incident light; $I_B$ can reach levels as high as 4500 pA at a light intensity of 3 mW/cm$^2$ and a wavelength of 850 nm. The light intensities shown in Figure 8 will not be normal for most applications, i.e., even though direct sunlight can have intensities of 50 mW/cm$^2$, office ambient light can be as low as 0.1 mW/cm$^2$.

When the MicroCSP package is assembled on the board with the bump-side of the die facing the PCB, reflected light from the PCB surface is incident on active silicon circuit areas and results in the increased $I_B$. No performance degradation will occur due to illumination of the backside (substrate) of the AD8605ACB. The AD8605ACB is particularly sensitive to incident light with wavelengths in the Near Infrared range (NIR, 700 nm to 1000 nm). Photons in this waveband have a longer wavelength and lower energy than photons in the visible (400 nm to 700 nm) and Near Ultraviolet (NUV, 200 nm to 400 nm) bands; therefore, they can penetrate more deeply into the active silicon. Incident light with wavelengths greater than 1100 nm has no photoelectric effect on the AD8605ACB since silicon is transparent to wavelengths in this range. The spectral content of conventional light sorces varies: sunlight has a broad spectral range, with peak intensity in the visible band that falls off in the NUV and NIR bands; flourescent lamps have significant peaks in the visible but not in the NUV or NIR bands.

Efforts have been made at a product level to reduce the effect of ambient light; the under bump metal (UBM) has been designed to shield the sensitive circuit areas on the active side (bump-side) of the die. However, if an application encounters any light sensitivity with the AD8605ACB, shielding the bump side of the MicroCSP package with opaque material should eliminate this effect. Shielding can be accomplished using materials such as silica filled liquid epoxies that are used in flip chip underfill techniques.

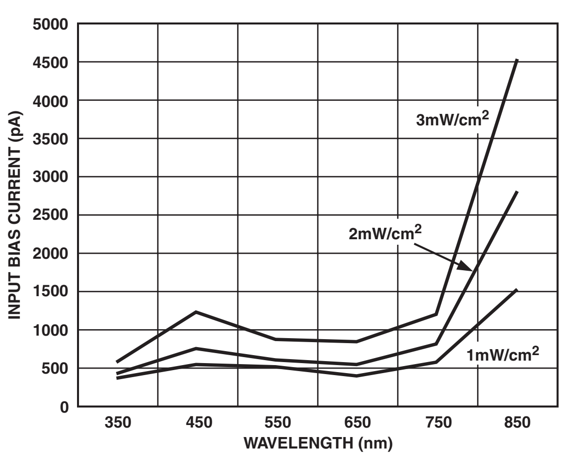



*Figure 8. AD8605ACB Input Bias Current Response to Direct Illumination of Varying Intensity and Wavelength*

**MicroCSP Assembly Considerations**

For detailed information on MicroCSP PCB assembly and reliability, refer to ADI Application Note AN-617 on the ADI website www.analog.com.

## I-V CONVERSION APPLICATIONS

**Photodiode Preamplifier Applications**

The low offset voltage and input current of the AD8605 make it an excellent choice for photodiode applications. In addition, the low voltage and current noise make the amplifier ideal for application circuits with high sensitivity.

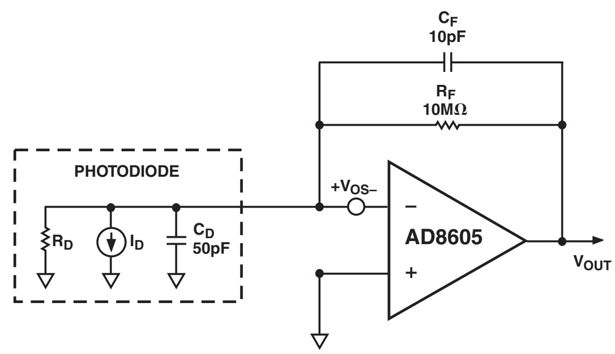



*Figure 9. Equivalent Circuit for Photodiode Preamp*

The input bias current of the amplifier contributes an error term that is proportional to the value of $R_F$.

The offset voltage causes a dark current induced by the shunt resistance of the diode, $R_D$. These error terms are combined at the output of the amplifier and the error voltage is written:

$$E_O = V_{OS}\left(1+\frac{R_F}{R_D}\right)+R_F I_B$$

Typically, $R_F$ is much smaller than $R_D$, thus $R_F/R_D$ can be ignored.

At room temperature, the AD8605 has an input bias current of 0.2 pA and an offset voltage of 100 µV. Typical values of $R_D$ are in the range of 1 GΩ.

For the circuit shown in Figure 9, the output error voltage is approximately 100 µV at room temperature, increasing to about 1 mV at 85°C.

The maximum achievable signal bandwidth is

$$f_{MAX} = \sqrt{\frac{f_t}{2\pi R_F C_T}}$$

where $f_t$ is the unity gain frequency of the amplifier.

**Audio and PDA Applications**

The AD8605's low distortion and wide dynamic range make it a great choice for audio and PDA applications, including microphone amplification and line output buffering.

Figure 10 shows a typical application circuit for headphone/line out amplification.

R1 and R2 are used to bias the input voltage at half the supply. This maximizes the signal bandwidth range. C1 and C2 are used to ac couple the input signal. C1 and R2 form a high-pass filter whose corner frequency is 1/2πR1C1.

The high output current of the AD8605 allows it to drive heavy resistive loads.

The circuit of Figure 10 was tested to drive a 16 W headphone. The THD + N is maintained at approximately –60 dB throughout the audio range.

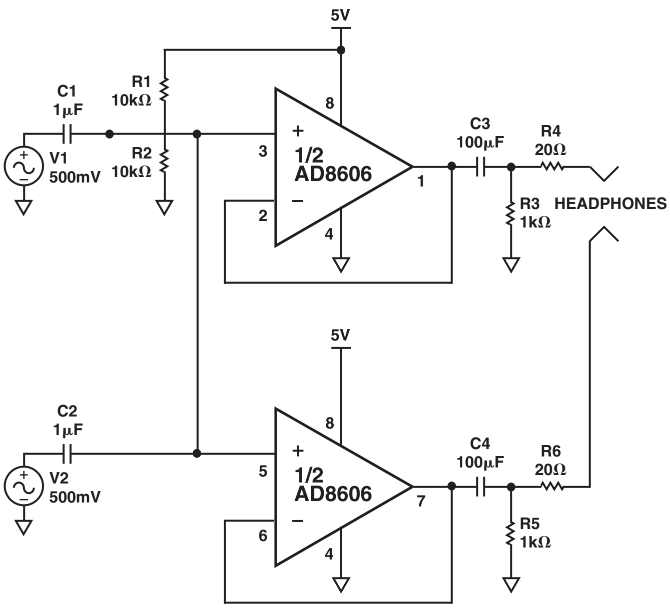



*Figure 10. Single-Supply Headphone/Speaker Amplifier*

**Instrumentation Amplifiers**

The low offset voltage and low noise of the AD8605 make it a great amplifier for instrumentation applications.

Difference amplifiers are widely used in high accuracy circuits to improve the common-mode rejection ratio.

Figure 10 shows a simple difference amplifier. The CMRR of the circuit is plotted versus frequency. Figure 11 shows the common-mode rejection for a unity gain configuration and for a gain of 10.

Making (R4/R3) = (R2/R1) and choosing 0.01% tolerance yields a CMRR of 74 dB and minimizes the gain error at the output.

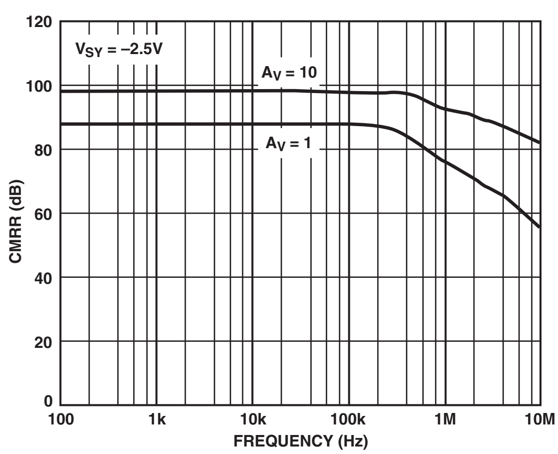



*Figure 11. Difference Amplifier CMRR vs. Frequency*

**D/A Conversion**

The low input bias current and offset voltage of the AD8605 make it an excellent choice for buffering the output of a current output DAC.

Figure 12 shows a typical implementation of the AD8605 at the output of a 12-bit DAC.

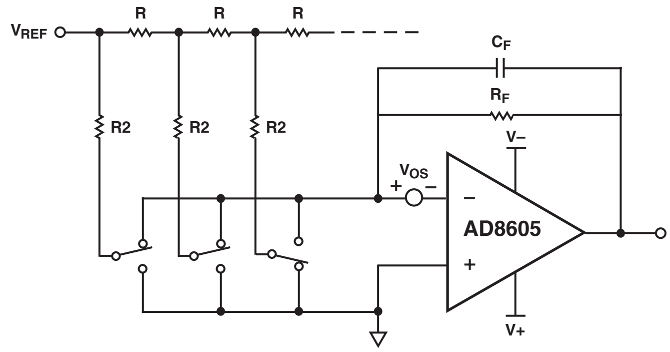



*Figure 12. Simplified Circuit of the DAC8143 with AD8605 Output Buffer*

The DAC8143 output current is converted to a voltage by the feedback resistor. The equivalent resistance at the output of the DAC varies with the input code, as does the output capacitance.

To optimize the performance of the DAC, insert a capacitor in the feedback loop of the AD8605 to compensate the amplifier from the pole introduced by the output capacitance of the DAC. Typical values for $C_F$ are in the range of 10 pF to 30 pF; it can be adjusted for the best frequency response. The total error at the output of the op amp can be computed by the formula:

$$E_O = V_{OS}\left(1+\frac{R_F}{Req}\right)$$

where *Req* is the equivalent resistance seen at the output of the DAC. As mentioned above, *Req* is code dependant and varies with the input. A typical value for *Req* is 15 kΩ. Choosing a feedback resistor of 10 kΩ yields an error of less than 200 μV.

Figure 13 shows the implementation of a dual-stage buffer at the output of a DAC. The first stage is used as a buffer. Capacitor C1, with Req, creates a low-pass filter and thus provides phase lead to compensate for frequency response. The second stage of the AD8606 is used to provide voltage gain at the output of the buffer.

Grounding the positive input terminals in both stages reduces errors due to the common-mode output voltage. Choosing R1, R2, and R3 to match within 0.01% yields a CMRR of 74 dB and maintains minimum gain error in the circuit.

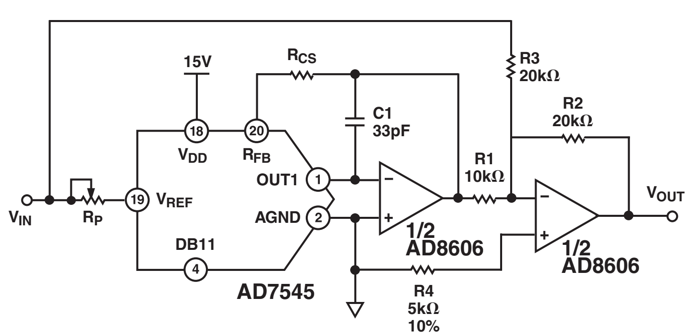
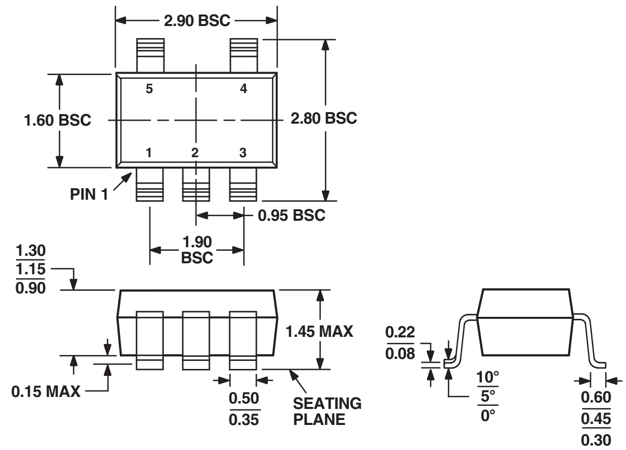



*Figure 13. Bipolar Operation*

## OUTLINE DIMENSIONS

### 5-Lead Small Outline Transistor Package [SOT-23] (RT-5)

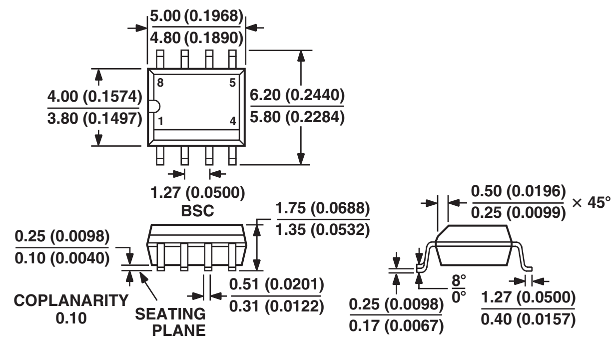
Dimensions shown in millimeters




COMPLIANT TO JEDEC STANDARDS MO-178AA

### 8-Lead Standard Small Outline Package [SOIC] Narrow Body (R-8)

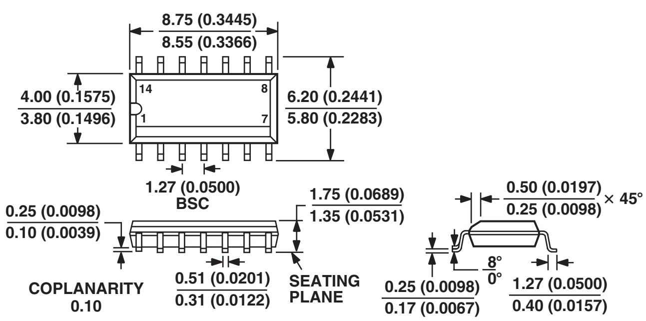
Dimensions shown in millimeters and (inches)




COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

### 14-Lead Standard Small Outline Package [SOIC] Narrow Body (R-14)

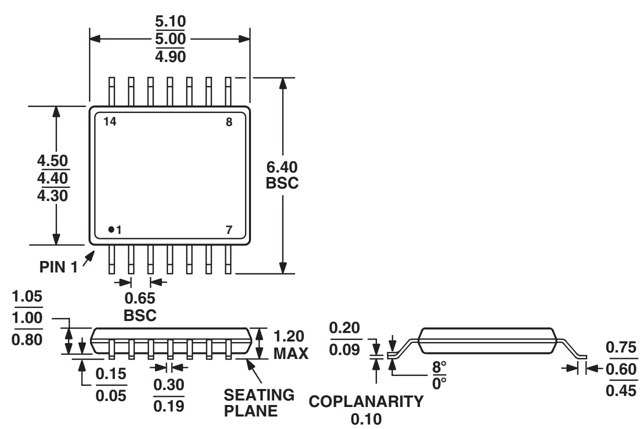
Dimensions shown in millimeters and (inches)




COMPLIANT TO JEDEC STANDARDS MS-012AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

### 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

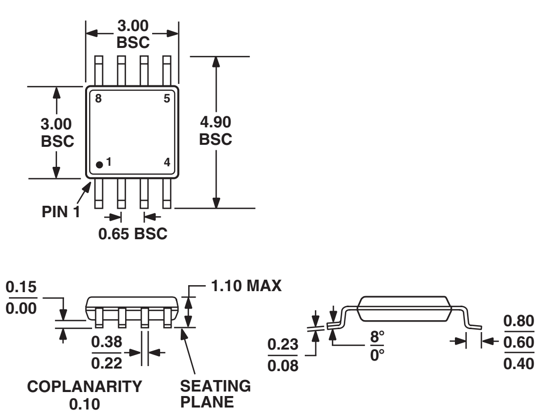
Dimensions shown in millimeters




COMPLIANT TO JEDEC STANDARDS MO-153AB-1

### 8-Lead Mini Small Outline Package [MSOP] (RM-8)

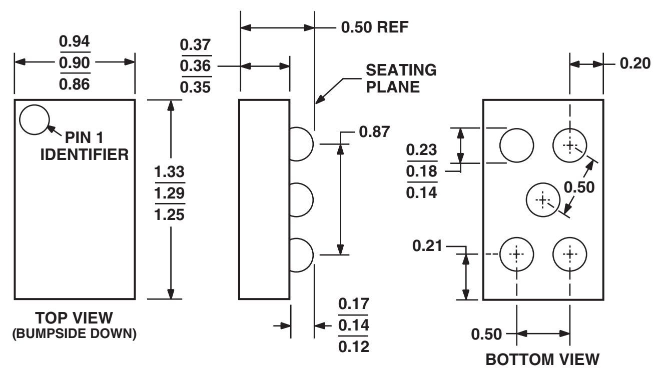
Dimensions shown in millimeters




COMPLIANT TO JEDEC STANDARDS MO-187AA

### 5-Bump 2 × 1 × 2 Array MicroCSP [WLCSP] (CB-5)

Dimensions shown in millimeters



## Revision History



C02731–0–7/03(C)