



64Kx16 SRAM

PRELIMINARY *

PIN CONFIGURATION
TOP VIEW

A0	1	44	A15
A1	2	43	A14
A2	3	42	A13
A3	4	41	OE
A4	5	40	UB
CS	6	39	LB
I/O1	7	38	I/O16
I/O2	8	37	I/O15
I/O3	9	36	I/O14
I/O4	10	35	I/O13
Vcc	11	34	Vss
Vss	12	33	Vcc
I/O5	13	32	I/O12
I/O6	14	31	I/O11
I/O7	15	30	I/O10
I/O8	16	29	I/O9
WE	17	28	NC
A5	18	27	A12
A6	19	26	A11
A7	20	25	A10
A8	21	24	A9
NC	22	23	NC

PIN DESCRIPTION

A0-15	Address Inputs
LB	Lower-Byte Control (I/O1-8)
UB	Upper-Byte Control (I/O9-16)
I/O1-16	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
Vss	Ground
NC	No Connection

PLASTIC PLUS™ FEATURES

- Access Times of 15, 17, 20ns
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- Industry Standard 44 Lead Plastic SOJ Package
- Electrical and Speed Characteristics for:
 - Military Temperature (-55°C to +125°C)
 - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Organized as 64K x 16
- Center Power/Ground Pins (Revolutionary)
- Data Byte Control:
 - Lower Byte (LB) = I/O1-8
 - Upper Byte (UB) = I/O9-16
- 5 Volt Power Supply
- I/O Compatible with 3.3V Devices
- Low Power Dissipation CMOS
- TTL Compatible Inputs and Outputs
- Battery Back-Up Operation
- Reliability Test Data Available:
 - High Temperature Operating Life
 - High Temperature Storage
 - Pressure Cooker Test
 - Wet High Temperature Operating Life
 - Thermal Shock
 - Temperature Cycling

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	Data I/O		Power
						I/O ₁₋₈	I/O ₉₋₁₆	
H	X	X	X	X	Not Select	High Z	High Z	Standby
L	H	H	X	X	Output Disable	High Z	High Z	Active
L	X	X	H	H		High Z	High Z	
L	H	L	L	H	Read	Data Out	High Z	Active
			H	L		High Z	Data Out	
			L	L		Data Out	Data Out	
L	L	X	L	H	Write	Data In	High Z	Active
			H	L		High Z	Data In	
			L	L		Data In	Data In	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T _A	-55	+125	°C
Operating Temperature (Ind.)	T _A	-40	+85	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} + 0.5	V
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T _A	-55	+125	°C
Operating Temperature (Ind.)	T _A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	6	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	8	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		200	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		8	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions				Units
			Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		0.25	1.0*	mA

* Also available in Low Power version. Please call factory for information.



AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t _{RC}	15		17		20		ns
Address Access Time	t _{AA}		15		17		20	ns
Output Hold from Address Change	t _{OH}	3		3		4		ns
Chip Select Access Time	t _{ACS}		15		17		20	ns
Output Enable to Output Valid	t _{OE}		10		11		12	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		8		9		10	ns
Output Disable to Output in High Z	t _{OHZ} ¹		8		9		10	ns
LB, UB Access Time	t _{BA}		10		11		12	ns
LB, UB Enable to Low Z Output	t _{BLZ} ¹	0		0		0		ns
LB, UB Disable to High Z Output	t _{BHZ} ¹		8		9		10	ns

1. This parameter is guaranteed by design but not tested.

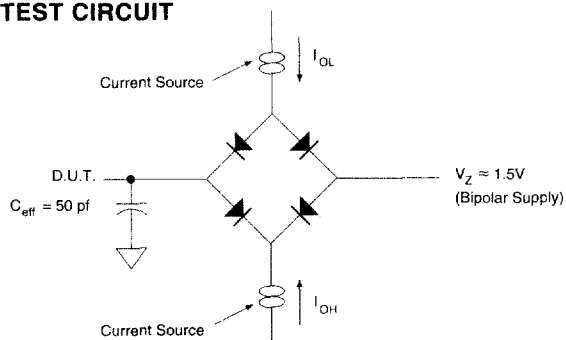
AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t _{WC}	15		17		20		ns
Chip Select to End of Write	t _{CW}	12		14		15		ns
Address Valid to End of Write	t _{AW}	12		14		15		ns
Data Valid to End of Write	t _{DW}	9		10		12		ns
Write Pulse Width	t _{WP}	12		14		15		ns
Address Setup Time	t _{AS}	0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		ns
Output Active from End of Write	t _{OW} ¹	0		0		0		ns
Write Enable to Output in High Z	t _{WHZ} ¹		10		10		10	ns
Data Hold Time	t _{DH}	0		0		0		ns
LB, UB Valid to End of Write	t _{BW}	12		14		15		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

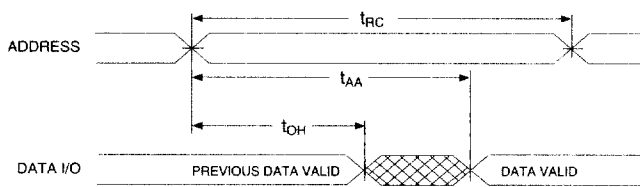
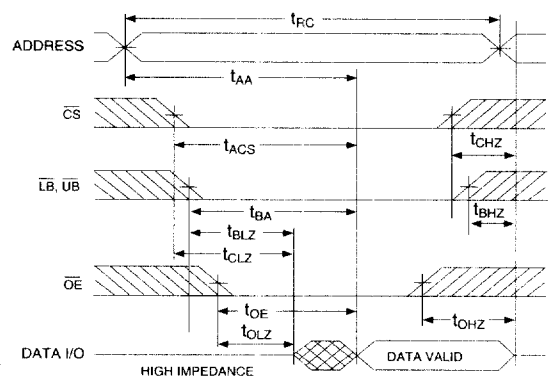
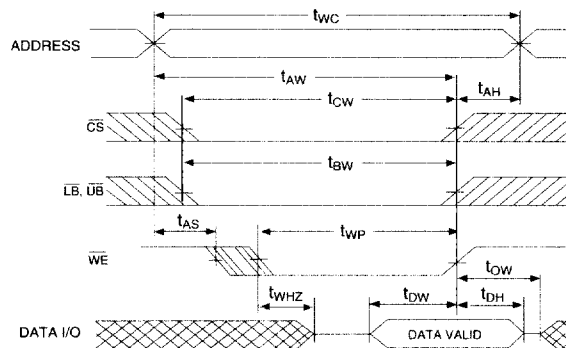
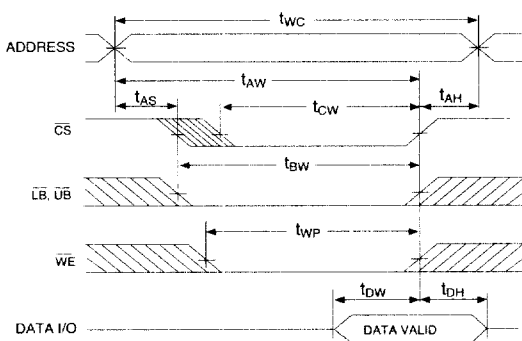
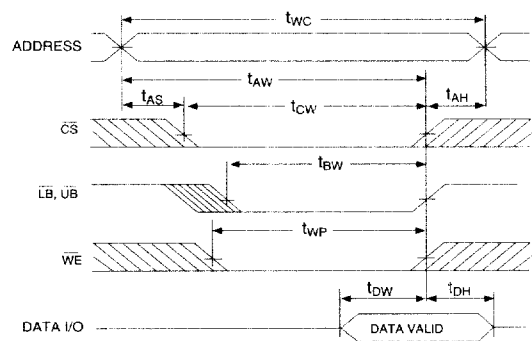
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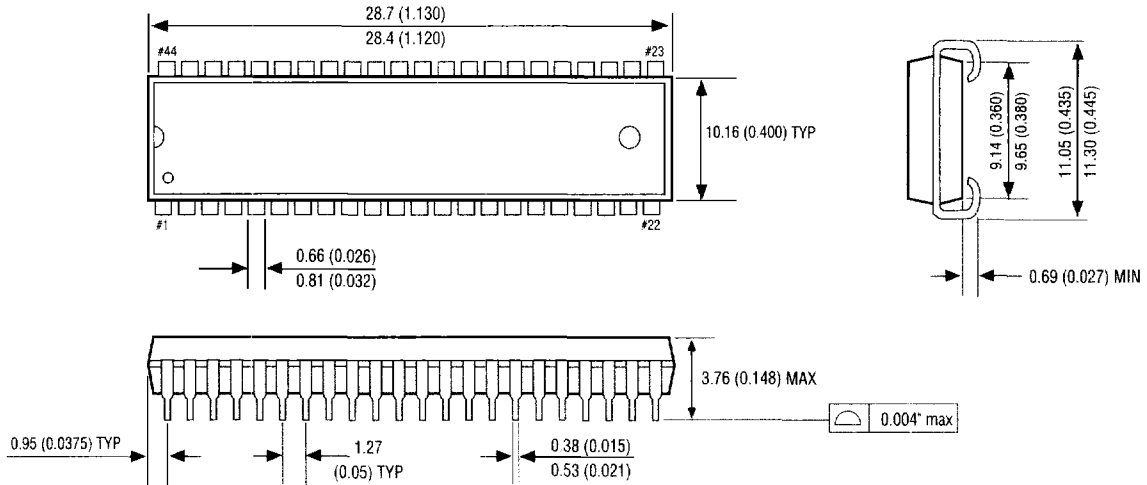
V_Z is programmable from -2V to +7V.I_{OL} & I_{OH} programmable from 0 to 16mA.Tester Impedance Z₀ = 75 Ω.V_Z is typically the midpoint of V_{OH} and V_{OL}.I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.



TIMING WAVEFORM - READ CYCLE

READ CYCLE 1 ($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$, $\overline{WE} = V_{IH}$)READ CYCLE 2 ($\overline{WE} = V_{IH}$)WRITE CYCLE - $\overline{WE}$ CONTROLLEDWRITE CYCLE 1, $\overline{WE}$ CONTROLLEDWRITE CYCLE - $\overline{CS}$ CONTROLLEDWRITE CYCLE 2, $\overline{CS}$ CONTROLLEDWRITE CYCLE - $\overline{LB}$, $\overline{UB}$ CONTROLLEDWRITE CYCLE 3, $\overline{LB}$, $\overline{UB}$ CONTROLLED

**44 LEAD, PLASTIC SOJ (400 mil)**

DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION**W P S 64K 16 X - XXX LJ X****DEVICE GRADE:**

M = Military Temperature -55°C to +125°C
I = Industrial Temperature -40°C to +85°C

PACKAGE:

LJ = 44 Lead Plastic SOJ

ACCESS TIME (ns)**IMPROVEMENT MARK**

B = Burn-in
T = Temperature Cycling
C = Burn-in and Temperature Cycle

ORGANIZATION, 64K x 16**SRAM****PLASTIC PLUS™****WHITE MICROELECTRONICS**