# **NPIC6C596**

# Power logic 8-bit shift register; open-drain outputs

Rev. 2 — 4 July 2013

**Product data sheet** 

### 1. General description

The NPIC6C596 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and open-drain outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset  $\overline{\text{MR}}$  input. A LOW on  $\overline{\text{MR}}$  resets both the shift register and storage register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register. To provide additional hold time in cascaded applications, the serial output QS7 is clocked out on the falling edge of SHCP. Data in the storage register drives the gate of the output extended-drain NMOS (EDNMOS) transistor whenever the output enable input ( $\overline{\text{OE}}$ ) is LOW. A HIGH on  $\overline{\text{OE}}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{\text{OE}}$  input does not affect the state of the registers.

The open-drain outputs are 33 V/100 mA continuous current extended-drain NMOS transistors designed for use in systems that require moderate load power such as LEDs. Integrated voltage clamps in the outputs provide protection against inductive transients making the device suitable for power driver applications such as relays, solenoids and other low-current or medium-voltage loads.

#### 2. Features and benefits

- Specified from -40 °C to +125 °C
- Low R<sub>DSon</sub>
- Eight Power EDNMOS transistor outputs of 100 mA continuous current
- 250 mA current limit capability
- Output clamping voltage 33 V
- 30 mJ avalanche energy capability
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption
- ESD protection:
  - ◆ HBM JDS-001 Class 2 exceeds 2500 V
  - CDM JESD22-C101E exceeds 1000 V



#### Power logic 8-bit shift register; open-drain outputs

## 3. Applications

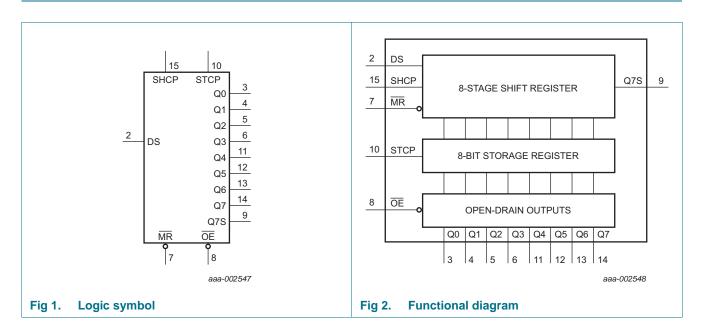
- LED sign
- Graphic status panel
- Fault status indicator

## 4. Ordering information

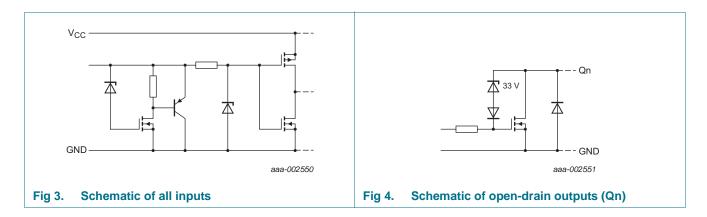
Table 1. Ordering information

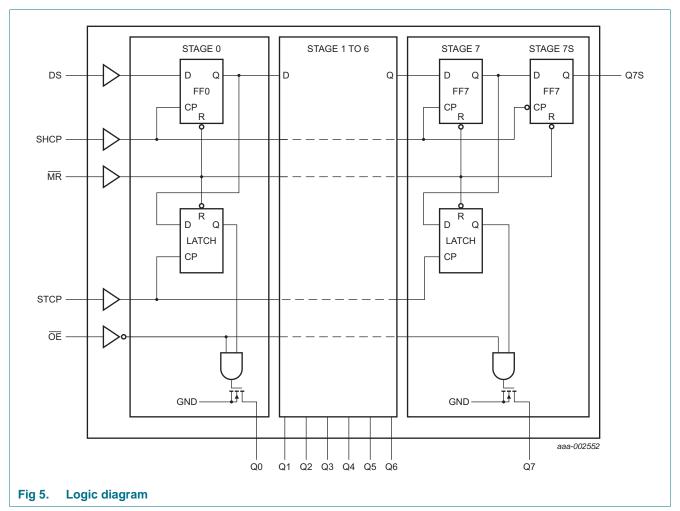
Type number	Package								
	Temperature range	Name	Description	Version					
NPIC6C596D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1					
NPIC6C596PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1					
NPIC6C596BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5\times3.5\times0.85$ mm	SOT763-1					

## 5. Functional diagram

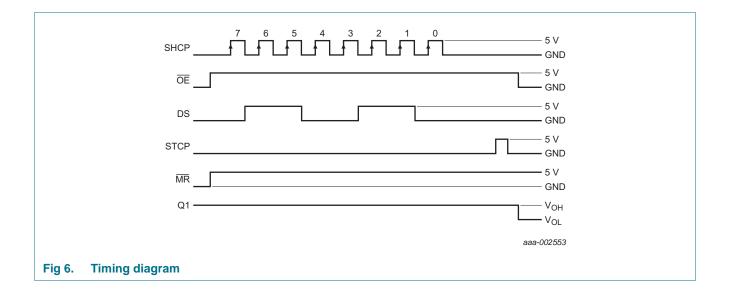


#### Power logic 8-bit shift register; open-drain outputs





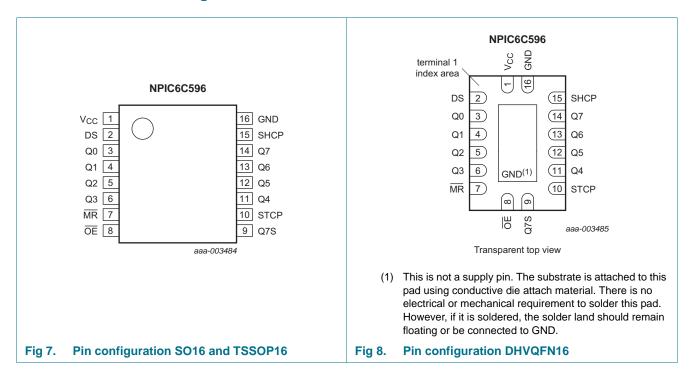
### Power logic 8-bit shift register; open-drain outputs



#### Power logic 8-bit shift register; open-drain outputs

## 6. Pinning information

#### 6.1 Pinning



#### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V <sub>CC</sub>	1	supply voltage
DS	2	serial data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	3, 4, 5, 6, 11, 12, 13, 14	parallel data output (open-drain)
MR	7	master reset (active LOW)
ŌE	8	output enable input (active LOW)
Q7S	9	serial data output
STCP	10	storage register clock input
SHCP	15	shift register clock input
GND	16	ground (0 V)

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#### Power logic 8-bit shift register; open-drain outputs

### **Limiting values**

Table 3. **Limiting values** 

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC}$	supply voltage			-0.5	+7.0	V
$V_{I}$	input voltage			-0.3	+7.0	V
$V_{DS}$	drain-source voltage	power EDNMOS drain-source voltage	<u>[1]</u>	-	+33	V
I <sub>d(SD)</sub>	source-drain diode current	continuous		-	250	mA
		pulsed	[2]	-	500	mA
I <sub>D</sub>	drain current	T <sub>amb</sub> = 25 °C				
		continuous; each output; all outputs on	-	100	mA	
		pulsed; each output; all outputs on	[2]	-	250	mA
I <sub>DM</sub>	peak drain current	single output; T <sub>amb</sub> = 25 °C	[2]	-	250	mA
E <sub>AS</sub>	avalanche energy	single pulse; see Figure 9	<u>[3]</u>	-	30	mJ
I <sub>AL</sub>	avalanche current	see <u>Figure 9</u>	<u>[3]</u>	-	200	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[4	<u>4]</u>		
		SO16		-	800	mW
		TSSOP16		-	725	mW
		DHVQFN16		-	1825	mW
		T <sub>amb</sub> = 125 °C	[4	<u>4]</u>		
		SO16		-	160	mW
		TSSOP16		-	145	mW
		DHVQFN16		-	365	mW

<sup>[1]</sup> Each power EDNMOS source is internally connected to GND.

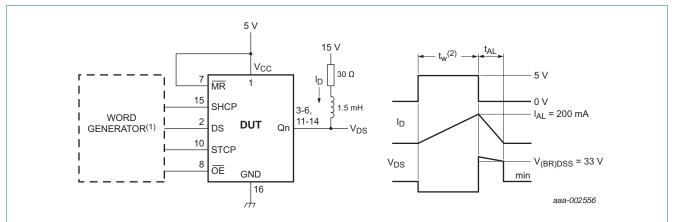
<sup>[2]</sup> Pulse duration  $\leq$  100  $\mu$ s and duty cycle  $\leq$  2 %.

<sup>[3]</sup>  $V_{DS} = 15 \text{ V}$ ; starting junction temperature ( $T_i$ ) = 25 °C; L = 1.5 H; avalanche current ( $I_{AL}$ ) = 200 mA.

<sup>[4]</sup> For SO16 packages: above 25 °C the value of Ptot derates linearly with 6.4 mW/°C. For TSSOP16 packages: above 25 °C the value of Ptot derates linearly with 5.8 mW/°C. For DHVQFN16 packages: above 25 °C the value of Ptot derates linearly with 14.6 mW/°C.

#### Power logic 8-bit shift register; open-drain outputs

#### 7.1 Test circuit and waveform



- (1) The word generator has the following characteristics:  $t_r$ ,  $t_f \le 10$  ns;  $Z_O = 50 \Omega$ .
- (2) The input pulse duration ( $t_W$ ) is increased until peak current  $I_{AL}$  = 200 mA. Energy test level is defined as:  $E_{AS} = I_{AL} \times V_{(BR)DSS} \times t_{AL}/2 = 30$  mJ.

Fig 9. Test circuit and waveform for measuring single-pulse avalanche energy

### 8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_{I}$	input voltage		0	-	5.5	V
I <sub>D</sub>	drain current	pulsed drain output current; $V_{CC} = 5 \text{ V}; T_{amb} = 25 ^{\circ}\text{C};$ all outputs on	[1][2] -	-	250	mA
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C

<sup>[1]</sup> Pulse duration  $\leq$  100  $\mu$ s and duty cycle  $\leq$  2 %.

#### 9. Static characteristics

Table 5. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	V <sub>CC</sub> = 5.	$V_{CC} = 5.0 \text{ V}; T_{amb} = 25 ^{\circ}\text{C}$				
			Min	Тур	Max			
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.85V <sub>CC</sub>	-	-	V		
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.15V <sub>CC</sub>	V		
$V_{OH}$	HIGH-level	serial data output Q7S; $V_I = V_{IH}$ or $V_{IL}$						
	output voltage	$I_{O} = -20 \mu A$ ; $V_{CC} = 4.5 V$	4.4	4.49	-	V		
		$I_{O} = -4 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.0	4.2	-	V		

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<sup>[2]</sup> Technique should limit  $T_i - T_{amb}$  to 10 °C maximum.

#### Power logic 8-bit shift register; open-drain outputs

**Table 5. Static characteristics** ...continued
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		V <sub>CC</sub> =	5.0 V; T <sub>amb</sub>	= 25 °C	Uni
				Min	Тур	Max	
V <sub>OL</sub>	LOW-level output	serial data output Q7S; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
	voltage	$I_O = 20 \mu A; V_{CC} = 4.5 V$		-	0.005	0.1	V
		$I_{O} = 4 \text{ mA}; V_{CC} = 4.5 \text{ V}$		-	0.3	0.5	V
I <sub>IH</sub>	HIGH-level input current	$V_{CC} = 5.5 \text{ V}; V_{I} = V_{CC}$		-	-	1	μΑ
I <sub>IL</sub>	LOW-level input current	$V_{CC} = 5.5 \text{ V}; V_{I} = 0 \text{ V}$		<b>–1</b>	-	-	μΑ
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$I_D = 1 \text{ mA}$		33	37	-	V
$V_{SD}$	source-drain voltage	diode forward voltage; I <sub>F</sub> = 100 mA		-	0.85	1.2	V
I <sub>CC</sub>	supply current	logic supply current; $V_{CC} = 5.5 \text{ V}$ ; $V_I = V_{CC}$ or GND					
		all outputs off		-	0.004	200	μΑ
		all outputs on	[1]	-	0.006	500	μΑ
		all outputs off; SHCP = 5 MHz; C <sub>L</sub> = 30 pF; see <u>Figure 14</u> and <u>Figure 16</u>		-	0.75	5	mA
I <sub>O(nom)</sub>	nominal output current	$V_{DS}$ = 0.5 V; $T_{amb}$ = 85 °C; $I_{out}$ = $I_{D}$	[2][3][4]	-	140	-	mA
I <sub>DSX</sub>	drain cut-off	$V_{CC} = 5.5 \text{ V}; V_{DS} = 30 \text{ V}$		-	0.002	0.2	μΑ
	current	V <sub>CC</sub> = 5.5 V; V <sub>DS</sub> = 30 V; T <sub>amb</sub> = 125 °C		-	0.15	0.3	μΑ
R <sub>DSon</sub>	drain-source	see Figure 17 and Figure 18	[2][3]				
	on-state resistance	$V_{CC} = 4.5 \text{ V}; I_D = 50 \text{ mA}$		-	3.0	9	Ω
	Todistarios	$V_{CC}$ = 4.5 V; $I_D$ = 50 mA; $T_{amb}$ = 125 °C			5.4	12	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>D</sub> = 100 mA		-	3.1	10	Ω

<sup>[1]</sup> Output currents below 250 mA current limit.

<sup>[2]</sup> Technique should limit  $T_j - T_{amb}$  to 10 °C maximum.

<sup>[3]</sup> These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

<sup>[4]</sup> Nominal output current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T<sub>amb</sub> = 85 °C.

#### Power logic 8-bit shift register; open-drain outputs

### 10. Dynamic characteristics

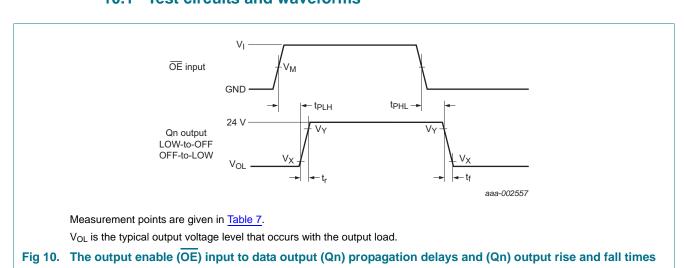
Table 6. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see Figure 14.

Symbol	Parameter	Conditions		V <sub>CC</sub> =	5.0 V; T <sub>amb</sub>	= 25 °C	Unit	
				Min	Тур	Max		
t <sub>PLH</sub>	LOW to HIGH propagation delay	OE to Qn; I <sub>D</sub> = 75 mA; see <u>Figure 10</u> and <u>Figure 19</u>	·	-	97	-	ns	
t <sub>PHL</sub>	HIGH to LOW propagation delay	$\overline{OE}$ to Qn; $I_D = 75$ mA; see $\overline{Figure 10}$ and $\overline{Figure 19}$		-	9	-	ns	
t <sub>r</sub>	rise time	$\overline{OE}$ to Qn; $I_D = 75$ mA; see $\underline{Figure 10}$ and $\underline{Figure 19}$		-	60	-	ns	
t <sub>f</sub>	fall time	$\overline{OE}$ to Qn; $I_D = 75$ mA; see $\overline{Figure 10}$ and $\overline{Figure 19}$		-	18	-	ns	
t <sub>pd</sub>	propagation delay	SHCP to Q7S; $I_D = 75$ mA; see Figure 11	[1]	-	5	-	ns	
$f_{\text{max}}$	maximum frequency	SHCP; I <sub>D</sub> = 75 mA; see Figure 11	[2]	-	-	10	MHz	
t <sub>rr</sub>	reverse recovery time	$I_F$ = 100 mA; dI/dt = 10 A/ $\mu$ s; see Figure 13	[3][4]	-	120	-	ns	
ta	reverse recovery current rise time	$I_F$ = 100 mA; dI/dt = 10 A/ $\mu$ s; see Figure 13	[3][4]	-	100	-	ns	
t <sub>su</sub>	set-up time	DS to SHCP; see Figure 12		15	-	-	ns	
t <sub>h</sub>	hold time	DS to SHCP; see Figure 12		15	-	-	ns	
t <sub>W</sub>	pulse width			40	-	-	ns	

<sup>[1]</sup>  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

#### 10.1 Test circuits and waveforms



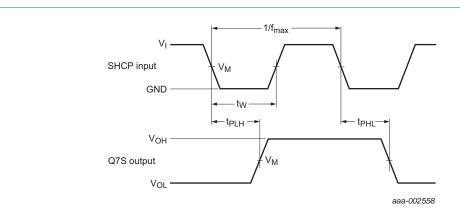
NPIC6C596

This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SHCP  $\rightarrow$  Q7S propagation delay and setup time plus some timing margin.

<sup>[3]</sup> Technique should limit  $T_j - T_{amb}$  to 10 °C maximum.

<sup>[4]</sup> These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

#### Power logic 8-bit shift register; open-drain outputs



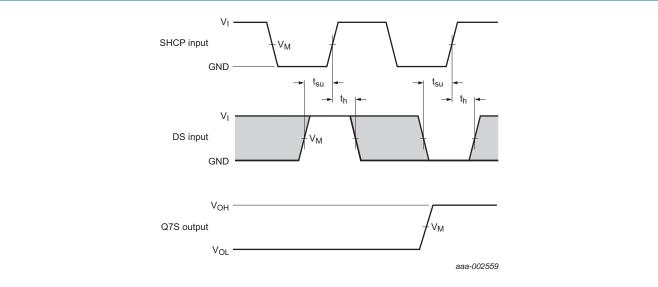
Measurement points are given in Table 7.

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are the typical output voltage levels that occur with the output load.

Fig 11. The shift clock (SHCP) to serial data output (Q7S) propagation delays with the minimum shift clock pulse width and maximum shift clock frequency

Table 7. Measurement points

Supply voltage	Input	Output							
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>					
5 V	0.5V <sub>CC</sub>	0.5V <sub>DS</sub>	0.1V <sub>DS</sub>	0.9V <sub>DS</sub>					



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are the typical output voltage levels that occur with the output load.

Fig 12. The data set-up and hold times for the serial data input (DS)

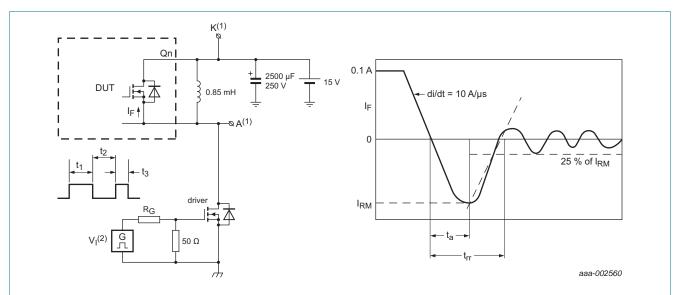
Table 8. Measurement points

Supply voltage	Input	Output
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>
5 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>

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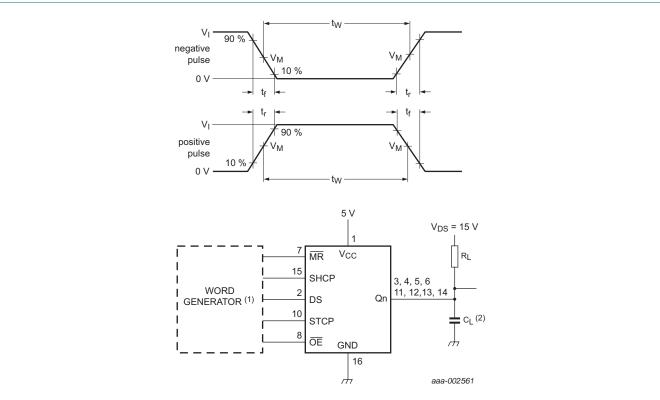
#### Power logic 8-bit shift register; open-drain outputs



- (1) The open-drain Qn terminal under test is connected to test point K. All other terminals are connected together and connected to
- The  $V_I$  amplitude and  $R_G$  are adjusted for dI/dt = 10 A/ $\mu$ s. A  $V_I$  double-pulse train is used to set  $I_F$  = 0.1 A, where  $t_1$  = 10  $\mu$ s,  $t_2$  = 7  $\mu$ s and  $t_3 = 3 \mu$ s.

Fig 13. Test circuit and waveform for measuring reverse recovery current

#### Power logic 8-bit shift register; open-drain outputs



- (1) The word generator has the following characteristics:  $t_r$ ,  $t_f \le 10$  ns;  $t_W = 300$  ns; pulsed repetition rate (PRR) = 5 kHz;  $Z_O = 50 \ \Omega$ .
- (2) C<sub>L</sub> includes probe and jig capacitance.

Test data is given in Table 9. Definitions for test circuit:

 $V_{DS}$  = External voltage for Power EDNMOS drain-source voltage.

R<sub>L</sub> = Load resistance.

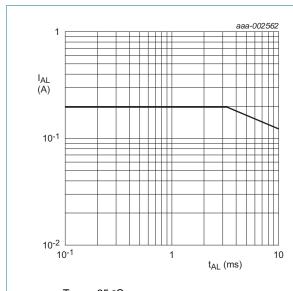
C<sub>L</sub> = Load capacitance including jig and probe capacitance.

Fig 14. Test circuit for measuring switching times

Table 9. Test data

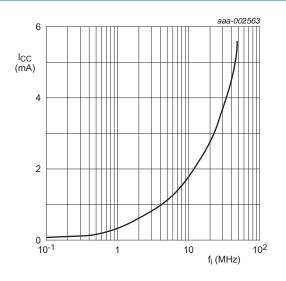
Supply voltage	Input			Load		
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	V <sub>M</sub>	CL	R <sub>L</sub>	
5 V	5 V	≤ 10 ns	50 %	30 pF	200 Ω	

#### Power logic 8-bit shift register; open-drain outputs



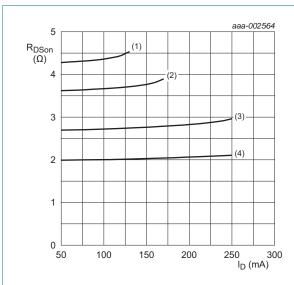
 $T_{amb}$  = 25 °C.

Fig 15. Avalanche current (peak) versus time duration of avalanche



 $T_{amb} = -40 \, ^{\circ}\text{C} \text{ to } +125 \, ^{\circ}\text{C}; \, V_{CC} = 5 \, \text{V}.$ 

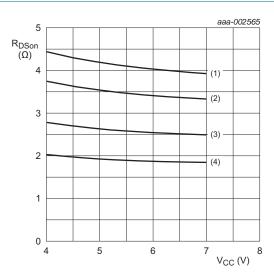
Fig 16. Supply current versus frequency



 $V_I = V_{CC}$  or GND and  $V_O = GND$  or  $V_{CC}$ .

- (1)  $T_{amb} = 125 \, ^{\circ}C$
- (2)  $T_{amb} = 85 \, ^{\circ}C$
- (3)  $T_{amb} = 25 \, ^{\circ}C$
- (4)  $T_{amb} = -40 \, ^{\circ}C$

Fig 17. Drain-source on-state resistance versus drain current

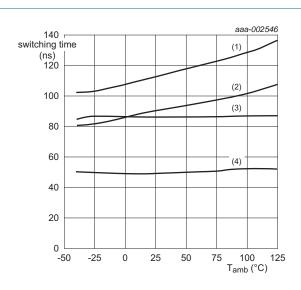


 $V_I = V_{CC}$  or GND and  $V_O =$  open circuit.

- (1)  $T_{amb} = 125 \, ^{\circ}C$
- (2)  $T_{amb} = 85 \, ^{\circ}C$
- (3)  $T_{amb} = 25 \, ^{\circ}C$
- (4)  $T_{amb} = -40 \, ^{\circ}C$

Fig 18. Static drain-source on-state resistance versus supply voltage

#### Power logic 8-bit shift register; open-drain outputs



Technique limit  $T_J - T_C$  to 10 °C maximum.

- (1) t<sub>PLH</sub>.
- (2) t<sub>r</sub>.
- (3) t<sub>f</sub>.
- (4) t<sub>PHL</sub>.

Fig 19. Switching time versus case temperature

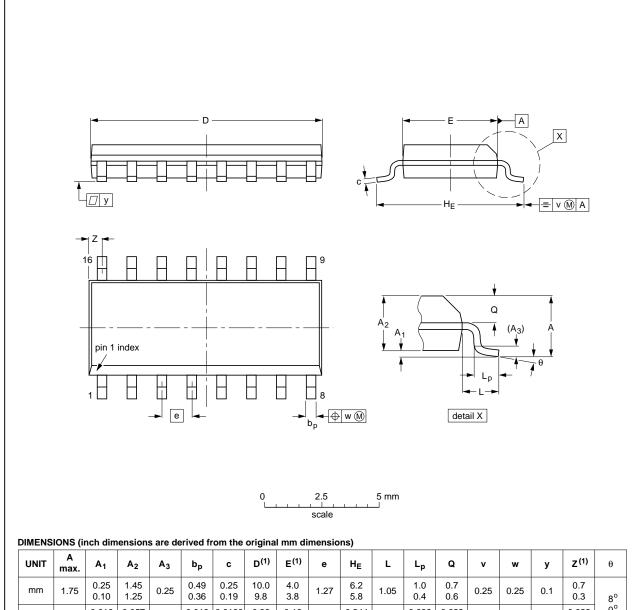
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#### Power logic 8-bit shift register; open-drain outputs

### 11. Package outline

#### SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	I	0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			<del>99-12-27</del> 03-02-19
	•				

Fig 20. Package outline SOT109-1 (SO16)

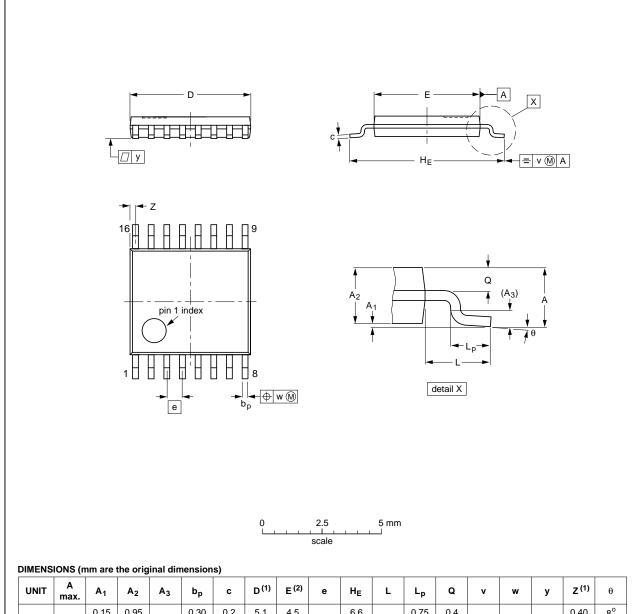
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#### Power logic 8-bit shift register; open-drain outputs

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E (2)	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ	
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°	İ

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				<del>-99-12-27</del> 03-02-18	

Fig 21. Package outline SOT403-1 (TSSOP16)

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#### Power logic 8-bit shift register; open-drain outputs

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

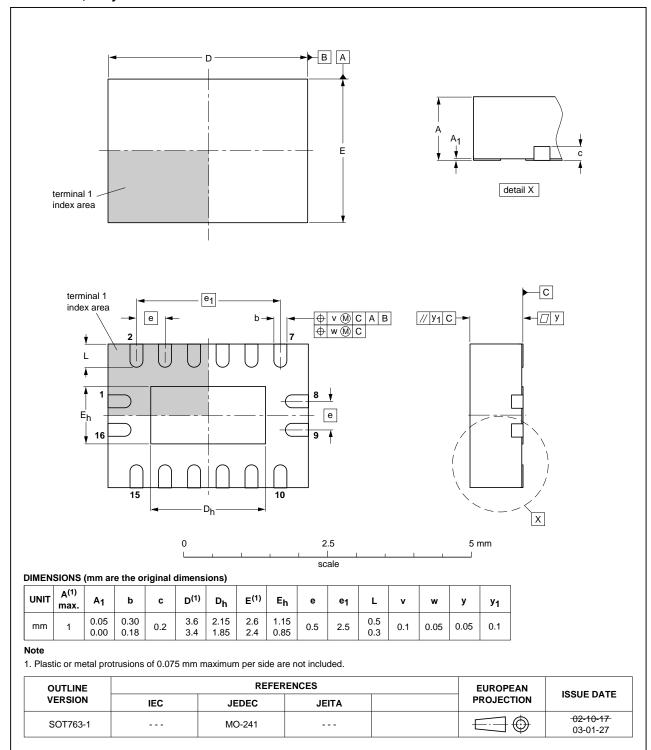


Fig 22. Package outline SOT763-1 (DHVQFN16)

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### Power logic 8-bit shift register; open-drain outputs

### 12. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
EDNMOS	Extended Drain Negative Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

# 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NPIC6C596 v.2	20130704	Product data sheet	-	NPIC6C596 v.1
Modifications:	<ul> <li>Figure 5 cor</li> </ul>	rected (errata).		
NPIC6C596 v.1	20120821	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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