MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX604 v.23 Compatible Modem

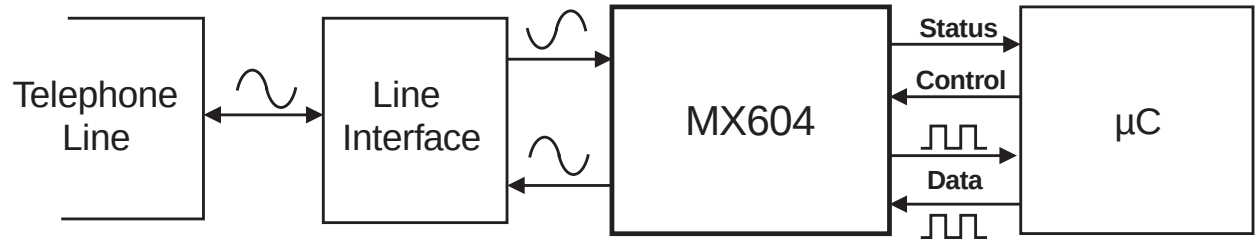
PRELIMINARY INFORMATION

FEATURES

- **1200bps forward, 75bps back channels**
- **Conforms to relevant sections of v.23 and ETSI specifications**
- **Line Equalization**
- **1200bps Data Retiming Facility can eliminate external UART**
- **Low Voltage Operation (3.3 to 5.0V)**

APPLICATIONS

- **Low Power Operation**
  1mA typ. @ 3.3V Operating Mode
  1μA typ. Zero-Power Mode
- **Standard 3.58Mhz Xtal/Clock**
- **Telephone Telemetry System Applications**



The MX604 is a low voltage, low power CMOS device, used for the reception or transmission of asynchronous 1200bps data and full-duplex 75bps back channel data in accordance with CCITT V.23 and ETSI specifications.

This device provides an optional Tx and Rx data retiming function which can eliminate, based on user preference, the need for an external UART when operating at 1200bps. The device can disable the back channel or be operated so only the mark or space tone is produced. The optional line equalizer is incorporated into the receive path and is controlled by an external logic level.

The MX604 may be used in a wide range of telephone telemetry systems. Low voltage capability, a low operating current (1mA typ. @ V_{DD} = 3.3V), and a very low current 'sleep' mode (1μA typ.) make the MX604 ideal for both portable terminal and line powered applications.

The MX604 is available in the following packages: 24-pin TSSOP (MX604TN), 16-pin SOIC (MX604DW) and 16-pin PDIP (MX604P).

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1. Block Diagram

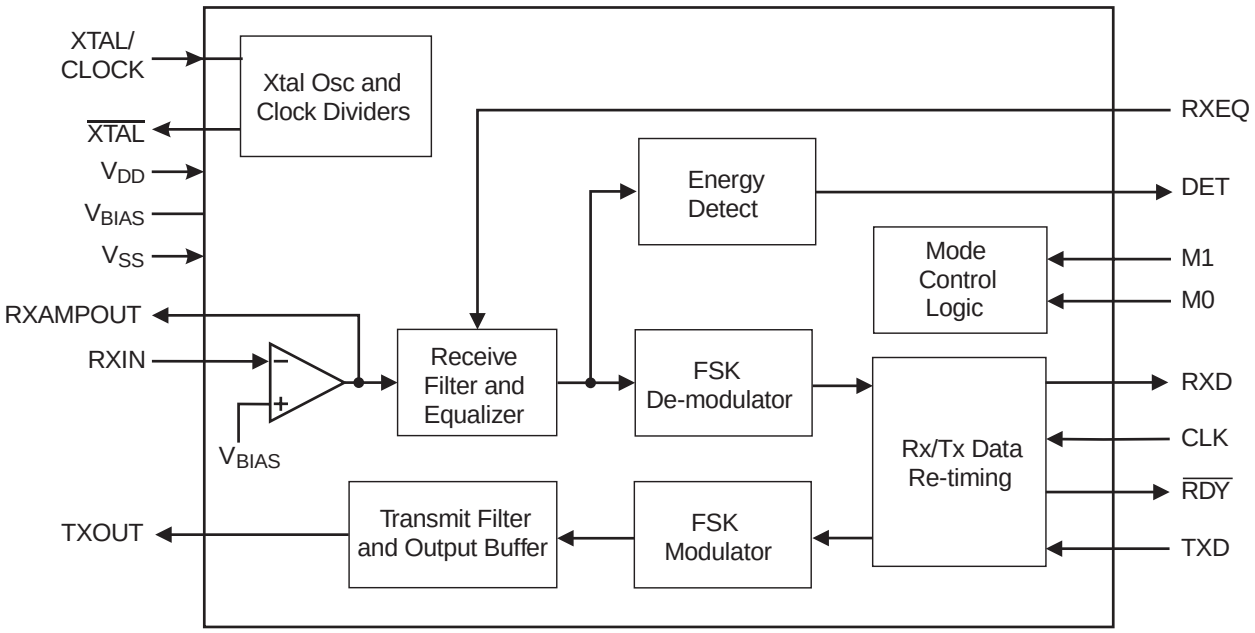

Figure 1: Block Diagram

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2. Signal List

Pin No.		Name	Type	Description
P, DW	TN			
1	1	$\overline{XTAL}$	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier.
7	11	TXOUT	output	Output of the FSK generator.
8	12	V_{SS}	power	Negative supply (ground).
9	13	V_{BIAS}	output	Internally generated bias voltage, held at V_{DD} /2 when the device is not in 'Zero-Power' mode. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in/out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip energy detect circuit.
15	23	$\overline{RDY}$	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated μC. An external pull-up resistor should be connected between this output and V_{DD}.
16	24	V_{DD}	power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
	3, 4, 9, 10 ,15, 16, 21, 22	N/C		No internal connections

This device is capable of detecting and decoding small amplitude signals. Achieving the V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that decoupling capacitors be placed so the connection between them and the device pins is as short as possible. A ground plane protecting the receive path will help attenuate interfering signals.

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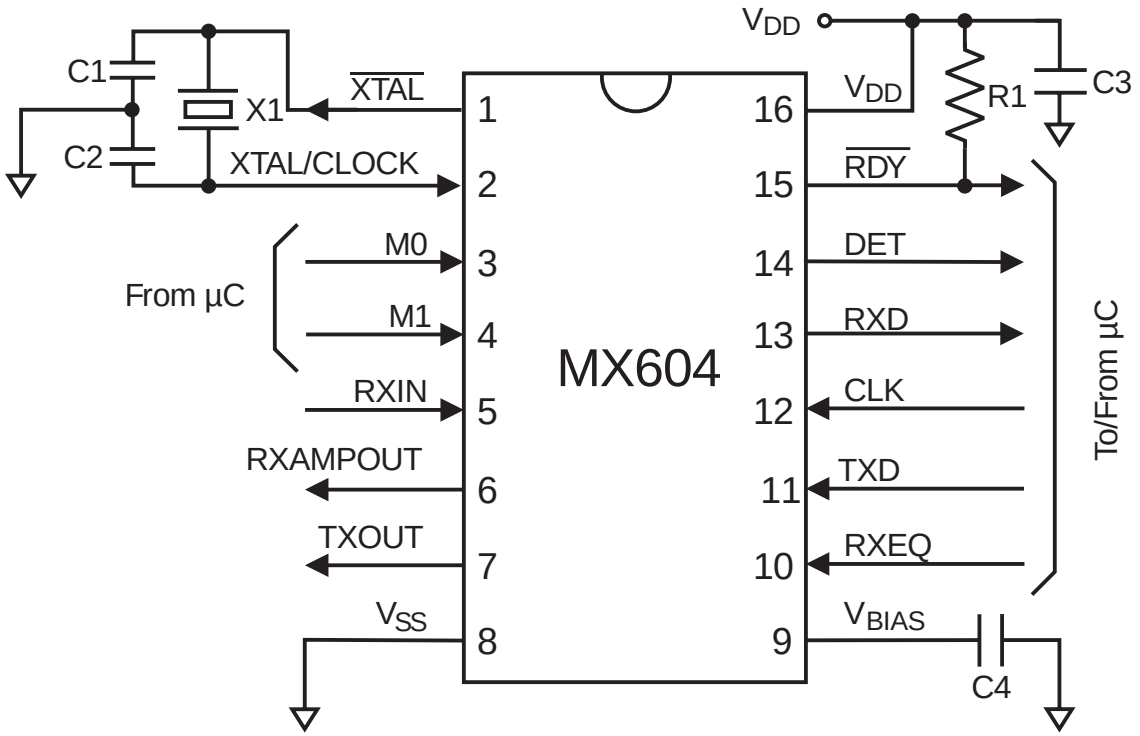
3. External Components



R1		100kΩ	±5%,
C1, C2		18pF	±10%
C3		0.1µF	±10%
C4		0.1µF	±10%
X1	Note 1	3.579545MHz	

Figure 2: Recommended External Components for Typical Application

External Components Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4. General Description

4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX604 is determined by a 3.579545MHz clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or it may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be used.

The on-chip oscillator is disabled in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX604 as well as generating undefined states of the RXD, DET and $\overline{RDY}$ outputs.

4.2 Mode Control Logic

The MX604's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Rx Mode	Tx Mode	Data Retime[1]
0	0	1200bps	75bps	Rx
0	1	off	1200bps	Tx
1	0	1200bps	off	Rx
1	1	'Zero-Power'		-

[1] If enabled.

Note: On applying power to the device the mode must be set to 'ZP', i.e. M0=1, M1=1, until V_{DD} has stabilized.

In the 'Zero-Power' mode, power is removed from all internal circuitry. When leaving 'Zero-Power' mode there must be a 20ms delay before any Tx data is passed to, or Rx data read from, the device to allow the bias level, filters and oscillator to stabilize.

4.3 Rx Input Amplifier

The Rx Input Amplifier is used to adjust the signal received to the correct amplitude for the FSK receiver and Energy Detect circuits (see section 5.1).

4.4 Receive Filter and Equalizer

The Receive Filter and Equalizer is used to attenuate out of band noise and interfering signals, especially the locally generated 75bps transmit tones which might otherwise reach the 1200bps FSK Demodulator and Energy Detector circuits. This block also includes a switchable equalizer section. When the RXEQ pin is low the overall group delay of the receive filter is flat over the 1200bps frequency range. If the RXEQ pin is high the receive filter's typical overall group delay will be as shown in Figure 3.

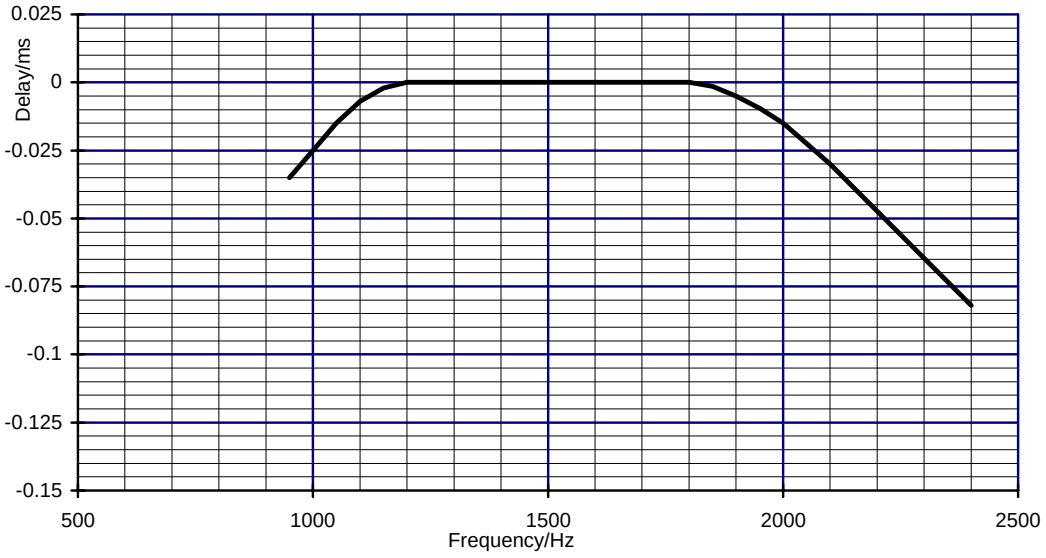


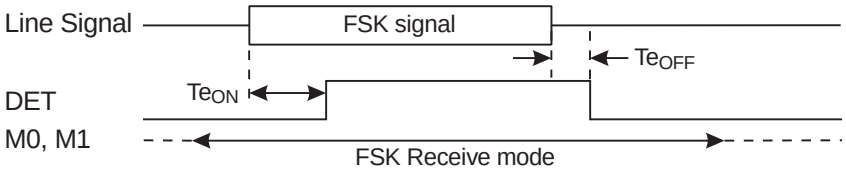
Figure 3: Rx Equalizer Group Delay (RXEQ = 1) with respect to 1700Hz

4.5 Energy Detector

The Energy Detector block operates by measuring the level of the signal at the output of the Receive Filter, and comparing it against a preset threshold.

The DET output will be set high when the level has exceeded the threshold for a sufficient time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note: This circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of Te_{ON} and Te_{OFF}

Figure 4: FSK Level Detector Operation

4.6 FSK Demodulator

The FSK Demodulator block converts the 1200bps FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.8). This output does not depend on the state of the DET output.

When the Rx 1200bps mode is 'off' or in 'ZP' the DET and RXD pins are held low.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data. For this reason it is advised that the RXD pin be read only when data is expected.

4.7 FSK Modulator and Transmit Filter

The FSK Modulator and Transmit Filter blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = 0	TXD = 1
1	1	-	
1	0	0Hz[1]	
0	0	450Hz	390Hz
0	1	2100Hz	1300Hz

FSK Modulator and Transmit Filter Note:

[1] TXOUT held at approx. $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 5 and Figure 6, assuming that the signal on the line is at -6dBm or less.

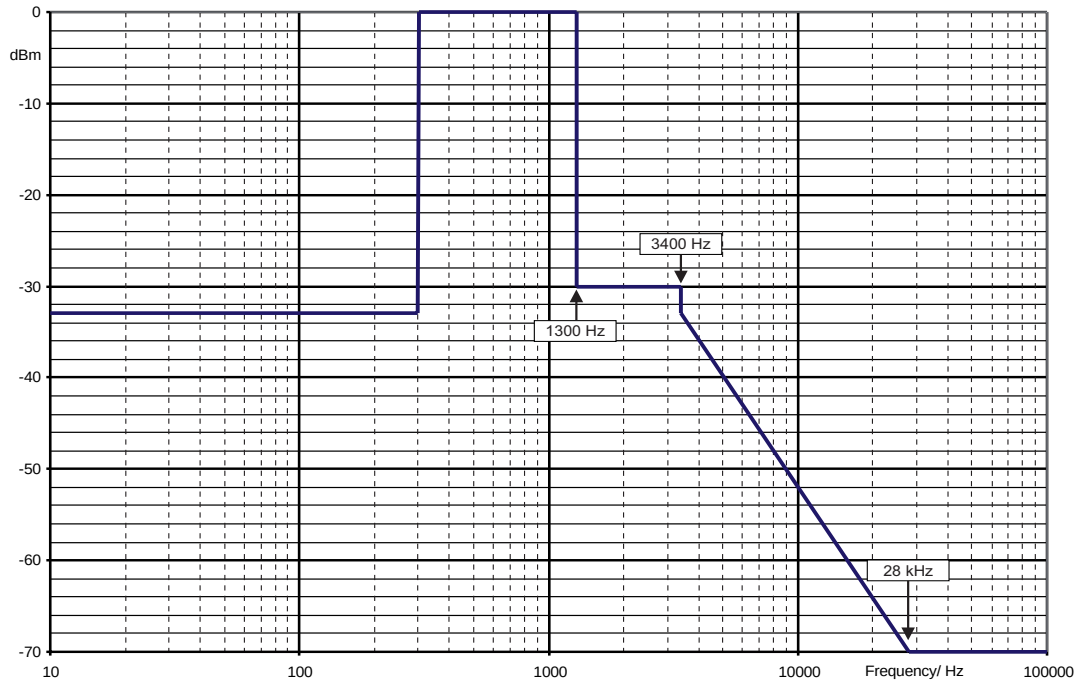


Figure 5: Tx limits at 75bps rate

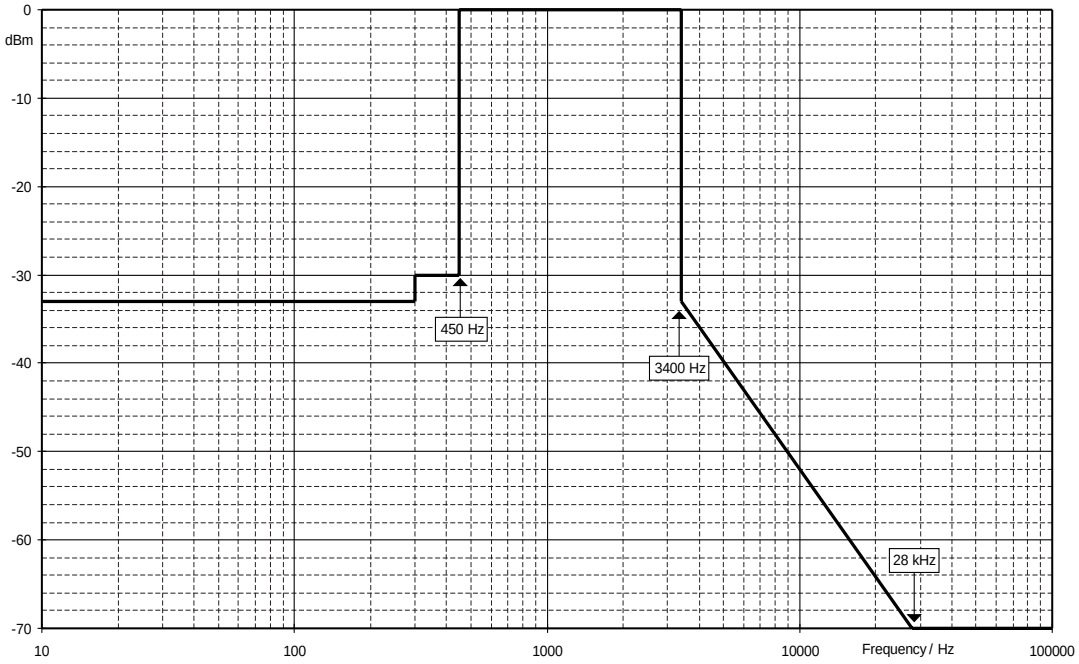


Figure 6: Tx limits at 1200bps rate

4.8 Rx Data Retiming

The Rx Data Retiming function may be used when the received data consists of 1200bps asynchronous characters, each character consisting of one start bit followed by a minimum of 9 formatted bits as shown in the table below.

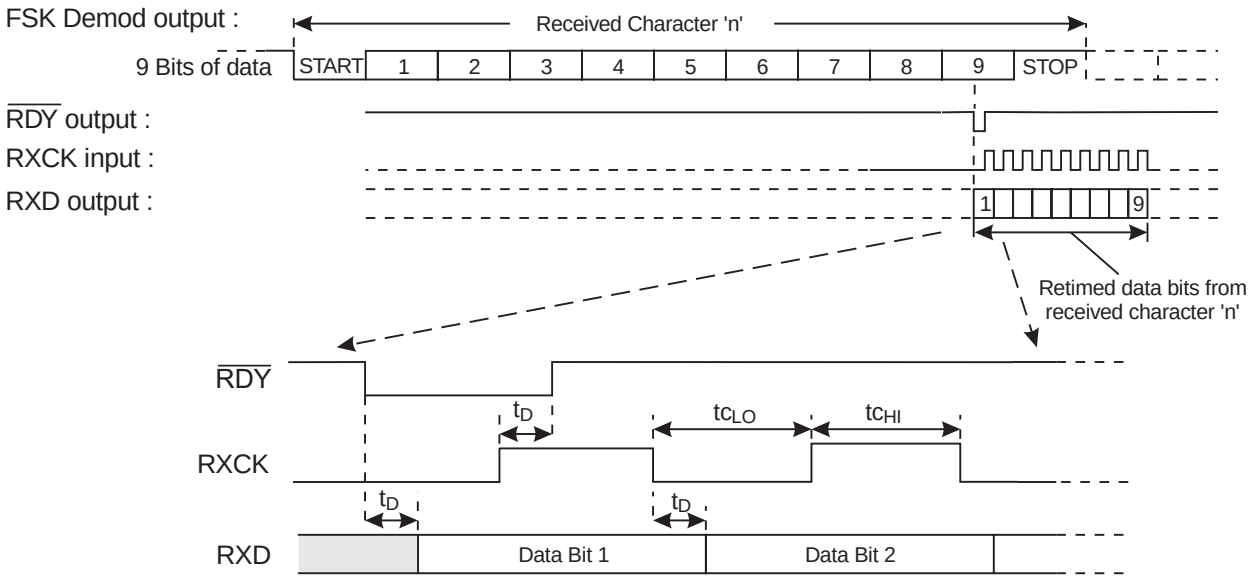
Data bits	Parity bits	Stop bits
7	0	≥2
7	1	≥1
8	0	≥1
8	1	≥1
9	0	≥1

When enabled in receive mode, the Data Retiming block extracts the first 9 bits of each character following the start bit, from the received asynchronous data stream, and presents them to the μC, under the control of strobe pulses applied to the CLK input. The timing of these pulses is not critical. They may be generated easily by a simple software loop. This facility removes the need for a UART in the μC without incurring an excessive software overhead.

The receive retiming block consists of two 9-bit shift registers, the input of the first is connected to the output of the FSK demodulator and the output of the second is connected to the RXD pin. The first register is clocked by an internally generated signal that stores the 9 received bits following the timing reference of a high to low transition at the output of the FSK demodulator. When the 9th bit is clocked into the first register these 9 bits are transferred to the second register, a new stop-start search is initiated and the CLK input is sampled. If the CLK input is low at this time the $\overline{RDY}$ pin is pulled low and the first received bit is output on the RXD pin. The CLK pin should then be pulsed high 9 times, the first 8 high to low transitions will be used by the device to clock out the bits in the second register. The $\overline{RDY}$ output is cleared the first time the CLK input goes high. At the end of the 9th pulse the RXD pin will be connected to the FSK demodulator output.

To use the Data Retiming function, the CLK input should be kept low until the $\overline{RDY}$ output goes low; if the Data Retiming function is not required then the CLK input should be kept high at all times.

The only restrictions on the timing of the CLK waveform are those shown in Figure 7 and the need to complete the transfer of all nine bits into the μC within the time of a complete character at 1200bps.



t_D = Internal MX604 delay, tc_{HI} = CLK high time, tc_{LO} = CLK low time

Figure 7: FSK Operation with Rx Data Re-timing

Note: If enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the MX604 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the $\overline{RDY}$ output will not be activated by the FSK signal. This case is illustrated by the example in Figure 8

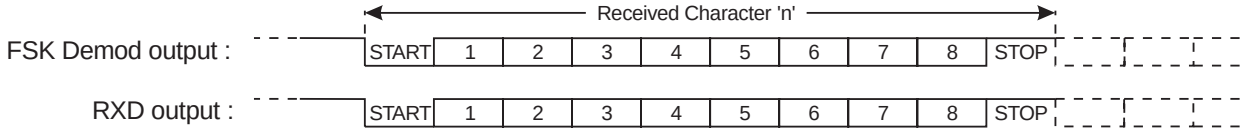


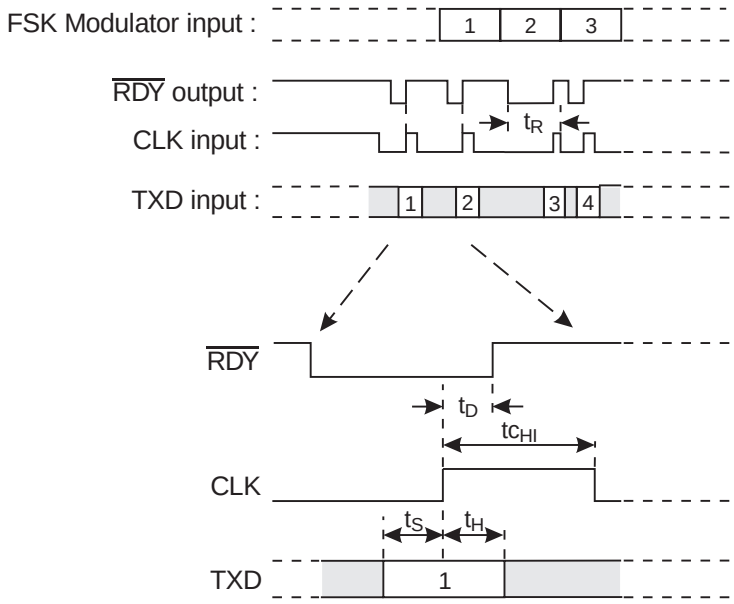
Figure 8: FSK Operation without Rx Data Re-timing (CLK always high)

4.9 Tx Data Retiming

The Tx Data Retiming block, when enabled in 1200bps transmit mode, requires the controlling μC to load 1 bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical. It may be generated easily by a simple software loop. This facility removes the need for a UART in the μC without incurring an excessive software overhead.

The Tx retiming circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the $\overline{RDY}$ pin is pulled low. The $\overline{RDY}$ output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

To use the retiming option, the CLK input should be held low until the $\overline{RDY}$ output is pulled low. When the $\overline{RDY}$ pin goes low, the next data bit should be applied to the TXD input and the CLK input pulled high and then low within the time limits defined in Figure 9.



t_D = Internal MX604 delay; t_R = low to CLK going low; t_S = data set up time
tc_{HI} = CLK high time, t_H = data hold time

Figure 9: FSK Operation with Tx Data Retiming

To ensure synchronization between controlling device and the MX604 when entering Tx retiming mode the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

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If the data retiming facility is not required, then the CLK input to the MX604 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 10 and will also be the case when transmitting 75bps data which has no retime option.

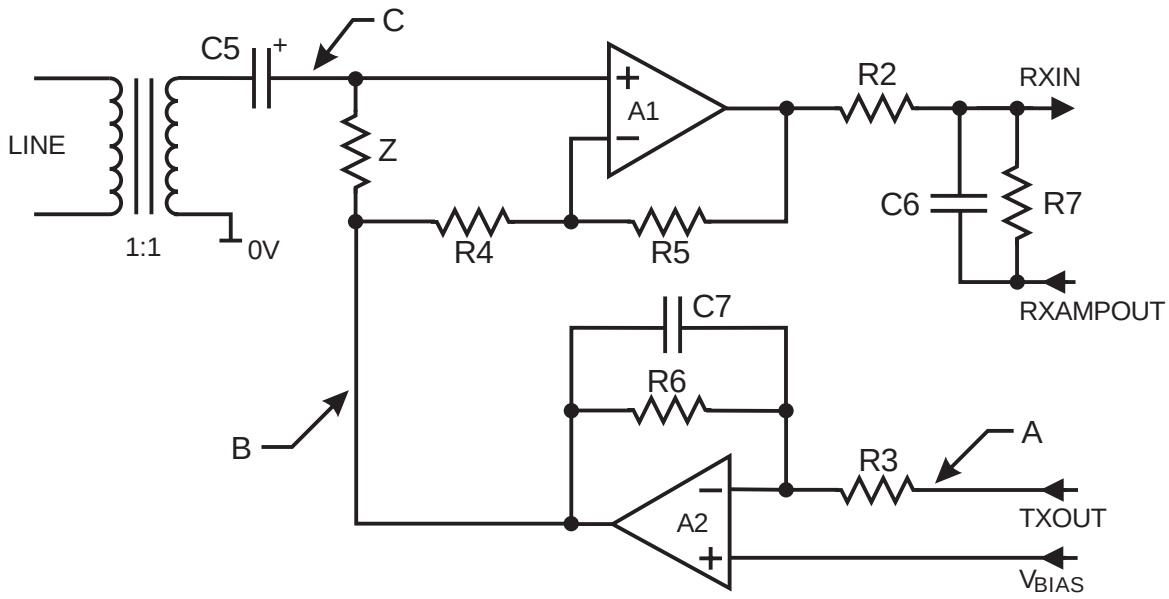
Figure 10: FSK Operation without Tx Data Re-timing (CLK always high)

5. Application

5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the MX604. A Line Interface circuit is necessary to:

- Provide high voltage and dc isolation
- Attenuate the Tx signal present at the Rx input
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals



R2	See Notes	±1%,
R3	See Notes	±1%,
R4-R7	100kΩ	±1%,

C5	22μF	±20%
C6	100pF	±10%
C7	330pF	±10%

Figure 11: Line Interface Circuit

Line Interface Notes:

- The components 'Z' between points B and C should match the line impedance.
- Device A2 must be able to drive 'Z' and the line.
- R2: For optimum results R2 should be set so that the gain is $V_{DD}/5.0$, i.e. R2 = 100kΩ at V_{DD} = 5.0V, rising to 150kΩ at V_{DD} = 3.3V.
- R3: The levels in dB (relative to a 775mV_{RMS} signal) at 'A', 'B' and 'C' in the line interface circuit are:

'A' = 20Log(V_{DD}/5)

'B' = 'A' + 20Log(100kΩ/R3)

'C' = 'B' - 6

V_{DD}	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C

Xtal Frequency = 3.579545MHz ± 0.1%, 0dBV corresponds to 1.0V_{RMS}, 0dB = 0dBm = 775mV_{RMS} into 600Ω.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0='1', M1='1')	1, 2		1		µA
I_{DD} (M0 or M1='0') at V_{DD} = 3.0V	1		1.0	1.25	mA
I_{DD} (M0 or M1='0') at V_{DD}= 5.0V	1		1.7	2.5	mA
Logic '1' Input Level		70%			V_{DD}
Logic '0' Input Level				30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0		1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD}-0.4			V
Output Logic '0' Level (I_{OL} = 360µA)				0.4	V
Output 'off' State Current (V_{OUT} = V_{DD})				1.0	µA
FSK Demodulator					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1280	1300	1320	Hz
Space (Logical 0) Frequency		2068	2100	2132	Hz
Valid Input Level Range	3	-40.0		-8.0	dBV
Acceptable Twist (Mark Level WRT Space Level)		-7.0		7.0	dB
Acceptable Signal to Noise Ratio	4	20.0			dB
Level Detector 'On' Threshold Level	3			-40.0	dBV
Level Detector 'Off' to 'On' Time (Figure 4 Te_{ON})				25.0	ms
Level Detector 'On' to 'Off' Time (Figure 4 Te_{OFF})		8.0			ms
FSK Retiming					
Acceptable Rx Data Rate		1188	1200	1212	Baud
Tx Data Rate		1194		1206	Baud
FSK Modulator					
TXOUT Level	5	-1.0	0	1.0	dB
Twist (Mark Level WRT Space Level)		-2.0	0	2.0	dB
1200bps (M1='0', M0='1').					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1297		1303	Hz
Space (Logical 0) Frequency		2097		2103	Hz
75bps (M1='0', M0='0').					
Bit Rate		0	75	76	Baud
Mark (Logical 1) Frequency		388		392	Hz
Space (Logical 0) Frequency		448		452	Hz

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	Notes	Min.	Typ.	Max.	Units
Input Amplifier					
Impedance (RXIN Pin)	6	10.0			MΩ
Voltage Gain	6		500		V/V
XTAL/CLOCK Input					
'High' Pulse Width	7	100			ns
'Low' Pulse Width	7	100			ns

Operating Characteristics Notes:

1. Not including any current drawn from the MX604 pins by external circuitry other than X1, C1 and C2.
2. TXD, RXEQ and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Measured at the Rx Input Amplifier output (pin RXAMPOUT) for 1300Hz and V_{DD}= 5.0V. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1
4. Flat noise in 300-3400Hz band.
5. Relative to 775mV_{RMS} with V_{DD}= 5.0V for load resistance greater than 40kΩ.
6. Open loop, small signal low frequency measurements.
7. Timing for an external input to the XTAL/CLOCK pin.

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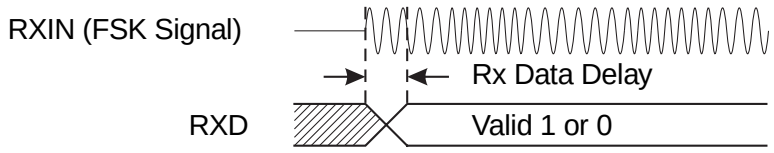
6.2 Timing

Data and Mode Timing	Notes	Min.	Typ.	Max.	Units
Rx Data Delay (RXIN to RXD)	1, 5		2.55		ms
Tx Delay Data (TXD to TXOUT)	1, 6		0.1		ms
Mode change delay ZP to Tx or Rx	2			20	ms
Mode change delay Tx1200 to Rx1200	2			4.0	ms
Mode change delay Rx1200 to Tx1200	2			0.2	ms
t_D = Internal MX604 delay	3, 4			1	µs
tc_{HI} = CLK High time	3, 4	1			µs
tc_{LO} = CLK low time	3	1			µs
t_R = RDY low to CLK going low	4			800	µs
t_S = Data Set-up time	4	1			µs
t_H = Data Hold time	4	1			µs

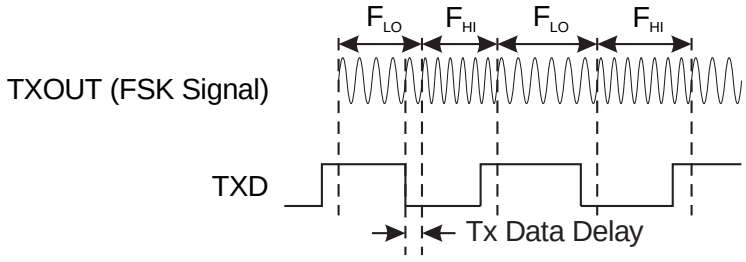
Timing Notes

1. When data retiming is not enabled.
2. Delay from mode change to reliable data at TXOUT or RXD pins.
3. Reference Figure 7.
4. Reference Figure 9.
5. Reference Figure 12.
6. Reference Figure 13.



Note: M0 and M1 are preset and stable.

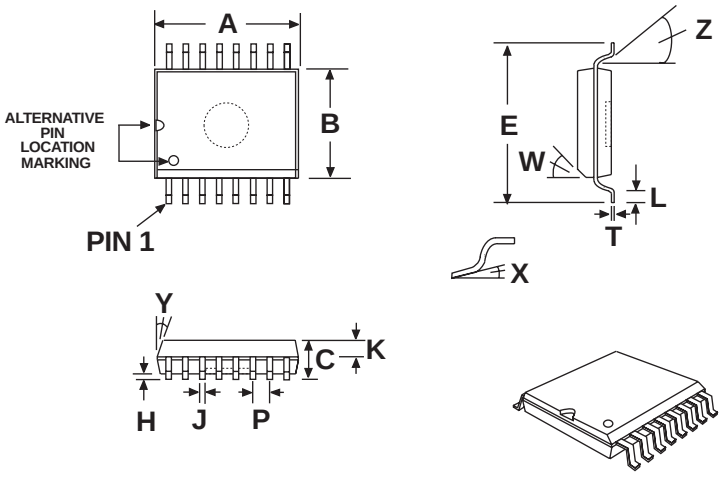
Figure 12: RXIN to RXD Delay time



Note: M0 and M1 are preset and stable. F_{LO} and F_{HI} are the two FSK signaling frequencies.

Figure 13: TXD to TXOUT Delay time

6.3 Packaging

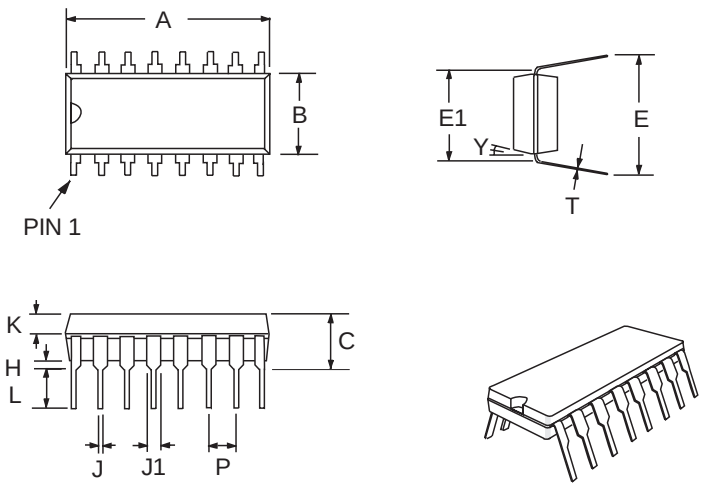


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 16-pin SOIC Mechanical Outline: *Order as part no. MX604DW*

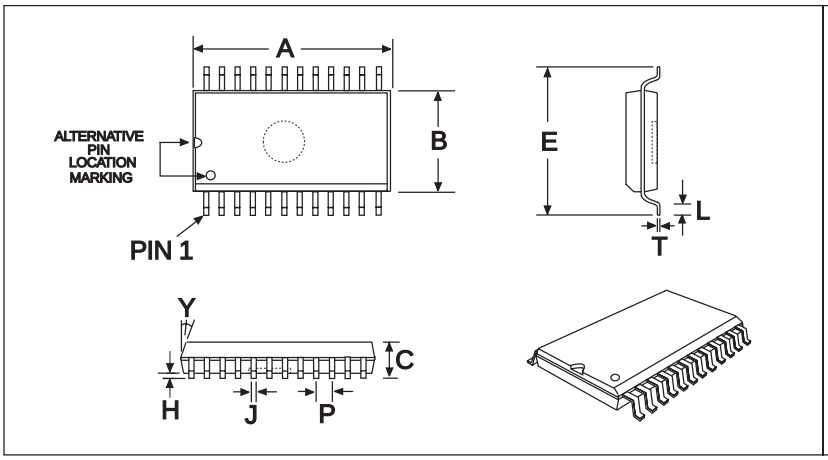


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE: All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 16-pin PDIP Mechanical Outline: *Order as part no. MX604P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin TSSOP Mechanical outline: *Order as part no. MX604TN*

