

MSM514256RS/JS/ZS**262,144-WORD × 4-BITS DYNAMIC RAM****GENERAL DESCRIPTION**

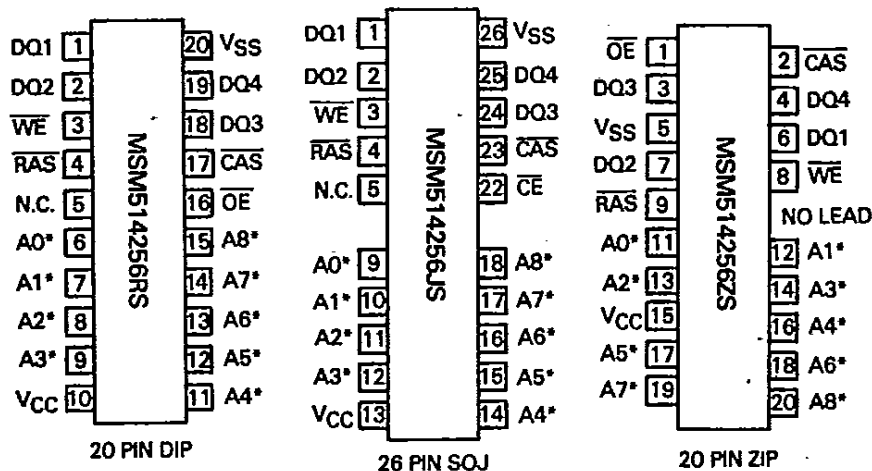
The MSM514256 is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM514256 is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514256-10	100 ns	190 ns	413 mW	5.5 mW
MSM514256-12	120 ns	220 ns	385 mW	

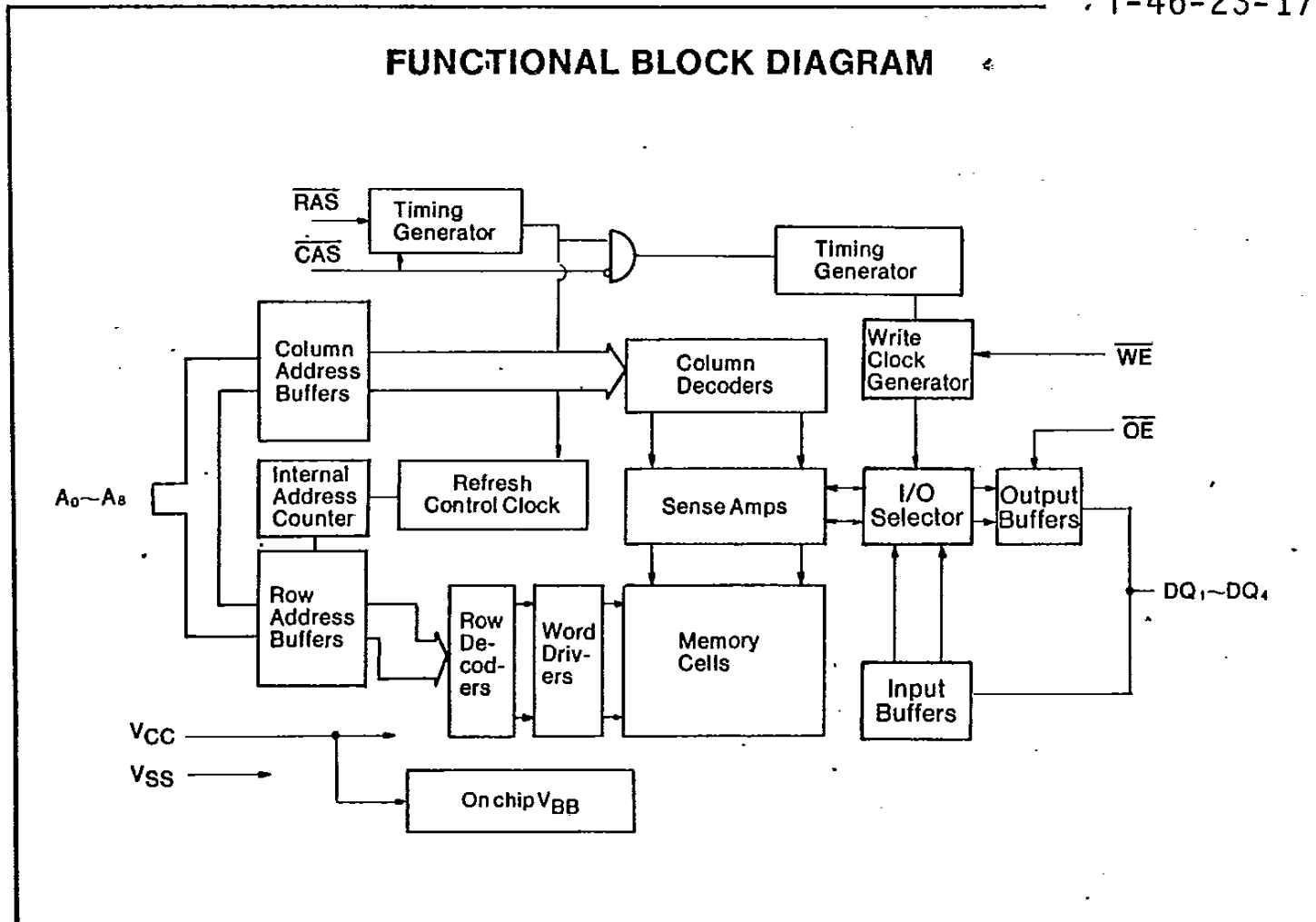
- Single +5V supply, $\pm 10\%$ tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and OE operations
- Fast page mode, read/write capability
- CAS before RAS refresh, CAS before RAS hidden refresh, RAS only refresh capability
- "Gated" CAS
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)

Pin Names	Function
A0 to A8	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
VCC	Power Supply (+5V)
VSS	Ground (0V)
N.C.	No Connection

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	$T_a = 25^\circ\text{C}$	-1.0 to +7.0	V
Short circuit output current	I_{OS}	$T_a = 25^\circ\text{C}$	50	mA
Power dissipation	P_D	$T_a = 25^\circ\text{C}$	1	W
Operating temperature	T_{opr}	—	0 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

($T_a = 0$ to $+70^\circ$)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	—	4.5	5.0	5.5	V
	V_{SS}	—	0	0	0	V
Input high voltage	V_{IH}	—	2.4	—	6.5	V
Input low voltage	V_{IL}	—	-1.0	—	0.8	V

DC CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$)

Parameter	Symbol	Conditions	MSM 514256-10		MSM 514256-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	$I_{OH} = -5.0$ mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	$I_{OL} = 4.2$ mA	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	$0V \leq V_I \leq 6.5V$; all other pins not under test = 0V	-10	10	-10	10	μA	
Output leakage current	I_{LO}	DOUT disable $0V \leq V_O \leq 5.5V$	-10	10	-10	10	μA	
Average power supply current* (Operating)	I_{CC1}	\overline{RAS} , \overline{CAS} cycling, $t_{RC} = \min$	-	75	-	70	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IH}$ DOUT = HZ	TTL	-	2	-	2	mA
		MOS	-	1	-	1		
Average power supply current* (\overline{RAS} only refresh)	I_{CC3}	\overline{RAS} cycling, $\overline{CAS} = V_{IH}$ $t_{RC} = \min$	-	75	-	70	mA	
Average power supply current* (\overline{CAS} before \overline{RAS} refresh)	I_{CC6}	\overline{RAS} cycling, \overline{CAS} before \overline{RAS}	-	75	-	70	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS} = V_{IL}$, \overline{CAS} cycling $t_{PC} = \min$	-	55	-	50	mA	

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

($T_a = 25^\circ C$, $f = 1$ MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	-	-	6	pF
Input capacitance (\overline{RAS} , \overline{CAS} , \overline{WE})	C_{IN2}	-	-	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	-	-	7	pF

(V_{CC} = 5V ±10%, T_a = 0 to +70°C)

Note 1, 2, 3

Parameter	Symbol	MSM514256-10		MSM514256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t _{REF}	—	8	—	8	ms	
Random read or write cycle time	t _{RC}	190	—	220	—	ns	
Read/write cycle time	t _{RWC}	255	—	295	—	ns	
Fast page mode cycle time	t _{PC}	55	—	70	—	ns	
Fast page mode read/write cycle time	t _{PRMW}	120	—	140	—	ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}	—	100	—	120	ns	4, 5, 6
Access time from $\overline{\text{CAS}}$	t _{CAC}	—	35	—	45	ns	4, 5
Access time from column address	t _{AA}	—	50	—	60	ns	4, 6
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	50	—	65	ns	4
Output low impedance time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	ns	4
Output buffer turn-off delay	t _{OFF}	0	25	0	30	ns	
Transition time	t _T	3	50	3	50	ns	3
$\overline{\text{RAS}}$ precharge time	t _{RP}	80	—	90	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	100	10000	120	10000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	35	—	45	—	ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode cycle only)	t _{CP}	10	—	15	—	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	35	10000	45	10000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	100	—	120	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	25	65	25	75	ns	5
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	20	50	20	60	ns	6
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	ns	
$\overline{\text{Row}}$ address set-up time	t _{ASR}	0	—	0	—	ns	
$\overline{\text{Row}}$ address hold time	t _{RAH}	15	—	15	—	ns	
Column address set-up time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	20	—	25	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t _{AR}	75	—	90	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	50	—	60	—	ns	

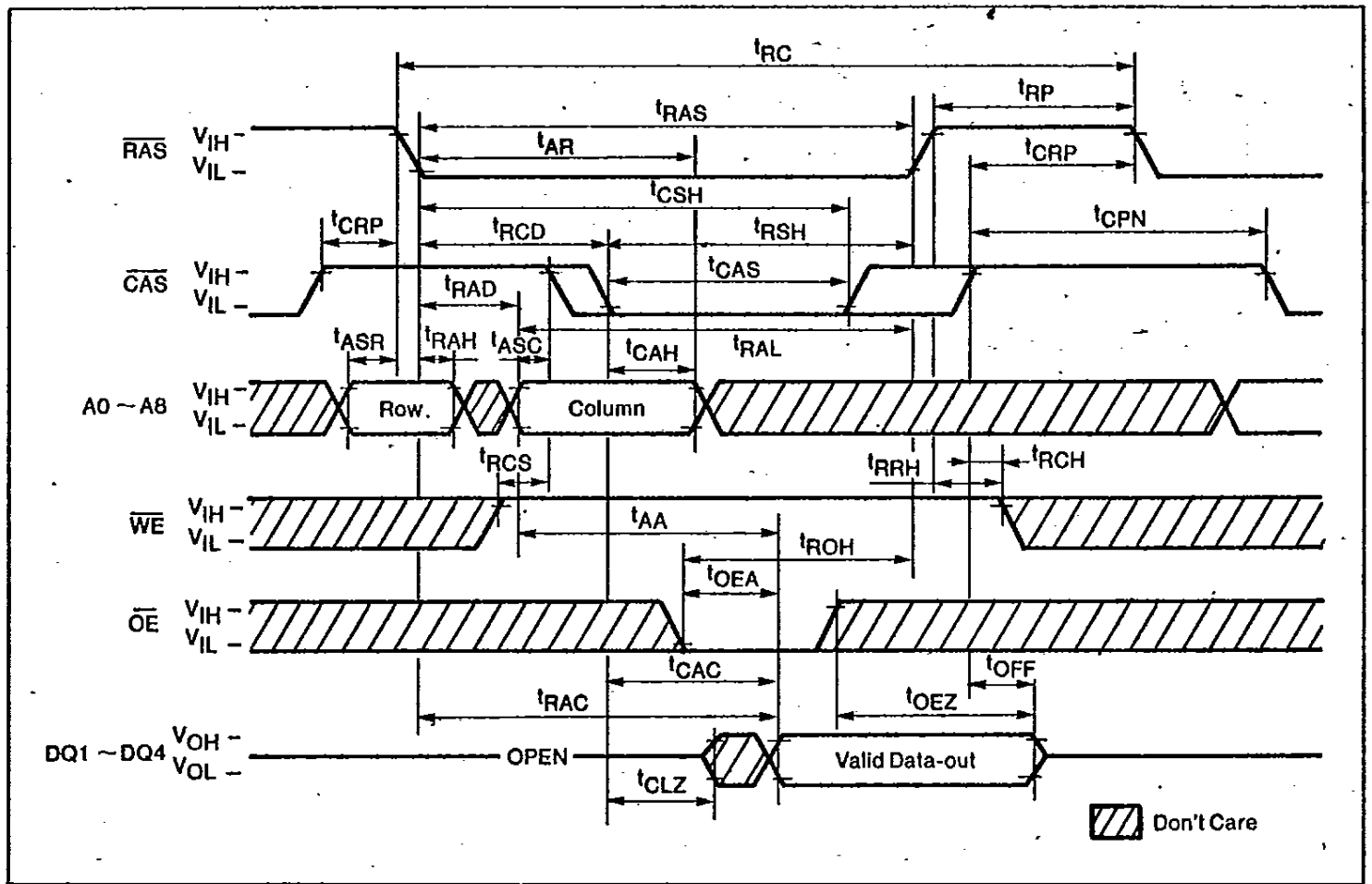
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514256-10		MSM514256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	8
Write command hold time from \overline{RAS}	t_{WCR}	75	—	90	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	ns	7
Write command hold time	t_{WCH}	20	—	25	—	ns	
Write command pulse width	t_{WP}	20	—	25	—	ns	
Write command to \overline{RAS} lead time	t_{RWL}	25	—	30	—	ns	
Write command to \overline{CAS} lead time	t_{CWL}	25	—	30	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	ns	
Data-in hold time	t_{DH}	20	—	25	—	ns	
Data-in hold time from \overline{RAS}	t_{DHR}	75	—	90	—	ns	
\overline{CAS} to \overline{WE} delay	t_{CWD}	70	—	85	—	ns	7
\overline{RAS} to \overline{WE} delay	t_{RWD}	135	—	160	—	ns	7
Column address to \overline{WE} delay time	t_{AWD}	85	—	100	—	ns	7
Read command hold time reference to \overline{RAS}	t_{RRH}	10	—	10	—	ns	8
\overline{RAS} to \overline{CAS} set-up time (CAS before \overline{RAS})	t_{CSR}	10	—	10	—	ns	
\overline{RAS} to \overline{CAS} hold time (CAS before \overline{RAS})	t_{CHR}	30	—	30	—	ns	
\overline{CAS} active delay from \overline{RAS} precharge	t_{RPC}	10	—	10	—	ns	
\overline{CAS} precharge time (Refresh counter test)	t_{CPT}	50	—	60	—	ns	
\overline{CAS} precharge time	t_{CPN}	15	—	20	—	ns	
\overline{RAS} hold time reference to \overline{OE}	t_{ROH}	20	—	20	—	ns	
Access time from \overline{OE}	t_{OEA}	—	25	—	30	ns	
\overline{OE} delay time	t_{OED}	25	—	30	—	ns	
\overline{OE} to data output buffer turn-off delay	t_{OEZ}	0	25	0	30	ns	
\overline{OE} command hold time	t_{OEH}	25	—	30	—	ns	

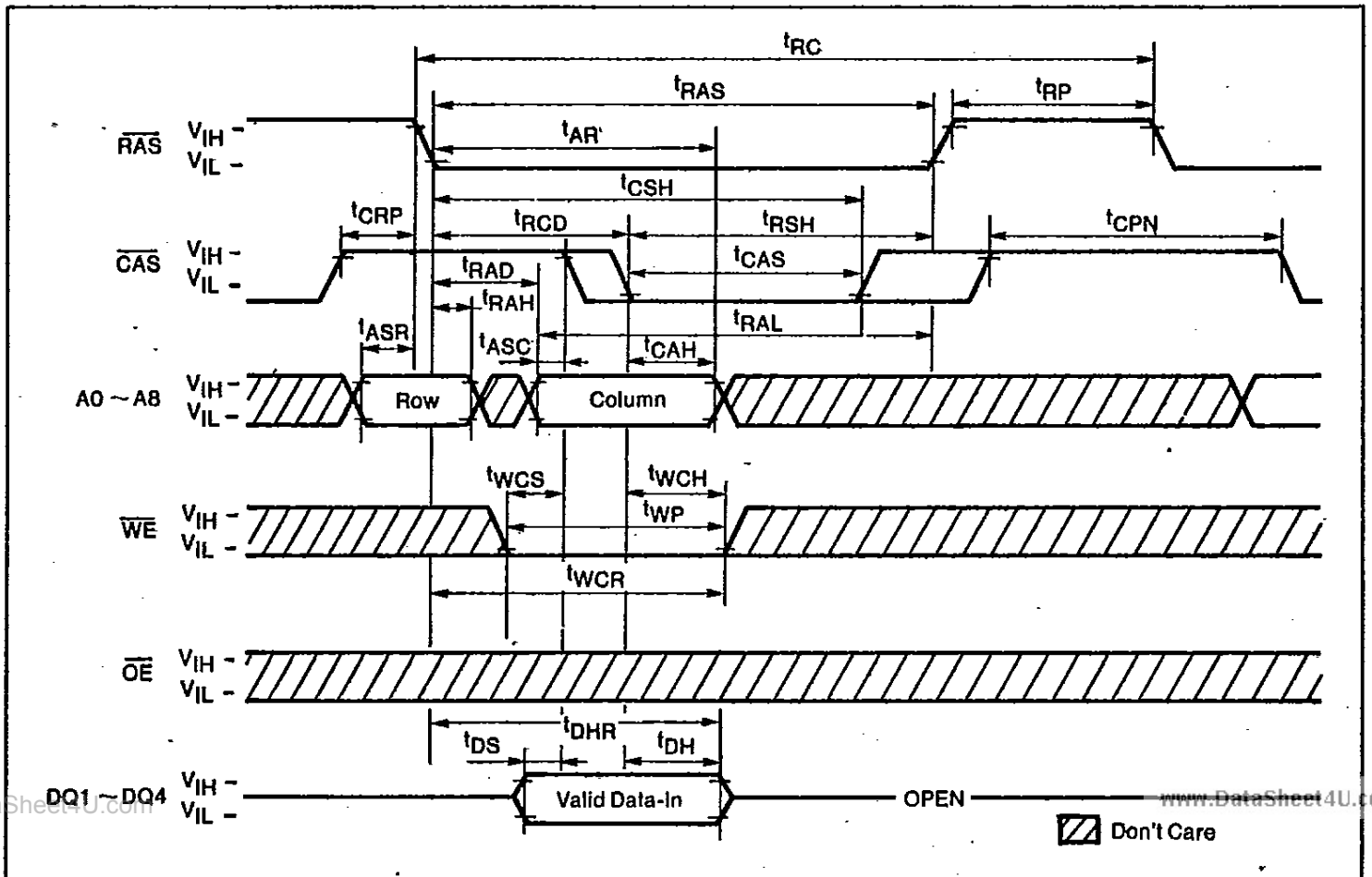
- Notes:**
- 1 An initial pause of 100 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles (Example: $\overline{\text{RAS}}$ only) before proper device operation is achieved.
 - 2 The AC characteristics assume at $t_T = 5$ ns.
 - 3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - 4 Measured with a load circuit equivalent to 2TTL + 100 pF.
 - 5 Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC} .
 - 6 Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA} .
 - 7 t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), $t_{RWD} \geq t_{RWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
 - 8 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

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READ CYCLE

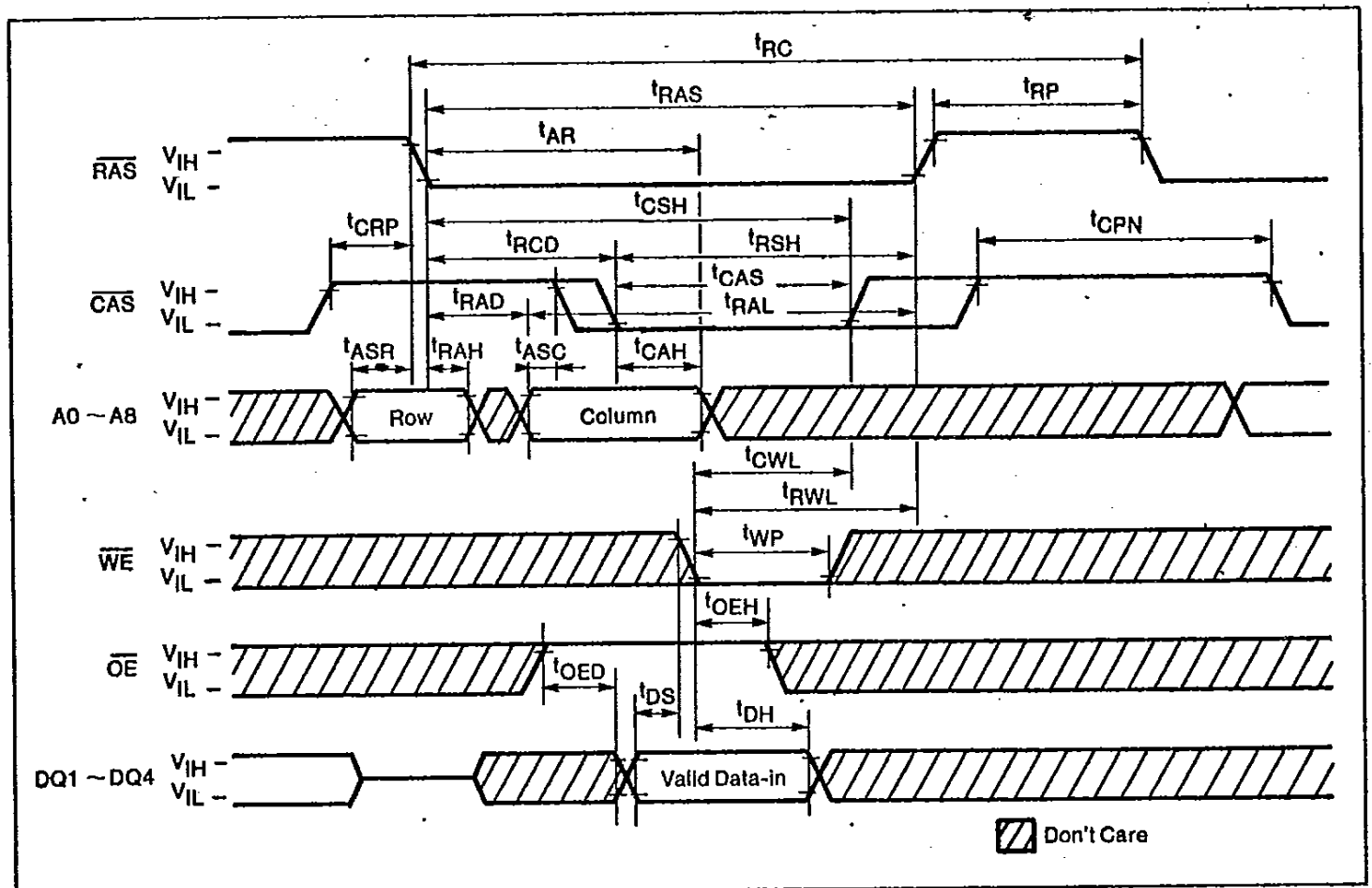


WRITE CYCLE (EARLY WRITE)



WRITE CYCLE (\overline{OE} CONTROL WRITE)

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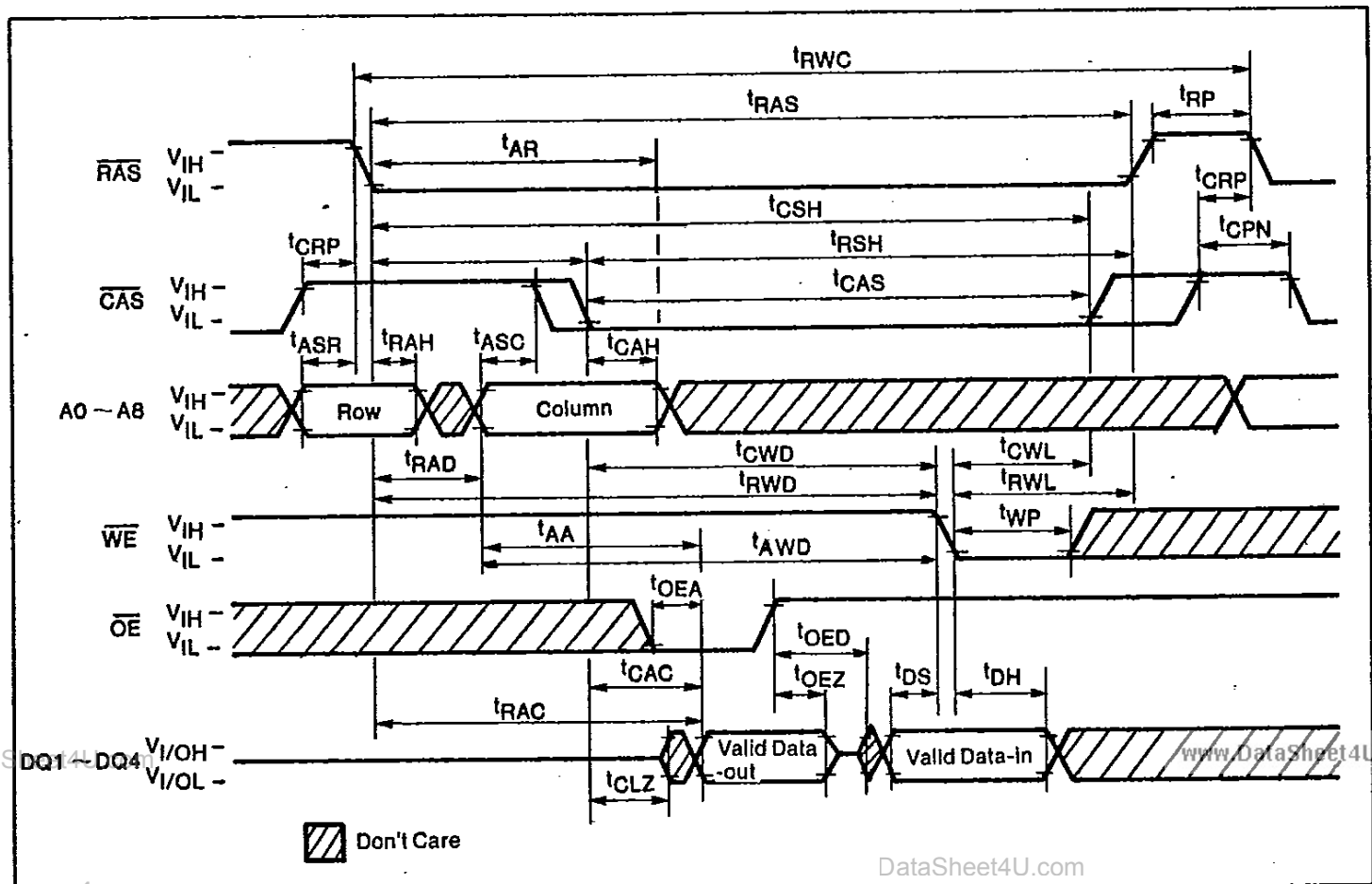


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READ/WRITE CYCLE



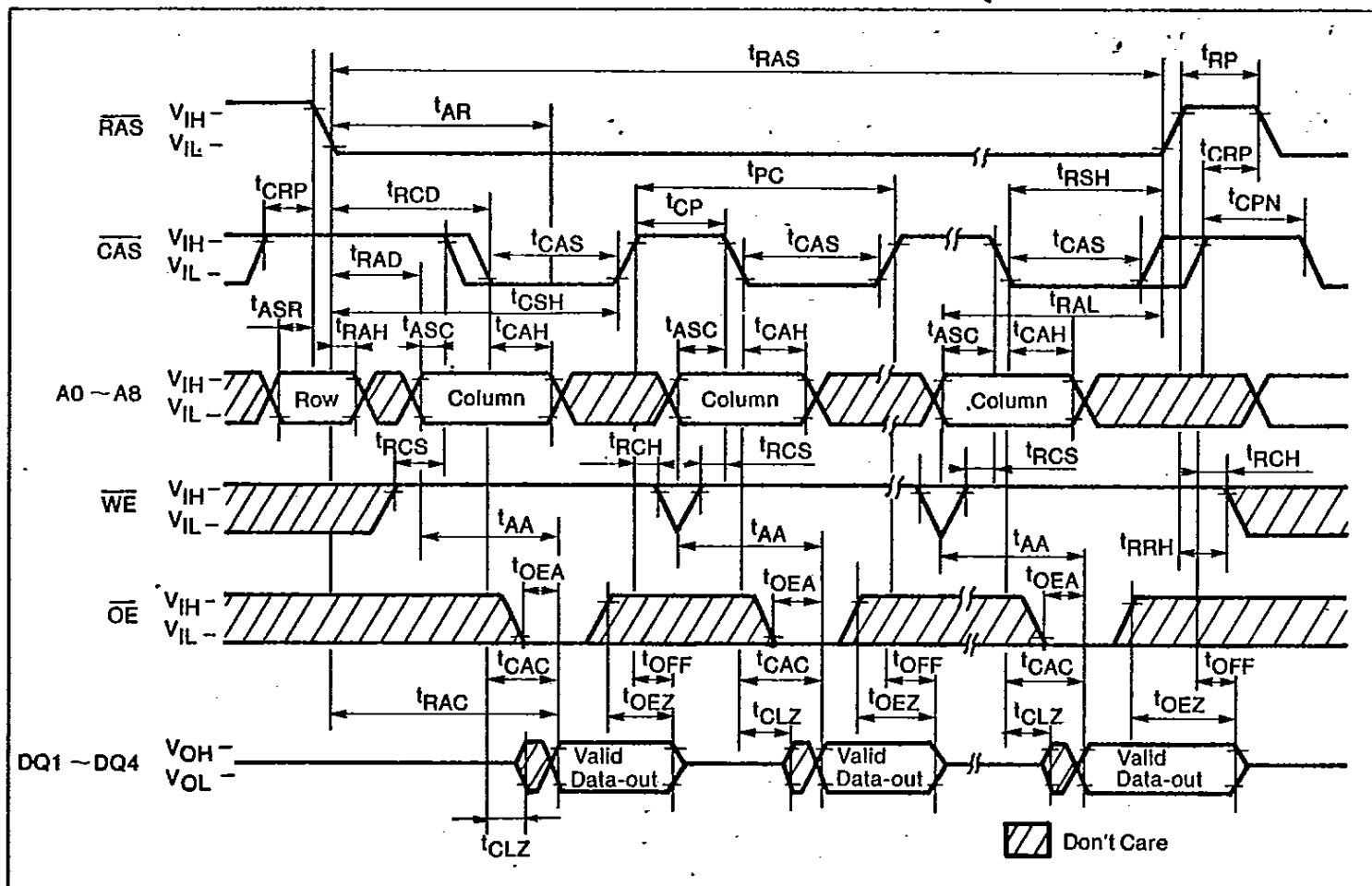
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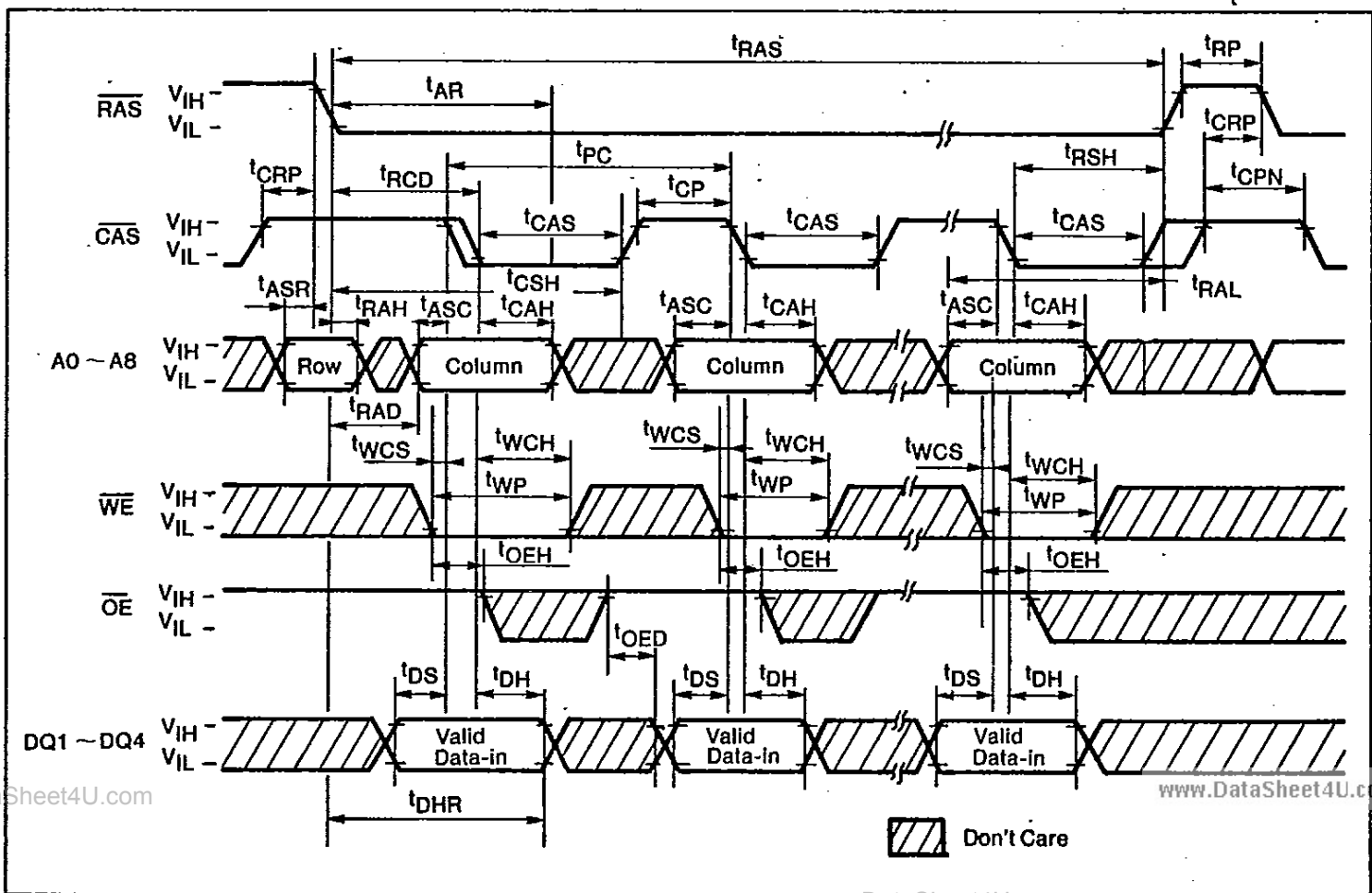
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FAST PAGE MODE READ CYCLE

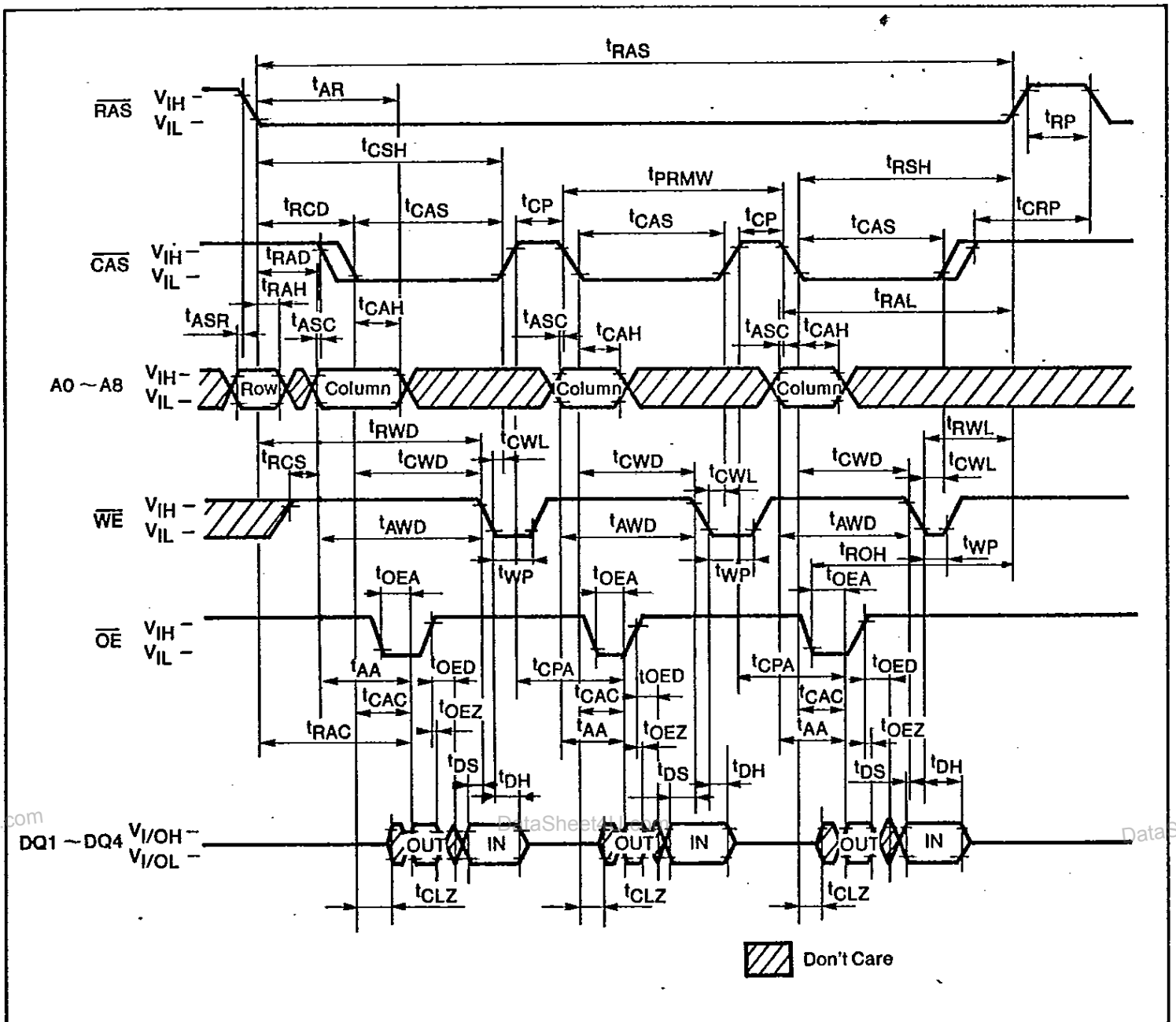


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

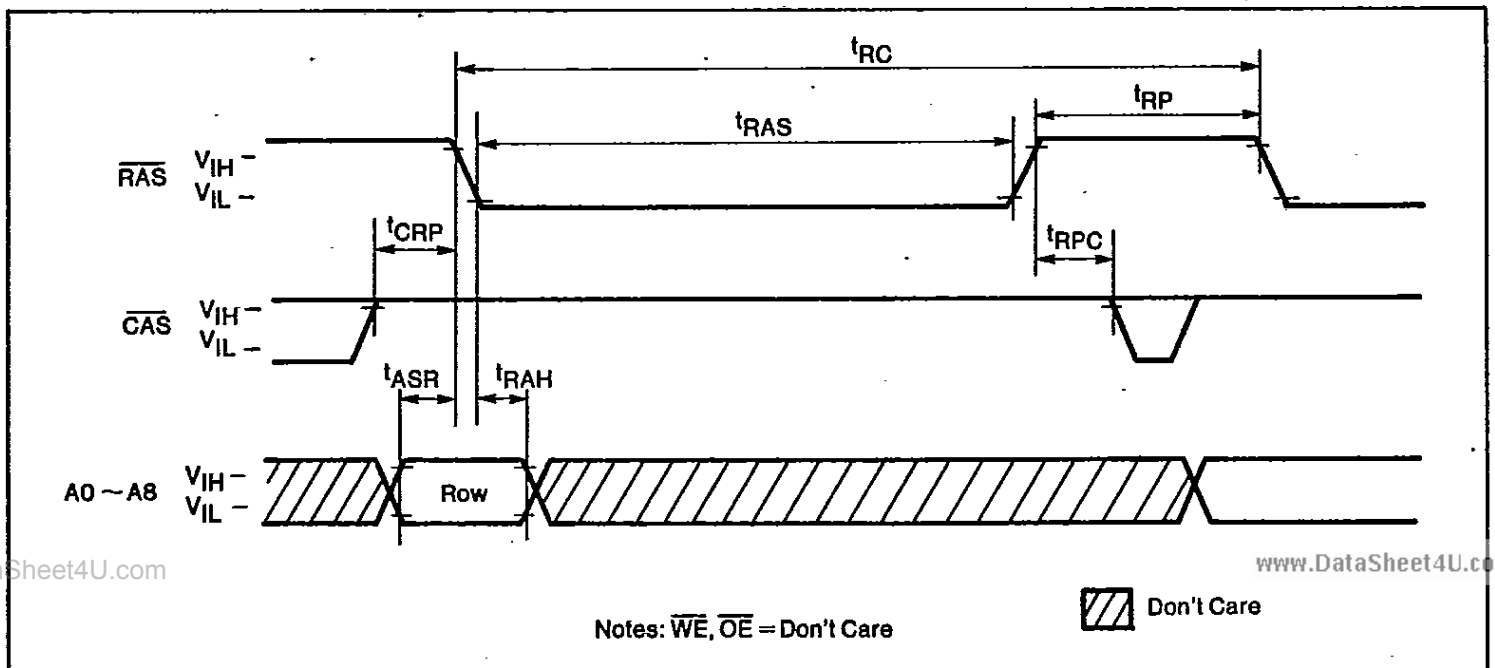


FAST PAGE MODE READ/WRITE CYCLE

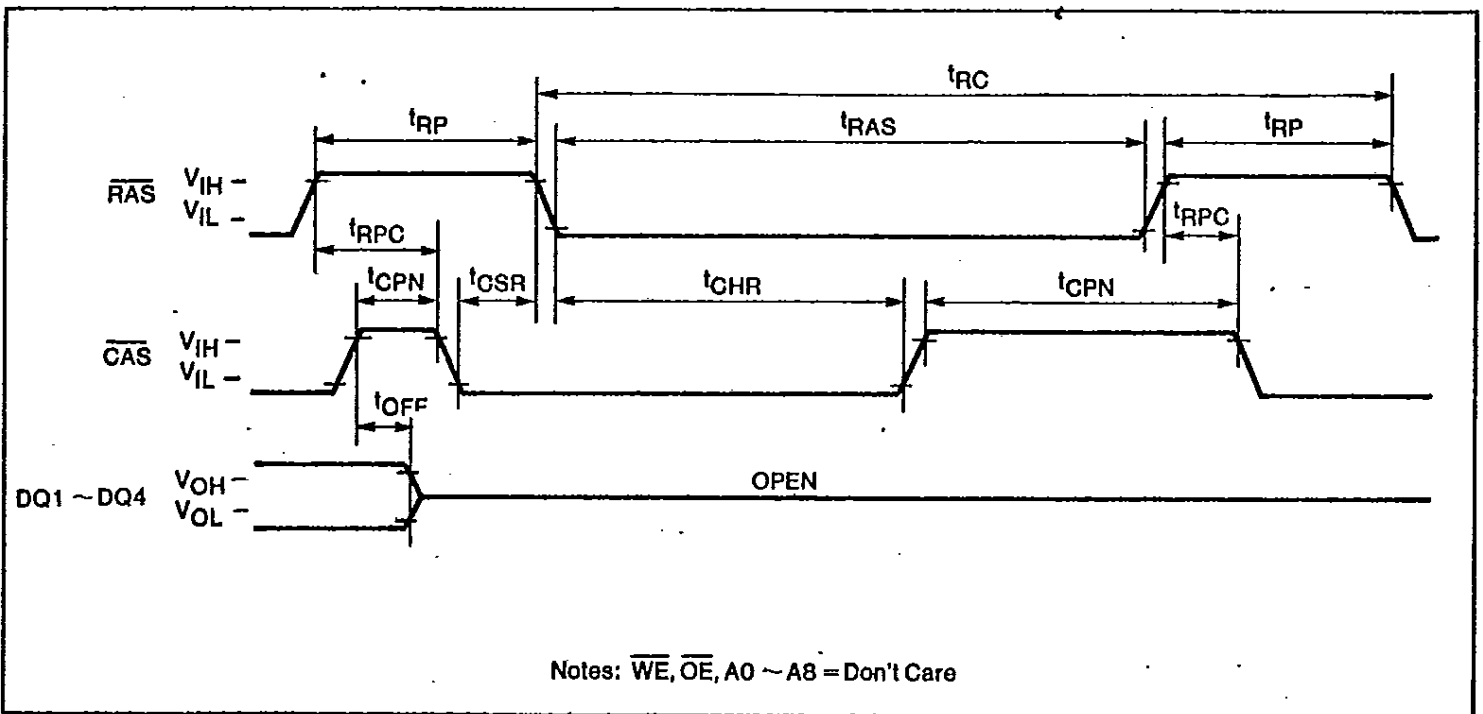
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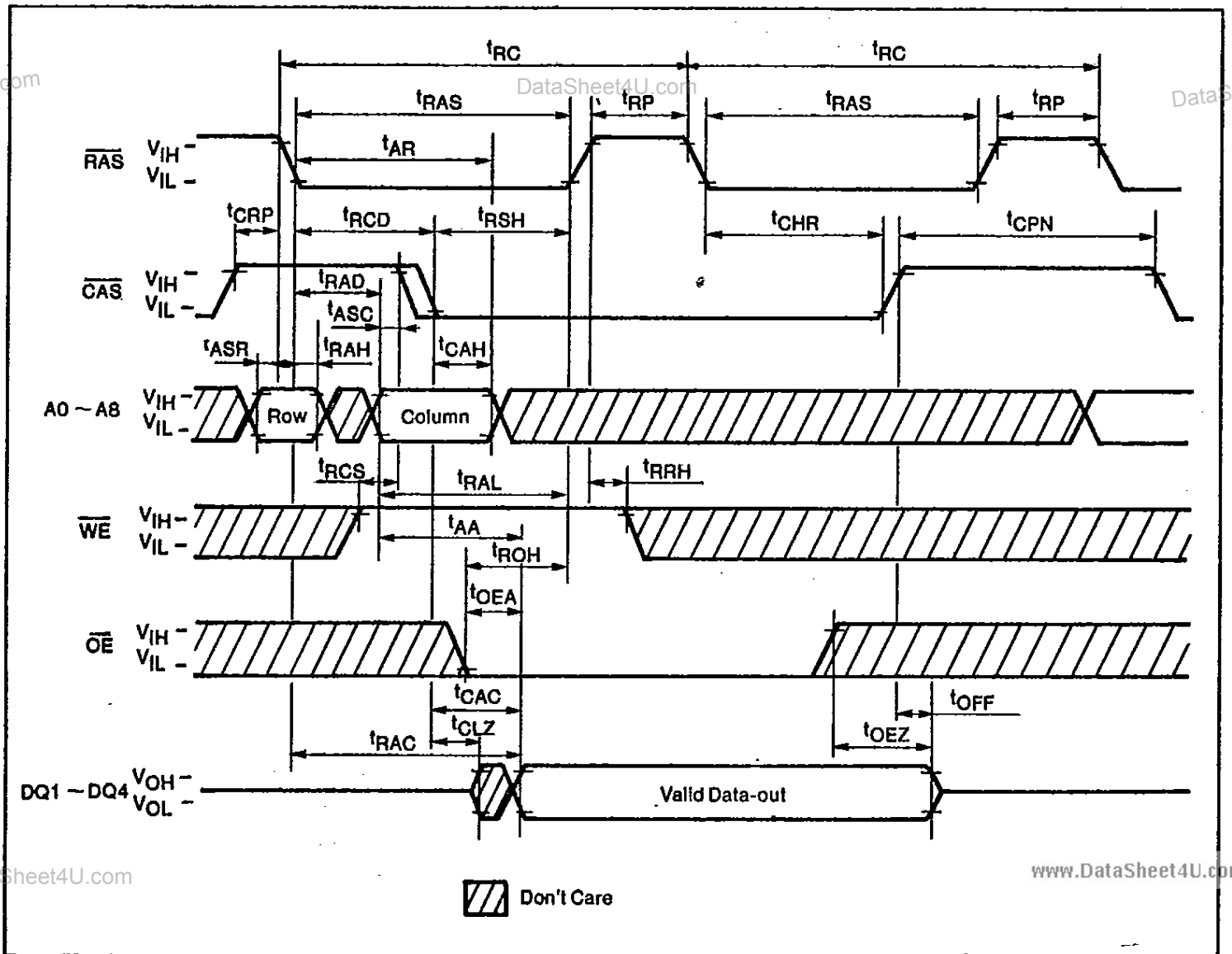
RAS ONLY REFRESH CYCLE

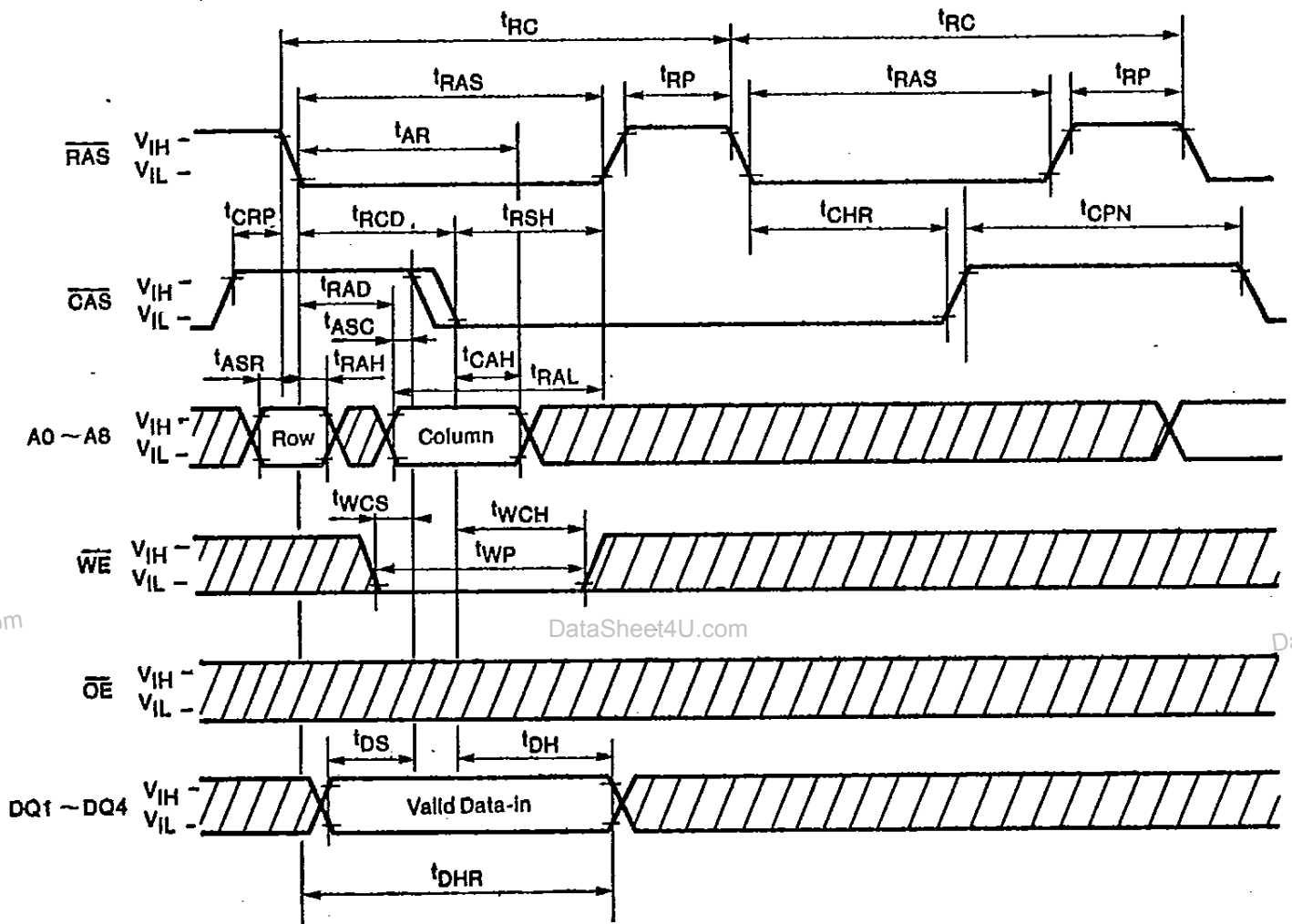


CAS BEFORE RAS AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE





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CAS BEFORE RAS REFRESH COUNTER TEST

