FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12602-1E

8-bit Proprietary Microcontrollers

CMOS

F²MC-8FX MB95110A Series

MB95116A/F118AS/F118AW/FV100A-101

■ DESCRIPTION

The MB95110A series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

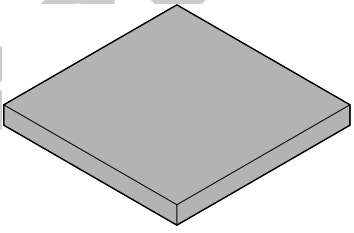
■ FEATURES

- F²MC-8FX CPU core
  Instruction set that is optimum to the controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operation
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Subclock (for dual clock product)
  - Sub PLL clock (for dual clock product)

(Continued)

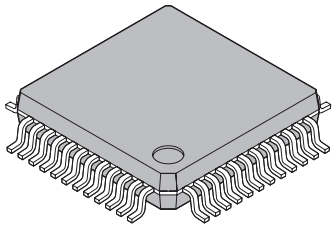
■ PACKAGES

48-pin plastic BCC



(LCC-48P-M09)

48-pin plastic-LQFP



(FPT-48P-M26)

FUJITSU

(Continued)

- Timer
  - 8/16-bit compound timer × 2 channels
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG
  - Timebase timer
  - Watch prescaler (for dual clock product)
- LIN-UART
  - Full duplex double buffer
  - Clock asynchronous or synchronous serial transfer capable
- UART/SIO
  - Clock asynchronous or synchronous serial transfer capable
- I^2C*
  - Built-in wake-up function
- External interrupt
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption modes.
- 10-bit A/D converter
  - 10-bit resolution
- Low-power consumption (standby mode)
  - Stop mode
  - Sleep mode
  - Watch mode (for dual clock product)
  - Timebase timer mode
- I/O port: Max 40
  - General-purpose I/O ports (Nch open drain) : 2 ports
  - General-purpose I/O ports (CMOS) : 38 ports

* : Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent Rights to use, these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

■ PRODUCT LINEUP

Parameter \ Part number		MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
Type		MASK product	FLASH product		EVA product
ROM capacity		32 Kbytes	60 Kbytes		
RAM capacity		1 Kbytes	2 Kbytes		3.75 Kbytes
Reset output		No			
Option		Selectable single/dual -system*2	Single-system	Dual-system	Selectable single/dual -system*1
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 0.1 µs (at internal 10 MHz) Interrupt processing time : 0.9 µs (at internal 10 MHz)			
Peripheral functions	Ports (Max 40 ports)	General-purpose I/O port (Nch open drain) : 2 ports General-purpose I/O port (CMOS) : 38 ports			
	Timebase timer	Interrupt cycle : 0.5 ms, 2.05 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)			
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Minimum 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Minimum 250 ms			
	Wild register	Capable of replacing 3 bytes of data			
	I^2C bus	Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function			
	UART/SIO	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator Transfer rate : 2400 bps to 125000 bps (at machine clock 10 MHz) NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock synchronous (SIO) or clock asynchronous (UART) data transfer capable			
	LIN-UART	Dedicated reload timer allowing a wide range of communication speeds to be set. Capable of data transfer synchronous or asynchronous to clock signal. LIN functions available as the LIN master or LIN slave.			
	A/D converter (8 channels)	8-bit or 10-bit resolution can be selected.			
	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as “8-bit timer × 2 channels” or “16-bit timer × 1 channel”. Built-in timer function, PWC function, PWM function, capture function and square waveform output Count clock : 7 internal clocks and external clock can be selected.			

(Continued)

(Continued)

Parameter \ Part number		MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
Peripheral functions	16-bit PPG	PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start			
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”. Counter operating clock : Eight selectable clock sources			
	Watch counter (for dual clock product)	Count clock : Four selectable clock sources (125ms, 250ms, 500ms, or 1s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute)			
	Watch prescaler (for dual clock product)	Four selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)			
	External interrupt (8 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected) Can be used to recover from standby modes.			
Standby mode		Sleep, stop, watch, and timebase timer			

*1 : Change by the switch on MCU board.

*2 : Specify clock mode when ordering MASK ROM.

■ SELECT OF OSCILLATION STABILIZATION WAIT TIME (MASK PRODUCT ONLY)

For the MASK product, you can set the mask option when ordering MASK ROM to select the initial value of main clock oscillation stabilization wait time from among the following four values.

Note that the EVA and FLASH products are fixed their initial value of main clock oscillation stabilization wait time at the maximum value.

Selection of oscillation stabilization wait time	Remarks
$(2^2 - 2) /F_{CH}$	0.5 µs (at main oscillation clock 4 MHz)
$(2^{12} - 2) /F_{CH}$	Approx. 1.02 ms (at main oscillation clock 4 MHz)
$(2^{13} - 2) /F_{CH}$	Approx. 2.05 ms (at main oscillation clock 4 MHz)
$(2^{14} - 2) /F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
LCC-48P-M09	○	○	○	×
FPT-48P-M26	○	○	○	×
BGA-224P-M08	×	×	×	○

○ : Available
× : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

- Notes on Using EVA Products

  The EVA product has not only the functions of the MB95110A series but also those of other products to support software development for multiple series and products of F^2MC-8FX family. The I/O addresses for peripheral resources not used by the MB95110A series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

  Take particular care not to use word, long word, or similar access to read or write odd numbered bytes in the prohibited areas.

  Note that the values read from barred addresses are different between the EVA product and the FLASH or MASK product. Therefore, the data must not be used for software processing.

  The EVA product does not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. Since the EVA, FLASH, and MASK products are designed to behave completely the same way in terms of hardware and software, you do not have to pay special attention to specific products.

- Difference of Memory Spaces

  If the amount of memory on the EVA product is different from that of the FLASH or MASK product, carefully check the difference in the amount of memory from the product to be actually used when developing software.

- Current Consumption
  - The current consumption of FLASH product is typically greater than for MASK product.
  - For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

- Package

  For details of information on each package, see “■ PACKAGE DIMENSIONS”.

- Operating voltage

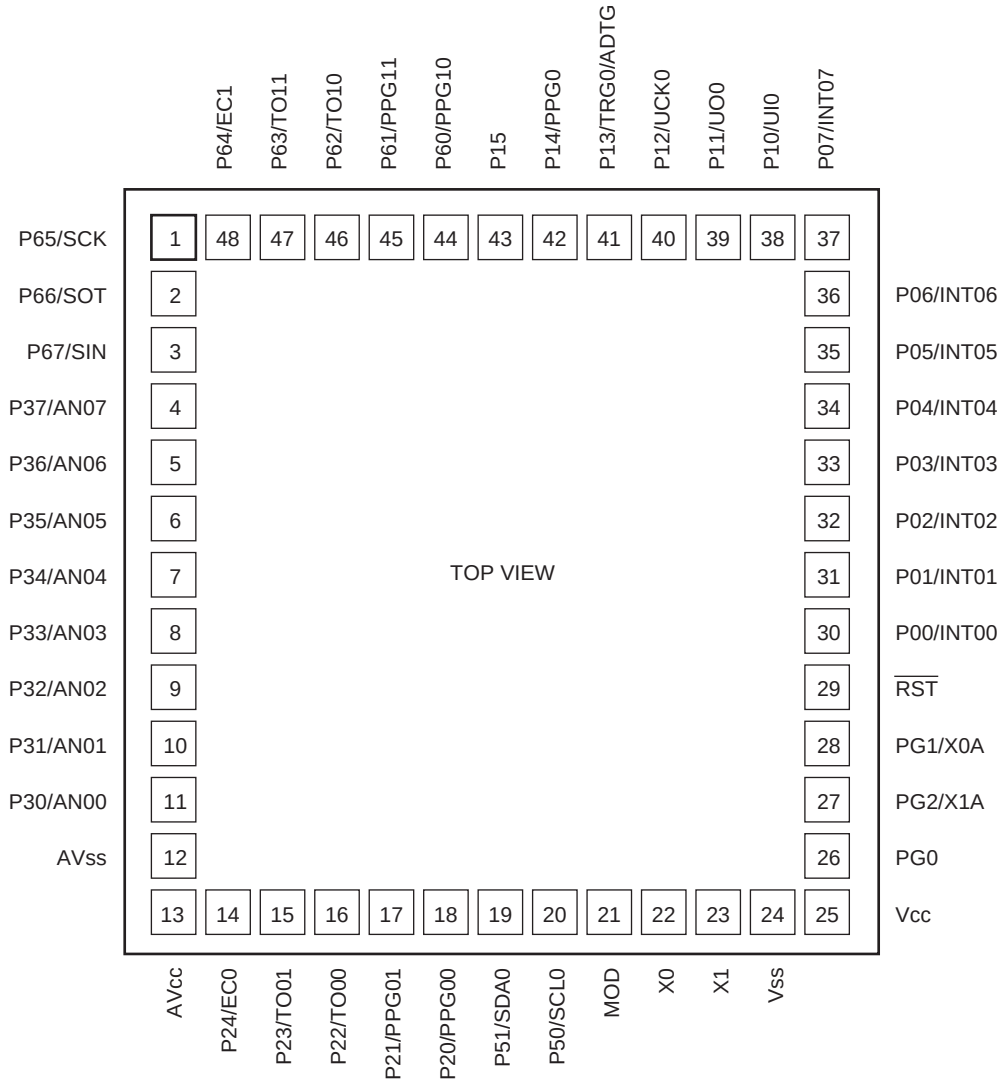
  The operating voltage are different among the EVA, FLASH and MASK products.

  For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”

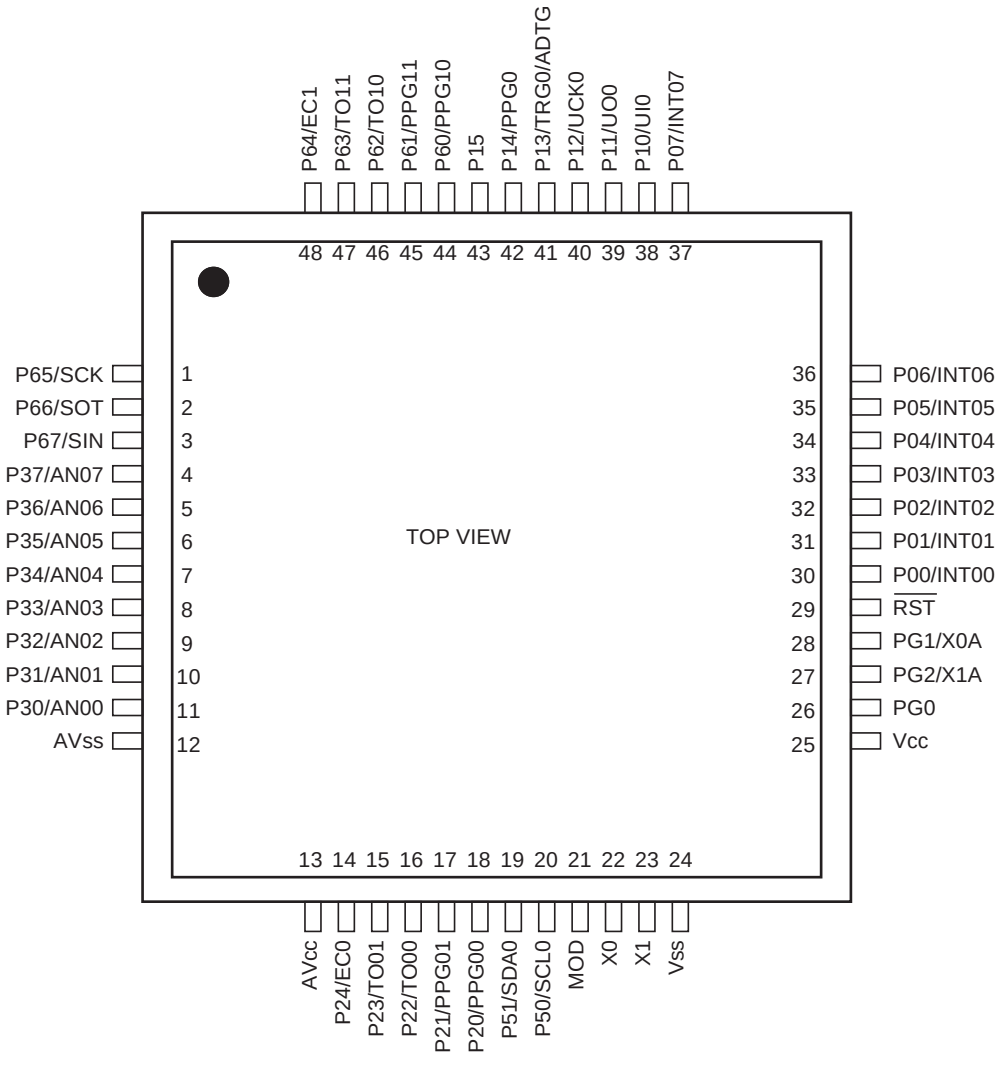
- Difference between $\overline{\text{RST}}$ and MOD pins

  The $\overline{\text{RST}}$ and MOD pins are hysteresis inputs on the MASK product. A pull-down resistor is provided for the MOD pin of the MASK product.

■ PIN ASSIGNMENTS



(LCC-48P-M09)


P64/EC1
P63/TO11
P62/TO10
P61/PPG11
P60/PPG10
P15
P14/PPG0
P13/TRG0/ADTG
P12/UCK0
P11/UO0
P10/UI0
P07/INT07
48 47 46 45 44 43 42 41 40 39 38 37
P65/SCK 1
P66/SOT 2
P67/SIN 3
P37/AN07 4
P36/AN06 5
P35/AN05 6
P34/AN04 7
P33/AN03 8
P32/AN02 9
P31/AN01 10
P30/AN00 11
AVss 12
TOP VIEW
36 P06/INT06
35 P05/INT05
34 P04/INT04
33 P03/INT03
32 P02/INT02
31 P01/INT01
30 P00/INT00
29 RST
28 PG1/X0A
27 PG2/X1A
26 PG0
25 Vcc
13 14 15 16 17 18 19 20 21 22 23 24
AVcc
P24/EC0
P23/TO01
P22/TO00
P21/PPG01
P20/PPG00
P51/SDA0
P50/SCL0
MOD
X0
X1
Vss

(FPT-48P-M26)

■ PIN DESCRIPTION

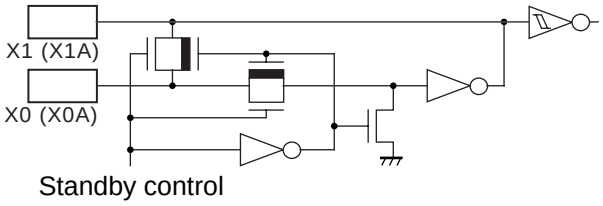
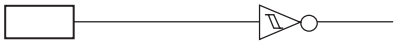
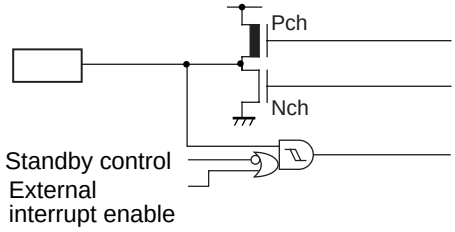
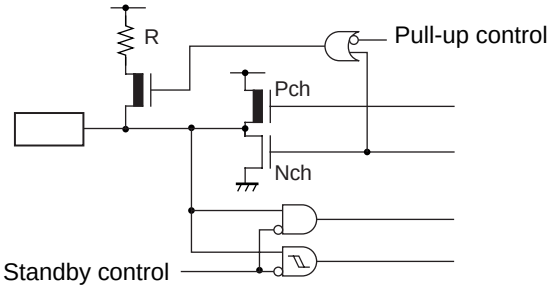
Pin no.	Pin name	Circuit type	Description
1	P65/SCK	K	General-purpose I/O port. The pin is shared with LIN-UART clock I/O.
2	P66/SOT		General-purpose I/O port. The pin is shared with LIN-UART data output.
3	P67/SIN	L	General-purpose I/O port. The pin is shared with LIN-UART data input.
4	P37/AN07	J	General-purpose I/O port. The pins are shared with A/D analog input.
5	P36/AN06		
6	P35/AN05		
7	P34/AN04		
8	P33/AN03		
9	P32/AN02		
10	P31/AN01		
11	P30/AN00		
12	AVss	—	A/D power supply pin (GND)
13	AVcc	—	A/D power supply pin
14	P24/EC0	H	General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch0 clock input.
15	P23/TO01		General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch0 output.
16	P22/TO00		
17	P21/PPG01		General-purpose I/O port. The pins are shared with 8/16-bit PPG ch0 output.
18	P20/PPG00		
19	P51/SDA0	I	General-purpose I/O port. The pin is shared with I^2C ch0 data I/O.
20	P50/SCL0		General-purpose I/O port. The pin is shared with I^2C ch0 clock I/O.
21	MOD	B	Operating mode designation pin
22	X0	A	Crystal oscillation pin
23	X1		
24	Vss	—	Power supply pin (GND)
25	Vcc	—	Power supply pin
26	PG0	H	General-purpose I/O port.
27	PG2/X1A	H/A	Single-system product is general-purpose port. Dual-system product is Crystal oscillation pin (32 kHz).
28	PG1/X0A		
29	$\overline{RST}$	B’	Reset pin

(Continued)

(Continued)

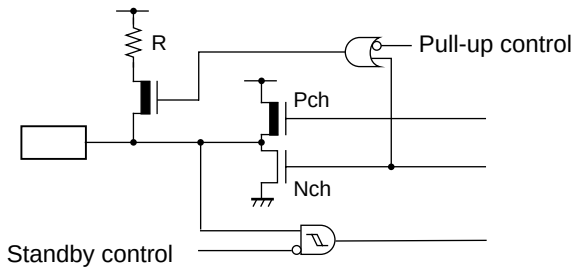
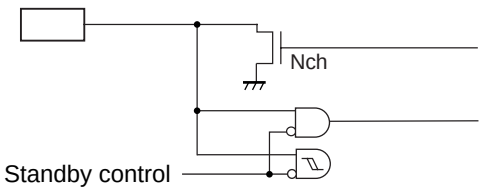
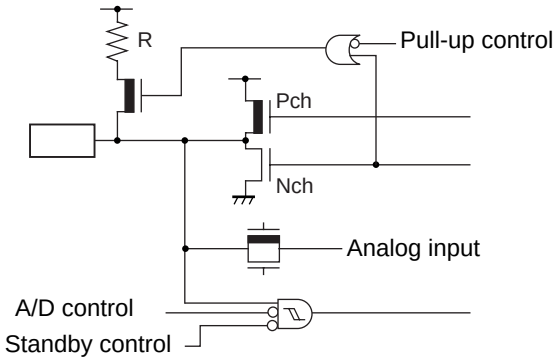
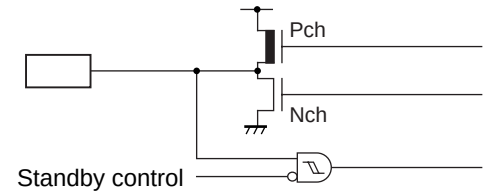
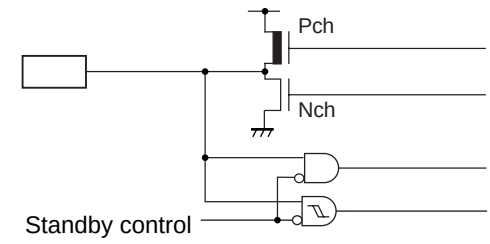
Pin no.	Pin name	Circuit type	Description
30	P00/INT00	C	General-purpose I/O port. The pins are shared with external interrupt input. Large current port.
31	P01/INT01		
32	P02/INT02		
33	P03/INT03		
34	P04/INT04		
35	P05/INT05		
36	P06/INT06		
37	P07/INT07		
38	P10/UI0	G	General-purpose I/O port. The pin is shared with UART/SIO ch0 data input.
39	P11/UO0	H	General-purpose I/O port. The pin is shared with UART/SIO ch0 data output.
40	P12/UCK0		General-purpose I/O port. The pin is shared with UART/SIO ch0 clock I/O.
41	P13/TRG0/ ADTG		General-purpose I/O port. The pin is shared with 16-bit PPG ch0 trigger input (TRG0) and A/D trigger input (ADTG).
42	P14/PPG0		General-purpose I/O port. The pin is shared with 16-bit PPG ch0 output.
43	P15		General-purpose I/O port.
44	P60/PPG10	K	General-purpose I/O port. The pins are shared with 8/16-bit PPG ch1 output.
45	P61/PPG11		
46	P62/TO10		General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch1 output.
47	P63/TO11		
48	P64/EC1		General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch1 clock input.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation circuit • High-speed side Feedback resistance value : approx. 1 MΩ • Low-speed side Feedback resistance : approx. 24 MΩ (EVA product : approx. 10 MΩ) Dumping resistance : approx. 144 kΩ (EVA product : without dumping resistance)
B		• Only for input • Hysteresis input only for MASK product • With pull-down resistor only for MASK product
B’		• Hysteresis input only for MASK product
C		• CMOS output • Hysteresis input
G		• CMOS output • CMOS input • Hysteresis input • With pull-up control

(Continued)

(Continued)

Type	Circuit	Remarks
H		• CMOS output • Hysteresis input • With pull-up control
I		• Nch open drain output • CMOS input • Hysteresis input
J		• CMOS output • Hysteresis input • Analog input • With pull-up control
K		• CMOS output • Hysteresis input
L		• CMOS output • CMOS input • Hysteresis input

■ HANDLING DEVICES

- Preventing Latchup

  Care must be taken to ensure that maximum voltage ratings are not exceeded when it is used.

  Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} and V_{SS}.

  When latchup occurs, power supply current increases rapidly and might thermally damage elements.

  Also, take care to prevent the analog power supply voltage (AV_{CC}) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

- Stable Supply Voltage

  Supply voltage should be stabilized.

  A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.

  For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50 Hz to 60 Hz) not to exceed 10% of the Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Treatment of Unused Input Pin

  An unused input pin may cause a malfunction if it is left open. It should be connected to a pull-up or pull-down resistor.

- Treatment of Power Supply Pins on A/D Converter

  Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.

- Precautions for Use of External Clock

  Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

- Precaution against Noise to the External Reset Pin ($\overline{RST}$)

  An input of a reset pulse below the specified level to the external reset pin ($\overline{RST}$) may cause malfunctions. Be sure not to allow an input of a reset pulse below the specified level to the external reset pin ($\overline{RST}$).

■ PROGRAMMING FLASH MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported Parallel Programmers and Adapters

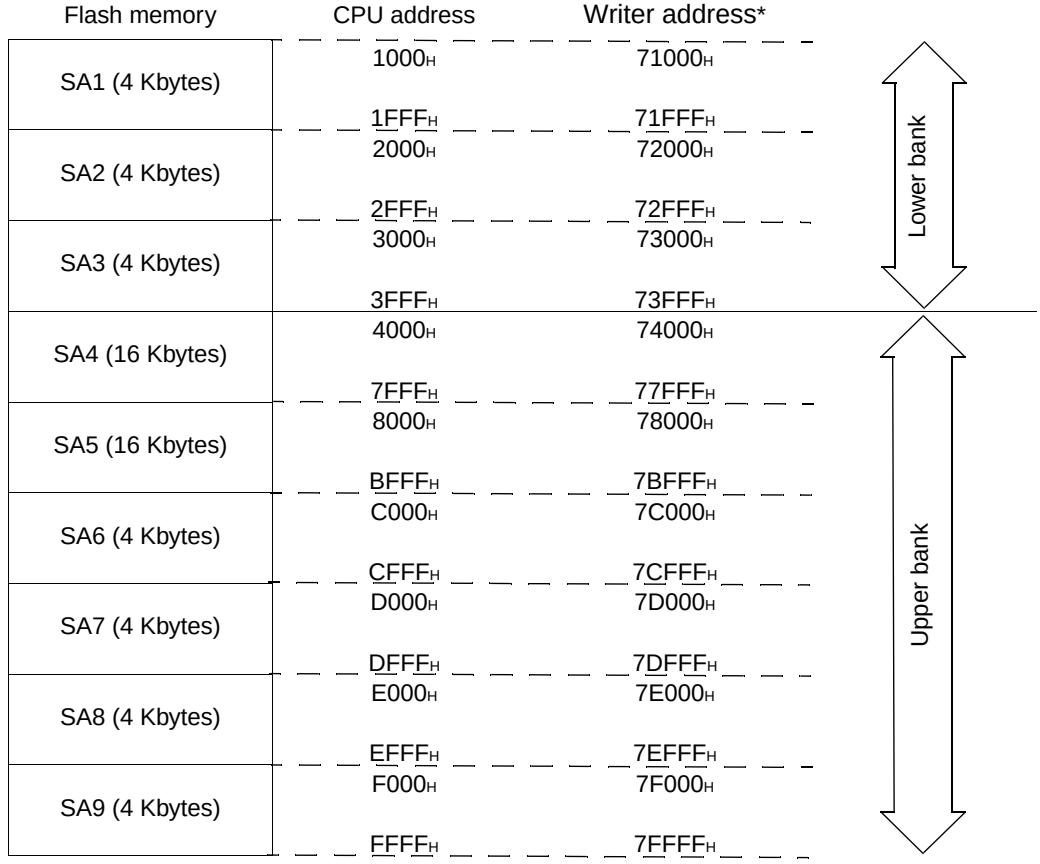
The following table lists supported parallel programmers and adapters.

Package	Applicable adapter model	Parallel programmers
FPT-48P-M26	TEF110-108F37AP	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
LCC-48P-M09	TEF100-108F41AP	

Notes: • Set all of the J1 to J3 switches on the adapter to "95F108".
• For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: 053-428-8380

• Sector Configuration

The individual sectors of flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:



*: Programmer addresses are equivalent to CPU addresses, used when the parallel programmer programs data into flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in flash memory.

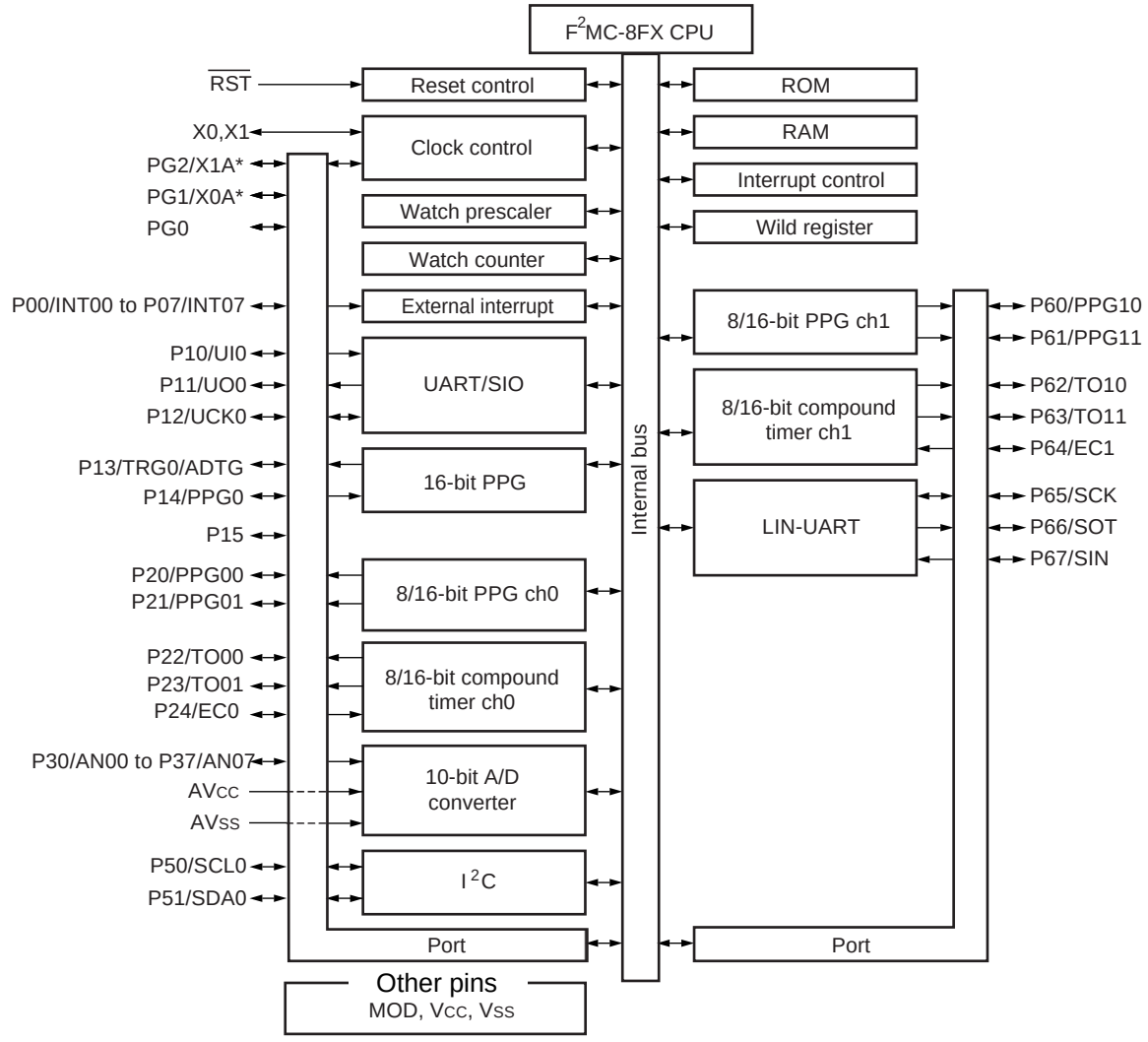
• Programming Method

1) Set the type code of the parallel programmer to 17226.

2) Load program data to programmer addresses 71000H to 7FFFFH.

3) Programmed by parallel programmer

■ BLOCK DIAGRAM



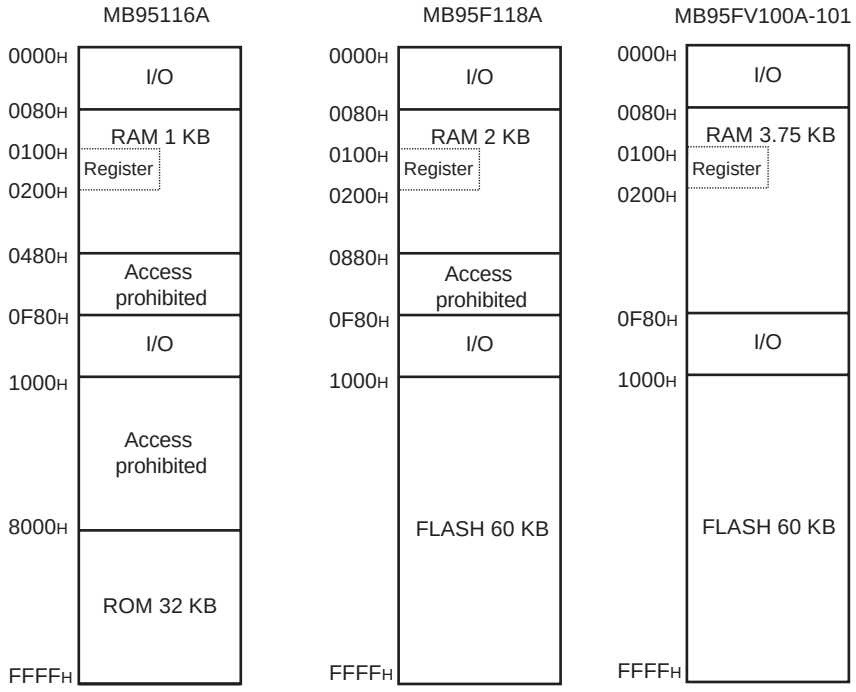
* : Single-system product is general-purpose port, and dual-system product is subclock oscillation.

■ CPU CORE

1. Memory space

Memory space of the MB95110A series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95110A series shown in below.

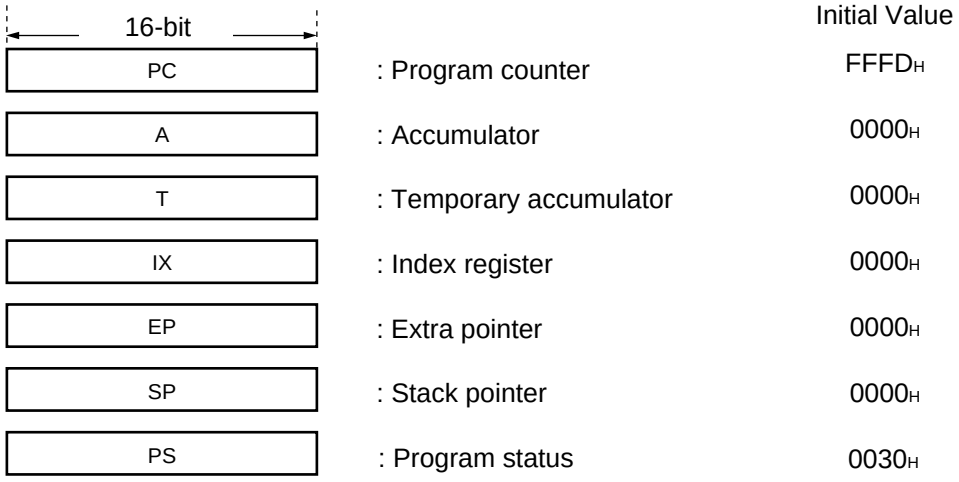
• Memory Map



2. Register

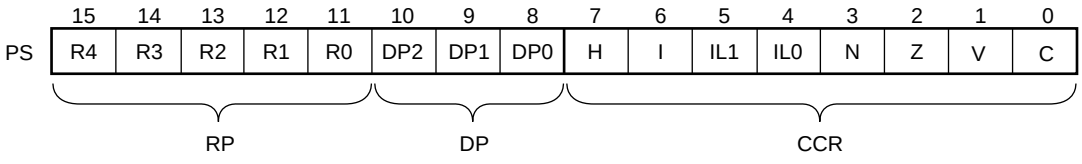
The MB95110A series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

Program counter (PC)	:	A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	:	A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
Index register (IX)	:	A 16-bit register for index modification
Extra pointer (EP)	:	A 16-bit pointer to point to a memory address.
Stack pointer (SP)	:	A 16-bit register to indicate a stack area.
Program status (PS)	:	A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register



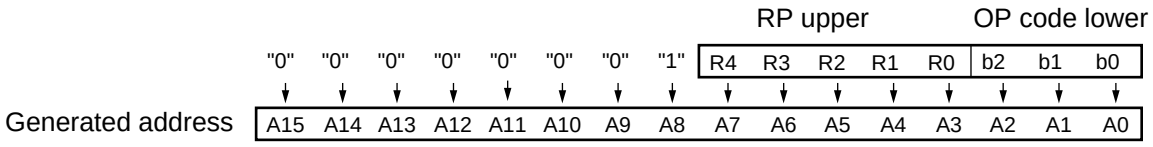
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

- Structure of the program status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

- Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080_H to $00FF_H$.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
Don't care	0000_H to $007F_H$	0000_H to $007F_H$ (without mapping)
000_B (initial value)	0080_H to $00FF_H$	0080_H to $00FF_H$ (without mapping)
001_B		0100_H to $017F_H$
010_B		0180_H to $01FF_H$
011_B		0200_H to $027F_H$
100_B		0280_H to $02FF_H$
101_B		0300_H to $037F_H$
110_B		0380_H to $03FF_H$
111_B		0400_H to $047F_H$

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is set to "0" when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	Priority
0	0	0	High
0	1	1	↕
1	0	2	
1	1	3	Low = no interruption

N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".

Z flag : Set to "1" when an arithmetic operation results in 0. Cleared to "0" otherwise.

V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.

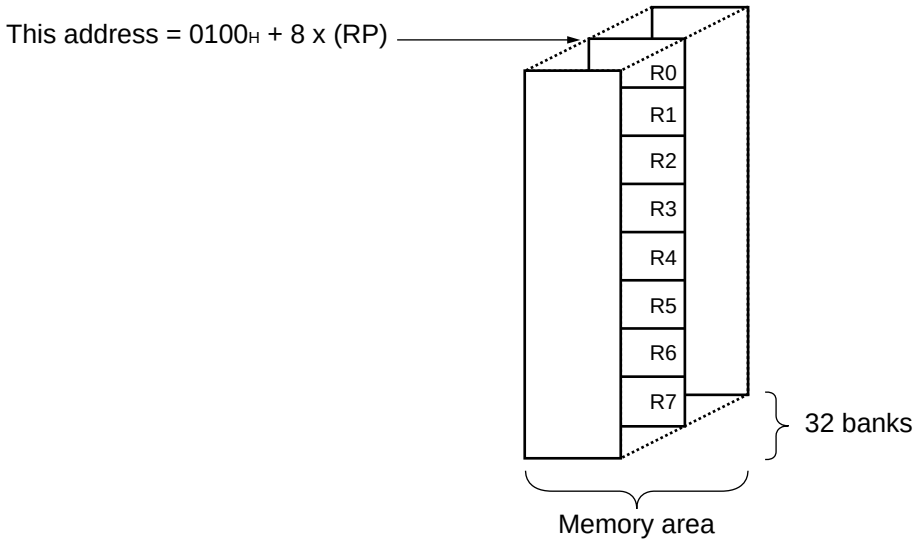
C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB95110A series. The bank currently in use is indicated by the register bank pointer (RP).

- Register Bank Configuration



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Vacancy)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	PLLC	PLL control register	R/W	00000000_B
0007_H	SYCC	System clock control register	R/W	$1010X011_B$
0008_H	STBC	Standby control register	R/W	00000000_B
0009_H	RSRR	Reset source register	R	$XXXXXXXX_B$
$000A_H$	TBTC	Timebase timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$	—	(Vacancy)	—	—
$000E_H$	PDR2	Port 2 data register	R/W	00000000_B
$000F_H$	DDR2	Port 2 direction register	R/W	00000000_B
0010_H	PDR3	Port 3 data register	R/W	00000000_B
0011_H	DDR3	Port 3 direction register	R/W	00000000_B
0012_H	—	(Vacancy)	—	—
0013_H				
0014_H	PDR5	Port 5 data register	R/W	00000000_B
0015_H	DDR5	Port 5 direction register	R/W	00000000_B
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to 0029_H	—	(Vacancy)	—	—
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	—	(Vacancy)	—	—
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$	PUL2	Port 2 pull-up register	R/W	00000000_B
$002F_H$	PUL3	Port 3 pull-up register	R/W	00000000_B
0030_H to 0034_H	—	(Vacancy)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit compound timer 01 control status register 1 ch0	R/W	00000000B
0037H	T00CR1	8/16-bit compound timer 00 control status register 1 ch0	R/W	00000000B
0038H	T11CR1	8/16-bit compound timer 11 control status register 1 ch1	R/W	00000000B
0039H	T10CR1	8/16-bit compound timer 10 control status register 1 ch1	R/W	00000000B
003AH	PC01	8/16-bit PPG1 control register ch0	R/W	00000000B
003BH	PC00	8/16-bit PPG0 control register ch0	R/W	00000000B
003CH	PC11	8/16-bit PPG1 control register ch1	R/W	00000000B
003DH	PC10	8/16-bit PPG0 control register ch1	R/W	00000000B
003EH to 0041H	—	(Vacancy)	—	—
0042H	PCNTH0	16-bit PPG status control register (Upper byte) ch0	R/W	00000000B
0043H	PCNTL0	16-bit PPG status control register (Lower byte) ch0	R/W	00000000B
0044H to 0047H	—	(Vacancy)	—	—
0048H	EIC00	External interrupt circuit control register ch0/1	R/W	00000000B
0049H	EIC10	External interrupt circuit control register ch2/3	R/W	00000000B
004AH	EIC20	External interrupt circuit control register ch4/5	R/W	00000000B
004BH	EIC30	External interrupt circuit control register ch6/7	R/W	00000000B
004CH to 004FH	—	(Vacancy)	—	—
0050H	SCR	LIN-UART serial control register	R/W	00000000B
0051H	SMR	LIN-UART serial mode register	R/W	00000000B
0052H	SSR	LIN-UART serial status register	R/W	00001000B
0053H	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000B
0054H	ESCR	LIN-UART extended status control register	R/W	00000100B
0055H	ECCR	LIN-UART extended communication control register	R/W	000000XXB
0056H	SMC10	UART/SIO serial mode control register 1 ch0	R/W	00000000B
0057H	SMC20	UART/SIO serial mode control register 2 ch0	R/W	00100000B
0058H	SSR0	UART/SIO serial status register ch0	R/W	00000001B
0059H	TDR0	UART/SIO serial output data register ch0	R/W	00000000B
005AH	RDR0	UART/SIO serial input data register ch0	R	00000000B
005BH to 005FH	—	(Vacancy)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0060H	IBCR00	I²C bus control register 0 ch0	R/W	00000000B
0061H	IBCR10	I²C bus control register 1 ch0	R/W	00000000B
0062H	IBSR0	I²C bus status register ch0	R	00000000B
0063H	IDDR0	I²C data register ch0	R/W	00000000B
0064H	IAAR0	I²C address register ch0	R/W	00000000B
0065H	ICCR0	I²C clock control register ch0	R/W	00000000B
0066H to 006BH	—	(Vacancy)	—	—
006CH	ADC1	A/D control register 1	R/W	00000000B
006DH	ADC2	A/D control register 2	R/W	00000000B
006EH	ADDH	A/D data register (Upper byte)	R/W	00000000B
006FH	ADDL	A/D data register (Lower byte)	R/W	00000000B
0070H	WCSR	Watch counter status register	R/W	00000000B
0071H	—	(Vacancy)	—	—
0072H	FSR	Flash memory status register	R/W	000X0000B
0073H	SWRE0	Flash memory sector writing control register 0	R/W	00000000B
0074H	SWRE1	Flash memory sector writing control register 1	R/W	00000000B
0075H	—	(Vacancy)	—	—
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	(Mirror of register bank pointer (RP) and direct bank pointer (DP))	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(Vacancy)	—	—
0F80H	WRARH0	Wild register address setting register (Upper byte) ch0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (Lower byte) ch0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (Upper byte) ch1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (Lower byte) ch1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch1	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F86H	WRARH2	Wild register address setting register (Upper byte) ch2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (Lower byte) ch2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch2	R/W	00000000B
0F89H to 0F91H	—	(Vacancy)	—	—
0F92H	T01CR0	8/16-bit compound timer 01 control status register 0 ch0	R/W	00000000B
0F93H	T00CR0	8/16-bit compound timer 00 control status register 0 ch0	R/W	00000000B
0F94H	T01DR	8/16-bit compound timer 01 data register ch0	R/W	00000000B
0F95H	T00DR	8/16-bit compound timer 00 data register ch0	R/W	00000000B
0F96H	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch0	R/W	00000000B
0F97H	T11CR0	8/16-bit compound timer 11 control status register 0 ch1	R/W	00000000B
0F98H	T10CR0	8/16-bit compound timer 10 control status register 0 ch1	R/W	00000000B
0F99H	T11DR	8/16-bit compound timer 11 data register ch1	R/W	00000000B
0F9AH	T10DR	8/16-bit compound timer 10 data register ch1	R/W	00000000B
0F9BH	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch1	R/W	00000000B
0F9CH	PPS01	8/16-bit PPG1 cycle setting buffer register ch0	R/W	11111111B
0F9DH	PPS00	8/16-bit PPG0 cycle setting buffer register ch0	R/W	11111111B
0F9EH	PDS01	8/16-bit PPG1 duty setting buffer register ch0	R/W	11111111B
0F9FH	PDS00	8/16-bit PPG0 duty setting buffer register ch0	R/W	11111111B
0FA0H	PPS11	8/16-bit PPG1 cycle setting buffer register ch1	R/W	11111111B
0FA1H	PPS10	8/16-bit PPG0 cycle setting buffer register ch1	R/W	11111111B
0FA2H	PDS11	8/16-bit PPG1 duty setting buffer register ch1	R/W	11111111B
0FA3H	PDS10	8/16-bit PPG0 duty setting buffer register ch1	R/W	11111111B
0FA4H	PPGS	8/16-bit PPG starting register	R/W	00000000B
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H to 0FA9H	—	(Vacancy)	—	—
0FAAH	PDCRH0	16-bit PPG down counter register (Upper byte) ch0	R	00000000B
0FABH	PDCRL0	16-bit PPG down counter register (Lower byte) ch0	R	00000000B
0FACH	PCSRH0	16-bit PPG cycle setting buffer register (Upper byte) ch0	R/W	11111111B
0FADH	PCSRL0	16-bit PPG cycle setting buffer register (Lower byte) ch0	R/W	11111111B
0FAEH	PDUTH0	16-bit PPG duty setting buffer register (Upper byte) ch0	R/W	11111111B
0FAFH	PDUTL0	16-bit PPG duty setting buffer register (Lower byte) ch0	R/W	11111111B

(Continued)

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0FB0_H$ to $0FBB_H$	—	(Vacancy)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$	PSSR0	UART/SIO prescaler selection register ch0	R/W	00000000_B
$0FBF_H$	BRSR0	UART/SIO baud rate setting register ch0	R/W	00000000_B
$0FC0_H$ to $0FC2_H$	—	(Vacancy)	—	—
$0FC3_H$	AIDRL	A/D input disable register (Lower byte)	R/W	00000000_B
$0FC4_H$ to $0FE2_H$	—	(Vacancy)	—	—
$0FE3_H$	WCDR	Watch counter data register	R/W	00111111_B
$0FE4_H$ to $0FED_H$	—	(Vacancy)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$	WICR	Interrupt pin control register	R/W	01000000_B
$0FF0_H$ to $0FFF_H$	—	(Vacancy)	—	—

- Read/write access symbols

R/W : Readable and Writable
R : Read only
W : Write only

- Initial value symbols

0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch0	IRQ0	FFFA$_H$	FFFB$_H$	L00 [1 : 0]	High
External interrupt ch4					
External interrupt ch1	IRQ1	FFF8$_H$	FFF9$_H$	L01 [1 : 0]	
External interrupt ch5					
External interrupt ch2	IRQ2	FFF6$_H$	FFF7$_H$	L02 [1 : 0]	
External interrupt ch6					
External interrupt ch3	IRQ3	FFF4$_H$	FFF5$_H$	L03 [1 : 0]	
External interrupt ch7					
UART/SIO ch0	IRQ4	FFF2$_H$	FFF3$_H$	L04 [1 : 0]	
8/16-bit compound timer ch0 (Lower)	IRQ5	FFF0$_H$	FFF1$_H$	L05 [1 : 0]	
8/16-bit compound timer ch0 (Upper)	IRQ6	FFEE$_H$	FFEF$_H$	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC$_H$	FFED$_H$	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA$_H$	FFEB$_H$	L08 [1 : 0]	
8/16-bit PPG ch1 (Lower)	IRQ9	FFE8$_H$	FFE9$_H$	L09 [1 : 0]	
8/16-bit PPG ch1 (Upper)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1 : 0]	
(Unused)	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1 : 0]	
8/16-bit PPG ch0 (Upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1 : 0]	
8/16-bit PPG ch0 (Lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1 : 0]	
8/16-bit compound timer ch1 (Upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1 : 0]	
16-bit PPG ch0	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1 : 0]	
I^{2}C ch0	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1 : 0]	
(Unused)	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1 : 0]	
10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1 : 0]	
Watch prescaler/counter	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1 : 0]	
(Unused)	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1 : 0]	
8/16-bit compound timer ch1 (Lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1 : 0]	
FLASH	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1 : 0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	Vcc, AVcc	Vss − 0.3	Vss + 4.0	V	*2
	AVR	Vss − 0.3	Vss + 4.0		*2 MB95FV100A-101 only
Input voltage*1	V_{I1}	Vss − 0.3	Vss + 4.0	V	Other than P50, P51*3
	V_{I2}	Vss − 0.3	Vss + 6.0		P50, P51
Output voltage*1	V_O	Vss − 0.3	Vss + 4.0	V	*3
Maximum clamp current	I_{CLAMP}	− 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins*4
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P00 to P07
	I_{OL2}		15		P00 to P07
"L" level average current	I_{OLAV1}	—	4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P00 to P07 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (total of pins)
"H" level maximum output current	I_{OH1}	—	− 15	mA	Other than P00 to P07
	I_{OH2}		− 15		P00 to P07
"H" level average current	I_{OHAV1}	—	− 4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		− 8		P00 to P07 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	− 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	− 50	mA	Total average output current = operating current × operating ratio (total of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	− 40	+ 85	°C	Other than MB95FV100A-101
Storage temperature	Tstg	− 55	+ 150	°C	

(Continued)

(Continued)

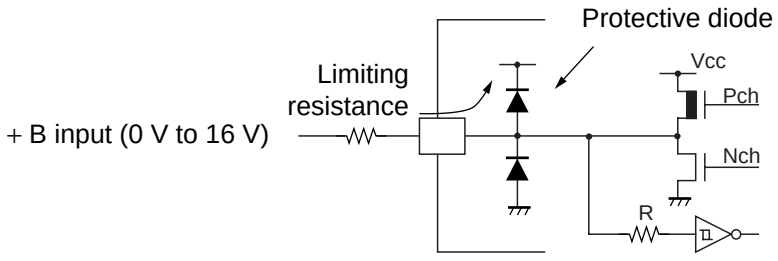
*1 : The parameter is based on $AV_{CC} = V_{SS} = 0.0$ V.

*2 : Apply equal potential to AVcc and Vcc. AVR should not exceed AVcc + 0.3 V.

*3 : V_{I1} and V_O should not exceed V_{CC} + 0.3 V. V_{I1} must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_{I1} rating.

*4 :
- Applicable to pins : P00 to P07, P10 to P15, P20 to P24, P30 to P37, PG0
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Sample recommended circuits :

• Input/Output Equivalent Circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	1.8*1	3.3*2	V	At normal operating, FLASH product, T_A = –10 °C to +85 °C
		1.8*1	3.6		At normal operating, MASK product, T_A = –10 °C to +85 °C
		2.0*1	3.3*2		At normal operating, FLASH product, T_A = –40 °C to +85 °C
		2.0*1	3.6		At normal operating, MASK product, T_A = –40 °C to +85 °C
		2.6	3.6		MB95FV100A-101
		1.5	3.3*2		Retain status of stop operation, FLASH product
		1.5	3.6		Retain status of stop operation, MASK product
Operating temperature	T_A	− 40	+ 85	°C	Other than MB95FV100A-101

*1 : The values vary with the operating frequency.

*2 : Consult Fujitsu separately for a guarantee of a maximum value of 3.6 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(Vcc = AVcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C [MB95FV100A-101 is T_A = +25 °C])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P10, P67	*1	0.7 Vcc	—	Vcc + 0.3	V	At selecting of CMOS input level (hysteresis input)
	V_{IH2}	P50, P51	*1	0.7 Vcc	—	Vss + 5.5	V	At selecting of CMOS input level (hysteresis input)
	V_{IHS1}	P00 to P07, P10 to P15, P20 to P24, P30 to P37, P60 to P67, PG0, PG1*2, PG2*2	*1	0.8 Vcc	—	Vcc + 0.3	V	Hysteresis input
	V_{IHS2}	P50, P51	*1	0.8 Vcc	—	Vss + 5.5	V	Hysteresis input
	V_{IHM}	$\overline{RST}$, MOD	—	0.7 Vcc	—	Vcc + 0.3	V	CMOS input (FLASH product)
			—	0.8 Vcc	—	Vcc + 0.3	V	Hysteresis input (MASK product)
"L" level input voltage	V_{IL}	P10, P50, P51, P67	*1	Vss − 0.3	—	0.3 Vcc	V	At selecting of CMOS input level (hysteresis input)
	V_{ILS}	P00 to P07, P10 to P15, P20 to P24, P30 to P37, P50, P51, P60 to P67, PG0, PG1*2, PG2*2	*1	Vss − 0.3	—	0.2 Vcc	V	Hysteresis input
	V_{ILM}	$\overline{RST}$, MOD	—	Vss − 0.3	—	0.3 Vcc	V	CMOS input (FLASH product)
			—	Vss − 0.3	—	0.2 Vcc	V	Hysteresis input (MASK product)
Open drain output application voltage	V_D	P50, P51	—	Vss − 0.3	—	Vss + 5.5	V	
"H" level output voltage	V_{OH1}	Output pin other than P00 to P07	I_{OH} = − 4.0 mA	2.4	—	—	V	MB95FV100A-101 a conditional : I_{OH} = − 2.0 mA
	V_{OH2}	P00 to P07	I_{OH} = − 8.0 mA	2.4	—	—	V	MB95FV100A-101 a conditional : I_{OH} = − 5.0 mA

(Continued)

(Continued)

(Vcc = AVcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C [MB95FV100A-101 is T_A = +25 °C])

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	Output pin other than P00 to P07	I_{OL} = 4.0 mA	—	—	0.4	V	MB95FV100A-101 a conditional : I_{OL} = 3.0 mA
	V_{OL2}	P00 to P07	I_{OL} = 12 mA	—	—	0.4	V	MB95FV100A-101 a conditional : I_{OL} = 8.0 mA
Input leakage current (High-Z output leakage current)	I_{LI}	Port other than P50, P51	0.0 V < V_I < Vcc	− 5	—	+ 5	µA	When no pull-up resistor is specified
Open drain output leakage current	I_{LIOD}	P50, P51	0.0 V < V_I < Vss + 5.5 V	—	—	+ 5	µA	
Pull-up resistor	R_{PULL}	P10 to P15, P20 to P24, P30 to P37, PG0, PG1*2, PG2*2	V_I = 0.0 V	25	50	100	kΩ	When pull-up resistor is specified
Pull-down resistor	R_{MOD}	MOD	V_I = Vcc	50	100	200	kΩ	MASK product only
Power supply current*3	I_{CC}	Vcc (external clock operation)	F_{CH} = 20 MHz fmp = 10 MHz Main clock mode (divided by 2)	—	11	14	mA	FLASH product
				—	7.3	10	mA	MASK product
				—	30	35	mA	FLASH product (at FLASH writing and erasing)
	I_{CCS}		F_{CH} = 20 MHz fmp = 10 MHz Main Sleep mode (divided by 2)	—	4.5	6	mA	
	I_{CCL}		F_{CL} = 32 kHz fmpl = 16 kHz Subclock mode (divided by 2) , T_A = + 25 °C	—	25	35	µA	
	I_{CCLS}		F_{CL} = 32 kHz fmpl = 16 kHz Sub sleep mode (divided by 2) , T_A = + 25 °C	—	7	15	µA	

(Continued)

(Continued)

(Vcc = AVcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C [MB95FV100A-101 is T_A = +25 °C])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I_{CCT}	V_{CC} (external clock operation)	F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25 °C	—	2	10	µA	FLASH product
				—	1	5	µA	MASK product
	I_{CCMPLL}		F_{CH} = 4 MHz fmp = 10 MHz Main PLL mode (multiplied by 2.5)	—	10	14	mA	FLASH product
				—	6.7	10	mA	MASK product
	I_{CCSPLL}		F_{CL} = 32 kHz fmpl = 128 kHz Sub PLL mode (multiplied by 4), T_A = + 25 °C	—	190	250	µA	
	I_{CTS}		F_{CH} = 10 MHz Timebase timer mode T_A = + 25 °C	—	0.4	0.5	mA	
	I_{CCH}		Substop mode T_A = + 25 °C	—	1	5	µA	
	I_A	AVcc	F_{CH} = 10 MHz At A/D converting	—	1.3	2.2	mA	
	I_{AH}		F_{CH} = 10 MHz At A/D converting stop T_A = + 25 °C	—	1	5	µA	
Input capacitance	C_{IN}	Other than AVcc, AVss, Vcc, and Vss	—	—	5	15	pF	

*1 : P10, P50, P51, and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR).

*2 : Single-clock products only

*3 : The power-supply current is determined by the external clock.
- Refer to “4. AC characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC characteristics (2) Source Clock/Machine Clock” for fmp and fmpl.

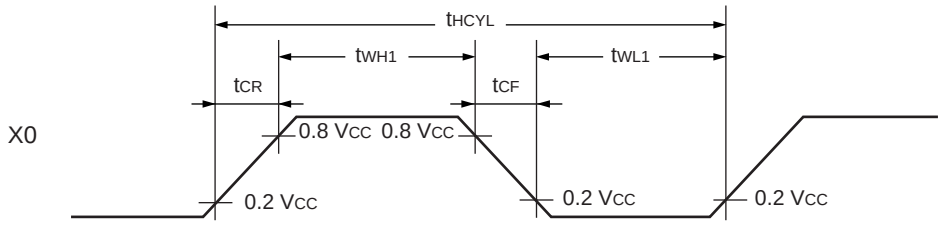
4. AC Characteristics

(1) Clock Timing

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

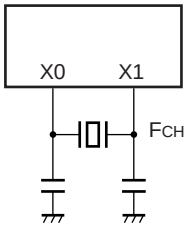
Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	10	MHz	When using Main oscillation circuit
				1	—	20	MHz	When using external clock
				3	—	10	MHz	Main PLL multiplied by 1
				3	—	5	MHz	Main PLL multiplied by 2
				3	—	4	MHz	Main PLL multiplied by 2.5
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When using Sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL FLASH product : Vcc = 2.3 V to 3.3 V MASK product : Vcc = 2.3 V to 3.6 V
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	When using Main oscillation circuit
				50	—	1000	ns	When using Sub oscillation circuit
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	Subclock
Input clock pulse width	t_{WH1} t_{WL1}	X0		10	—	—	ns	When using external clock Duty ratio is about 30% to 70%.
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A		—	—	5	ns	When using external clock

- X0 and X1 Timing and Applying Conditions

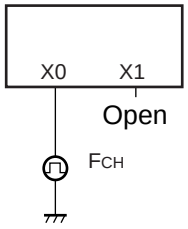


- Main Clock Applying Conditions

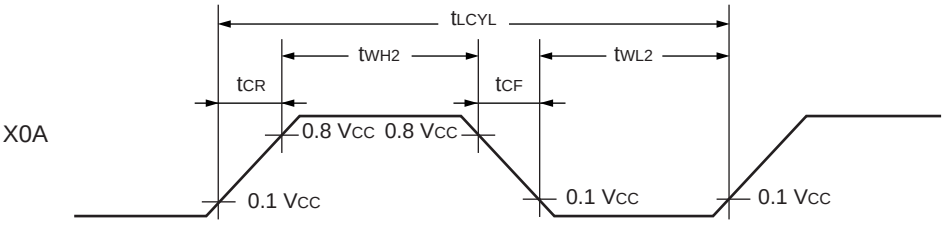
When using a crystal or ceramic oscillator



When using external clock

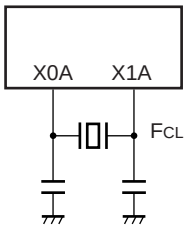


- X0A and X1A Timing and Applying Conditions

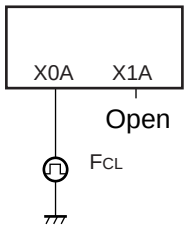


- Subclock Applying Conditions

When using a crystal or ceramic oscillator



When using external clock



(2) Source Clock/Machine Clock

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock*1 (Clock before setting division)	SCLK	—	100	—	2000	ns	When using Main clock Min : F_{CH} = 10 MHz, PLL multiplied by 1 Max : F_{CH} = 1 MHz, divided by 2
			7.6	—	61.0	µs	When using Subclock Min : F_{CL} = 32 kHz, PLL multiplied by 4 Max : F_{CL} = 32 kHz, divided by 2
Source clock frequency	f_{sp}	—	0.5	—	10.0	MHz	When using Main clock
	f_{spl}	—	16.384	—	131.072	kHz	When using Subclock
Machine clock*2 (Minimum instruction execution time)	MCLK	—	100	—	32000	ns	When using Main clock Min : SLCK = 10 MHz, no division Max : SLCK = 0.5 MHz, divided by 16
			7.6	—	976.5	µs	When using Subclock Min : SLCK = 131 kHz, no division Max : SLCK = 16 kHz, divided by 16
Machine clock frequency	f_{mp}	—	0.031	—	10.000	MHz	When using Main clock
	f_{mpl}		1.024	—	131.072	kHz	When using Subclock

*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follow.

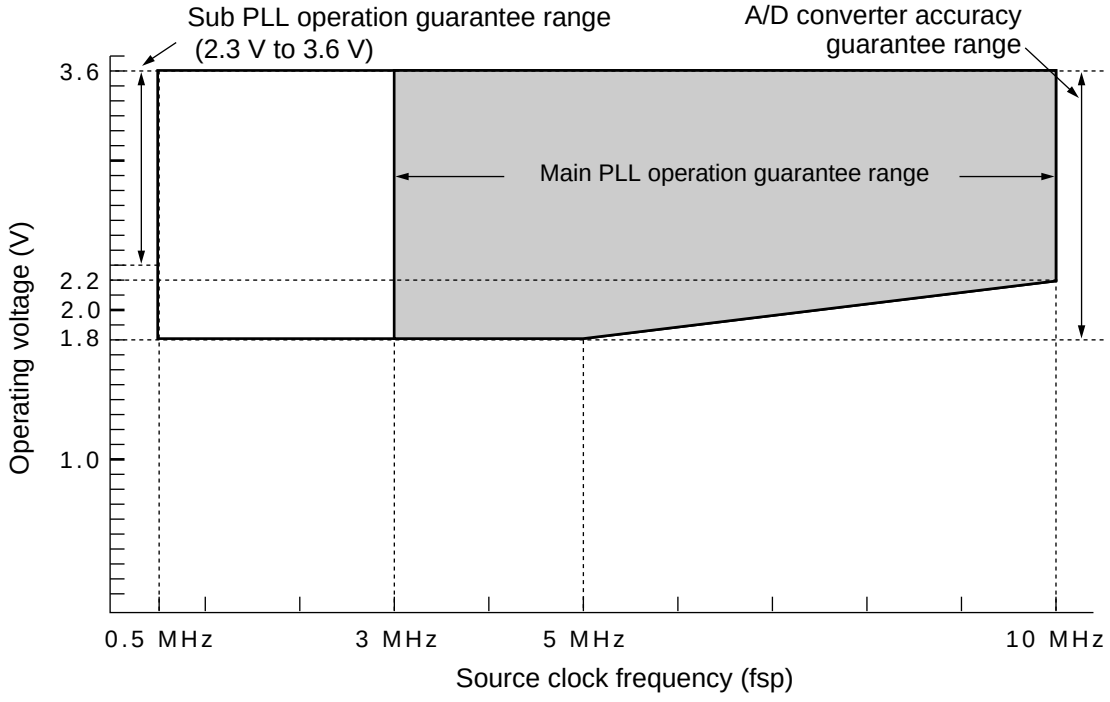
- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5 multiplication)
- Subclock divided by 2
- PLL multiplication of subclock (select from 2, 3, 4 multiplication)

*2 : Operation clock of the microcontroller. Machine clock can be selected as follow.

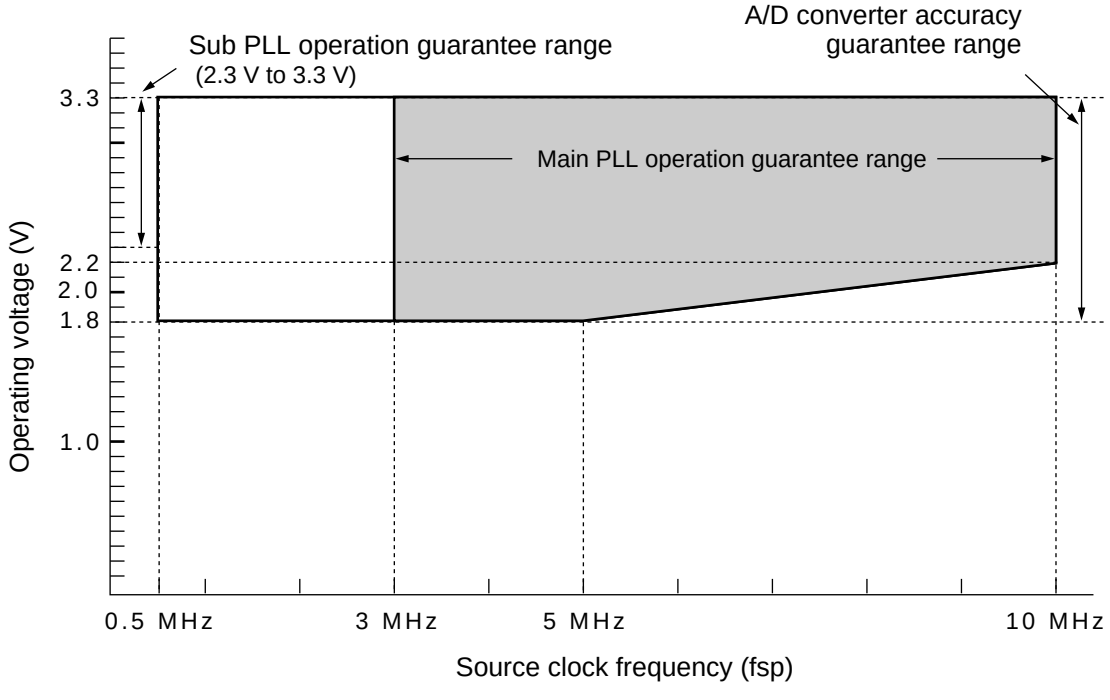
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• **Operating voltage** – **Operating frequency**

• MASK product

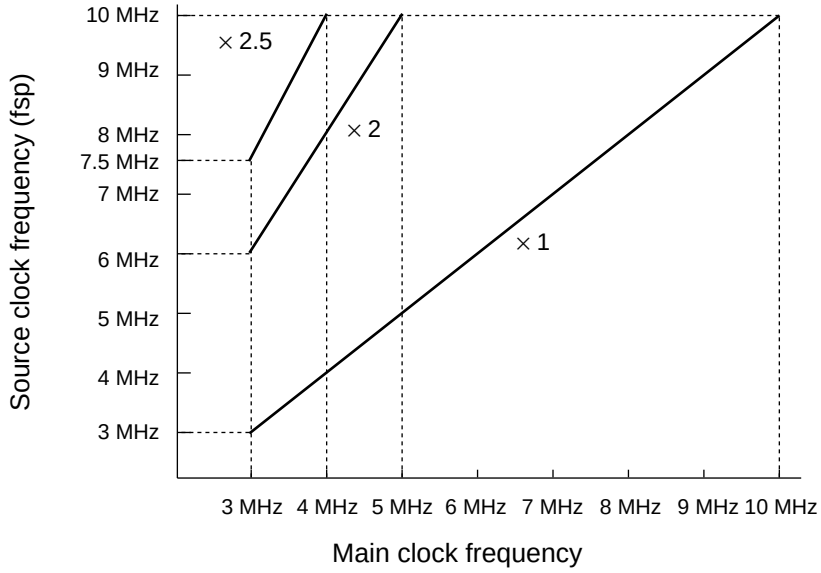


• FLASH product



Note: In operating by 2.0 V or less, only “T_A = -10 °C to +85 °C” is guaranteed.

• Main PLL operation frequency



(3) Reset Timing

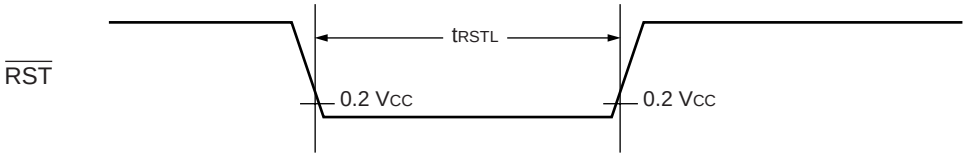
(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 MCLK*1	—	ns	At normal operating
		Oscillation time of oscillator*2 + 2 MCLK*1	—	ns	At stop mode, subclock mode, Sub sleep mode, and watch mode

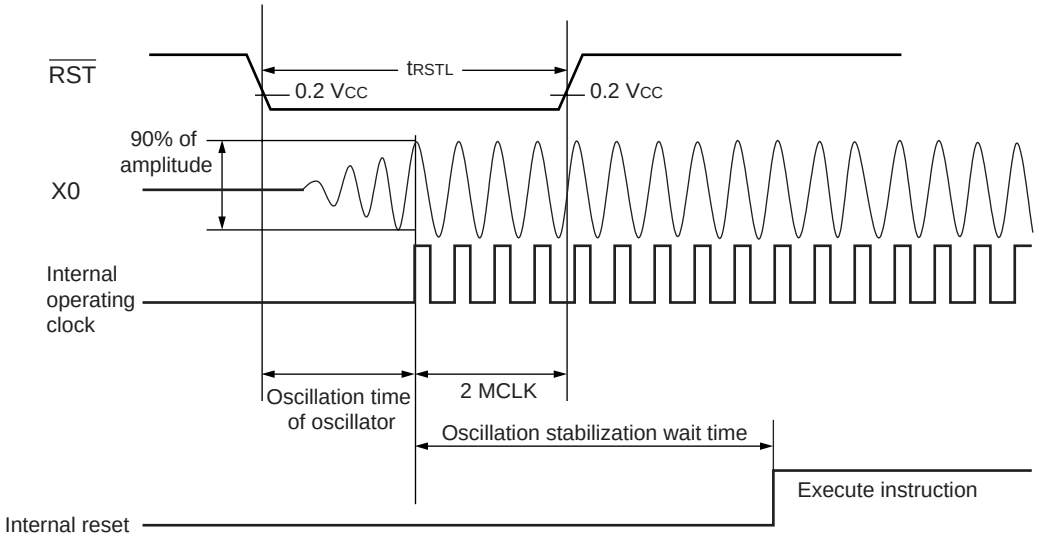
*1 : Refer to " (2) Source Clock/Machine Clock" for MCLK.

*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In FAR/ceramic oscillators, the oscillation time is between hundreds of μs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



• At stop mode, subclock mode, sub sleep mode, and watch mode

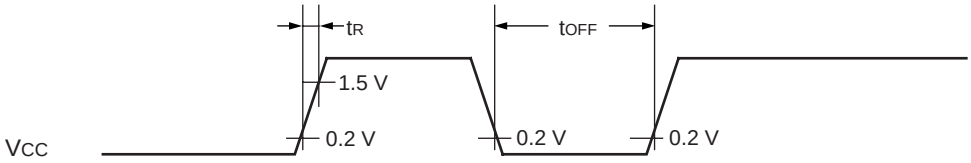


(4) Power-on Reset

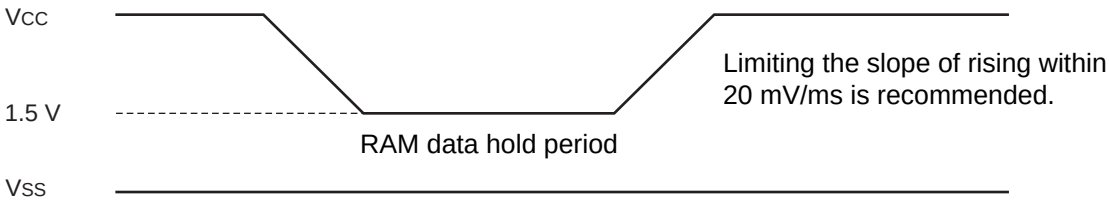
(AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	36	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Due to repeated operations

Note : The power supply must be turned on within the selected oscillation stabilization time.



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 20 mV/ms as shown below. In this case, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.

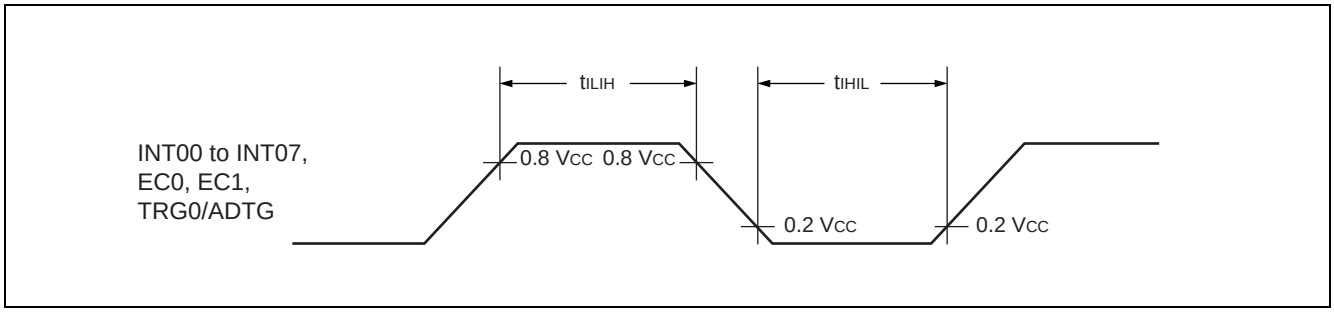


(5) Peripheral Input Timing

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, TRG0/ADTG	2 MCLK*	—	ns	
Peripheral input “L” pulse width	t_{IHIL}		2 MCLK*	—	ns	

* : Refer to “ (2) Source Clock/Machine Clock” for MCLK.



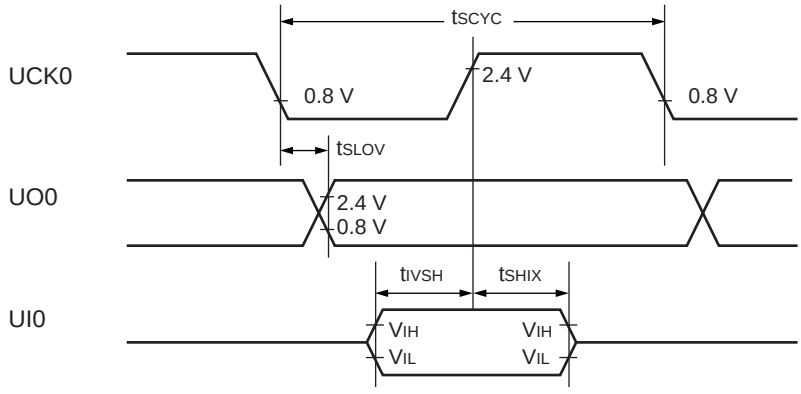
(6) UART/SIO, Serial I/O Timing

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

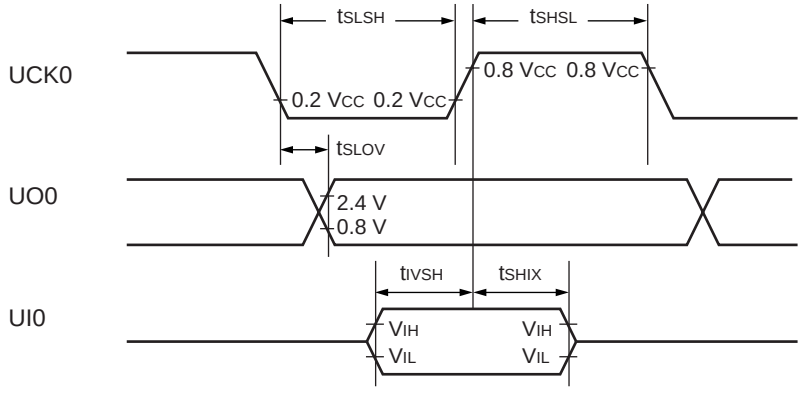
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 MCLK*	—	ns	
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	190	ns	
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 MCLK*	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 MCLK*	—	ns	
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 MCLK*	—	ns	
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 MCLK*	—	ns	
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns	
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 MCLK*	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 MCLK*	—	ns	

* : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

• Internal shift clock mode



• External shift clock mode



(7) LIN-UART Timing

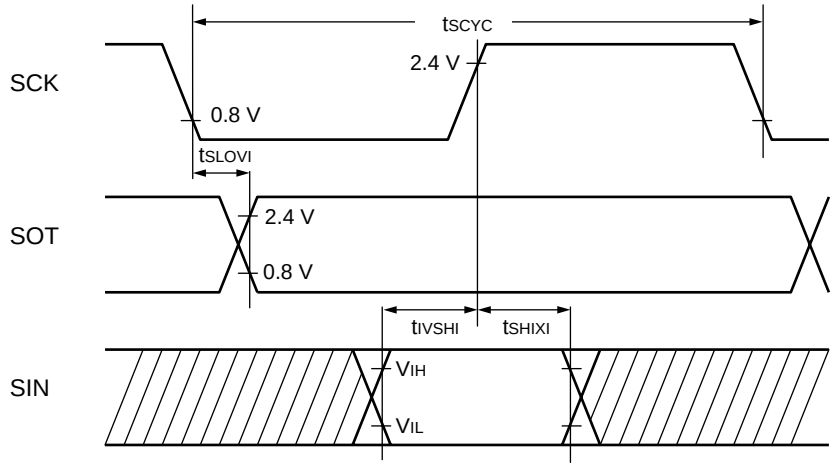
ESCR : SCES = 0, ECCR : SCDE = 0

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

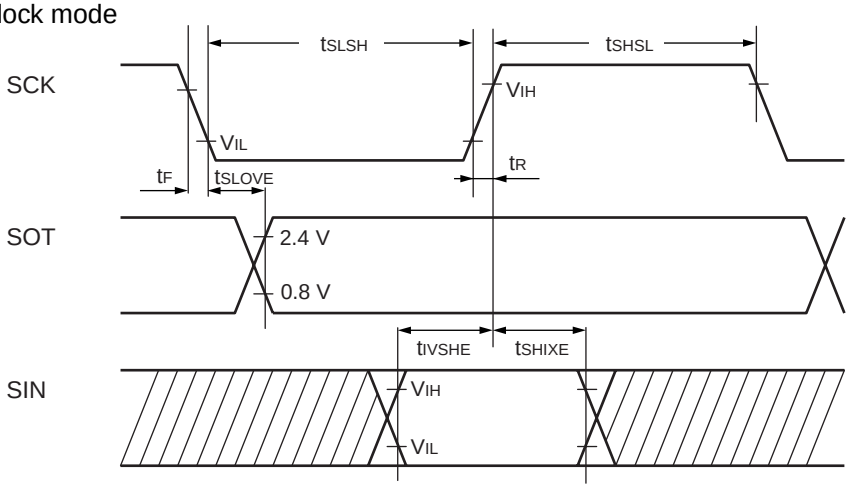
Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 MCLK* – t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		MCLK* + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 MCLK* + 95	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK, SIN		MCLK* + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

* : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

- Internal shift clock mode



- External shift clock mode



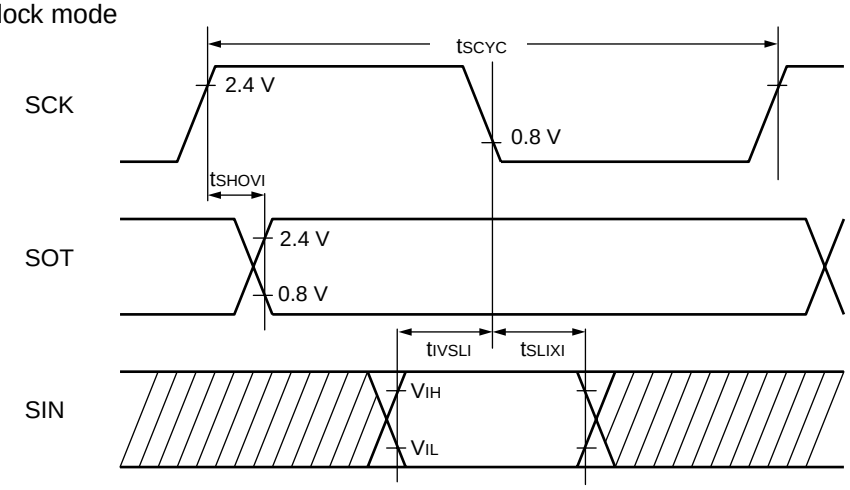
ESCR : SCES = 1, ECCR : SCDE = 0

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

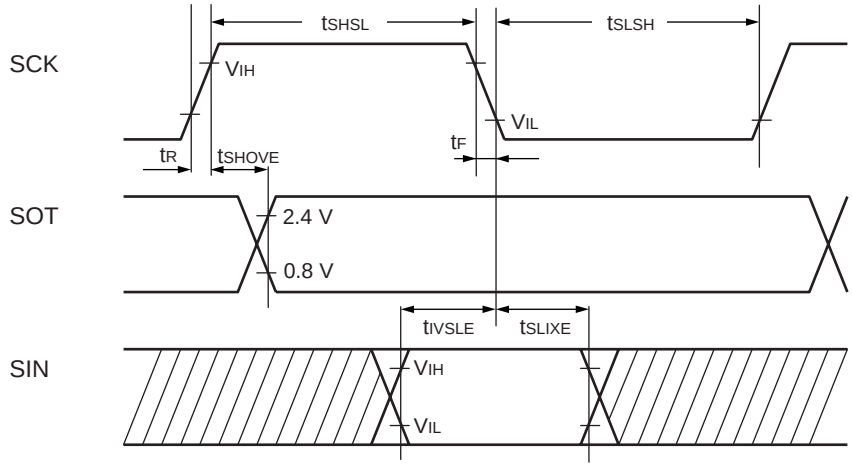
Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 MCLK* – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		MCLK* + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 MCLK* + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK, SIN		MCLK* + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

* : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

- Internal shift clock mode



- External shift clock mode

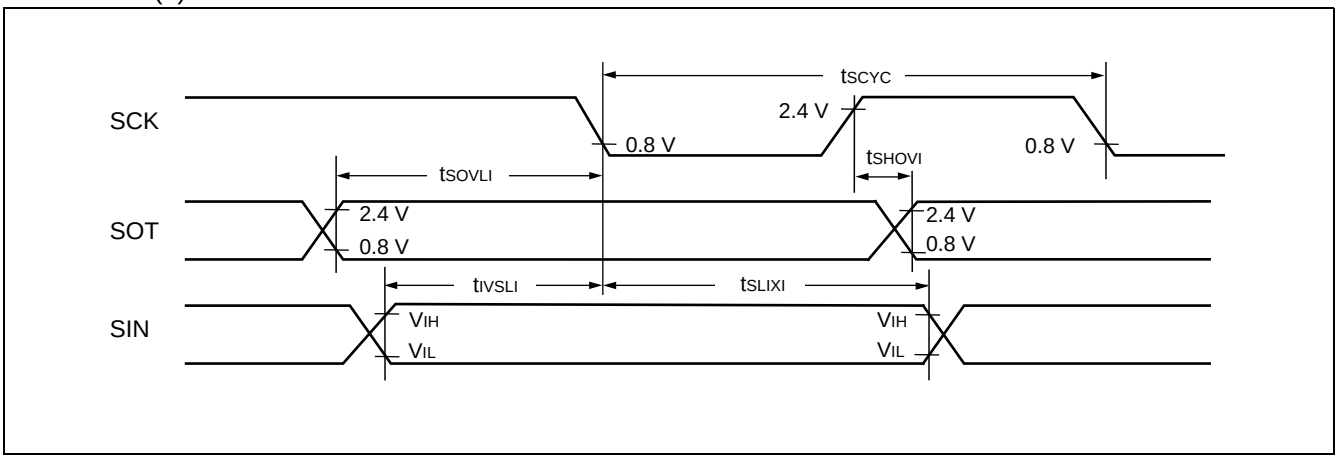


ESCR : SCES = 0, ECCR : SCDE = 1

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	95	ns
Valid SIN→SCK↓	t_{IVSLI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 MCLK*	ns

* : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

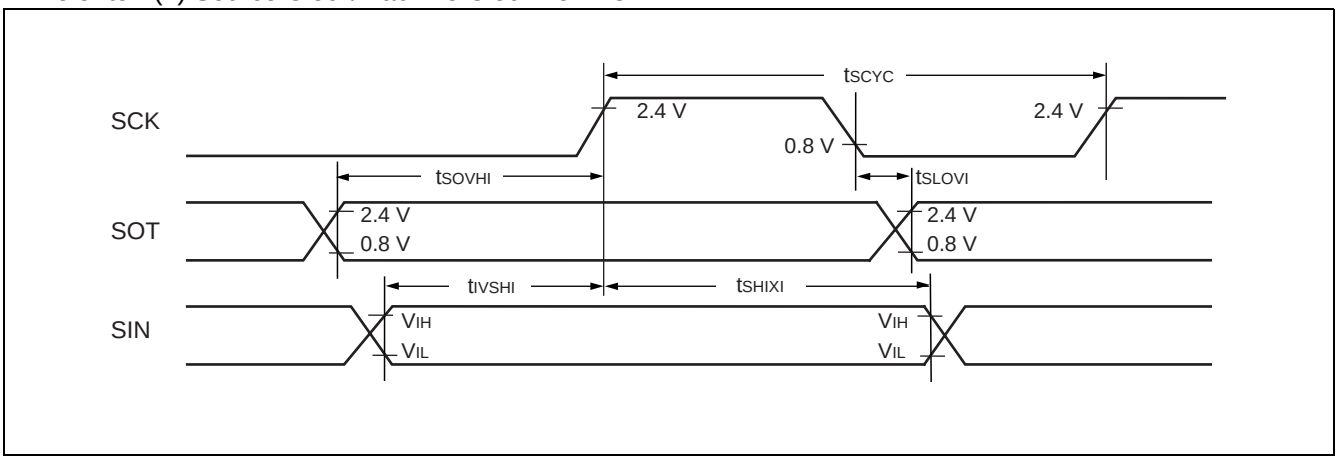


ESCR : SCES = 1, ECCR : SCDE = 1

(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		MCLK* + 190	—	ns
SCK ↑ →valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	tS_{OVHI}	SCK, SOT		—	4 MCLK*	ns

* : Refer to “ (2) Source Clock/Machine Clock” for MCLK.



(8) I²C Timing

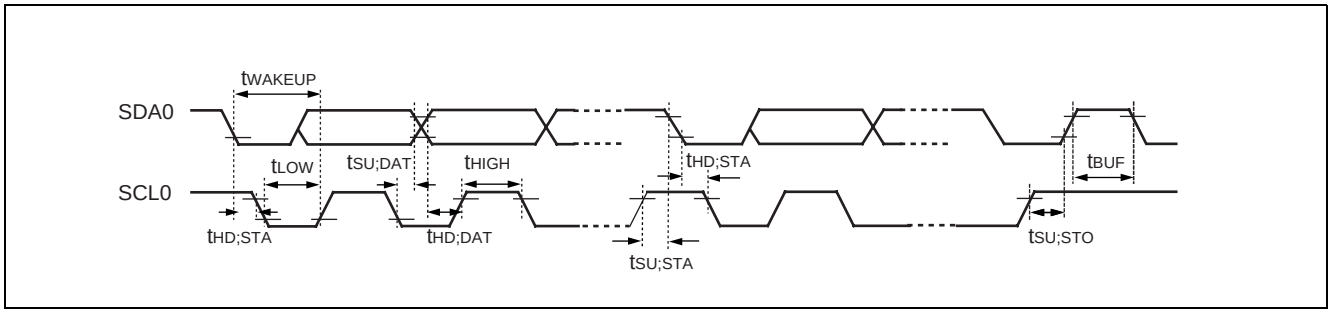
(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value				Unit	Remarks
			Standard-mode		Fast-mode			
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz	
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$		4.0	—	0.6	—	µs	
SCL clock “L” width	t_{LOW}		4.7	—	1.3	—	µs	
SCL clock “H” width	t_{HIGH}		4.0	—	0.6	—	µs	
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$		4.7	—	0.6	—	µs	
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$		0.25	—	0.1	—	µs	
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$		4	—	0.6	—	µs	
Bus free time between stop condition and start condition	t_{BUF}		4.7	—	1.3	—	µs	

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HD;DAT}$ have only to be met if the device dose not stretch the “L” width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must then be met.



(Vcc = 3.3 V, AVss = Vss = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Sym-bol	I/O Timing		Unit	Remarks
		Min	Max		
SCL clock “L” width	t_{LOW}	(2 + nm*2 / 2) MCLK*1 – 20	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	(nm*2 / 2) MCLK*1 – 20	(nm*2 / 2) MCLK*1 + 20	ns	Master mode
Start condition hold time	$t_{HD;STA}$	(–1 + nm*2 / 2) MCLK*1 – 20	(–1 + nm*2) MCLK*1 + 20	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	(1 + nm*2 / 2) MCLK*1 – 20	(1 + nm*2 / 2) MCLK*1 + 20	ns	Master mode
Start condition setup time	$t_{SU;STA}$	(1 + nm*2 / 2) MCLK*1 – 20	(1 + nm*2 / 2) MCLK*1 + 20	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	(2 nm*2 + 4) MCLK*1 – 20	—	ns	
Data hold time	$t_{HD;DAT}$	3 MCLK*1 – 20	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	(–2 + nm*2 / 2) MCLK*1 – 20	(–1 + nm*2 / 2) MCLK*1 + 20	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	(nm*2 / 2) MCLK*1 – 20	(1 + nm*2 / 2) MCLK*1 + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock “L” width	t_{LOW}	4 MCLK*1 – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	4 MCLK*1 – 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	2 MCLK*1 – 20	—	ns	Undetected when 1 MCLK is used at reception
Stop condition detection	$t_{SU;STO}$	2 MCLK*1 – 20	—	ns	Undetected when 1 MCLK is used at reception
Restart condition detection condition	$t_{SU;STA}$	2 MCLK*1 – 20	—	ns	Undetected when 1 MCLK is used at reception
Bus free time	t_{BUF}	2 MCLK*1 – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	2 MCLK*1 – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	t_{LOW} – 3 MCLK*1 – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	MCLK*1 – 20	—	ns	At reception

(Continued)

(Continued)

Parameter	Sym-bol	I/O Timing		Unit	Remarks
		Min	Max		
SDA↓→SCL↑ (at wakeup function)	$t_{WAKE-UP}$	Oscillation stabilization wait time + 2 MCLK*1 – 20	—	ns	

*1 : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

*2 :
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of clock control register (ICCR) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of clock control register (ICCR) .
- Actual timing of I^2C is determined by m and n values set by the machine clock (MCLK) and ICCR [4 : 0].
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < MCLK (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < MCLK ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < MCLK ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < MCLK ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < MCLK ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < MCLK (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < MCLK ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < MCLK ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < MCLK ≤ 10 MHz

5. A/D Converter

(1) A/D Converter Electrical Characteristics

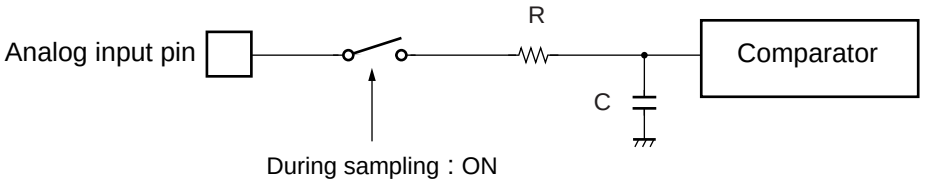
(AVcc = Vcc = 1.8 V to 3.3 V [FLASH product], AVcc = Vcc = 1.8 V to 3.6 V [MASK product], AVss = Vss = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		− 3.0	—	+ 3.0	LSB	
Linearity error		− 2.5	—	+ 2.5	LSB	
Differential linear error		− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AVss − 1.5 LSB	AVss + 0.5 LSB	AVss + 2.5 LSB	V	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V
		AVss − 0.5 LSB	AVss + 1.5 LSB	AVss + 3.5 LSB	V	1.8 V ≤ AVcc < 2.7 V
Full-scale transition voltage	V_{FST}	AVcc − 3.5 LSB	AVcc − 1.5 LSB	AVcc + 0.5 LSB	V	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V
		AVcc − 2.5 LSB	AVcc − 0.5 LSB	AVcc + 1.5 LSB	V	1.8 V ≤ AVcc < 2.7 V
Compare time	—	0.6	—	16,500	µs	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V
		20	—	16,500	µs	1.8 V ≤ AVcc < 2.7 V
Sampling time	—	0.4	—	∞	µs	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V external impedance < at 1.8 kΩ
		30	—	∞	µs	1.8 V ≤ AVcc < 2.7 V external impedance < at 14.8 kΩ
Analog input current	I_{AIN}	–0.3	—	0.3	µA	
Analog input voltage range	V_{AIN}	AVss	—	AVcc	V	
Reference voltage	—	AVss + 1.8	—	AVcc	V	AVcc pin
Reference voltage supply current	I_R	—	400	600	µA	AVcc pin, During A/D operation
	I_{RH}	—	—	5	µA	AVcc pin, at stop mode

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sanple and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



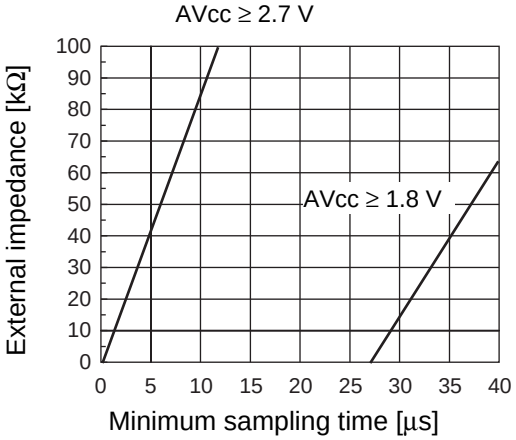
	R	C
2.7 V ≤ AVcc ≤ 3.6 V	1.7 kΩ (Max)	14.5 pF (Max)
1.8 V ≤ AVcc < 2.7 V	84 kΩ (Max)	25.2 pF (Max)

Note : The values are reference values.

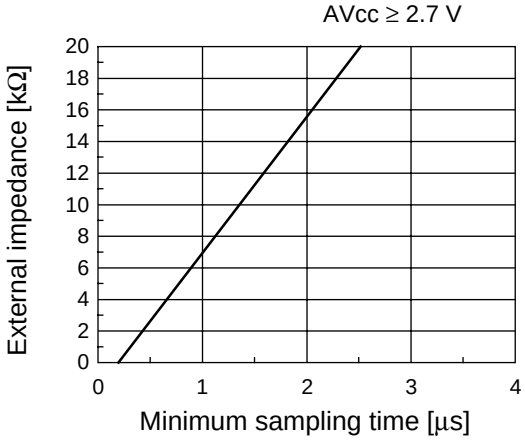
  - To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



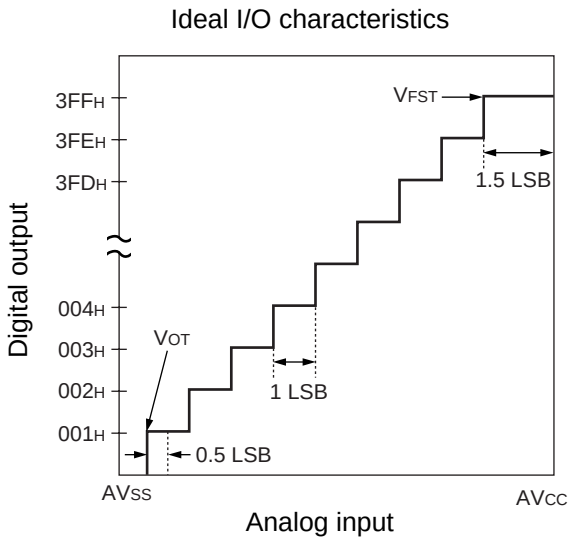
  - If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

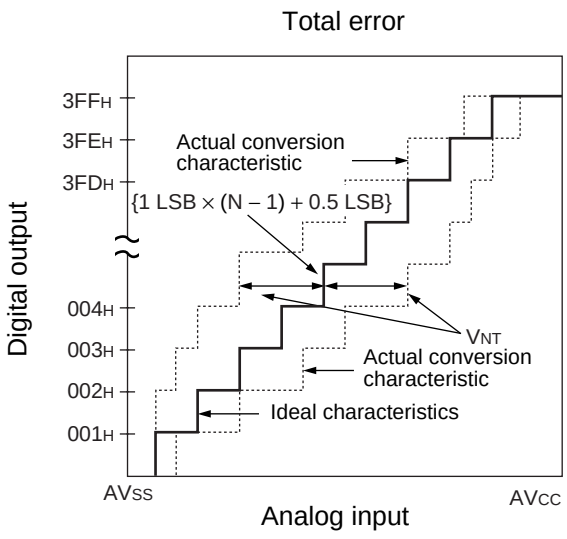
- **About errors**

As |AV_{CC} – AV_{SS}| becomes smaller, values of relative errors grow larger.

(3) Definition of A/D Converter Terms

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.





$$1\ \text{LSB} = \frac{AV_{CC} - AV_{SS}}{1024}\ \text{(V)}$$

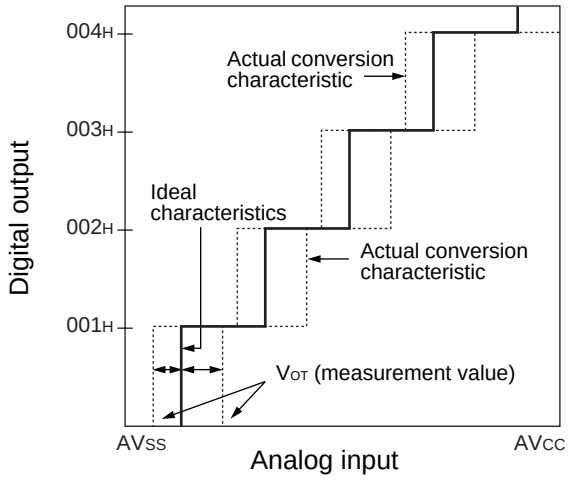
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1)\ + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

V_{NT} : A voltage at which digital output transits from (N – 1) to N.

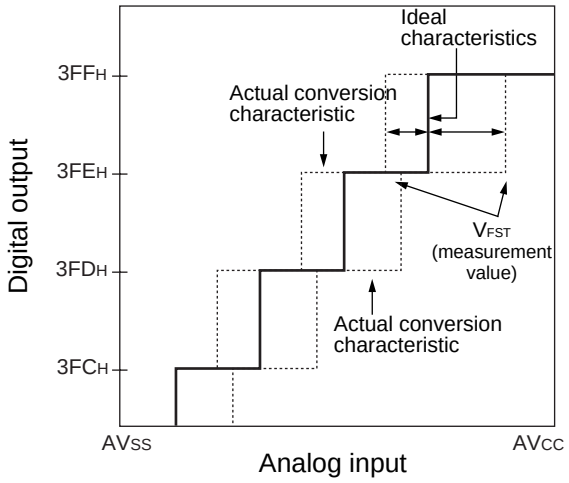
(Continued)

(Continued)

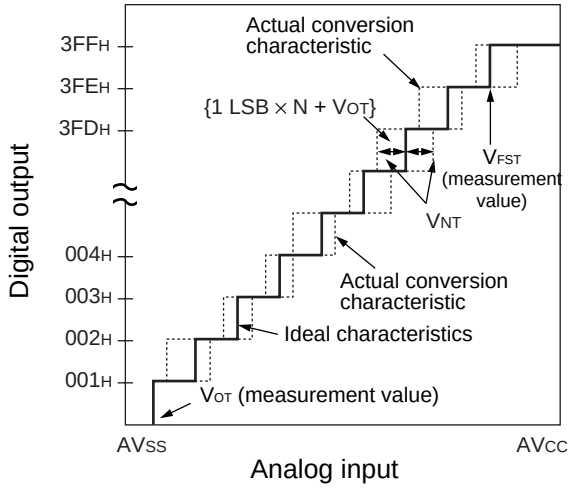
Zero transition error



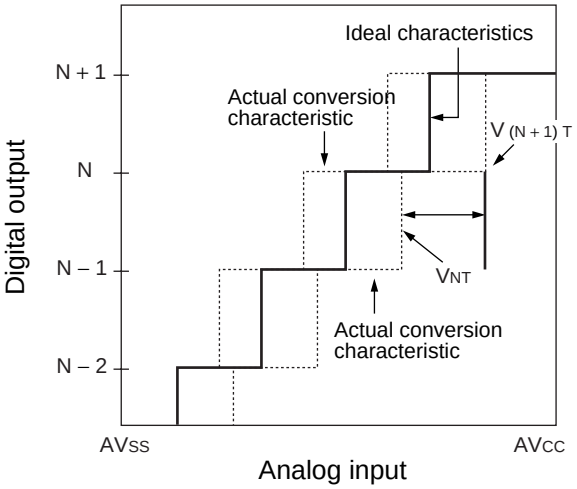
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

V_{NT} : A voltage at which digital output transits from (N – 1) to N.
V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = AV_{CC} – 1.5 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (4 Kbytes sector)	—	0.2*1	3*2	s	Excludes 00_H programming prior erasure
Sector erase time (16 Kbytes sector)	—	0.5*1	12*2	s	Excludes 00_H programming prior erasure
Byte programming time	—	32	3600	µs	Excludes system-level overhead
Erase/program cycle	10,000	—	—	cycle	
Power supply voltage at erase/program	2.7	—	3.3	V	
Flash data retension time	20*3	—	—	year	Average T_A = +85 °C

*1 : T_A = +25 °C, Vcc = 3.0 V, 10,000 cycles

*2 : T_A = +85 °C, Vcc = 2.7 V, 10,000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ MASK OPTIONS

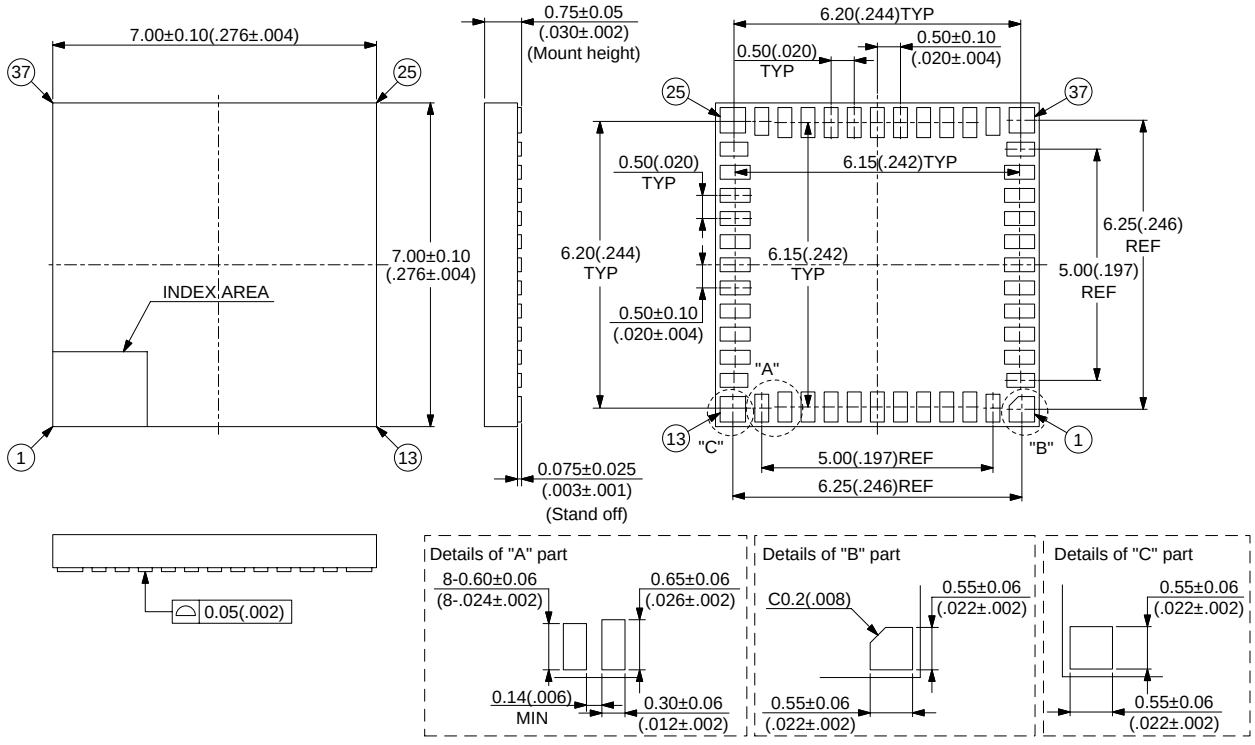
No	Part number	MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
	Specifying procedure	Specify when ordering MASK	Setting disabled	Setting disabled	Setting disabled
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Selectable	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Selection of oscillation stabilization wait time • Selectable the initial value of main clock oscillation stabilization wait time	Selectable 1 : (2^2 – 2) /F_{CH} 2 : (2^{12} – 2) /F_{CH} 3 : (2^{13} – 2) /F_{CH} 4 : (2^{14} – 2) /F_{CH}	Fixed to oscillation stabilization wait time of (2^{14}-2) /F_{CH}	Fixed to oscillation stabilization wait time of (2^{14}-2) /F_{CH}	Fixed to oscillation stabilization wait time of (2^{14}-2) /F_{CH}

■ ORDERING INFORMATION

Part number	Package	Remarks
MB95116APV MB95F118ASPV MB95F118AWPV	48-pin plastic BCC (LCC-48P-M09)	
MB95116APMT MB95F118ASPMT MB95F118AWPMT	48-pin plastic LQFP (FPT-48P-M26)	
MB2146-301 (MB95FV100A-101PBT)	MCU board (244-pin plastic PFBGA (BGA-244P-M08))	

■ PACKAGE DIMENSIONS

48-pin plastic BCC
(LCC-48P-M09)



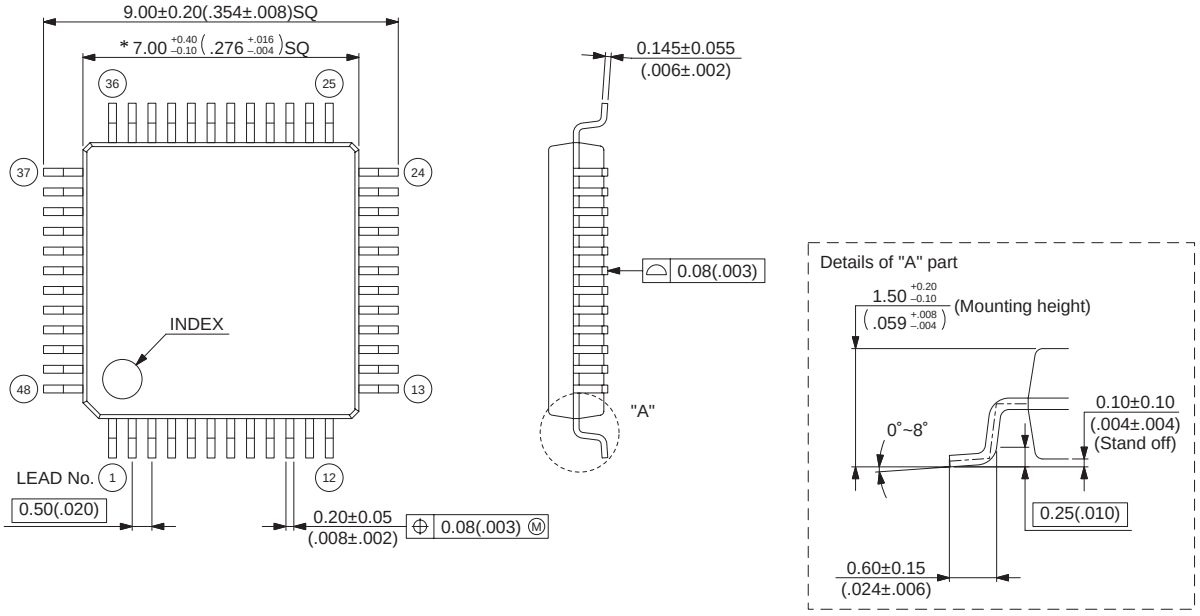
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

(Continued)

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0502