LH64258

CMOS 1M (256K × 4) Dynamic RAM

FEATURES

- 262,144 × 4 bit organization
- Access times: 100/120 ns (MAX.)
- Cycle times: 160/190 ns (MIN.)
- Cycle time in static column mode: 55/65 ns (MIN.)
- Power supply: +5 V ± 10%
- Power consumption (MAX.):
  Operating: 374/340 mW
  Standby: 11 mW
- TTL compatible I/O
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CS}$ before $\overline{RAS}$ refresh capability
- 512 refresh cycle
  (refresh period (MAX.) = 8 ms)
- Packages:
  20-pin, 300-mil DIP
  26-pin, 300-mil SOJ
  20-pin, 400-mil ZIP

DESCRIPTION

The LH64258 is a 262,144 word × 4 bit dynamic RAM which provides a static column mode operation.

The LH64258 is fabricated using advanced CMOS process technology. With multiplexed address inputs and standard 20-pin DIP/ZIP or 26-pin SOJ packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH64258 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

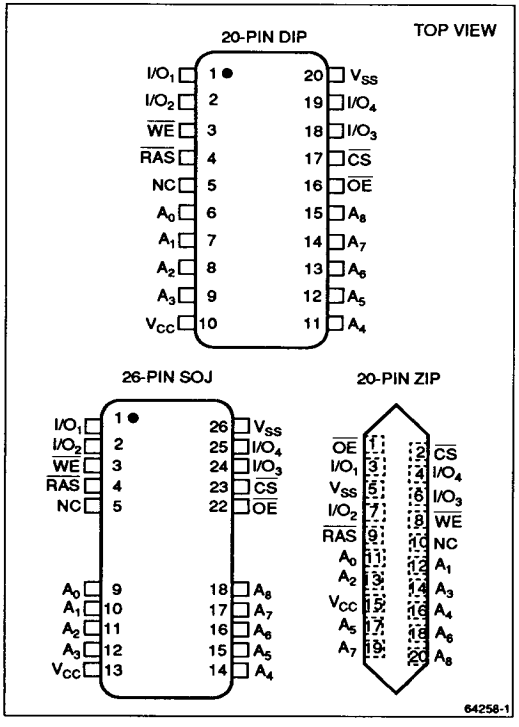

Figure 1. Pin Connections for DIP, SOJ, and ZIP Packages

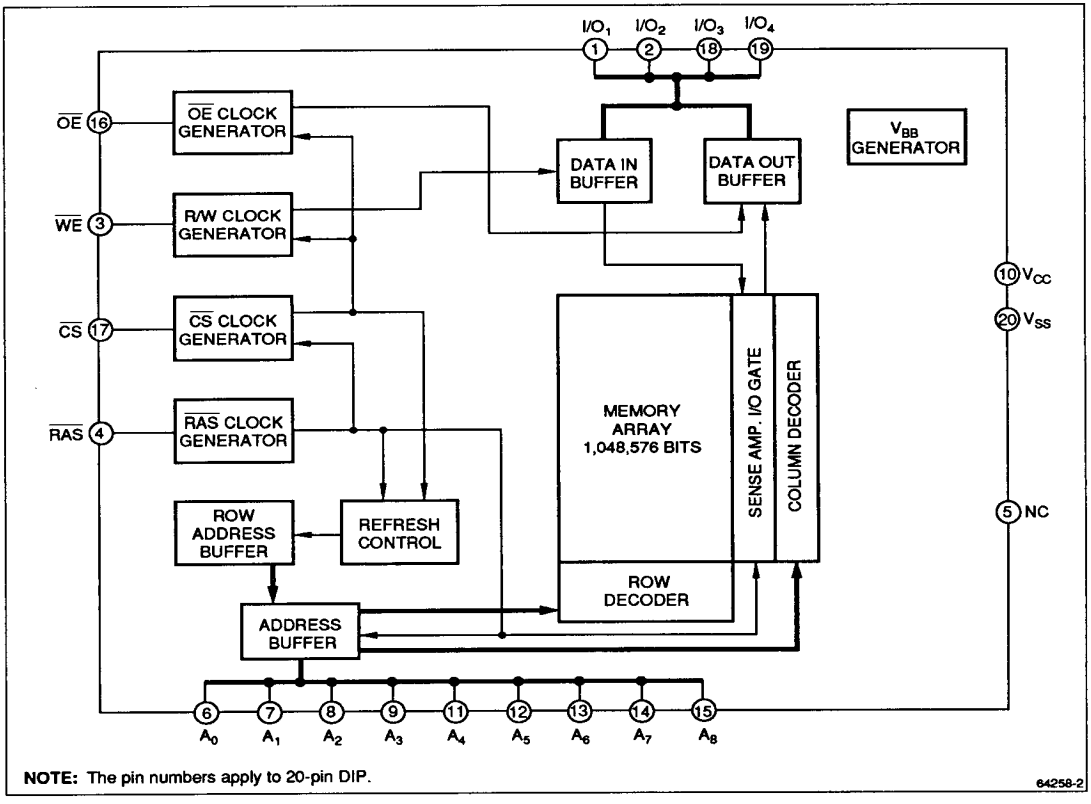

Figure 2. LH64258 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_8	Address input
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip Select
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Output short-circuit current	I_O	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8		1

NOTE:
1. Referenced to V_{SS}

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH64258-10	I_{CC1}	—	68(80)	mA	1, 2, 3
	LH64258-12		—	62(68)		
Average supply current in standby mode		I_{CC2}	—	2.0	mA	1
Average supply current in the static column mode	LH64258-10	I_{CC3}	—	60	mA	1, 2
	LH64258-12		—	55		
Average supply current in $\overline{CS}$ before $\overline{RAS}$ refresh cycle	LH64258-10	I_{CC4}	—	68(80)	mA	1, 2, 3
	LH64258-12		—	62(68)		
Average supply current in $\overline{RAS}$ only refresh cycle	LH64258-10	I_{CC5}	—	68(80)	mA	1, 2, 3
	LH64258-12		—	62(68)		
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	I_{L1}	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	I_{LO}	-10	10	µA	
Output "High" voltage	I_{OUT} = -5 mA	V_{OH}	2.4	—	V	
Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on the cycle time.
3. Cycle time: 190 ns (LH64258-10), 220 ns (LH64258-12).
   Figures in parenthesis indicate current under minimum cycle time operation.
   Address transition is occurs when $\overline{RAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	A_1 - A_7	C_{IN1}	—		5	pF
	A_0, A_8	CIN2	—		8	pF
	$\overline{OE}$, $\overline{CS}$	C_{IN3}	—		8	pF
	$\overline{RAS}$, $\overline{WE}$	C_{IN4}	—		5	pF
Input/Output capacitance	I/O_1 - I/O_4	C_{OUT1}	—		10	pF

AC ELECTRICAL CHARACTERISTICS [1, 2, 3, 4] (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH64258-10		LH64258-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
(1) READ CYCLE							
Random read or write cycle time	t_{RC}	160		190		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	7
Access time from $\overline{CS}$	t_{ACS}		25		30	ns	7
Access time from column address	t_{AA}		50		60	ns	7
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	7
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address delay time ($\overline{RAS}$)	t_{RAD}	20	50	20	60	ns	5
Column address lead time ($\overline{RAS}$)	t_{RAL}	50		60		ns	
Column address hold time ($\overline{RAS}$)	t_{AHR}	15		15		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		ns	
$\overline{CS}$ precharge time ($\overline{RAS}$ fall)	t_{CRP}	0		0		ns	
$\overline{CS}$ delay time ($\overline{RAS}$)	t_{RCD}	25	75	35	90	ns	6
$\overline{CS}$ lead time ($\overline{RAS}$)	t_{RSL}	25		30		ns	
$\overline{OE}$ command $\overline{RAS}$ lead time	t_{ROL}	0		0		ns	
Output data disable time ($\overline{CS}$)	t_{OFF}		25		30	ns	
Output data disable time ($\overline{OE}$)	t_{OEZ}		25		30	ns	
Output data hold time (address)	t_{AOH}	5		5		ns	
Output data hold time ($\overline{CS}$)	t_{SOH}	0		0		ns	
Output data hold time ($\overline{OE}$)	t_{OOH}	0		0		ns	
Read command set-up time ($\overline{CS}$)	t_{RCS}	0		0		ns	
Read command hold time ($\overline{CS}$)	t_{RCH}	10		10		ns	8
Read command hold time ($\overline{RAS}$ fall)	t_{RRHN}	110		130		ns	8
Read command hold time ($\overline{RAS}$ rise)	t_{RRHP}	10		10		ns	8
Transition time (rise and fall)	t_T	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8	ms	
(2) STATIC COLUMN MODE READ CYCLE							
Static column mode cycle time	t_{SC}	55		65		ns	
Column address hold time ($\overline{RAS}$)	t_{AR}	100		120		ns	
(3) WRITE CYCLE (EARLY WRITE)							
Column address set-up time ($\overline{CS}$)	t_{ASC}	0		0		ns	
Column address hold time ($\overline{CS}$)	t_{CAH}	20		20		ns	
Write command set-up time ($\overline{CS}$)	t_{WCS}	0		0		ns	9
Write command hold time ($\overline{CS}$)	t_{WCH}	15		20		ns	
Data input set-up time	t_{DS}	0		0		ns	
Data input hold time	t_{DH}	20		20		ns	
Write pulse width ($\overline{CS}$)	t_{WP}	15		20		ns	
($\overline{OE}$ CONTROL WRITE)							
$\overline{CS}$ set-up time ($\overline{WE}$)	t_{CWS}	0		0		ns	9
$\overline{CS}$ hold time ($\overline{WE}$)	t_{CWH}	15		20		ns	
Write command lead time ($\overline{RAS}$)	t_{RWL}	30		40		ns	
Write pulse width ($\overline{WE}$)	t_{WP}	15		20		ns	
$\overline{OE}$ hold time ($\overline{WE}$)	t_{OEH}	20		20		ns	10
Column address set-up time ($\overline{WE}$)	t_{ASW}	0		0		ns	
Column address hold time ($\overline{WE}$)	t_{WAH}	20		20		ns	

See next page for notes.

PARAMETER	SYMBOL	LH64258-10		LH64258-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
(4) READ-WRITE CYCLE							
Read-write cycle time	t_{RWC}	225		270		ns	
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	135		160		ns	
Column address delay time ($\overline{WE}$)	t_{AWD}	85		100		ns	
$\overline{WE}$ delay time ($\overline{CS}$)	t_{CWD}	60		70		ns	
$\overline{OE}$ delay time	t_{OED}	25		30		ns	
(5) STATIC COLUMN MODE WRITE CYCLE							
$\overline{WE}$ inactive time	t_{WI}	10		15		ns	
$\overline{CS}$ inactive time	t_{CI}	10		15		ns	
$\overline{CS}$ set-up time ($\overline{WE}$)	t_{CWS}	15		20		ns	11
Write command delay time ($\overline{RAS}$)	t_{RWD2}	100		120		ns	
(6) $\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE/HIDDEN REFRESH CYCLE							
$\overline{CS}$ set-up time ($\overline{RAS}$)	t_{CSR}	0		0		ns	
$\overline{CS}$ hold time ($\overline{RAS}$)	t_{CHR}	20		25		ns	
$\overline{CS}$ precharge time ($\overline{RAS}$ rise)	t_{RPCP}	10		10		ns	
$\overline{WE}$ precharge time ($\overline{RAS}$)	t_{WRP}	0		0		ns	
$\overline{CS}$ precharge time ($\overline{RAS}$ fall)	t_{RCPN}	100		120		ns	

NOTES:

1. For proper operation, at least 500 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristics assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. I_{CC} when power on depends on $\overline{RAS}$ input level.
   If $\overline{RAS}$ = V_{IL} when power on, LSI goes into an active cycle and may have a large current I_{CC}. It is recommended to rise $\overline{RAS}$ with V_{CC} or fix at V_{IH}, when power on.
5. t_{RAD} (MAX.), is the maximum point for t_{RAD} where t_{AA} (MAX.) is ensured, and does not represent a limit of operation.
   If $t_{RAD} \geq t_{RAD}$ (MAX.), the access time comes under the control of t_{AA}.
6. t_{RCD} (MAX.) is the maximum point for t_{RCD} where t_{ACS} (MAX.) is ensured, and does not represent a limit of operation.
   If $t_{RCD} \geq t_{RCD}$ (MAX.), the access time comes under the control of t_{ACS}.
7. 2TTL + 100 pF load
8. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.
9. t_{WCS}, t_{CWS} are not restrictive operating parameters. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out buffers remain inactive throughout entire cycle.
10. t_{OEH} is required to keep I/O pin floating.
    When $\overline{OE}$ goes "Low" with $\overline{CS}$ = "Low" and $\overline{WE}$ = "High", I/O pin is used to output data as written.
11. t_{CWS} is not restrictive operating parameter. When $t_{CWS} \leq t_{CWS}$ (MIN.), it may come into early write cycle.

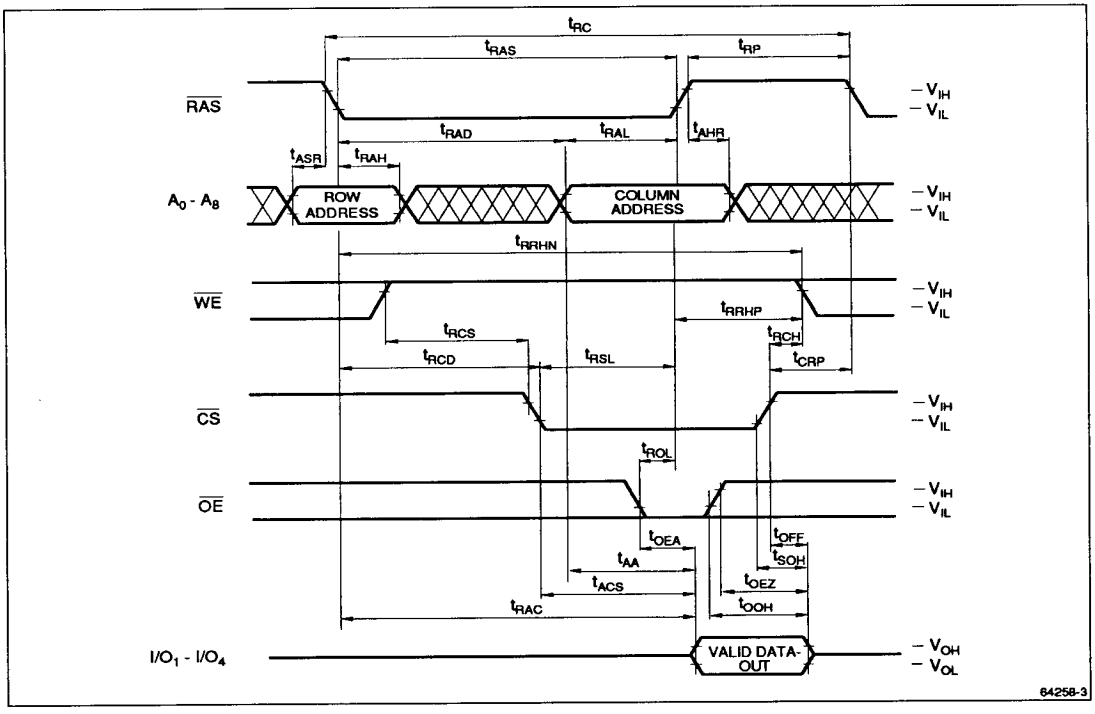

Figure 3. Read Cycle

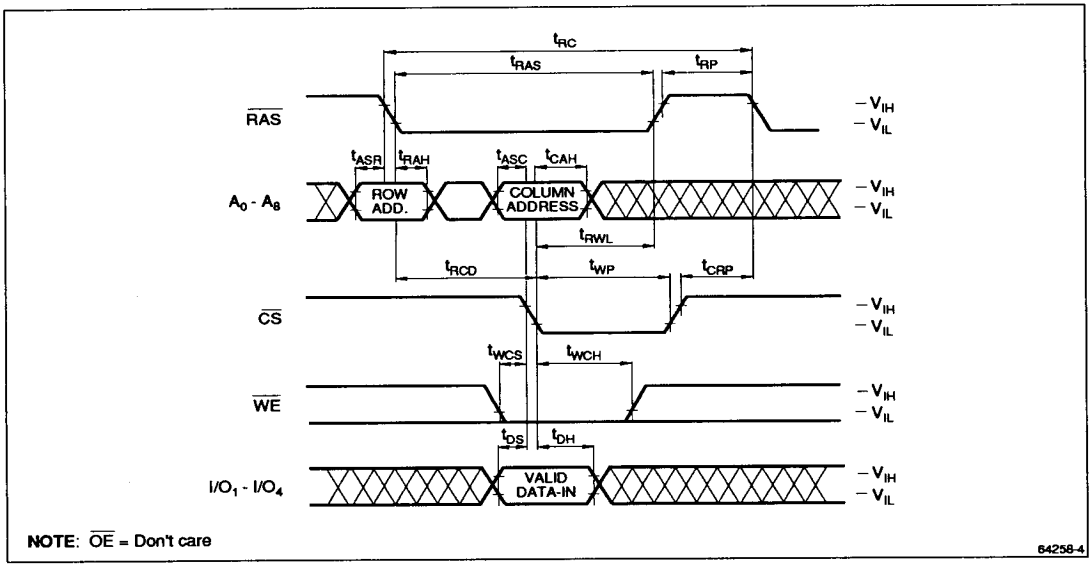

Figure 4. Write Cycle (Early Write)

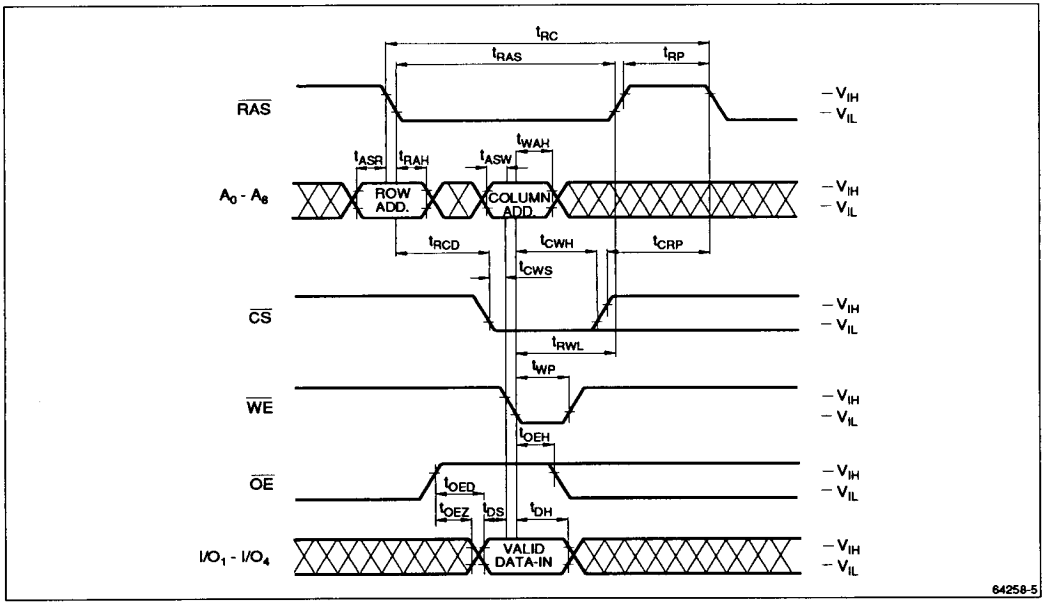

Figure 5. Write cycle ($\overline{OE}$ Controlled Write)

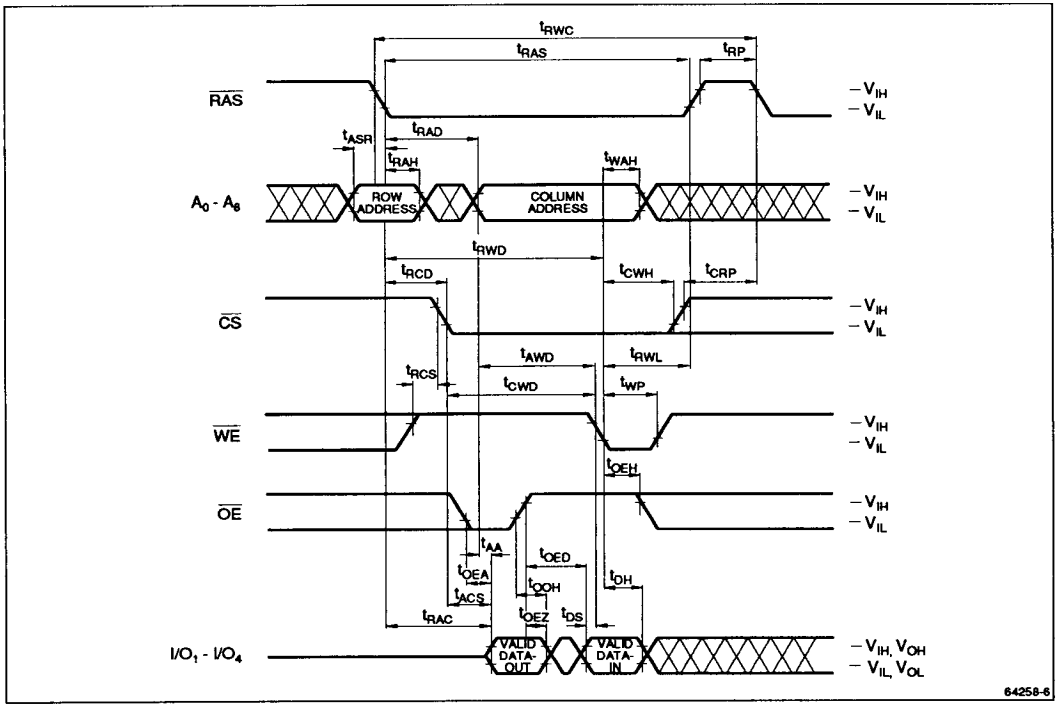

Figure 6. Read/Write Cycle

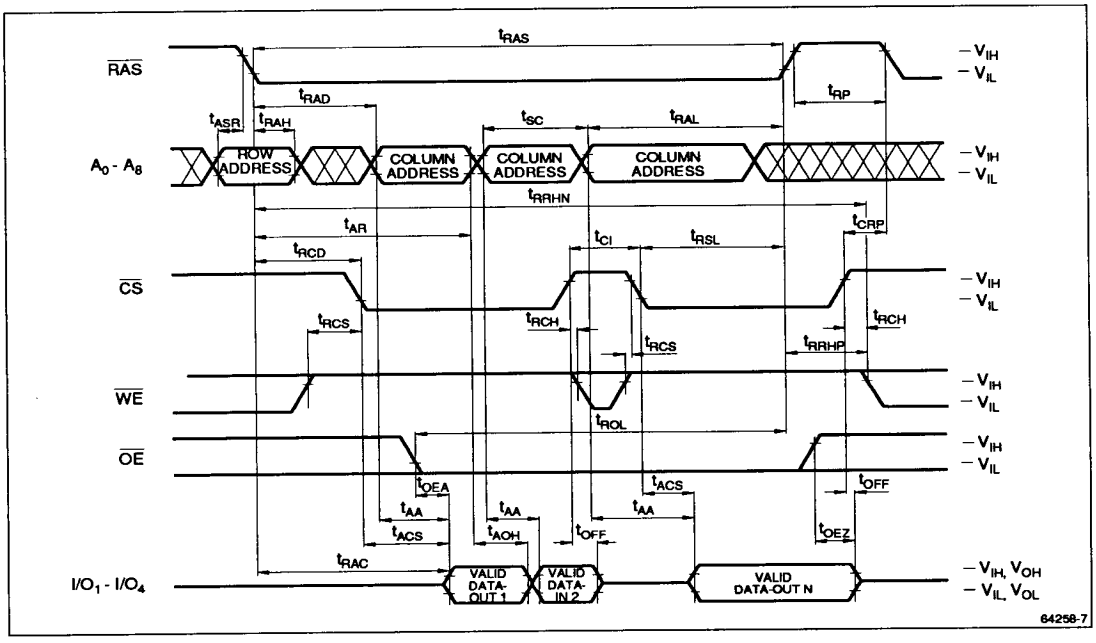

Figure 7. Static Column Mode Read Cycle

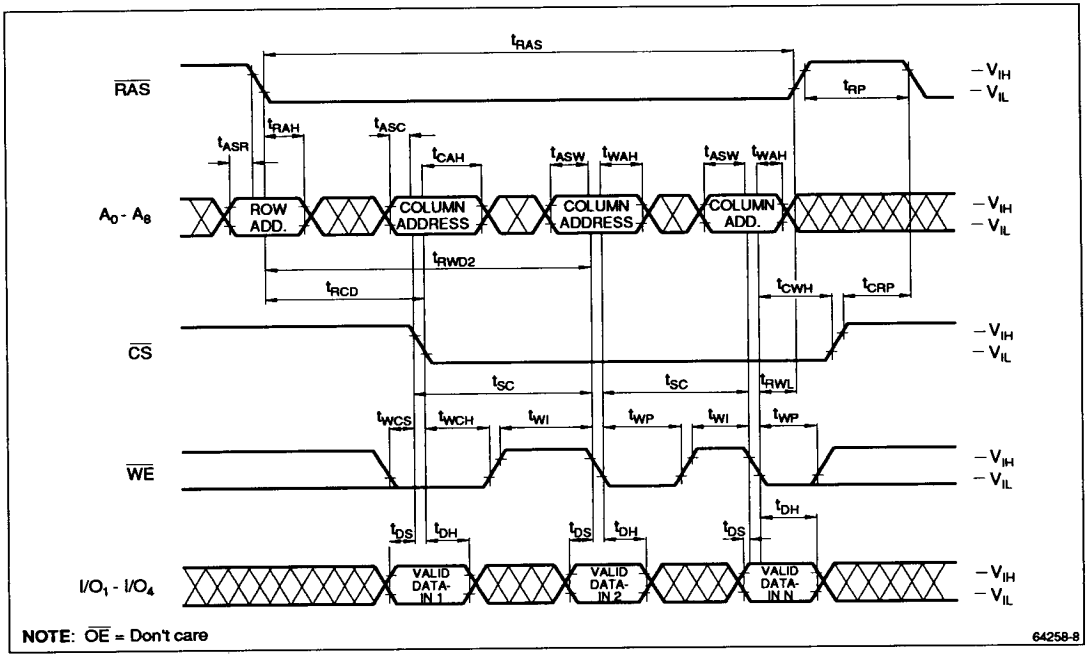

Figure 8. Static Column Mode Write Cycle (Early Write)

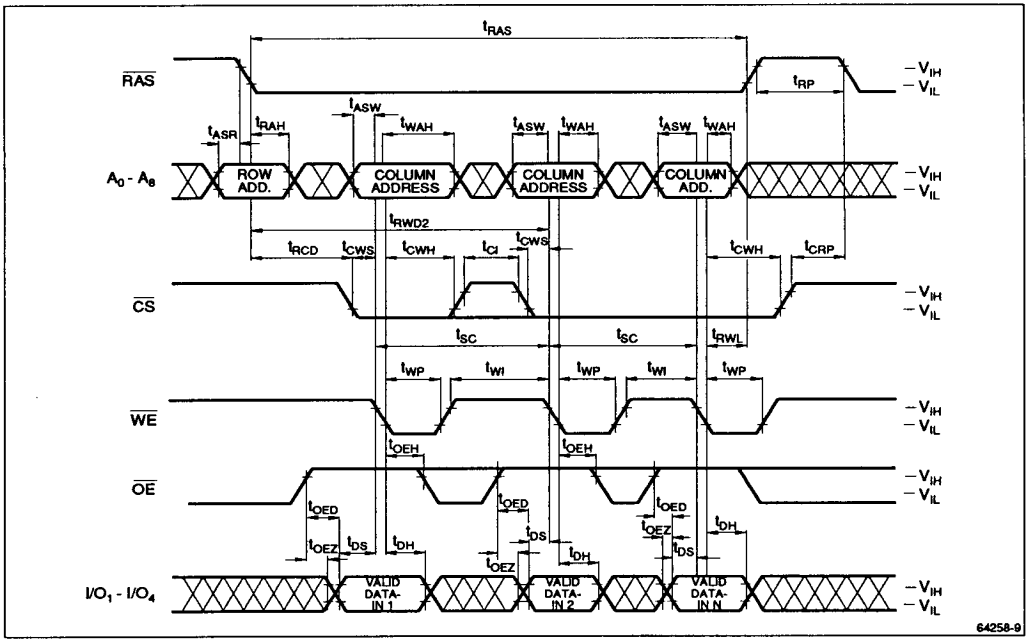

Figure 9. Static Column Mode Write Cycle ($\overline{OE}$ Control Write)

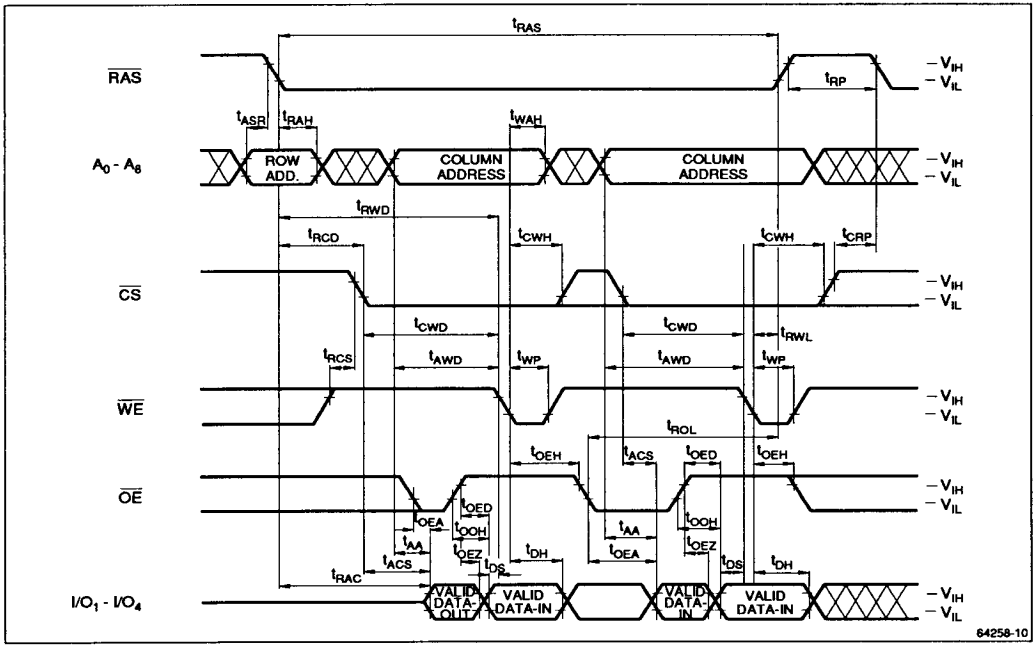

Figure 10. Static Column Mode Read/Write Cycle

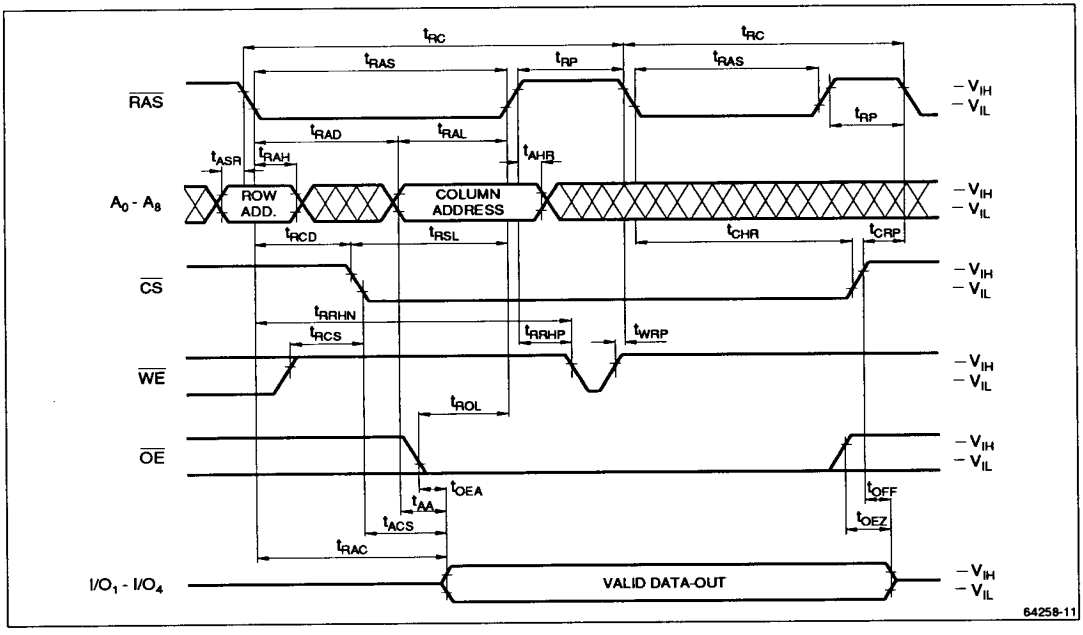

Figure 11. Hidden Refresh Cycle

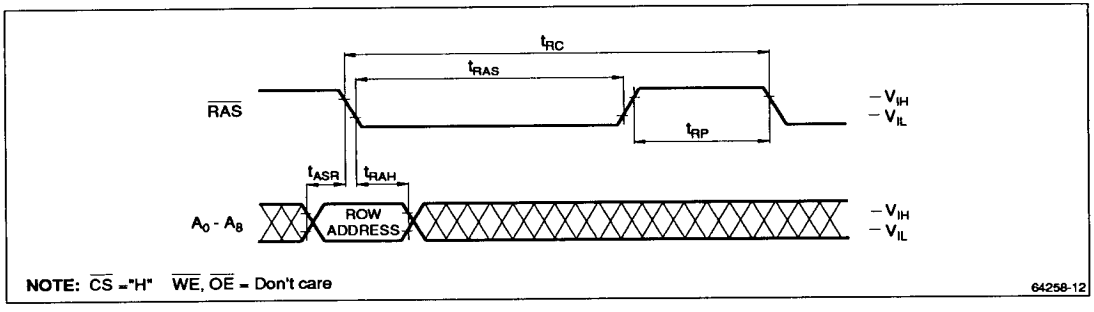

Figure 12. $\overline{RAS}$ Only Refresh Cycle

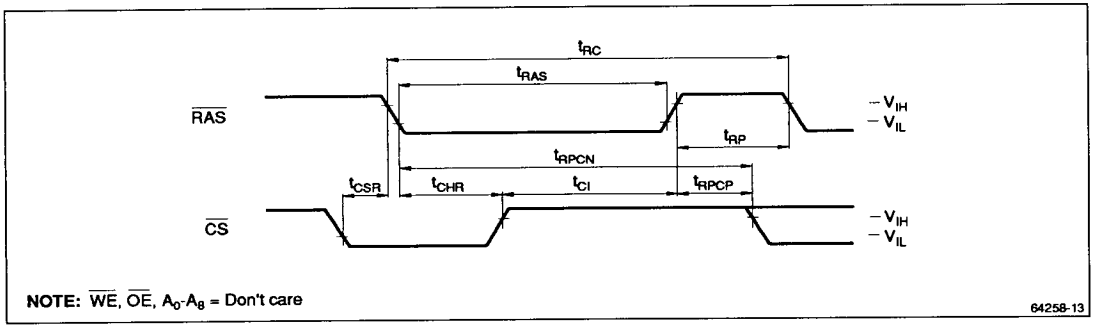

Figure 13. $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

ORDERING INFORMATION