BL8589

16-Channel Constant-Current LED Driver

DESCRIPTION

The BL8589 is designed for LED display applications. The device has an input shift register with corresponding data latches and 16 constant current sink drivers.

The device support digital input with internal shift registers and latches, hence can be controlled directly by microprocessor-based systems. With a standard 3.3V or 5V logic supply, serial data input rates can reach up to 30 MHz. The BL8589 allows user defined maximum LED drive current level which is set by a single external resistor. Chip build-in serial data output permits cascading of multiple devices in applications requiring additional drive lines.

The BL8589 is available in a variety of 24-terminal packages: QFN44-24, which has an exposed thermal pad, SSOP-24 and TSSOP-24. All packages are lead (Pb) free and RoHS compliable.

FEATURES

- 16 constant-current output channels, with maximum current capability up to 50 mA each
- 3.0 to 5.5 V logic supply range
- Schmitt trigger inputs for improved noise Immunity
- Power-On Reset , all register bits=0
- Low-power CMOS logic and latches
- High data input rate: 30MHz
- Output current accuracy: between channels < ±3% and between ICs ±6%, over the full operating temperature range
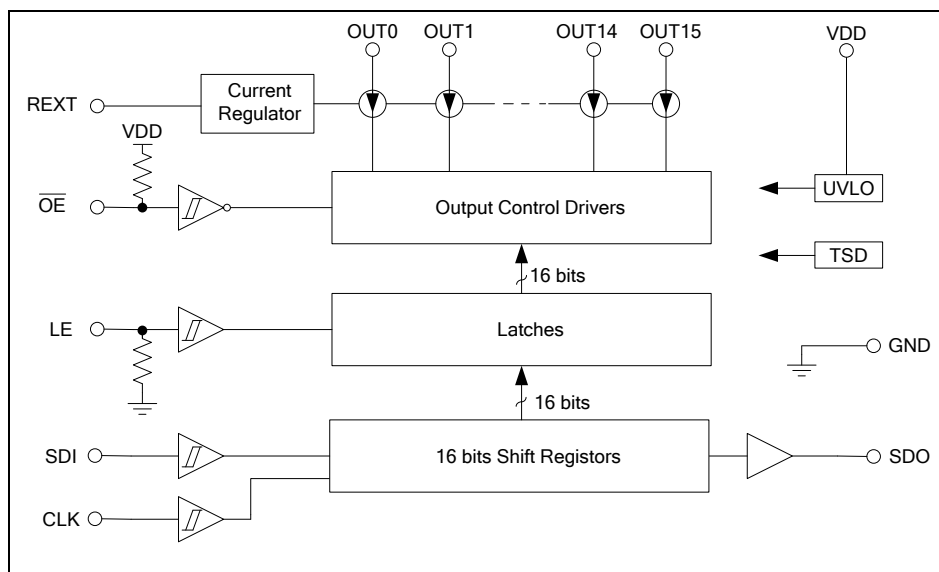- Internal UVLO and thermal shutdown (TSD) circuitry

APPLICATIONS

- Single-color, multicolor, or full-color LED display
- Single-color, multicolor, or full-color LED signboard
- Display backlighting
- Multicolor LED lighting

TYPICAL APPLICATION
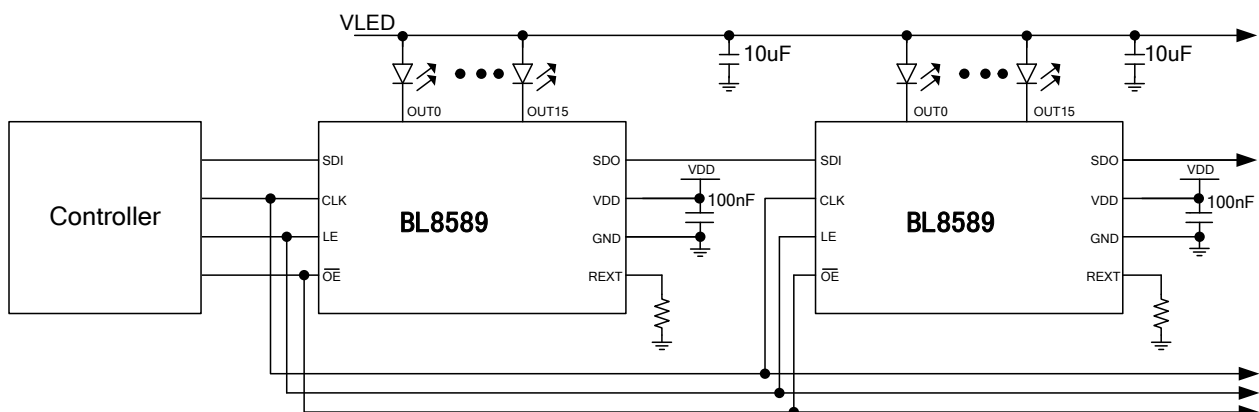
FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

Name	Number			Description
	QFN44-24	TSSOP-24 & SSOP-24		
CLK	6	3	3	Clock, data shift clock input terminal
GND	4	1	1	Ground
LE	7	4	4	Latch Enable input terminal, active high
$\overline{OE}$	24	21	21	Output Enable input terminal, active low
OUT0	8	5	5	Constant current outputs
OUT1	9	6	6	
OUT2	10	7	7	
OUT3	11	8	8	
OUT4	12	9	9	
OUT5	13	10	10	
OUT6	14	11	11	
OUT7	15	12	12	
OUT8	16	13	13	
OUT9	17	14	14	
OUT10	18	15	15	
OUT11	19	16	16	
OUT12	20	17	17	
OUT13	21	18	18	
OUT14	22	19	19	
OUT15	23	20	20	
PAD	-	-	-	Exposed pad for enhanced thermal dissipation, not connected internally, connect to GND.
REXT	2	23	23	Reference current terminal, sets output current for all channels
SDI	5	2	2	Serial Data in terminal
SDO	1	22	22	Serial Data out terminal
VDD	3	24	24	Logic supply terminal

PIN CONFIGURATION

QFN44
Top View
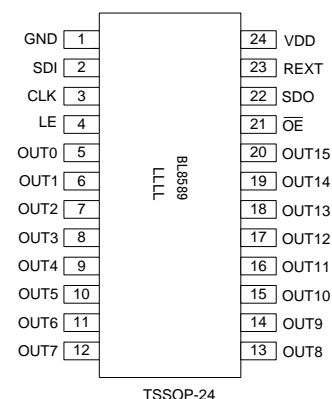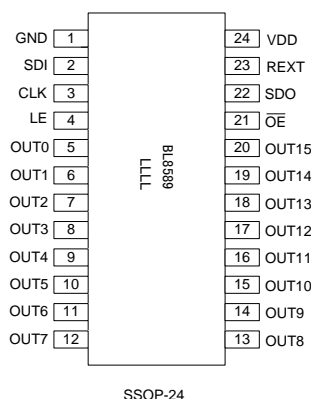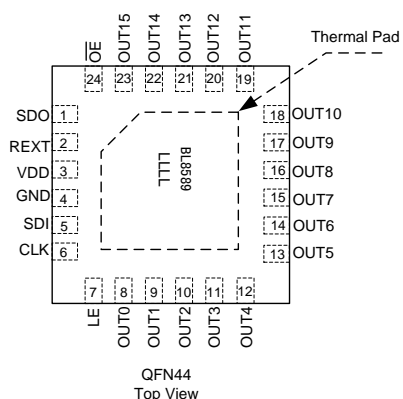
SSOP-24

Marking: LLLL: LOT No.

TSSOP-24

ORDERING INFORMATION

Product NO	Ordering Number	Pin Package	Devices per reel	Temperature range & Rohs
BL8589	BL8589CJLTR	QFN44-24	3000	-40~150°C & Pb free
BL8589	BL8589CPOTR	SSOP-24	2000	-40~150°C & Pb free
BL8589	BL8589CQOTR	TSSOP-24	2000	-40~150°C & Pb free

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Units
Supply Voltage	VDD	0~8.0	V
Input Voltage Range	V_{SDI}, V_{CLK}, V_{LE}, $V_{\overline{OE}}$	-0.3~VDD+0.3	V
OUT(X) Output Current	$I_{OUT(X)}$	+65	mA
OUT(X) Voltage Range	$V_{OUT(X)}$	-0.3~12	V
Clock Frequency	f_{CLK}	30	MHz
ESD Rating	HBM	2.0	KV
	CDM	1.0	KV
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55~165	°C

ELECTRICAL CHARACTERISTICS

(Test Conditions: T_A[1]=25°C, VDD=3.0 to 5.5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ[2]	Max.	Units
VDD	Input Voltage	Operating	3.0	5.0	5.5	V
VDD(UV)	Under voltage Lockout	VDD 0→5V	2.5	2.7	2.9	V
		VDD 5→0V	2.3	2.5	2.7	V
$I_{OUT(X)}$	Output Current	VDD=4.5 to 5.5V, $V_{OUT(X)}$=1V, R_{REXT}=374Ω	47.4	51.1	54.5	mA
		VDD=3.0 to 3.6V, $V_{OUT(X)}$=1V, R_{REXT}=374Ω	46.5	50.1	53.5	mA
		VDD=4.5 to 5.5V, $V_{OUT(X)}$=1V, R_{REXT}=910Ω	19.8	21.4	22.8	mA
		VDD=3.0 to 3.6V, $V_{OUT(X)}$=1V, R_{REXT}=910Ω	19.5	21.0	22.4	mA

ELECTRICAL CHARACTERISTICS (Continued)

(Test Conditions: $T_A{}^1$=25°C, VDD=3.0 to 5.5V, unless otherwise specified.)

‰Δ $I_{OUT(X)}$	Output Current Shift	VDD=5.5V, $V_{OUT(X)}$=1V, R_{REXT} =910Ω , TA=25°C; between one output on and all outputs on	-	-	±1	%
Err	Out to Out Matching[3]	$V_{OUT(X)}$=1V, R_{REXT} =374Ω , all outputs on	-	±1	±3	%
		$V_{OUT(X)}$=1V, R_{REXT} =910Ω , all outputs on	-	±1	±3	%
‰Δ $I_{OUT(X)(REG)}$	Output Current Regulation	VDD=5.5V, $V_{OUT(X)}$=1 to 3V, R_{REXT} =374Ω , all outputs on	-	1.7	3	%
		VDD=5.5V, $V_{OUT(X)}$=1 to 3V, R_{REXT}=910Ω , all outputs on	-	2.4	4	%
		VDD=3.6V, $V_{OUT(X)}$=1 to 3V, R_{REXT} =374Ω , all outputs on	-	1.2	2	%
		VDD=3.6V, $V_{OUT(X)}$=1 to 3V, R_{REXT} =910Ω , all outputs on	-	1.8	3	%
$I_{OUT(X)LK}$	Output Leakage Current	$V_{OUT(X)}$=12V, $V_{\overline{OE}}$=Logic "1"	-	-	0.5	uA
V_{IH}	Logic Input Voltage		0.8*VDD	-	VDD	V
V_{IL}			GND	-	0.2*GND	V
V_{IHYS}	Logic Input Voltage Hysteresis	All digital inputs	250	-	900	mV
I_L	Logic Input Current	All digital inputs	-1	-	1	uA
V_{OL}	SDO Voltage	I_{OL}=1mA	-	-	0.5	V
V_{OH}		I_{OH}=-1mA	VDD-0.5	-	-	V
$I_{VDD(OFF)}$		R_{REXT} =3.8kΩ, $V_{\overline{OE}}$=Logic "1"	-	-	6	mA
		R_{REXT} =910Ω, $V_{\overline{OE}}$ = Logic "1"	-	-	16	mA
		R_{REXT} =374Ω, $V_{\overline{OE}}$ = Logic "1"	-	-	40	mA
$I_{VDD(ON)}$	Supply Current[4]	All outputs on, R_{REXT} =910Ω, $V_{OUT(X)}$=1V, Data transfer 30MHz	-	-	20	mA
		All outputs on, R_{REXT} =374Ω, $V_{OUT(X)}$=1V, Data transfer 30MHz	-	-	45	mA
V_{REXT}	Reference Voltage	R_{REXT} =374Ω	-	1.21	-	V
T_{JTSD}	Thermal Shutdown	Temperature Increasing	-	150	-	°C
$T_{JTSDhys}$	Thermal Shutdown Hysterisis	Temperature Decreasing	-	30	-	°C

BL8589

SWITCHING CHARACTERISTICS

(Test Conditions: $T_A{}^1$=25°C, V_{IH}=VDD=5.0V, $V_{OUT(X)}$=1V, V_{IL}=0V, R_{REXT}=910Ω , V_L=2V, RL=51Ω , C_L=15pF(see also Timing section).

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Units
f_{CLK}	Clock Frequency		-	-	30	MHz
f_{CLKC}	Clock Frequency (cascade devices)		-	-	25	MHz
t_{wh0}	Clock pulse duration	CLK= Logic "1"	16	-	-	ns
t_{wh1}	LE pulse duration	LE= Logic "1"	20	-	-	ns
t_{su0}	Setup Time	SDI to CLK ↑	10	-	-	ns
t_{su1}		CLK ↑ to LE ↑	10	-	-	ns
t_{h0}	Hold Time	CLK ↑ to SDI	10	-	-	ns
t_{h1}		LE ↓ to CLK ↑	10	-	-	ns
t_{r0}	Rise Time	SDO, 10/90% points (measurement circuit A)	-	-	16	ns
t_{r1}		OUTx, VDD=5V, 10/90% points (measurement circuit B)	-	10	30	ns
t_{f0}	Fall Time	SDO, 10/90% points (measurement circuit A)	-	-	16	ns
t_{f1}		OUTx, VDD=5V, 10/90% points (measurement circuit B)	-	10	30	ns
t_{pd0}	Propagation Delay Time	CLK ↑ to SDO (measurement circuit A)	-	-	30	ns
t_{pd1}		$\overline{OE}$ ↓ to OUTx (measurement circuit B)	-	-	60	ns
t_{pd2}		LE ↑ to OUTx (measurement circuit B)	-	-	60	ns
$t_{w(\overline{OE})}$	Output Enable Pulse Duration	(see Timing Diagrams section)	60	-	-	ns

[1] Tested at 25°C. Specifications are assured by design and characterization over the operating temperature range of –40°C to 85°C.
[2] Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[3] Err = (I_O(min or max) – I_O(av)) / I_O(av). I_O(av) is the average current of all outputs. I_O(min or max) is the output current with the greatest Difference from I_O(av).
[4] Recommended operating range: V_O = 1.0 to 3.0 V.

INPUT-OUTPUT TRUTH TABLE

SDI	CLK	Shift Register Contents I_0 I_1 I_2 … I_{15}		SDO	LE	Latch Contents I_0 I_1 I_2 … I_{15}	$\overline{OE}$	Output Contents I_0 I_1 I_2 … I_{15}
H	⌐	H R_0 R_1 … R_{14}		R_{15}				
L	⌐	L R_0 R_1 … R_{14}		R_{15}				
X	⌐	R_0 R_1 R_2 … R_{15}		X				
		X X X … X			L	R_0 R_1 R_2 … R_{15}		
		P_0 P_1 P_2 … P_{15}			H	P_0 P_1 P_2 … P_{15}	L	P_0 P_1 P_2 … P_{15}
						X X X … X	H	Hiz Hiz Hiz… Hiz

L = Low logic (voltage) input, H = High logic (voltage) input, X = Don't care, P = Present state, R = Previous state，Hiz=High impedance
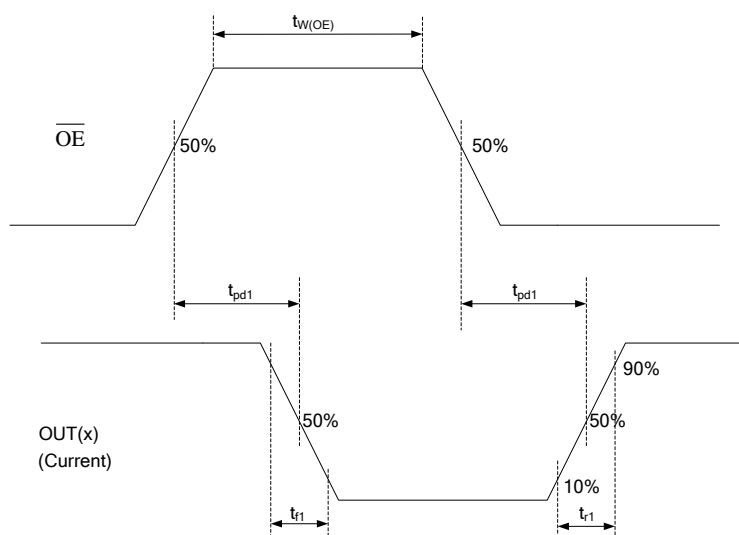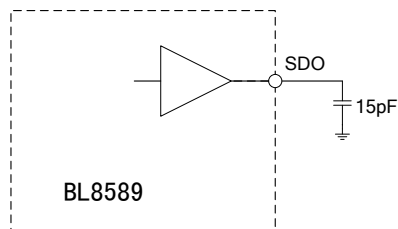
BL8589

TIMING DIAGRAMS

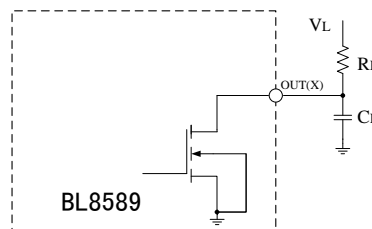|	Do not care		On status		High impedance
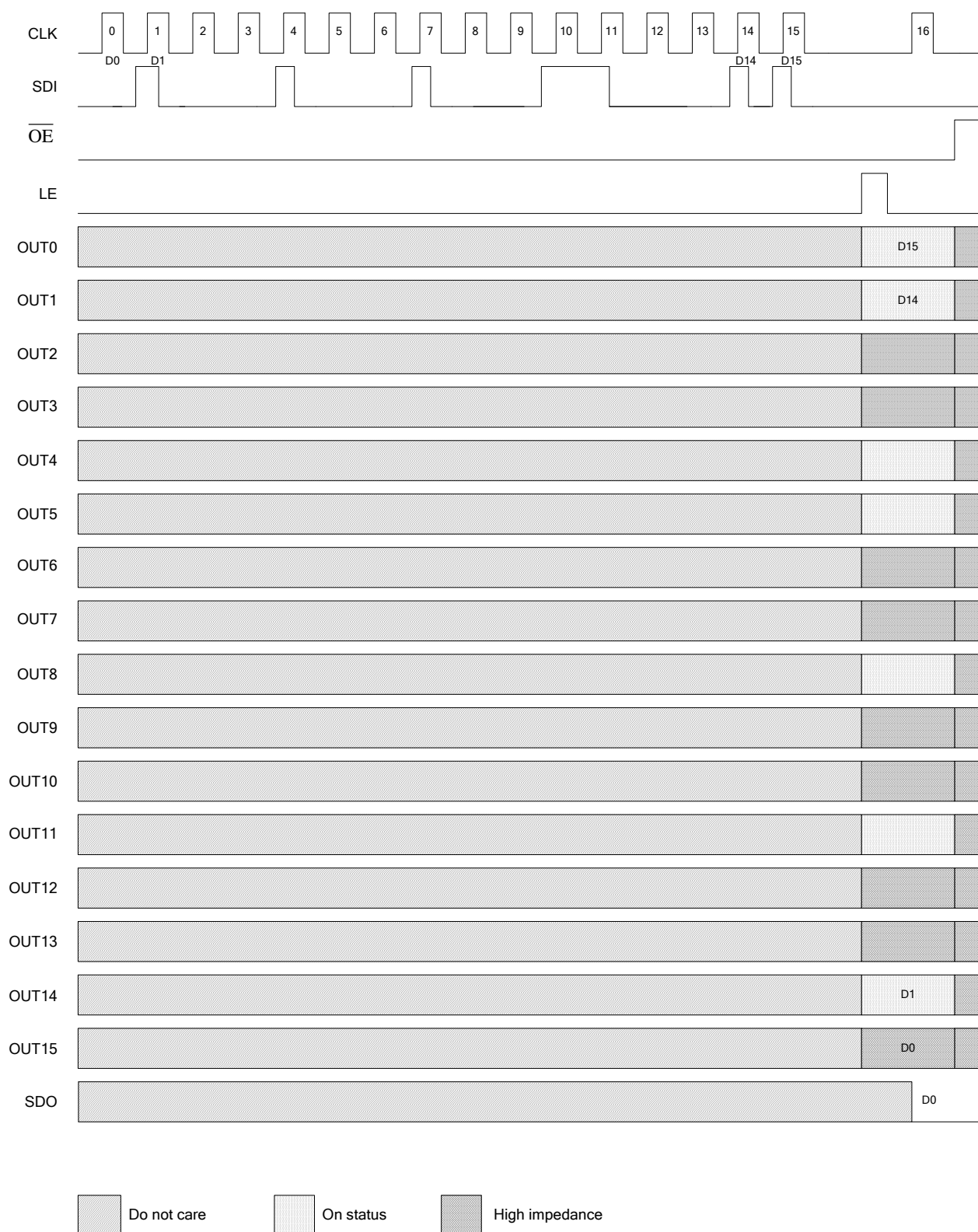
TIMING DIAGRAMS (Continued)
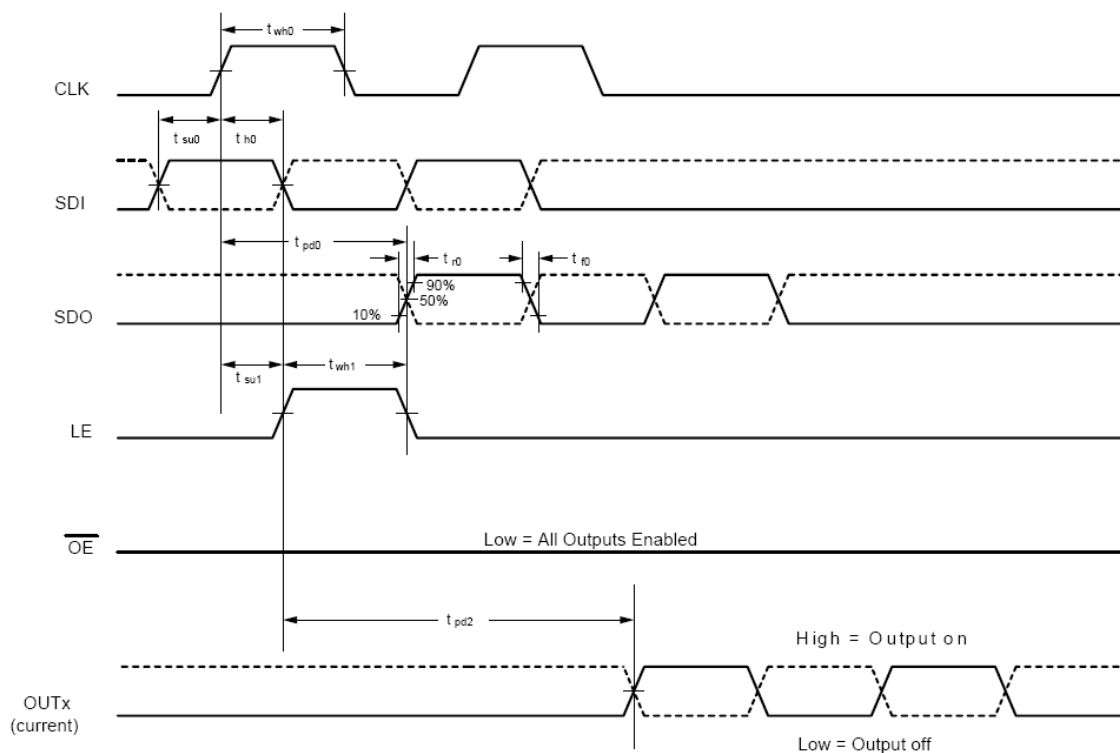
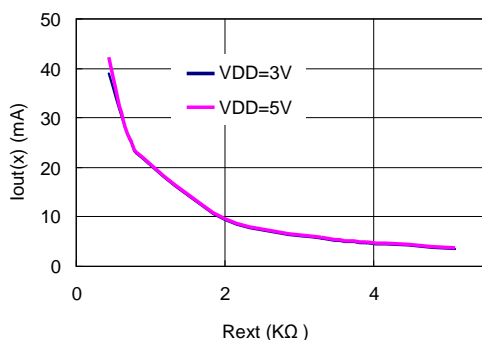*Disabling Outputs*

PARAMETER MEASUREMENT CIRCUITS

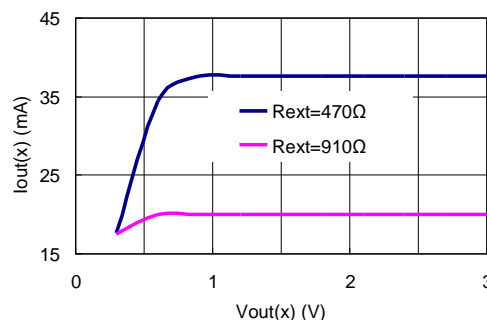(A) Circuit for t_{f0}, t_{pd0}, t_{r0}

(B) Circuit for t_{f1}, t_{pd1}, t_{pd2} and t_{r1}

OPERATING CHARACTERISTICS

Channel Output Current vs External Resistance

Channel Output Current vs OUT(X) Voltage

APPLICATION INFORMATION

Normal Operation

A CLK (Clock) input pulse or more specifically the rising edge of the CLK starts the transfer of serial data from the SDI (Serial Data In) input to the shift register. For proper and accurate transfer, the serial data must appear at the input prior to the rising edge of the CLK waveform. The register stores the SDI data and forward to the SDO (Serial Data Out) output upon succeeding CLK pulses.

Access to the data stored in the register from corresponding latches can be enabled by holding LE high (serial-to-parallel conversion). Holding $\overline{OE}$ (Output Enable) high disables the output sink drivers. While with $\overline{OE}$ active (low), the outputs are controlled by the state of their respective latches. When both LE and $\overline{OE}$

pins are high during serial data entry the latches are bypassed.

Setting Maximum Channel Current

The maximum individual channel output current is determined by the external resistor, R_{REXT}, which is placed between the REXT pin and GND. The voltage on R_{REXT}, V_{REXT}, is set by build-in bandgap reference, of which the typical value is 1.21V.

Following equations can be used to calculate the maximum channel output current:

$I_{OUT(X)}$ (max) = (1.24/ R_{REXT}) *15

where R_{REXT} is the value of the external resistor, which should larger than 374 Ω. The maximum per channel (OUT0 to OUT15) constant output current $I_{OUT(X)}$ (max) as a function of values of

R_{REXT} is shown in the Operating Characteristics section.

Under voltage Lockout

The BL8589 has an internal under voltage lockout (UVLO) function to ensure proper device operation. The outputs are disabled once the supply voltage drops below a minimum acceptable level. This feature is of significant importance for some critical applications. Upon recovery of the supply voltage after a UVLO event, all internal shift registers and latches are set to 0. The BL8589 is then operated in normal mode.

Thermal Shutdown Protection

The typical value of thermal shutdown threshold temperature T_{JTSD} is 150°C. If the junction temperature exceeds this value, the outputs will be turned off. There exists a thermal shutdown hysteresis, which is typically 30°C. Hence outputs are resumed once the device is cooled down and junction temperature falls below 135°C. However, the shift register and output latches register remain active during a thermal shutdown event. Therefore, stored data is preserved and there is no need to reset.

Load Supply Voltage (V_{LED})
The optimum driver voltage drops ($V_{OUT(X)}$) for the device is in the range of 1.0 to 3.0V. Higher

$V_{OUT(X)}$ will result in increased package power dissipation. To minimize package power dissipation, it is recommended that either lowest possible load supply voltage (V_{LED}) is used or to set a series voltage drop, V_{DROP}, according to the following equation:

$$V_{DROP} = V_{LED} - V_F - V_{OUT(X)},$$

in which V_F is the LED forward voltage. $V_{DROP} = I_O \times R_{DROP}$ for a single driver, for a Zener diode (V_Z), or for a series string of silicon diodes (approximately 0.7 V per diode) for a group of drivers (these configurations are shown in the figure). If the available voltage source will cause unacceptable power dissipation and series resistors or diodes are undesirable, a voltage regulator can be used to provide V_{LED}.
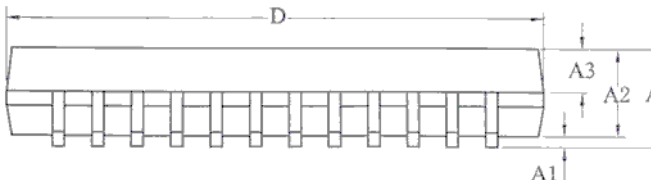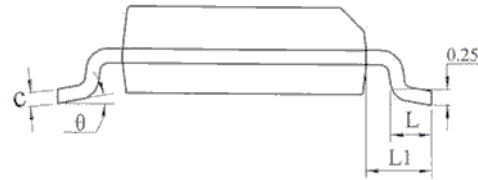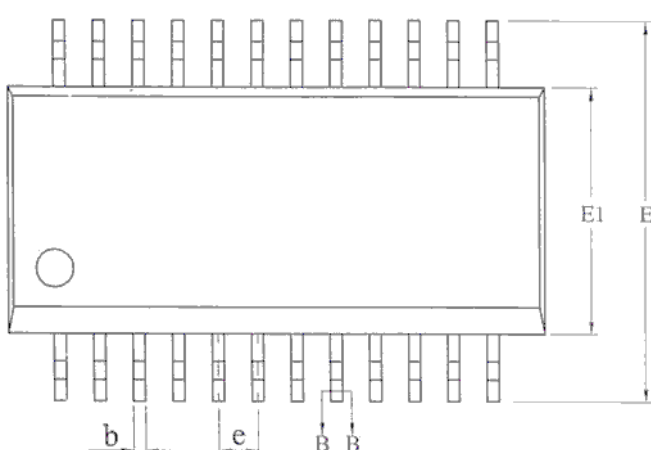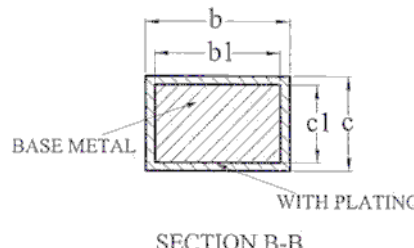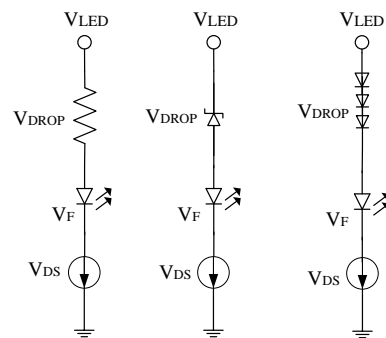

Typical Application Voltage Drops

BL8589

PACKAGE LINE

Package	QFN44-24	Devices per reel	3000Pcs	Unit	mm

Symbol	Dimension (mm)			Symbol	Dimension (mm)		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.77	0.82	0.87	Ne	2.50BSC		
A1	-	0.01	0.05	Nd	2.50BSC		
b	0.18	0.25	0.32	E	3.90	4.00	4.10
c	0.18	0.20	0.22	E2	2.50REF		
D	3.90	4.00	4.10	L	0.35	0.40	0.45
D2	2.50REF			h	0.30	0.35	0.40
e	0.50BSC						

BL8589

PACKAGE LINE (Continued)

Package	TSSOP-24	Devices per reel	2000Pcs	Unit	mm

Symbol	Dimension (mm)			Symbol	Dimension (mm)		
	MIN	NOM	MAX		MIN	NOM	MAX
A	-	-	1.77	D	8.45	8.65	8.85
A1	0.08	0.18	0.28	E	5.8	6.0	6.2
A2	1.20	1.40	1.60	E1	3.7	3.9	4.1
A3	0.55	0.65	0.75	e	0.635BSC		
b	0.23	-	0.33	L	0.5	0.65	0.8
b1	0.22	0.25	0.28	L1	1.05BSC		
c	0.21	-	0.26	θ	0	-	8°
c1	0.19	0.20	0.21				

BL8589

PACKAGE LINE (Continued)

Package	SSOP-24	Devices per reel	2000Pcs	Unit	mm

Symbol	Dimension (mm)			Symbol	Dimension (mm)		
	MIN	NOM	MAX		MIN	NOM	MAX
A	-	-	1.90	D	12.80	13.00	13.20
A1	0.05		0.15	E	7.70	7.90	8.10
A2	1.40	1.50	1.60	E1	5.80	6.00	6.20
A3	0.47	0.67	0.87	e	1.00BSC		
b	0.39	-	0.47	L	0.25	0.45	0.65
b1	0.38	0.40	0.43	L1	0.95BSC		
c	0.15	-	0.20	θ	0	-	8°
c1	0.14	0.15	0.16				