AK4413

High Performance 120dB 24-Bit 4ch DAC

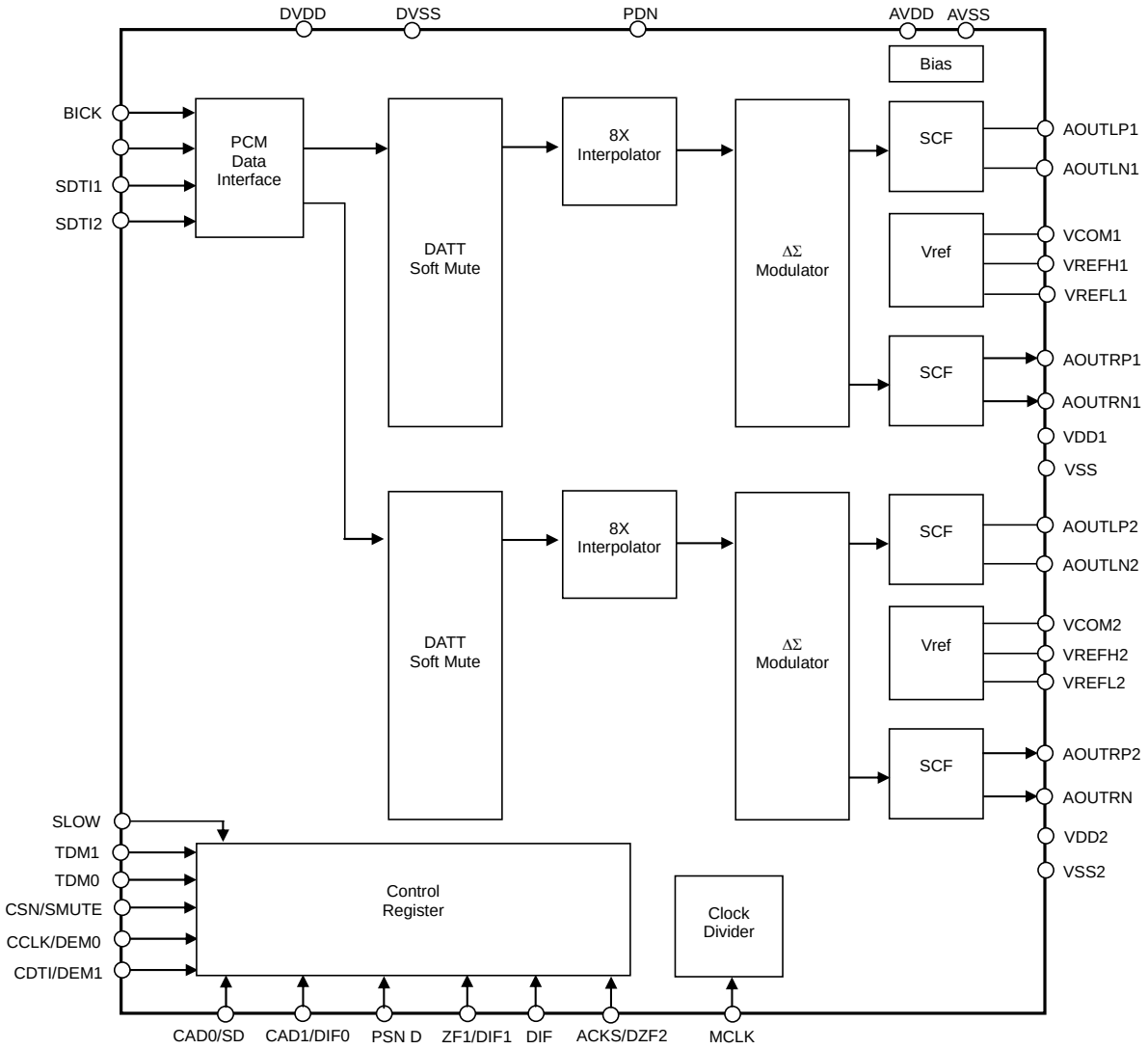
GENERAL DESCRIPTION

AK4413 is a 24-bit DAC, which corresponds to BD systems. An internal circuit includes newly developed 24bit Digital Filter for better sound q uality achiev ing low distortion charac teristics and wide dynamic range. The AK4413 has full differential SCF outputs, removing the need for AC coupling capacitors a nd increasing performance for systems with excessive clock jitter. The AK4413 accepts 216kHz PCM data, ideal for a wide range of applications including DVD-Audio.

FEATURES

- **128x Over sampling**
- **Sampling Rate: 30kHz ~ 216kHz**
- **24Bit 8x Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 80dB**
  - **High Quality Sound Short Delay Option; GD=7/fs and GD=5.5/fs**
  - **Sharp Roll-Off Filter**
  - **Slow Roll-Off Filter**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step)**
- **Stereo Mode**
- **THD+N: -104dB**
- **DR, S/N: 120dB (Stereo mode: 123dB)**
- **I/F Format: 24-bit MSB justified, 16/20/24bit LSB justified, I^2S, TDM**
- **Master Clock:**
  - **30kHz ~ 32kHz: 1152fs**
  - **30kHz ~ 54kHz: 512fs or 768fs**
  - **30kHz ~ 108kHz: 256fs or 384fs**
  - **108kHz ~ 216kHz: 128fs or 192fs**
- **Power Supply: DVDD=AVDD=2.7 ~ 3.6V, VDD1/2=4.75 ~ 5.25V**
- **Digital Input Level: CMOS**
- **Package: 44pin LQFP**

■ Block Diagram

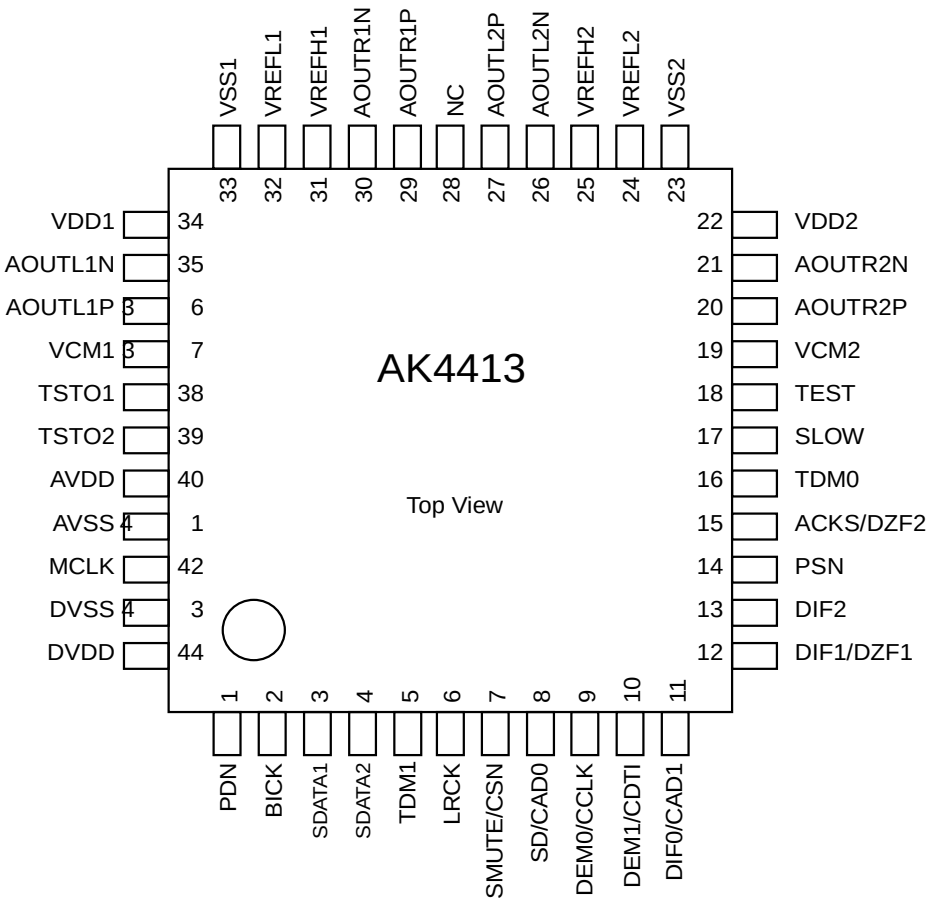


Block Diagram

■ Ordering Guide

AK4413EQ		−10 ~ +70°C	44	pin LQFP (0.8mm pitch)
AKD4413	Ev	aluation Board for AK4413		

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	PDN	I	Power-Down Mode When at "L", the AK4413 is in power-down mode and is held in reset. The AK4413 should always be reset upon power-up.
2	BICK	I	Audio Serial Data Clock in PCM Mode
3	SDATA1	I	Audio Serial Data Input in PCM Mode
4	SDATA2	I	Audio Serial Data Input in PCM Mode
5	TDM1	I	TDM I/F Format Mode in PCM Mode
6	LRCK	I	L/R Clock in PCM Mode
7	SMUTE	I	Soft Mute in Parallel Control Mode When this pin goes to "H", soft mute cycle is initiated. When returning to "L", the output mute releases.
	CSN	I	Chip Select in Serial Control Mode
8	SD		Digital Filter setting pin in Parallel Control mode
	CAD0	I	Chip Address 0 in Serial Control Mode (Internal pull-down pin)
9	DEM0	I	De-emphasis Enable 0 in Parallel Control Mode
	CCLK	I	Control Data Clock in Serial Control Mode
10	DEM1	I	De-emphasis Enable 1 in Parallel Control Mode
	CDTI	I	Control Data Input in Serial Control Mode
11	DIF0	I	Digital Input Format 0 in PCM Mode
	CAD1	I	Chip Address 1 in Serial Control Mode
12	DIF1	I	Digital Input Format 1 in PCM Mode
	DZF1	O	Zero Input Detect in Serial Control Mode
13	DIF2	I	Digital Input Format 2 in PCM Mode
14	PSN	I	Parallel/Serial Select (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
15	ACKS I		Auto Clock Setting Mode in Parallel Control mode "L": Manual Setting Mode, "H": Auto Setting Mode
	DZF2	O	Zero Input Detect in Serial Control Mode
16	TDM0	I	TDM I/F Format Mode in Parallel Control mode
17	SLOW	I	Digital filter setting pin
18	TEST	-	No internal bonding. Connect to DVSS.
19	VC M2	-	Common Voltage 2 Normally connected to VSS with a 10uF electrolytic cap.
20	AOUTR2P	O	Right Channel Positive Analog Output 2
21	AOUTR2N	O	Right Channel Negative Analog Output 2
22	VDD2	-	Analog Power Supply, 4.75 to 5.25V
23	VSS2	-	Ground (connected to DVSS, AVSS, VSS1 ground)
24	VREFL2	I	Low Level Voltage Reference Input 2
25	VREFH2	I	High Level Voltage Reference Input 2
26	AOUTL2N	O	Left Channel Negative Analog Output 2
27	AOUTL2P	O	Left Channel Positive Analog Output 2
28	NC	-	No internal bonding. Connect to GND.

No.	Pin Name	I/O	Function
29	AOUTR1P	O	Right Channel Positive Analog Output 1
30	AOUTR1N	O	Right Channel Negative Analog Output 1
31	VREFH1	I	High Level Voltage Reference Input 1
32	VREFL1	I	Low Level Voltage Reference Input 1
33	VSS1	-	Connected to DVSS, AVSS, VSS2 Ground
34	VD D1	-	Analog Power Supply Pin, 4.75 ~ 5.25V
35	AOUTL1N	O	Left Channel Negative Analog Output 1
36	AOUTL1P	O	Left Channel Positive Analog Output 1
37	VC M1	-	Common Voltage 1 Normally connected to VSS with a 10uF electrolytic cap.
38	TSTO 1	I	Test Output pin. “Hi-Z” at Normal Operation. Connect to AVSS.
39	TSTO 2	I	Test Output pin. “Hi-Z” at Normal Operation. Connect to AVSS.
40	AVDD	-	Analog Power Supply, 2.7 to 3.6V
41	AVSS	-	Analog Ground Pin
42	MCLK	I	Master Clock Input
43	DVSS	-	Digital Ground Pin
44	DV DD	-	Digital Power Supply, 3.0 ~ 3.6V

Note: All input pins except internal pull-up/down pins should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

(1) Parallel Mode

Classification	Pin Name	Setting
Analog	AOUTL1P, AOUTL1N	These pins must be open.
	AOUTR1P, AOUTR1N	These pins must be open.
	AOUTL2P, AOUTL2N	These pins must be open.
	AOUTR2P, AOUTR2N	These pins must be open.
Analog	TSTO1,TSTO2	This pin must be connected to AVSS
Digital	TEST	This pin must be connected to DVSS

(2) Serial Mode

Classification	Pin Name	Setting
Analog	AOUTL1P, AOUTL1N	These pins must be open.
	AOUTR1P, AOUTR1N	These pins must be open.
	AOUTL2P, AOUTL2N	These pins must be open.
	AOUTR2P, AOUTR2N	These pins must be open.
Analog	TSTO1,TSTO2	This pin must be connected to AVSS
Digital	DIF2,PSN,TDM0,SLOW,TEST	This pin must be connected to DVSS
	DZF1, DZF2	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1-2=AVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Analog	VDD1/2	–0.3	6.0	V
	Digital	DVDD	–0.3	4.6	V
	|AVSS – DVSS|	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, VSS1/2, DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-2=AVSS=DVSS=0V; Note 1)

Parameter Sym		bol	min	typ	max	Unit
Power Supplies (Note 3)	Analog	AVDD	2.7	3.0	3.6	V
	Analog	VDD1/2	4.75	5.0	5.25	V
	Digital	DVDD	2.7	3.0	3.6	V
Voltage Reference (Note 4)	"H" voltage reference	VREFH1	VDD1–0.5	-	VDD1	V
	"H" voltage reference	VREFH2	VDD2-0.5	-	VDD2	V
	"L" voltage reference	VREFL1	-	AVSS	-	V
	"L" voltage reference	VREFL2	-	AVSS	-	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, VDD1/2 and DVDD is not critical.
Note 4. The analog output voltage scales with the voltage of (VREFH1/2 – VREFL1/2).
Connect a resistor of 20ohm or less and a capacitor of 100uF or more to the VREFH1/2 pin. (Figure 19)
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH1/2 – VREFL1/2)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0V, VDD1/2=5.0V; AVSS=VSS1/2=DVSS=0V; VREFH1/2=VDD1/2, VREFL1/2= AVSS; Input data = 24bit; $R_L \geq 1k\Omega$; BICK=64fs; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 22; unless otherwise specified.)

Parameter min				typ	max	Unit
Resolution			-	-	24	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz (Note 6)	0dBFS	-	-104	-95	dB
	BW=20kHz	–60dBFS		-57	-	dB
	fs=96kHz	0dBFS	-	-99	-	dB
	BW=40kHz	–60dBFS	-	-54	-	dB
	fs=192kHz	0dBFS		-99	-	dB
	BW=40kHz	–60dBFS		-54	-	dB
	BW=80kHz	–60dBFS		-51	-	dB
Dynamic Range (–60dBFS with A-weighted)		(Note 6) 11	3	120		dB
S/N (A-weighted)		(Note 7) 11	3	120		dB
Interchannel Isolation (1kHz)			100	110		dB
DC Accuracy						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift		(Note 8)	- 20 -			ppm/°C
Output Voltage		(Note 9)	±2.65	±2.8	±2.95 V	pp
Load Capacitance			-	-	10	pF
Load Resistance		(Note 10)	1 -		-	kΩ
Power Supplies						
Power Supply Current						
	Normal operation (PDN pin = "H")					
	VDD1+VDD2		-	41	60	mA
	AVDD		-	1	1.5	mA
	DVDD (fs ≤ 44.1kHz)		-	7	11	mA
	DVDD (fs=96kHz)			12	18	mA
	DVDD (fs = 192kHz)		-	18	27	mA
	Power down (PDN pin = "L")	(Note 11)				
	AVDD+VDD1/2+DVDD		-	10	100	μA

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.

Note 6. Figure 22 External LPF Circuit Example 2. 100dB for 16-bit data.

Note 7. Figure 22 External LPF Circuit Example 2. S/N does not depend on input data size.

Note 8. The voltage on (VREFH1/2 – VREFL1/2) is held +5V externally.

Note 9. Full scale voltage (0dB). Output voltage scales with the voltage of (VREFH1/2 – VREFL1/2).
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH1/2 – VREFL1/2)/5.

Note 10. Regarding Load Resistance, AC load is 1kΩ (min) with a DC cut capacitor (Figure 22). DC load is 1.5kΩ (min) without a DC cut capacitor (Figure 21). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 11. In the power down mode. The PSN pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR	-0.0032	-	0.0032	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 13)		GD	-	29	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-0.2	-	0.2	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR	-0.0032	-	0.0032	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 13)		GD	-	29	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-0.3	-	0.3	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "0". SD bit="0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR	-0.0032	-	0.0032	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 13)		GD	-	29	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-1	-	0.1	dB

Note 12. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs, SB=0.546×fs.

Note 13. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24-bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)	±0.04dB	PB	0		8.1	kHz
	–3.0dB		-	18.2	-	kHz
Stopband (Note 14)		SB	39.2			kHz
Passband Ripple		PR	-0.043	-	0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 13)		GD	-	6	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 20.0kHz			-5	-	0.1	dB

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)	±0.04dB	PB	0		17.7	kHz
	–3.0dB		-	39.6	-	kHz
Stopband (Note 14)		SB	85.3			kHz
Passband Ripple		PR	-0.043	-	0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 13)		GD	-	6	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 40.0kHz			-4	-	0.1	dB

SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit="1", SD bit = "0")

Parameter Sym		bol	min	typ	max	Unit
Digital Filter						
Passband (Note 14)	±0.04dB	PB	0		35.5	kHz
	–3.0dB		-	79.1	-	kHz
Stopband (Note 14)		SB	171			kHz
Passband Ripple		PR	-0.043	-	0.043	dB
Stopband Attenuation		SA	73			dB
Group Delay (Note 13)		GD	-	6	-	1/fs
Digital Filter + SCF						
Frequency Response: 0 ~ 80.0kHz			-5	-	0.1	dB

Note 14. The passband and stopband frequencies scale with fs. For example, PB=0.185×fs, SB=0.888×fs.

SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note 12)		SB	24.1			kHz
Passband Ripple		PR	-0.0031	-	0.0031	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-0.2	-	0.2	dB

SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 48.0	43.5 -	kHz kHz
Stopband (Note 12)		SB	52.5			kHz
Passband Ripple		PR	-0.0031	-	0.0031	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-0.3	-	0.3	dB

SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB −6.0dB	PB	0 -	 96.0	87.0 -	kHz kHz
Stopband (Note 12)		SB	105			kHz
Passband Ripple		PR	-0.0031	-	0.0031	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 13)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-1	-	0.1	dB

SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		11.1	kHz
	−6.0dB		-	22.3	-	kHz
Stopband (Note 12)		SB	38.1			kHz
Passband Ripple		PR	-0.05	-	0.05	dB
Stopband Attenuation		SA	82			dB
Group Delay (Note 13)		GD	- 5.	5 -		1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-5	-	0.1	dB

SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		24.2	kHz
	−6.0dB		-	44.6	-	kHz
Stopband (Note 12)		SB	83.0			kHz
Passband Ripple		PR	-0.05	-	0.05	dB
Stopband Attenuation		SA	82			dB
Group Delay (Note 13)		GD	- 5.	5 -		1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-5	-	0.1	dB

SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	min	typ	max	Unit
Digital Filter						
Passband (Note 12)	±0.01dB	PB	0		48.4	kHz
	−6.0dB		-	89.2	-	kHz
Stopband (Note 12)		SB	165.9			kHz
Passband Ripple		PR	-0.05	-	0.05	dB
Stopband Attenuation		SA	82			dB
Group Delay (Note 13)		GD	- 5.	5 -		1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-5	-	0.1	dB

DC CHARACTERISTICS

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
High-Level Output Voltage	(Iout=–100μA)	VOH	DVDD–0.5	-	-	V
Low-Level Output Voltage	(Iout=100μA)	VOL	-	-	0.5	V
Input Leakage Current	(Note 15)	Iin	-		-	±10	μA

Note 15. The PSN pin has an internal pull-up device nominally 100kΩ. Therefore the PSN pin is not included.

SWITCHING CHARACTERISTICS

(Ta=25°C; VDD1/2=4.75 ~ 5.25V, AVDD=DVDD=2.7 ~ 3.6V)

Parameter Sym	bol	min	typ	max	Unit
Master Clock Timing					
Frequency	fCLK	2.048		41.472	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency (Note 16)					
Normal Mode (TDM0= "L", TDM1= "L")					
1152fs, 512fs or 768fs	fsn	8		54	kHz
256fs or 384fs	fsd	54		108	kHz
128fs or 192fs	fsq	108		216	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM0= "H", TDM1= "L")					
Normal Speed Mode High time	fsn	8		54	kHz
Low time	tLRH	1/256fs			ns
	tLRL	1/256fs			ns
TDM128 mode (TDM0= "H", TDM1= "H")					
Normal Speed Mode	fsn	8		54	kHz
Double Speed Mode	fsd	54		108	kHz
Quad Speed Mode	fsq	108		216	kHz
High time	tLRH	1/128fs			ns
Low time	tLRL	1/128fs			ns
PCM Audio Interface Timing					
Normal Mode (TDM0= "L", TDM1= "L")					
BICK Period					
1152fs, 512fs or 768fs	tBCK	1/128fsn			ns
256fs or 384fs	tBCK	1/64fsd			ns
128fs or 192fs	tBCK	1/64fsq			ns
BICK Pulse Width Low	tBCKL	14			ns
BICK Pulse Width High	tBCKH	14			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	14			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	14			ns
SDATA Hold Time	tSDH	5			ns
SDATA Setup Time	tSDS	5			ns
TDM256 mode (TDM0= "H", TDM1= "L")					
BICK Period					
Normal Speed Mode	tBCK	1/256fsn			ns
BICK Pulse Width Low	tBCKL	14			ns
BICK Pulse Width High	tBCKH	14			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	14			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	14			ns
SDATA1/2 Hold Time	tSDH	5			ns
SDATA1/2 Setup Time	tSDS	5			ns

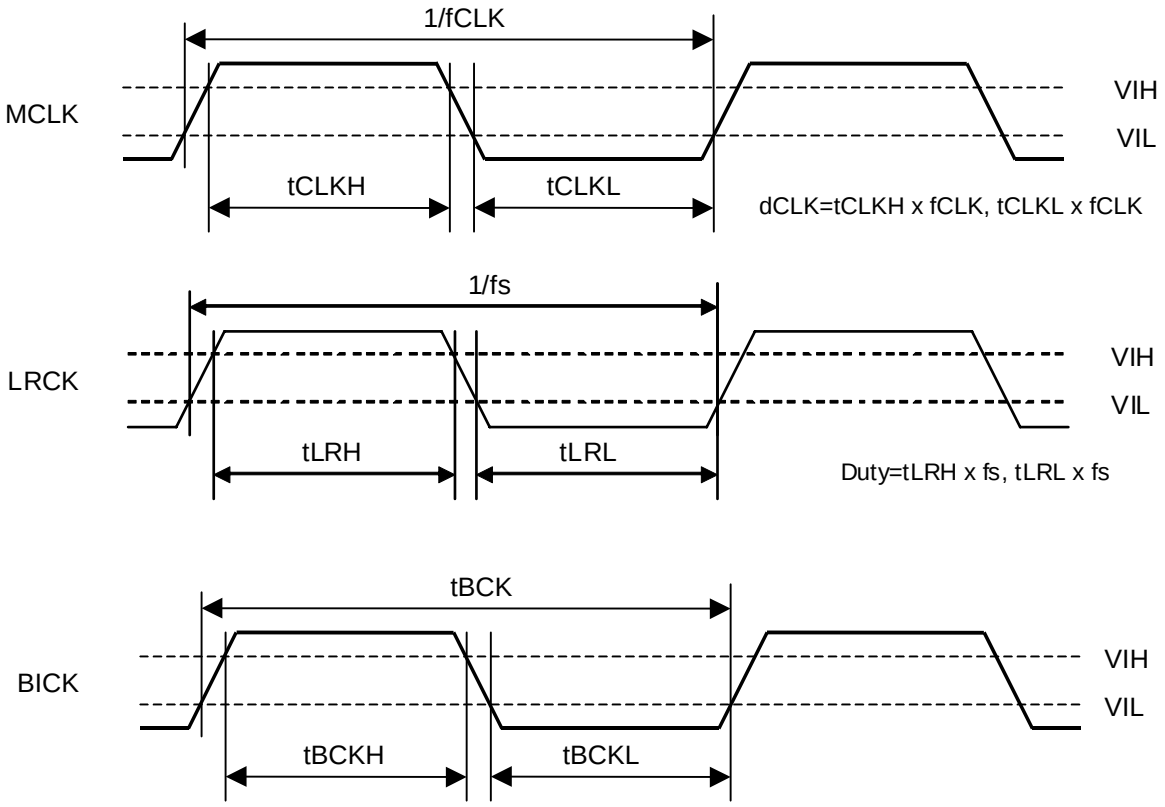
TDM128 mode (TDM0= "H", TDM1= "H")						
BICK Period						
Normal Speed Mode		tBCK	1/128fsn			ns
Double Speed Mode		tBCK	1/128fsd			ns
Quad Speed Mode		tBCK	1/128fsq			ns
BICK Pulse Width Low		tBCKL	14			ns
BICK Pulse Width High		tBCKH	14			ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	14			ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	14			ns
SDATA1/2 Hold Time		tSDH	5			ns
SDATA1/2 Setup Time		tSDS	5			ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	50			ns
CDTI Hold Time		tCDH	50			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 18)	tPD	150			ns

Note 16. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4413 should be reset by the PDN pin or RSTN bit.

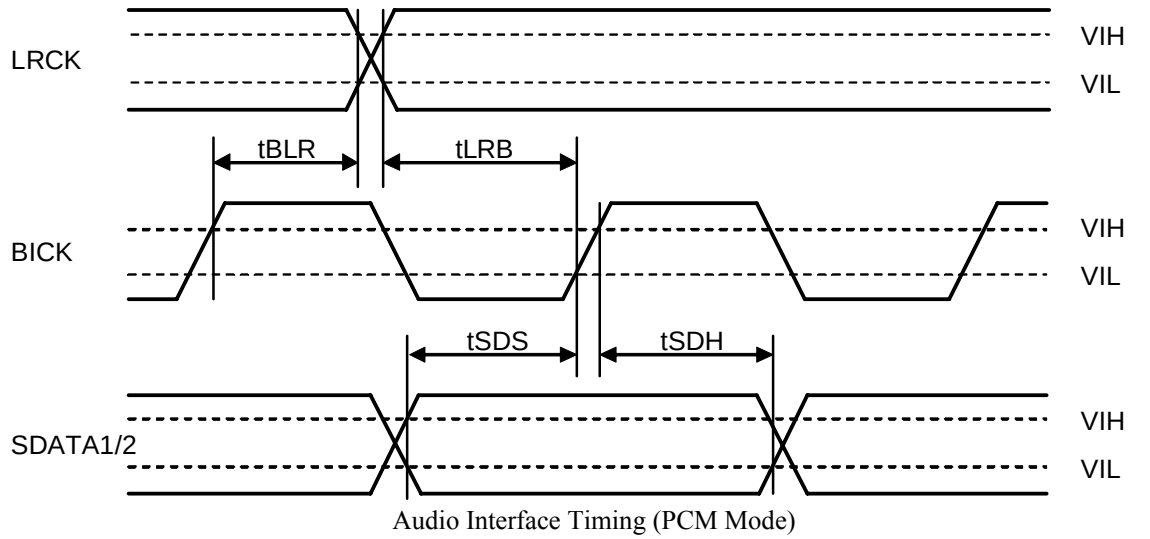
Note 17. BICK rising edge must not occur at the same time as LRCK edge.

Note 18. The AK4413 can be reset by bringing the PDN pin "L" to "H" upon power-up.

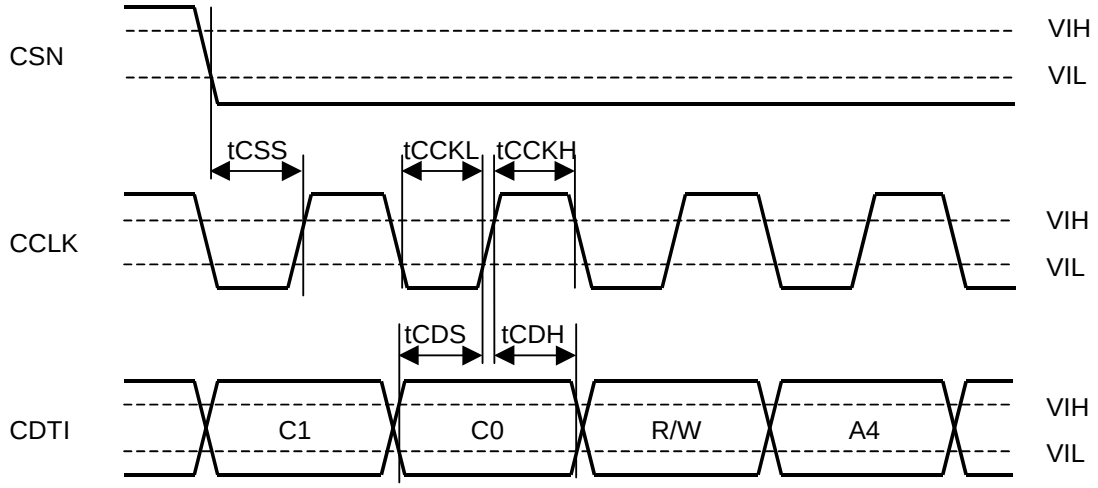
■ **Timing Diagram**



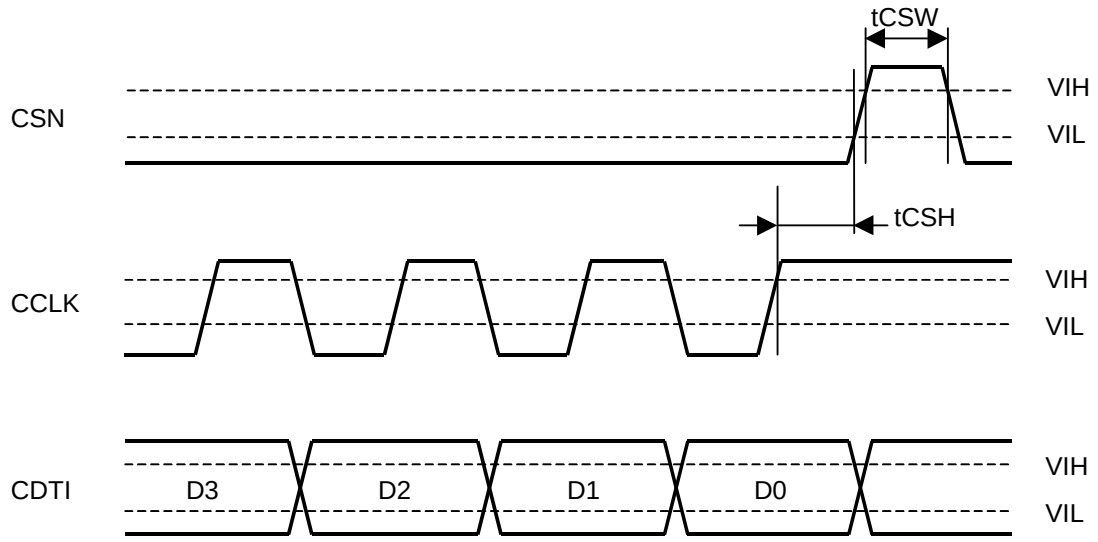
Clock Timing



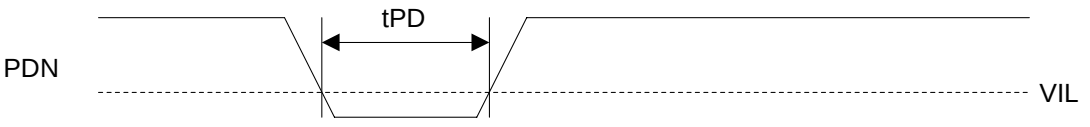
Audio Interface Timing (PCM Mode)



WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

[1] PCM Mode

The external clocks, which are required to operate the AK4413, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator.

The AK4413 is automatically placed in reset state when MCLK and LRCK are stopped during a normal operation (PDN pin ="H"), and the analog output becomes AVDD/2 (typ). When MCLK and LRCK are input again, the AK4413 exit reset state and starts the operation. After exiting system reset (PDN pin ="L"→"H") at power-up and other situations, the AK4413 is in power-down mode until MCLK and LRCK are supplied.

(1) Parallel Mode (PSN pin = "H")

1. Manual Setting Mode

In manual setting mode (ACKS pin = "L") only Normal Speed mode is supported with the sample rate range shown in (Table 1). The AK4413 automatically configures itself to operate with the supported MCLK frequencies which are required to be provided as input and are shown in (Table 2).

Sampling Rate (fs)	
Normal Speed Mode	8kHz ~ 54kHz

Table 1. Sampling Speed (Manual Setting Mode @Parallel Mode)

LRCK MCLK	(MHz)							BICK
fs	128fs 1	92fs 2	56fs	384fs 5	12fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880 16	.3840	24.5760 36	.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896 16	.9344	22.5792 33	.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880 18	.4320	24.5760 36	.8640	N/A	3.0720MHz

Table 2. System Clock Example (Manual Setting Mode @Parallel Mode), (N/A: Not available)

2. Auto Setting Mode (ACKS pin = "H")

In this mode, sampling speed and MCLK frequency are detected automatically (Table 3) The MCLK must be supplied at the correct frequency according to Table 4.

MCLK Sam		pling Speed
1152fs		Normal (fs≤32kHz)
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 3. Sampling Speed (Auto Setting Mode @Parallel Mode)

LRCK MCLK	(MHz)							Sampling Speed
fs	128fs 1	92fs 2	56fs 3	84fs	512fs 7	68fs	1152fs	
32.0kHz	N/A	N/A	(8.1920*)	(12.2880*)	16.3840 2	4.5760 3	6.8640	Normal/ (Double*)
44.1kHz N	/A	N/A	(11.2896*)	(16.9344*)	22.5792	33.8688	N/A	
48.0kHz N	/A	N/A	(12.2880*)	(18.4320*)	24.5760	36.8640	N/A	
88.2kHz N/A		N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz N/A		N/A	24.5760	36.8640	N/A N/A	N/A		
176.4kHz 22	.5792	33.8688	N/A N/A		N/A	N/A	N/A	Quad
192.0kHz 24	.5760	36.8640	N/A N/A		N/A N/A	N/A		

Table 4. System Clock Example (Auto Setting Mode @Parallel Mode), (N/A: Not available)

MCLK= 256fs/384fs sup ports sam pling rate of 32kHz~96kHz (Table 5). H owever, when t he s ampling rate is 32kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS pin	MCLK	DR,S/N
L	256fs/384fs/512fs/768fs	120dB
H	256fs/384fs	117dB
H	512fs/768fs	120dB

Table 5. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

3. Digital Filter Setting

SD pin	SLOW pin	Mode
0	0	Sharp roll-off filter
0	1	Slow roll-off filter
1	0	Short delay sharp roll-off
1	1	Short delay slow roll-off

Table 6. Digital Filter Setting (Parallel Mode)

(2) Serial Mode (PSN pin = "L")

1. Manual Setting Mode (ACKS bit = "0")

MCLK frequency is detected automatically and the sampling rate is set by DFS1-0 bits (Table 7). The MCLK frequency corresponding to each sampling speed should be provided externally (Table 8). The AK4413 is set to Manual Setting Mode at power-up (PDN pin = "L" →"H"). When DFS1-0 bits are changed, the AK4413 should be reset by RSTN bit.

DFS1 bit	DFS0 bit	Sampling Rate (fs)		
0 0		Normal Speed Mode	30kHz ~ 54kHz	(default)
0 1		Double Speed Mode	54kHz ~ 108kHz	
1 0		Quad Speed Mode	120kHz ~ 216kHz	

Table 7. Sampling Speed (Manual Setting Mode @Serial Mode)

LRCK MCLK (MHz)								BICK
fs	128fs 1	92fs 2	56fs	384fs 5	12fs	768fs	1152fs	64fs
32.0kHz	N/A	N/A	8.1920	12.2880 16	.3840	24.5760 36	.8640	2.0480MHz
44.1kHz	N/A	N/A	11.2896 16	.9344	22.5792 33	.8688	N/A	2.8224MHz
48.0kHz	N/A	N/A	12.2880 18	.4320	24.5760 36	.8640	N/A	3.0720MHz
88.2kHz	11.2896 16	.9344 22	.5792	33.8688	N/A	N/A	N/A	5.6448MHz
96.0kHz	12.2880 18	.4320 24	.5760	36.8640	N/A	N/A	N/A	6.1440MHz
176.4kHz 22	.5792	33.8688	N/A N/A		N/A N/A		N/A	11.2896MHz
192.0kHz 24	.5760	36.8640	N/A N/A		N/A N/A		N/A	12.2880MHz

Table 8. System Clock Example (Manual Setting Mode @Serial Mode)

2. Auto Setting Mode (ACKS bit = "1")

MCLK frequency and the sampling speed are detected automatically (Table 9) and DFS1-0 bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 10).

MCLK Sam	pling Speed
1152fs	Normal (fs≤32kHz)
512fs 7 68fs	Normal
256fs 3 84fs	Double
128fs 1 92fs	Quad

Table 9. Sampling Speed (Auto Setting Mode @Serial Mode)

LRCK MCLK (MHz)								Sampling Speed
fs	128fs 1	92fs 2	56fs 3	84fs	512fs 7	68fs	1152fs	
32.0kHz	N/A	N/A	(8.1920*)	(12.2880*)	16.3840 2	4.5760 3	6.8640	Normal/ (Double*)
44.1kHz N	/A	N/A	(11.2896*)	(16.9344*)	22.5792	33.8688	N/A	
48.0kHz N	/A	N/A	(12.2880*)	(18.4320*)	24.5760	36.8640	N/A	
88.2kHz N/A		N/A	22.5792	33.8688	N/A N/A	N/A		Double
96.0kHz N/A		N/A	24.5760	36.8640	N/A N/A	N/A		
176.4kHz 22	.5792	33.8688	N/A N/A		N/A N/A	N/A		Quad
192.0kHz 24	.5760	36.8640	N/A N/A		N/A N/A	N/A		

Table 10. System Clock Example (Auto Setting Mode @Serial Mode)

MCLK= 256fs/384fs supports sampling rate of 32kHz~96kHz (Table 11). However, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS pin	MCLK	DR,S/N
L 2	56fs/384fs/512fs/768fs	120dB
H 2	56fs/384fs	117dB
H 5	12fs/768fs	120dB

Table 11. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

3. Digital Filter Setting

SD bit	SLOW bit	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay sharp roll-off	(default)
1	1	Short delay slow roll-off	

Table 12. Digital Filter Setting (Serial Mode)

■ Audio Interface Format

[1] PCM Mode

(1) Parallel Control Mode (PSN pin = "H")

Twenty formats are selectable by DIF2-0 and TDM1-0 pins (Table 13). In this mode, register settings are ignored. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

If TDM1-0 pins = "LH" the audio interface is TDM256 mode (Table 13) and all eight channels of DAC data are input to the SDTI1 pin. The input data to the SDTI2 pin is ignored. BICK is fixed to 256fs, "H" time and "L" time of LRCK should be 1/256fs at least. The data format is MSB first, 2's complement and the SDTI1 is latched on the rising edge of BICK. Only the first four channels of DAC data may be selected to be converted into four channels of DAC analog output.

If TDM1-0 pins = "HH" the audio interface is TDM128 mode (Table 13) and the serial data of DAC (four channels: L1, R1, L2, R2) is input to the SDTI1 pin.

Mode	TDM	1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK
Normal	0	-	0	0	0	0	16-bit LSB justified	H/L	≥32fs
	1 0				0	1	20-bit LSB justified	H/L	≥40fs
	2			0	1	0	24-bit MSB justified	H/L	≥48fs
	3 0				1	1	24-bit I^{2}S compatible	L/H	≥48fs
	4 1				0	0	24-bit LSB justified	H/L	≥48fs
	5 1				0	1	32-bit LSB justified	H/L	≥64fs
	6			1	1	0	32-bit MSB justified	H/L	≥64fs
	7			1 1		1	32-bit I^{2}S compatible	L/H	≥64fs
TDM256	0	0 1			0	0	N/A		
				0	0	1	N/A		
	8			0	1	0	24-bit MSB justified	↑	256fs
	9 0				1	1	24-bit I^{2}S compatible	↓	256fs
	10 1				0	0	24-bit LSB justified	↑	256fs
	11 1				0	1	32-bit LSB justified	↑	256fs
	12			1	1	0	32-bit MSB justified	↑	256fs
	13			1 1		1	32-bit I^{2}S compatible	↓	256fs
TDM128	0	1 1			0	0	N/A		
	0				0	1	N/A		
	14			0	1	0	24-bit MSB justified	↑	128fs
	15 0				1	1	24-bit I^{2}S compatible	↓	128fs
	16 1				0	0	24-bit LSB justified	↑	128fs
	17 1				0	1	32-bit LSB justified	↑	128fs
	18			1	1	0	32-bit MSB justified	↑	128fs
	19			1 1		1	32-bit I^{2}S compatible	↓	128fs

Table 13. Audio Interface Format (Parallel mode)

(2) Serial Control Mode (PSN pin = "L")

Twenty formats are selected by setting DIF2-0 and TDM1-0 bits (Table 14). The initial setting of DIF2-0 bits is "010". In this mode, the DIF1 pin setting is ignored.

The audio I/F format is TDM256 mode (Table 14) and all the serial data of eight DAC channels are input to the SDTI1 pin (Figure 15). The input data to the SDTI2 pin is ignored. BICK is fixed to 256fs, high and low amplitude of LRCK is 1/256fs (min). The data format is MSB first, 2's complement and the SDTI1 is latched on the rising edge of BICK. The eight channels of DAC data may be mapped to two pieces of AK4413 (Table 15).

In TDM128 mode, the serial data of DAC (four channels: L1, R1, L2, R2) is input to the SDTI pin and other serial data of DAC (four channels: L3, R3, L4, R4) are input to the SDTI2 pin (Figure 14). BICK is fixed to 128fs. The data format is MSB first and 2's complement and the input data to SDTI1-2 pins are latched on the rising edge of BICK. The eight channels of DAC data may be mapped to two pieces of AK4413 (Table 15).

Mode	TDM	1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK
Normal	0 0	-	0		0	0	16-bit LSB justified	H/L	≥32fs
	1 0				0	1	20-bit LSB justified	H/L	≥40fs
	2			0	1	0	24-bit MSB justified	H/L	≥48fs
	3 0				1	1	24-bit I^{2}S compatible	L/H	≥48fs
	4 1				0	0	24-bit LSB justified	H/L	≥48fs
	5 1				0	1	32-bit LSB justified	H/L	≥64fs
	6			1	1	0	32-bit MSB justified	H/L	≥64fs
	7			1 1		1	32-bit I^{2}S compatible	L/H	≥64fs
TDM256	0	0 1			0	0	N/A		
				0	0	1	N/A		
	8			0	1	0	24-bit MSB justified	↑	256fs
	9 0				1	1	24-bit I^{2}S compatible	↓	256fs
	10 1				0	0	24-bit LSB justified	↑	256fs
	11 1				0	1	32-bit LSB justified	↑	256fs
	12			1	1	0	32-bit MSB justified	↑	256fs
	13			1 1		1	32-bit I^{2}S compatible	↓	256fs
TDM128	0	1 1			0	0	N/A		
				0	0	1	N/A		
	14			0	1	0	24-bit MSB justified	↑	128fs
	15 0				1	1	24-bit I^{2}S compatible	↓	128fs
	16 1				0	0	24-bit LSB justified	↑	128fs
	17 1				0	1	32-bit LSB justified	↑	128fs
	18			1	1	0	32-bit MSB justified	↑	128fs
	19			1 1		1	32-bit I^{2}S compatible	↓	128fs

Table 14. Audio Interface Format (Serial mode)

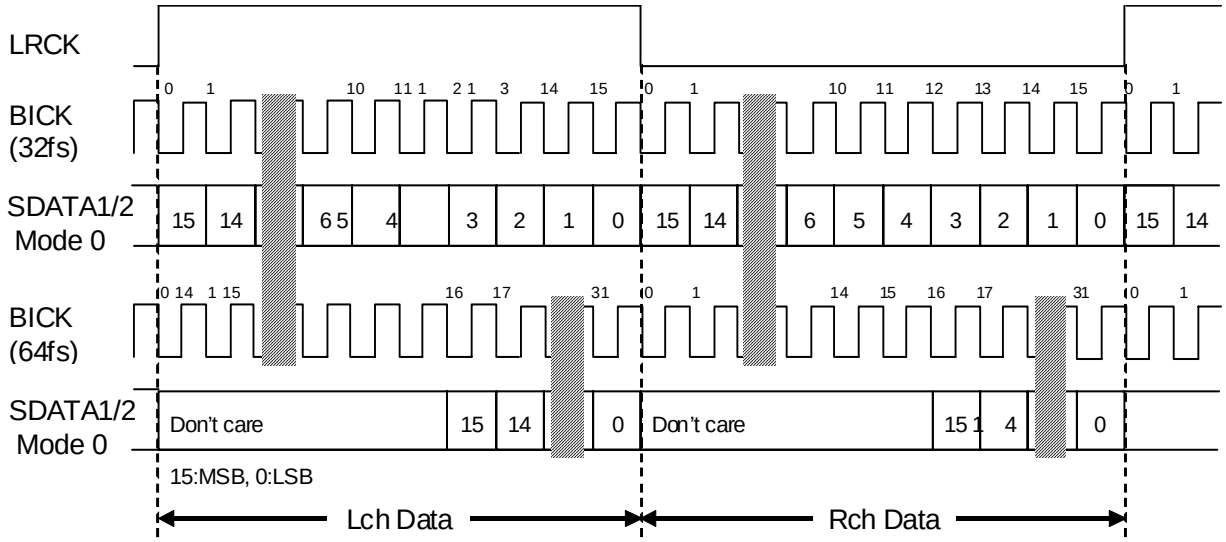


Figure 1. Mode 0 Timing

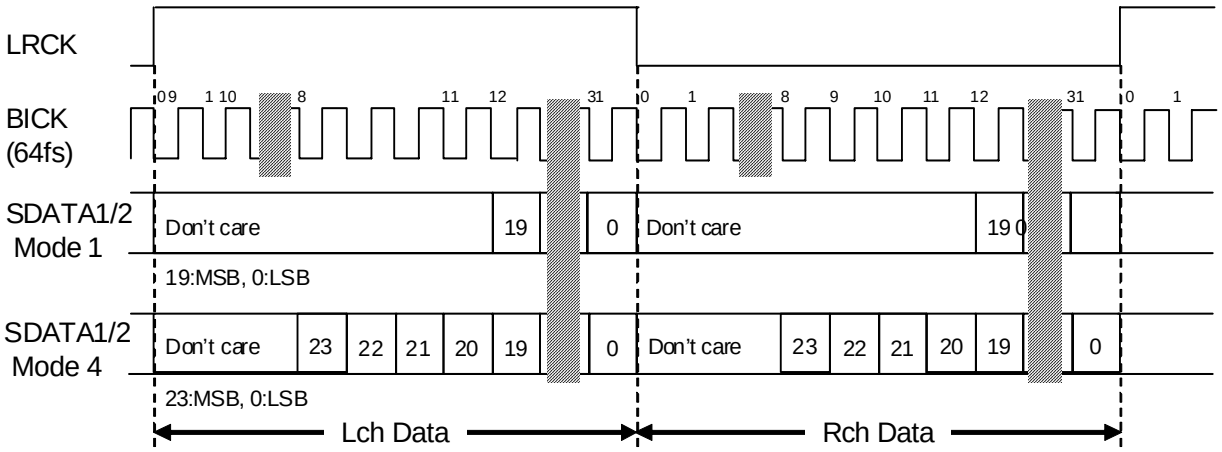


Figure 2. Mode 1/4 Timing

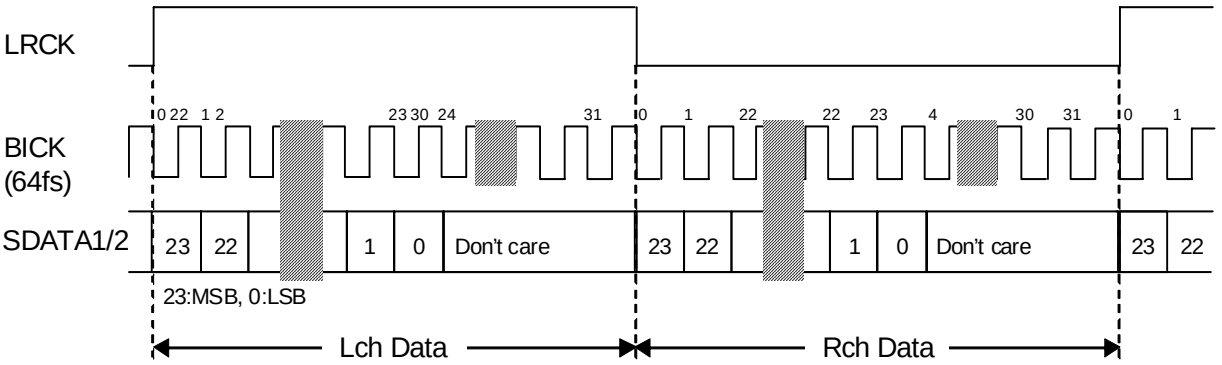


Figure 3. Mode 2 Timing

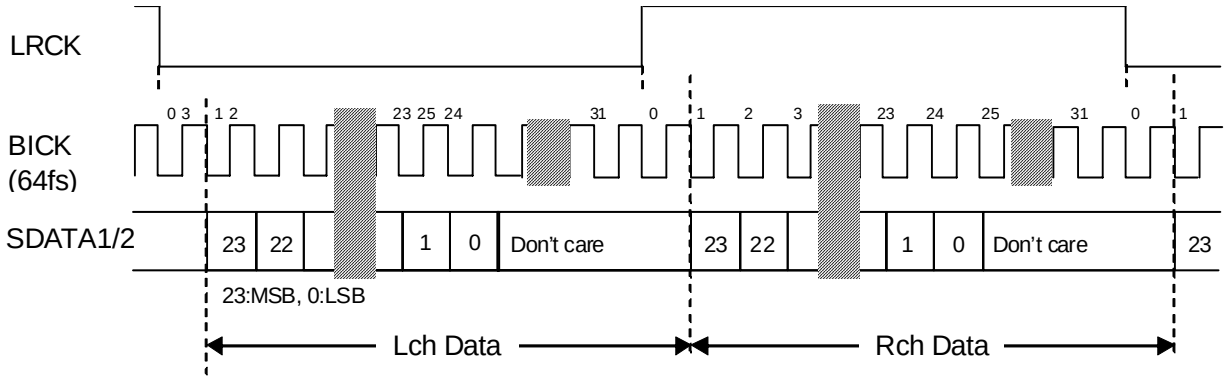


Figure 4. Mode 3 Timing

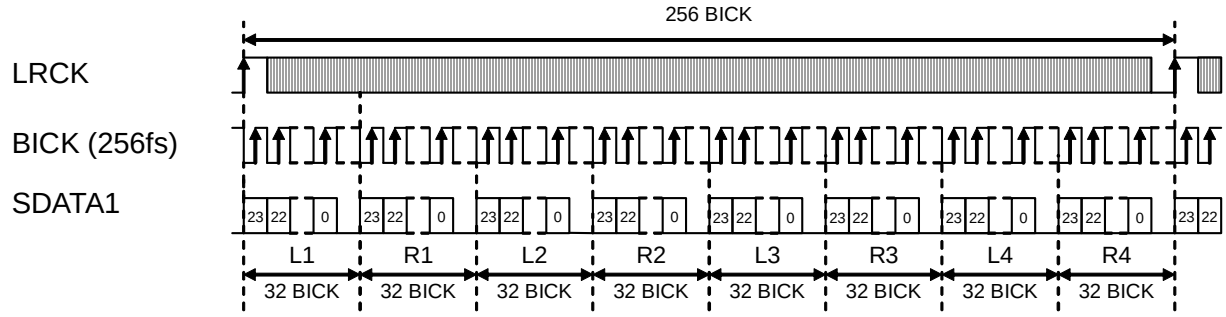


Figure 5. Mode 8 Timing

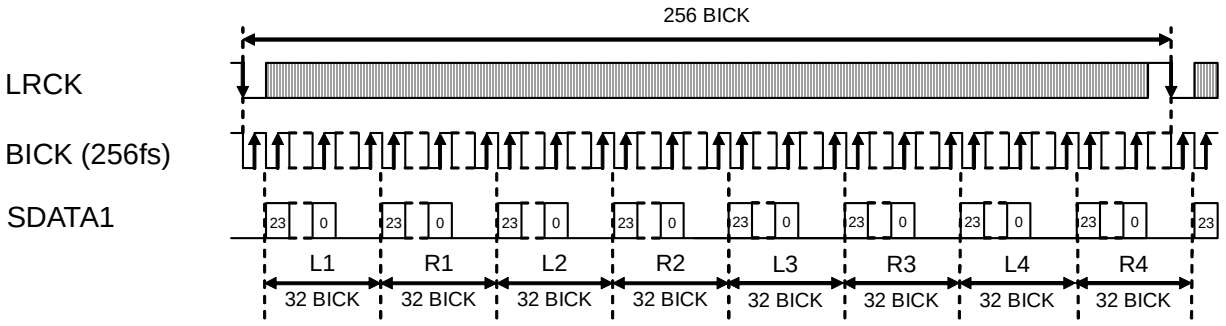


Figure 6. Mode 9 Timing

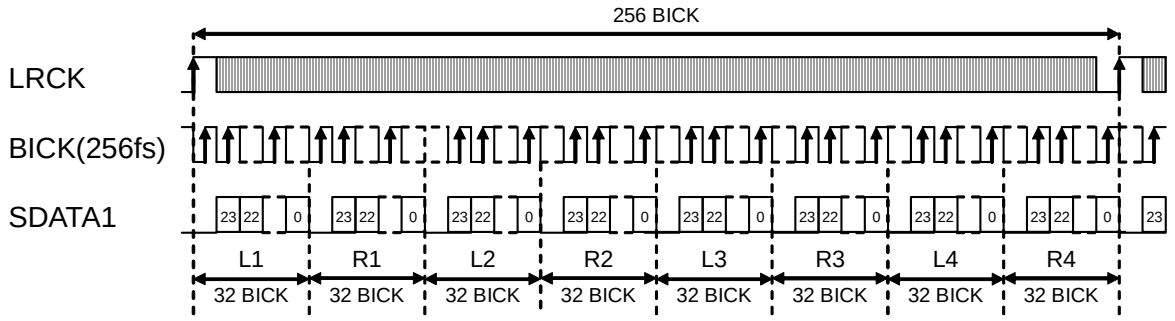


Figure 7. Mode 10 Timing

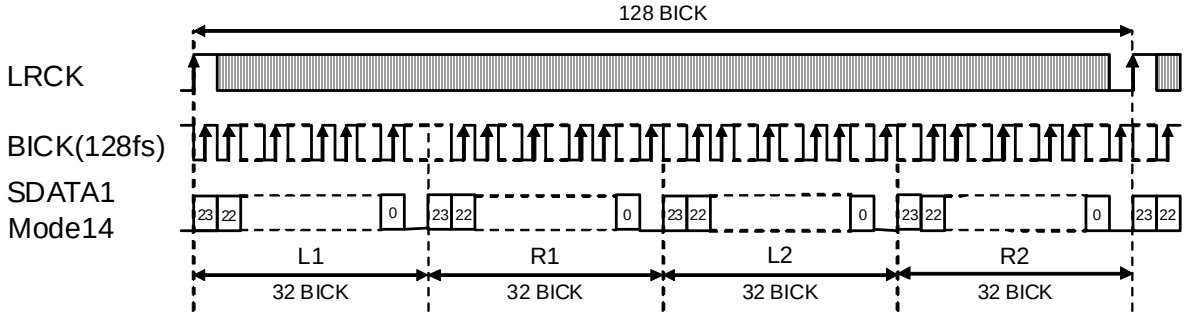


Figure 8. Mode 14 Timing

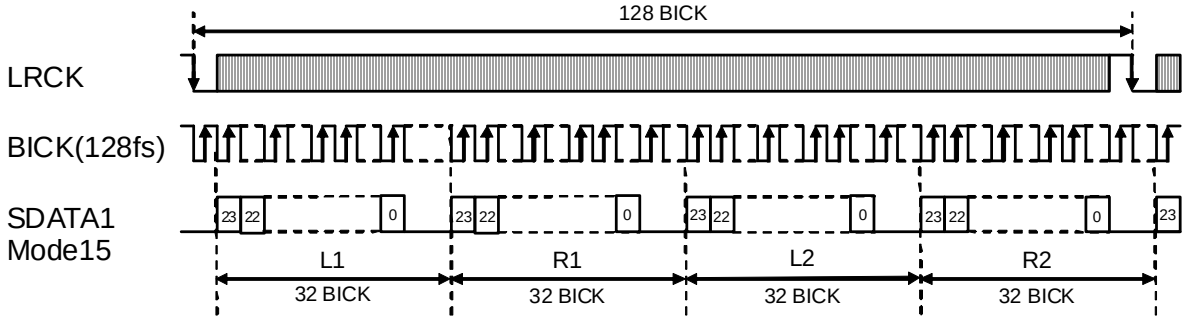


Figure 9. Mode 15/19 Timing

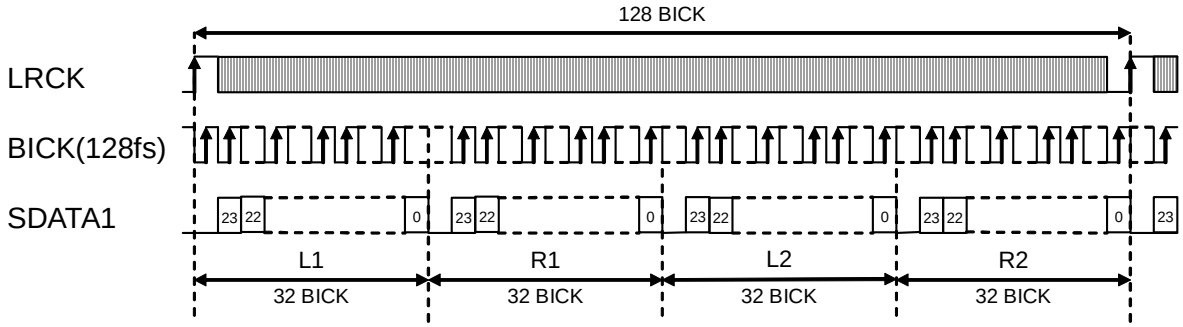


Figure 10. Mode 16 Timing

One data cycle of SDATA1 and SDATA2 for each format are defined as below. SDS2-1 bits control playback channel of each DAC.

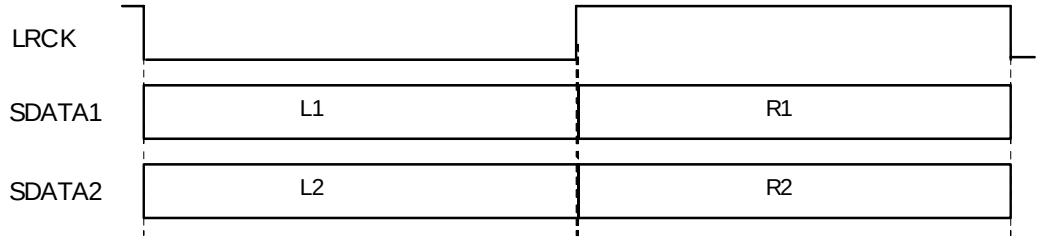


Figure 11. Data Slot in Normal Mode

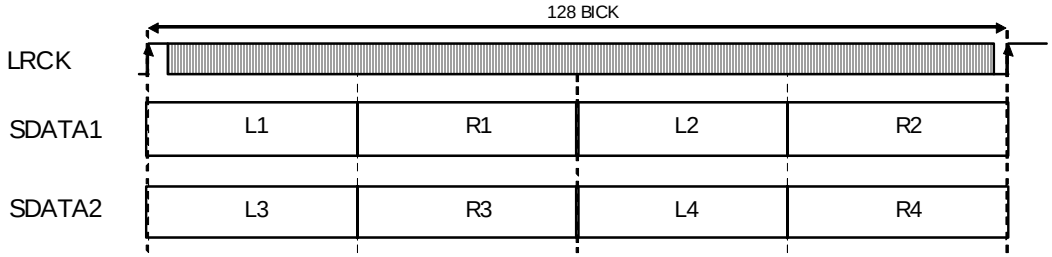


Figure 12. Data Slot in TDM128 Mode

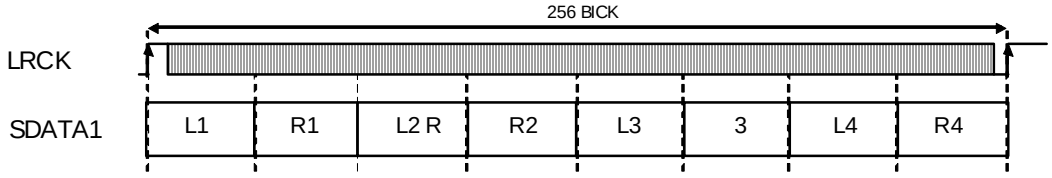


Figure 13. Data Slot in TDM256 Mode

AK4413 Data Select

SDS	1	SDS2	DAC1 DAC		2	
			Lch R	ch	Lch	Rch
Normal	0 0		L1	R1	L2	R2
	0 1		L1	R1	L1	R1
	1 0		L2	R2	L2	R2
	1 1		L2	R2	L1	R1
TDM128	0 0		L1	R1	L2	R2
	0 1		L1	R1	L4	R4
	1 0		L3	R3	L2	R2
	1 1		L3	R3	L4	R4
TDM256	0 0		L1	R1	L2	R2
	0 1		L1	R1	L4	R4
	1 0		L3	R3	L2	R2
	1 1		L3	R3	L4	R4

Table 15. Data Select

■ De-emphasis Filter

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM1-0 pins or DEM1-0 bits. In case of 256fs/384fs and 128fs/192fs, the digital de-emphasis filter is always off.

[1] Parallel Mode
The DEM1 and DEM0 pins control de-emphasis mode of DAC1 and DAC2. This setting is common for both of DAC's. In parallel mode, the filter setting cannot be applied independently.

DEM1 D	EM0	Mode	
L L		44.1kHz	
L H		OFF	(default)
H L		48kHz	
H H		32kHz	

Table 16. De-emphasis Control (Parallel Mode)

[2] Serial Mode
DEM1-0 bits and DEM3-2 bits control de-emphasis mode of DAC1 and DAC2, respectively.

DEM1 D	EM0	Mode	
0 0		44.1kHz	
0 1		OFF	(default)
1 0		48kHz	
1 1		32kHz	

Table 17. DAC1 De-emphasis Control (Serial Mode)

DEM3 D	EM2	Mode	
0 0		44.1kHz	
0 1		OFF	(default)
1 0		48kHz	
1 1		32kHz	

Table 18. DAC2 De-emphasis Control (Serial Mode)

■ Output Volume

The AK4413 includes channel independent digital output volumes (ATT) with 255 levels at 0.5dB step including MUTE. This volume control is in front of the DAC and it can attenuate the input data from 0dB to –127dB and mute. When changing output levels, transitions are executed in soft change; thus no switching noise occurs during these transitions. It takes 7424/fs from FFH (0dB) to 00H (Mute). The attenuation level is reset to FFH (0dB) by initial reset. By RSTN bit = "0", the attenuation level is initialized to FFH, and the attenuation level returns to the setting value by RSTN bit = "1".

Sampling Speed	Transition Time
	0dB to MUTE
fs=44.1kHz 16	8.3ms
fs=96kHz	77.3ms
fs=192kHz	38.6ms

Table 19. ATT Transition Time

■ Zero Detection

The AK4413 has channel-independent zeros detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately returns to "L" if the input data of each channel is not zero. If the RSTN bit is "0", the DZF pins of both channels go to "H". The DZF pins of both channels go to "L" after 4 ~ 5/fs when RSTN bit returns to "1". In this case, DZF pins of both channels are always "L". The DZFB bit can invert the polarity of the DZF pin. In parallel control mode, the zero detect function is unavailable.

Pin C	omment
DZF1	Zero Detection flag output of the channels set by register 08H.
DZF2	Zero Detection flag output of the channels set by register 09H.

Table 20. DZF pin function

■ Mono Output

Input and output signal combination of the AK4413 can be set by MONO bit and SELLR bit. Monaural output mode is enabled when MONO bit = "1". The output signal phase of DAC is controlled by INVL and INVLR bits. These settings are available for any audio format.

(L1/2 is the output signal of the AOUTL1N/2N and AOUTL1P/2P pins. R1/2 is the output signal of AOUTR1N/2N and AOUTR1P/2P pins)

MONO bit	SELLR1 bit	INVL1 bit	INVR1 bit	L1 (AOUTL1N, AOUTL1P pins)	R1 (AOUTR1N, AOUTR1P pins)
0 0		0	0	L1	R1
		1 0		L1 Invert	R1
		0 1		L1	R1 Invert
		1	1	L1 Invert	R1 Invert
0 1		0 0		R1	L1
		1 0		R1 Invert	L1
		0 1		R1	L1 Invert
		1	1	R1 Invert	L1 Invert
1 0		0 0		L1	L1
		1 0		L1 Invert	L1
		0	1	L1	L1ch In Invert
		1	1	L1 Invert	L1 Invert
1 1		0 0		R1	R1
		1 0		R1 Invert	R1
		0 1		R1	R1 Invert
		1	1	R1 Invert	R1 Invert

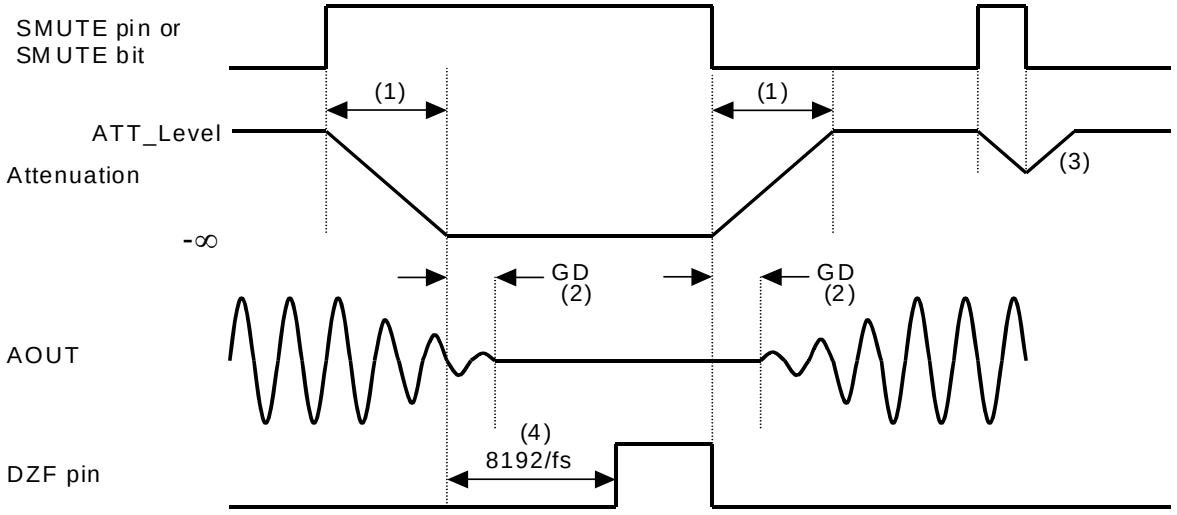
Table 21. Output Select for DAC1

MONO bit	SELLR2 bit	INVL2 bit	INVR2 bit	L2 (AOUTL2N, AOUTL2P pins)	R2 (AOUTR2N, AOUTR2P pins)
0	0	0	0	L2	R2
		1	0	L2 Invert	R2
		0 1		L2	R2 Invert
		1	1	L2 Invert	R2 Invert
0	1	0 0		R2	L2
		1 0		R2 Invert	L2
		0 1		R2	L2 Invert
		1	1	R2 Invert	L2 Invert
1	0	0 0		L2	L2
		1 0		L2 Invert	L2
		0 1		L2	L2 Invert
		1	1	L2 Invert	L2 Invert
1	1	0 0		R2	R2
		1 0		R2 Invert	R2
		0 1		R2	R2 Invert
		1	1	R2 Invert	R2 Invert

Table 22. Output Select for DAC2

■ Soft Mute Operation

The soft mute operation is performed at digital domain. When the SMUTE pin goes to "H" or the SMUTE bit set to "1", the output signal is attenuated by –∞ during ATT_DATA × ATT transition time from the current ATT level. When the SMUTE pin is returned to "L" or the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If the soft mute is cancelled before attenuating –∞, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time. For example, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.

(2) The analog output corresponding to the digital input has group delay (GD).

(3) If the soft mute is cancelled before attenuating –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data for each channel is continuously zeros for 8192 LRCK cycles, the DZF pin for each channel goes to "H". The DZF pin immediately returns to "L" if input data are not zero.

Figure 14. Soft Mute Function

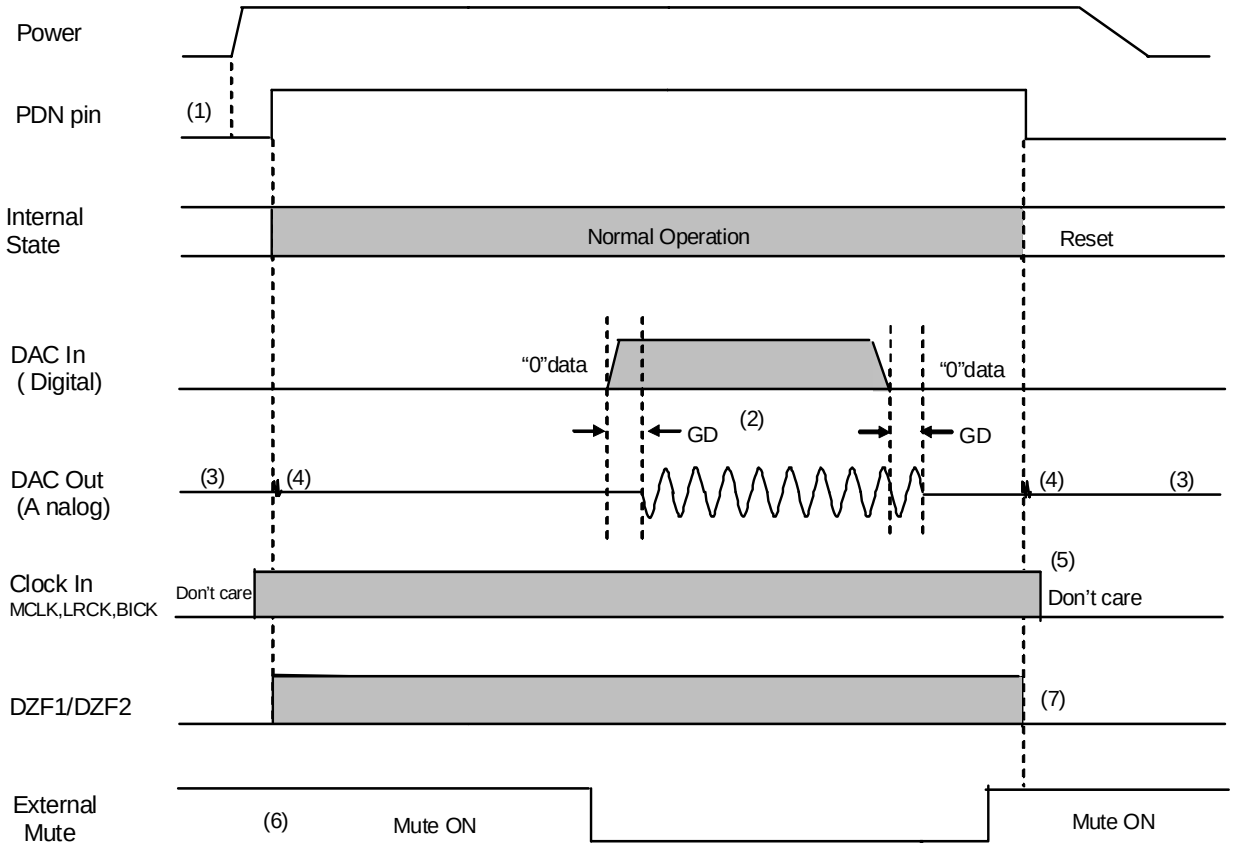
■ System Reset

The AK4413 should be reset once by bringing the PDN pin = "L" upon power-up. It initializes register settings of the device. The AK4413 exits this system reset (power-down mode) by MCLK after the PDN pin = "H", and the analog block exits power-down mode. The digital block exits power-down mode after the internal counter counts MCLK for 4/fs.

■ Power ON/OFF timing

The AK4413 is placed in the power-down mode by bringing the PDN pin "L" and the registers are initialized. The analog outputs are floating (Hi-Z). Since a click noise occurs at the edge of the PDN pin signal, the analog output should be muted externally if the click noise influences system application.

The DAC can be reset by setting RSTN bit to "0". In this case, the registers are not initialized and the corresponding analog outputs go to VCM1/2. Since a click noise occurs at the edge of RSTN signal, the analog output should be muted externally if click noise aversely affect system performance.



Notes:

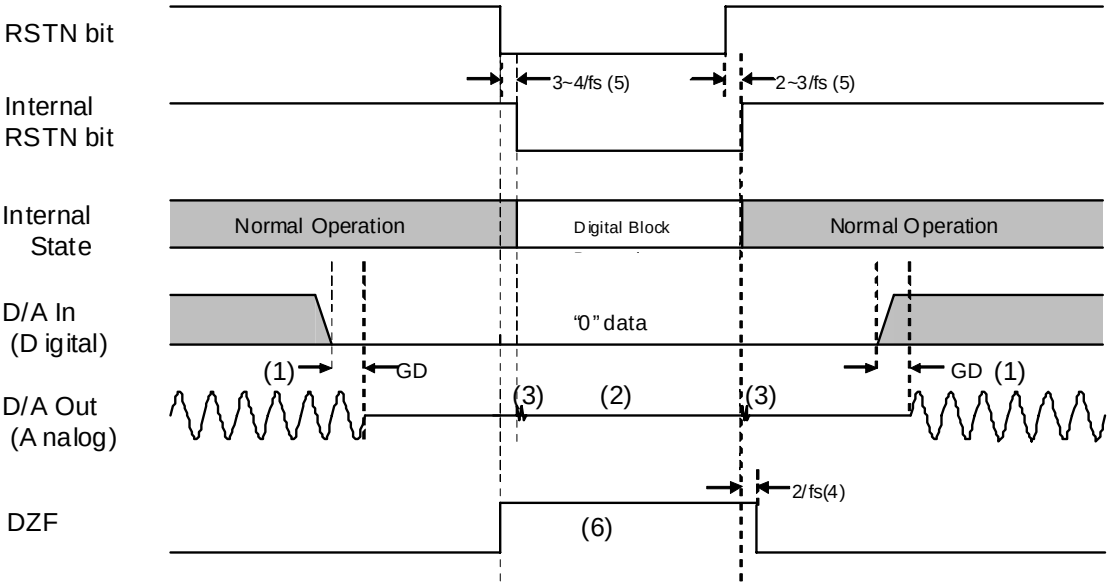
(1) After AVDD and DVDD are powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) Analog outputs are floating (Hi-Z) in power-down mode.
(4) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(5) MCLK, BICK and LRCK clocks can be stopped in power-down mode (PDN pin= "L").
(6) Mute the analog output externally if click noise (3) adversely affect system performance
The timing example is shown in this figure.
(7) DZF1/2 pins are "L" in the power-down mode (PDN pin = "L").

Figure 15. Power-down/up Sequence Example

■ Reset Function

(1) RESET by RSTN bit = "0"

When the RSTN bit = "0", the AK4413's digital block is powered down, but the internal register values are not initialized. In this time, the analog outputs go to VCM1/2 voltage and DZF1/2 pins are "H". Figure 16 shows an example of reset by RSTN bit.



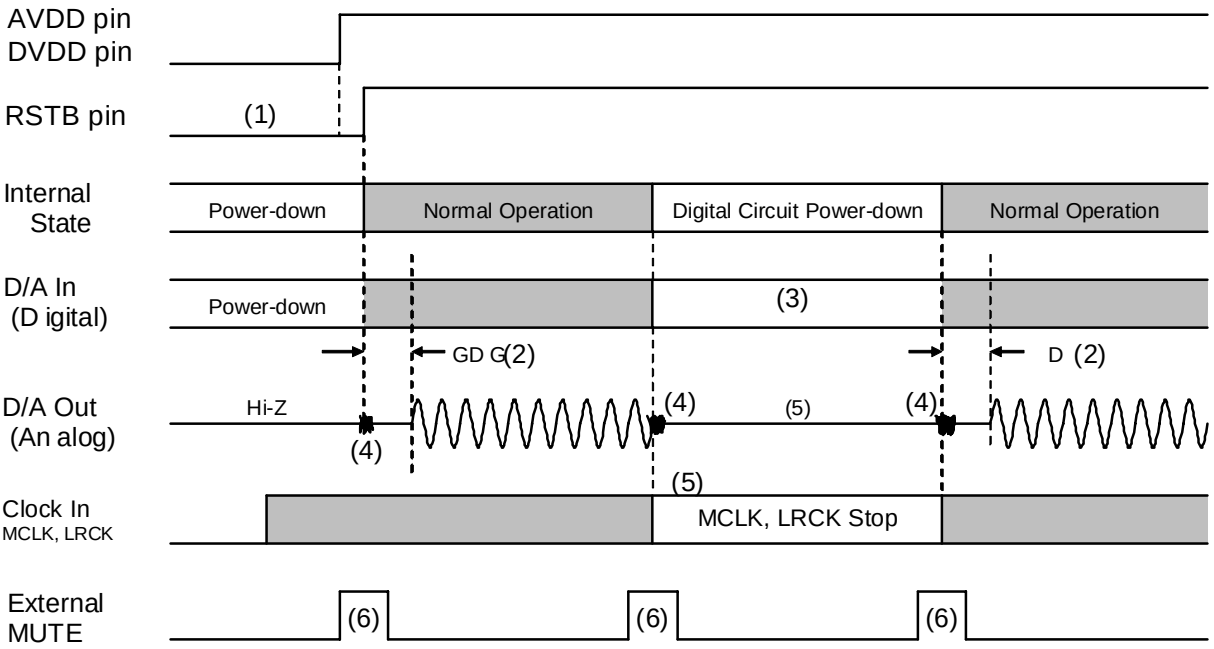
Notes:

(1) The analog output corresponding to digital input has group delay (GD).
(2) Analog outputs settle to VCOM voltage.
(3) Small pop noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The DZF pins change to "H" when the RSTN bit becomes "0", and return to "L" at 2/fs after RSTN bit becomes "1".
(5) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN bit "1".
(6) Mute the analog output externally if click noise (3) and Hi-Z (2) adversely affect system performance

Figure 16. Reset Sequence Example 1

(2) RESET by MCLK or LRCK Stop

The AK4413 is automatically placed in reset state when MCLK or LRCK is stopped during PCM mode (RSTN pin ="H"), and the analog outputs are floating (Hi-Z). When MCLK and LRCK are input again, the AK4413 exits reset state and starts the operation. Zero detect function is disable when MCLK or LRCK is stopped.



Notes:

(1) After AVDD and DVDD are powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) The digital data can be stopped. Click noise after MCLK and LRCK are input again can be reduced by inputting "0" data during this period.
(4) Click noise occurs within 3 ~ 4LRCK cycles from the riding edge ("↑") of the PDN pin or MCLK inputs. This noise occurs even when "0" data is input.
(5) Clocks (MCLK, BICK, LRCK) can be stopped in the reset state (MCLK or LRCK is stopped).
(6) Mute the analog output externally if click noise (4) influences system applications. The timing example is shown in this figure.

Figure 17. Reset Sequence Example 2

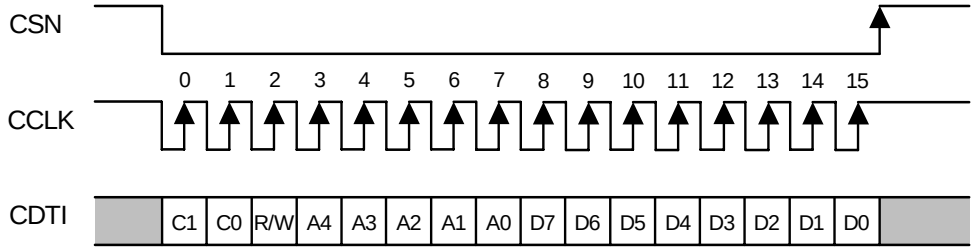
■ Register Control Interface

Pins (parallel control mode) or registers (serial control mode) can control the functions of the AK4413. In parallel control mode, the register setting is ignored, and in serial control mode the pin settings are ORed if the pin is not repurposed. When the state of the PSN pin is changed, the AK4413 should be reset by the PDN pin. The serial control interface is enabled by the PSN pin = "L". In this mode, pin settings must be all "L". Internal registers may be written to through3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2-bits, C1/0), Read/Write (1-bit; fixed to "1"), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). The AK4413 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data is valid when CSN "↑". The clock speed of CCLK is 5MHz (max).

Function	Parallel mode	Serial mode
Auto Setting Mode	Y	Y
Manual Setting Mode	Y	Y
Audio Format	Y	Y
De-emphasis Y		Y
SMUTE Y		Y
TDM Mode	Y (4-ch only)	Y
Digital Filter Option	Y	Y
Zero Detection	-	Y
Digital Attenuator	-	Y

Table 23. Function List 1 (Y: Available, -: Not available)

Setting the PDN pin to "L" resets the registers to their default values. In serial control mode, the internal timing circuit is reset by the RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (C1 bit =CAD1 pin, C0 bit =CAD0 pin)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: R egister Address
D7-D0: C ontrol Data

Figure 18. Control I/F Timing

* The AK4413 does not support the read command.
* When the AK4413 is in power down mode (PDN pin = "L") or the MCLK is not provided, a writing into the control registers is prohibited.
* The control data can not be written when the CCLK rising edge is 15 times or less or 17 times or more during CSN is "L".

Function List

Function Defau	lt	Address	Bit
Attenuation Level	0dB	03H 04H 06H 07H	ATT7-0
Audio Data Interface Modes	24bit MSB Justified	00H	DIF2-0
Data Zero Detect Enable	Disable	08H 09H	L1/R1/L2/R2
Minimum delay Filter Enable	Sharp roll-off filter	01H 02H	SD SLOW
Slow Rolloff Filter Enable			
Short delay Filter Enable			
De-emphasis Response	OFF	01H 0AH	DEM3-0
Soft Mute Enable	Normal Operation	01H	SMUTE
MONO mode Stereo mode select	Stereo	02H	MONO
Inverting Enable of DZF	“H” active	02H	DZFB
The data selection of L channel and R channel	R channel	02H 05H	SELLR1/2
The dat a sel ection of DAC 1 and DAC2	Normal 0A	H	SDS1/2
Data Invert Mode	OFF	05H	INVL1/L2/R1/R2

Table 24. Function List 2

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0			DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	0	0	0	0			MONO	DZFB	SELLR1	SLOW
03H	L1ch ATT	ATT7	ATT6	ATT5		ATT4	ATT3	ATT2	ATT1		ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5		ATT4	ATT3	ATT2	ATT1		ATT0
05H	Control 4	INVL1	INVR1		INVL2	INVR2		SELLR2	0	0	0
06H	L2ch ATT	ATT7	ATT6	ATT5		ATT4	ATT3	ATT2	ATT1		ATT0
07H	R2ch ATT	ATT7	ATT6	ATT5		ATT4	ATT3	ATT2	ATT1		ATT0
08H	DZF1 Control	L1	R1	L2	R2			0	0	0	0
09H	DZF2 Control	L1	R1	L2	R2			0	0	0	0
0AH	Control 5	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM3	DEM2

Notes:
Data must not be written into addresses from 0BH to 1FH.
When the PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit is set to “0”, only the internal timing is reset, and the registers are not initialized to their default values.
When the state of the PSN pin is changed, the AK4413 should be reset by the PDN pin.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0			DIF2	DIF1	DIF0	RSTN
Default		0	0	0	0	0	1	0	1

RSTN: Internal Timing Reset
0: Reset. All registers are not initialized.
1: Normal Operation (default)
Internal clock timings are reset but registers are not reset.

DIF2-0: Audio Data Interface Modes (Table 14)
Initial value is “010” (Mode 2: 24-bit MSB justified).

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM only)
0: Disable : Manual Setting Mode (default)
1: Enable : Auto Setting Mode
When ACKS bit = “1”, the sampling frequency and MCLK frequency are detected automatically.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
	Default	0	0	1	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM1-0: DAC1 De-emphasis Response (Table 17)
Initial value is “01” (OFF).

SD: Short delay Filter Enable.
0 : Sharp roll-off filter
1 : Short delay filter (default)

SD	SLOW	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay sharp roll-off	(default)
1	1	Short delay slow roll-off	

Table 25. Digital Filter setting

DFS1-0: Sampling Speed Control (Table 7)
The default values are “00”. A click noise occurs when changing DFS1-0 bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1				D0
02H	Control 3	0	0	0	0				MONO	DZFB	SELLR1	SLOW
Default		0	0	0	0	0	0	0				0

SLOW: Slow Roll-off Filter Enable. This setting is ORed with the pin setting.
0 : (default)
1 : Slow roll-off filter

SD	SLOW	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay sharp roll-off	(default)
1	1	Short delay slow roll-off	

Table 26. Digital Filter setting

SELLR1: The data selection of L channel and R channel, when MONO mode
0: All channel output L channel data, when MONO mode. (default)
1: All channel output R channel data, when MONO mode.
It is enabled when MONO bit is “1”, and outputs Lch date to both channels when “0”,outputs Rch data to both channels when “1”.

DZFB: Inverting Enable of DZF
0: DZF pin goes “H” at Zero Detection (default)
1: DZF pin goes “L” at Zero Detection

MONO: MONO mode Stereo mode select
0: Stereo mode (default)
1 : MONO mode
When MONO bit is “1”, MONO mode is enabled.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	Default	1	1	1	1	1	1	1	1

ATT7-0: Attenuation Level
25 5 levels, 0.5dB step

Data	Attenuation
FFH	0dB
FEH	-0.5dB
FDH	-1.0dB
:	:
:	:
02H	-126.5dB
01H	-127.0dB
00H	MUTE (-∞)

The transition between set values is soft transition of 7425 levels. It takes 7424/fs (168ms@fs=44.1kHz) from FFH (0dB) to 00H (MUTE). If the PDN pin goes to "L", the ATTs are initialized to FFH. The ATTs are FFH when RSTN bit= "0". When RSTN return to "1", the ATTs fade to their current value. This digital attenuator is independent of soft mute function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL1	INVR1	INVL2	INVR2		SELLR2	0	0	0
	Default	0	0	0	0	0	0	0	0

SELLR2: The data selection of AOUTL2-R2, when MONO mode
0: AOUTL2-R2 output L channel data, when MONO mode. (default)
1: AOUTL2-R2 output R channel data, when MONO mode.
When MONO bit is set to "1", Lch data is output by SELLR2 bit = "0" and Rch data is output by SELLR2 bit = "1".

INVR2: AOUTR2 output phase invert bit
0: Disable (default)
1 : Enable

INVL2: AOUTL2 output phase invert bit
0: Disable (default)
1 : Enable

INVR1: AOUTR1 output phase invert bit
0: Disable (default)
1 : Enable

INVL1: AOUTL1 output phase invert bit
0: Disable (default)
1 : Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	L2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	R2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	Default	1	1	1	1	1	1	1	1

ATT7-0: Attenuation Level
25 5 levels, 0.5dB step

Data	Attenuation
FFH	0dB
FEH	-0.5dB
FDH	-1.0dB
:	:
:	:
02H	-126.5dB
01H	-127.0dB
00H	MUTE (-∞)

The transition between set values is soft transition of 7425 levels. It takes 7424/fs (168ms@fs=44.1kHz) from FFH (0dB) to 00H (MUTE). If the PDN pin goes to "L", the ATTs are initialized to FFH. The ATTs are FFH when RSTN bit= "0". When RSTN return to "1", the ATTs fade to their current value. This digital attenuator is independent of soft mute function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	DZF1 Control	L1	R1	L2	R2				
09H	DZF2 Control	L1	R1	L2	R2				
	Default	0	0	0	0	0	0	0	0

L1-2, R1-2: Zero Detect Flag Enable Bit for the DZF1-2 pins
0: Disable
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 5	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM3	DEM2
	Default	0	0	0	0	1	1	0	1

DEM3-2: DAC2 De-emphasis Response (Table 18)
Initial value is "01" (OFF).

PW2-1: Power Down control for DAC
PW2: Power management for DAC2
0: DAC2 power OFF
1: DAC2 power ON (default)
PW1: Power management for DAC1
0: DAC1 power OFF
1: DAC1 power ON (default)

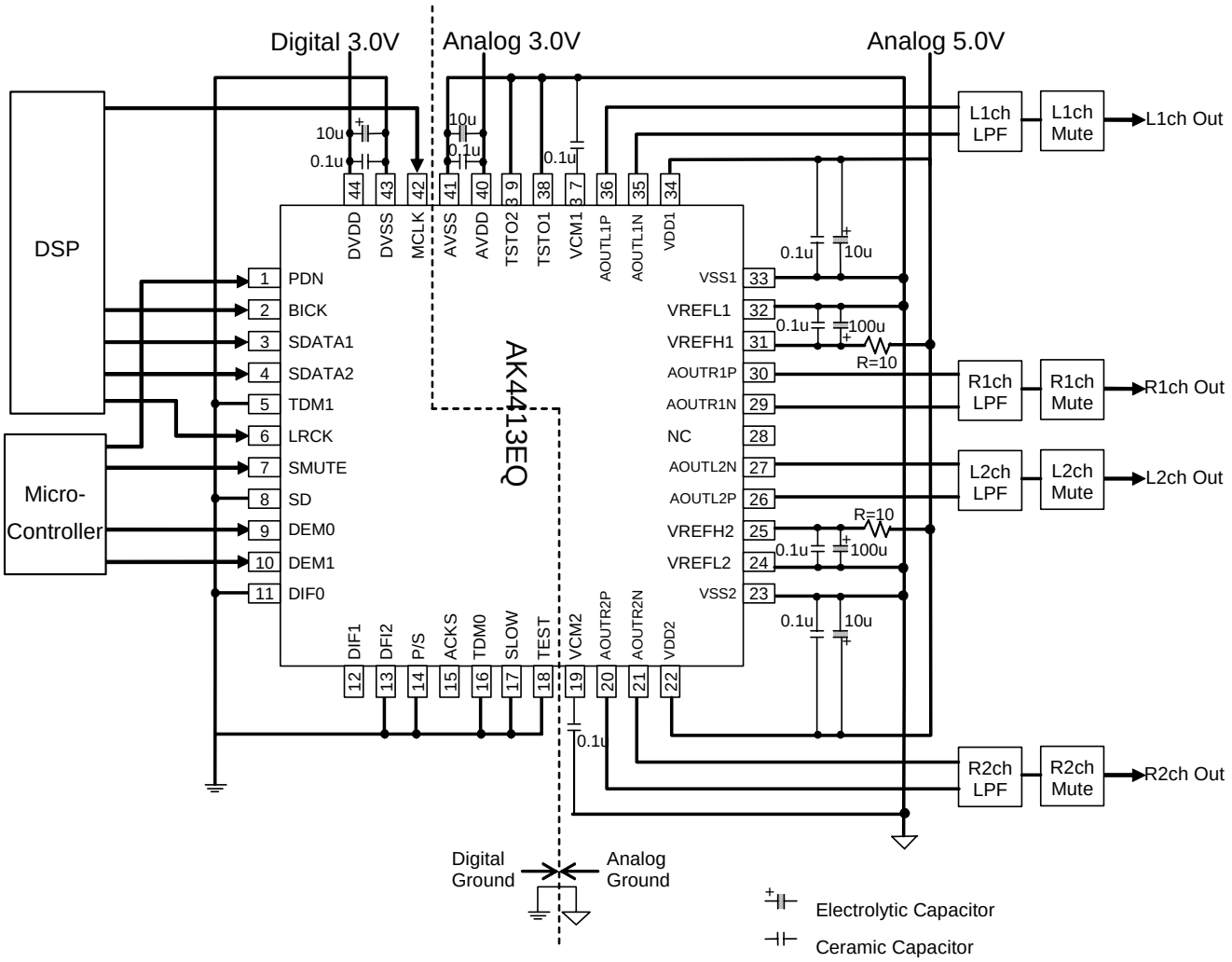
SDS1-2: DAC1and DAC2 data select
0: Normal Operation
1: Outputs other slot data
Refer to Table 15 for details.

TDM0-1: TDM Mode Select

Mode	TDM	1	TDM0	BICK	SDTI	Sampling Speed
Normal	0		0	32fs~	1-2	Normal, Double, Quad Speed
TDM256	0		1	256fs fixed	1	Normal Speed
TDM128		1	1	128fs fixed	1-2	Normal, Double, Quad Speed

SYSTEM DESIGN

Figure 19 shows the system connection diagram. Figure 21 and Figure 22 show the analog output circuit examples. The evaluation board (AKD4413) demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- VSS1-2, DVSS and AVSS must be connected to the same analog ground plane.
- When AOUT drives a capacitive load, some resistance should be added in series between AOUT and the capacitive load.
- All input pins except pull-down/pull-up pins should not be allowed to float.

Figure 19. Typical Connection Diagram (AVDD=3.0V, VDD1/2=5V, DVDD=3.0V, Serial Control Mode)

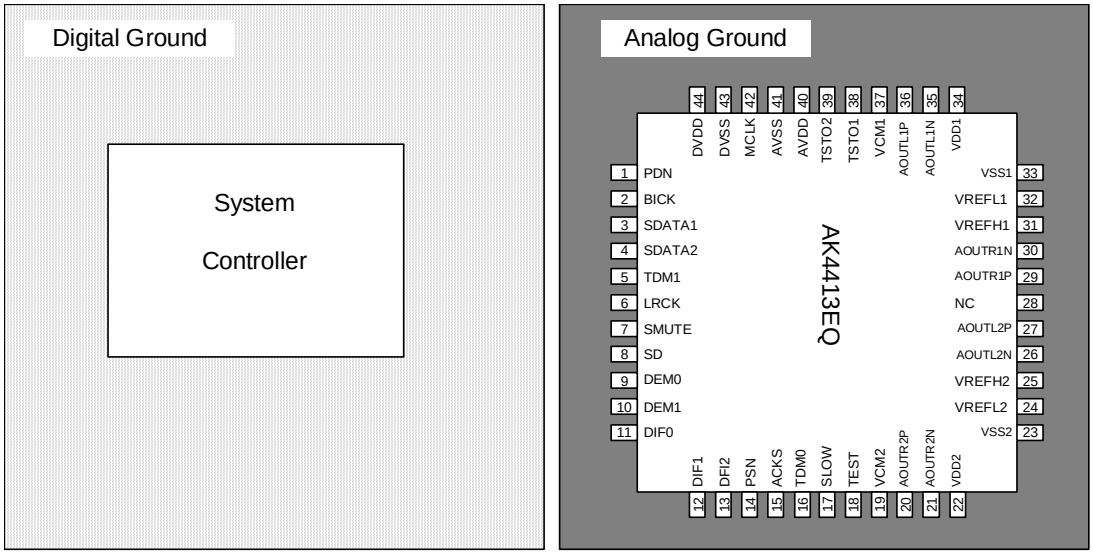


Figure 20. Ground Layout

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, VDD1/2 and DVDD respectively. AVDD and VDD1/2 are supplied from analog supply in system and DVDD is supplied from digital supply in system. Power lines of AVDD, VDD1/2 and DVDD should be distributed separately from the point with low impedance of regulator etc. The power up sequence between AVDD, VDD1/2 and DVDD is not critical. **VSS1-2, DVSS and AVSS must be connected to the same analog ground plane.** Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

2. Voltage Reference

The differential voltage between VREFH1/2 and VREFL1/2 sets the analog output range. The VREFH1/2 pin is normally connected to AVDD, and the VREFL1/2 pin is normally connected to VSS1/VSS2/AVSS. VREFH1/2 and VREFL1/2 should be connected with a 0.1μF ceramic capacitor as near as possible to the pin to eliminate the effects of high frequency noise. No load current may be drawn from VCM1/2 pin. All signals, especially clocks, should be kept away from the VREFH1/2 and VREFL1/2 pins in order to avoid unwanted noise coupling into the AK4413.

3. Analog Outputs

The analog outputs are full differential outputs and 2.8Vpp (typ, VREFH1/2 – VREFL1/2 = 5V) centered around AVDD/2. The differential outputs are summed externally, V_{AOUT} = (AOUT+) – (AOUT–) between AOUT+ and AOUT–. If the summing gain is 1, the output range is 5.6Vpp (typ, VREFH1/2 – VREFL1/2 = 5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Figure 21 shows an example of external LPF circuit summing the differential outputs by an op-amp.
Figure 22 shows an example of differential outputs and LPF circuit example by three op-amps.

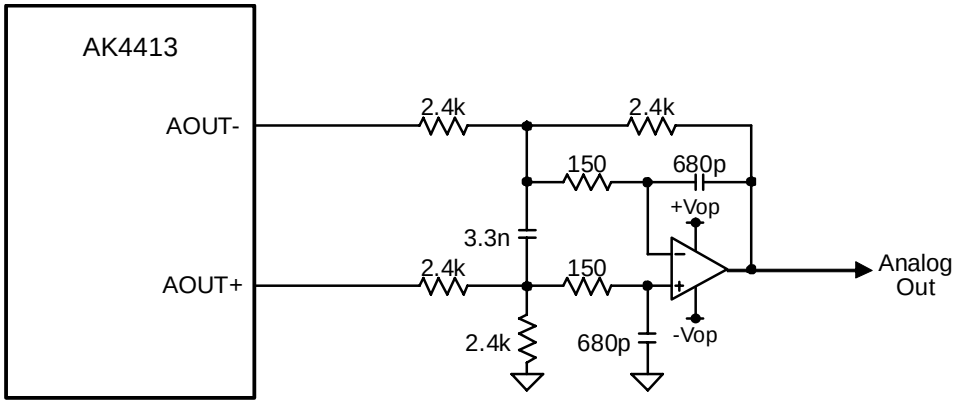


Figure 21. External LPF Circuit Example 1 for PCM (fc = 125kHz, Q=0.692)

Frequency Response	Gain
20kHz	–0.036dB
40kHz	–0.225dB
80kHz	–1.855dB

Table 27. Frequency Response of External LPF Circuit Example 1 for PCM

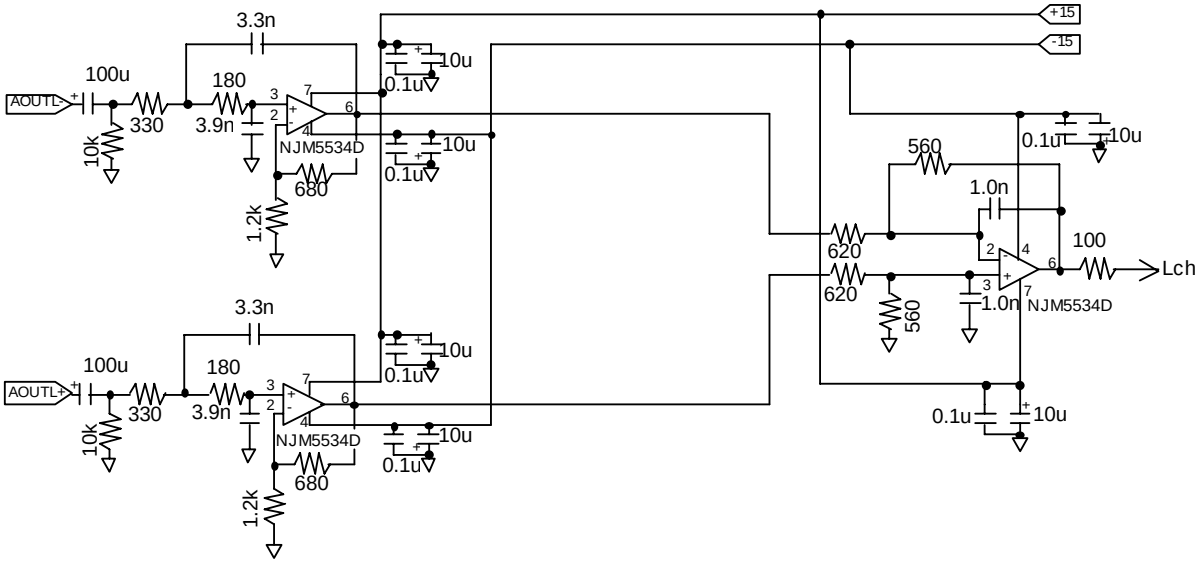


Figure 22. External LPF Circuit Example 2 for PCM

1		st Stage	2nd Stage	Total
Cut-off Frequency		182kHz	284kHz	-
Q		0.637	-	-
Gain		+3.9dB	-0.88dB	+3.02dB
Frequency Response	20kHz	-0.025	-0.021	-0.046dB
	40kHz	-0.106 -	0.085	-0.191dB
	80kHz	-0.517	-0.331	-0.848dB

Table 28. Frequency Response of External LPF Circuit Example 2 for PCM

4. Measurement Example

Figure 23 shows the relationship between THD+N and Frequency.

Measurement condition
Ta=25°C; AVDD=DVDD=3.3V, VDD1/2=5.0V; AVSS=VSS1/2=DVSS=0V; VREFH1/2=VDD1/2, VREFL1/2= AVSS;
Mono bit = "1"; Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz
Measured by Audio Precision System Two.

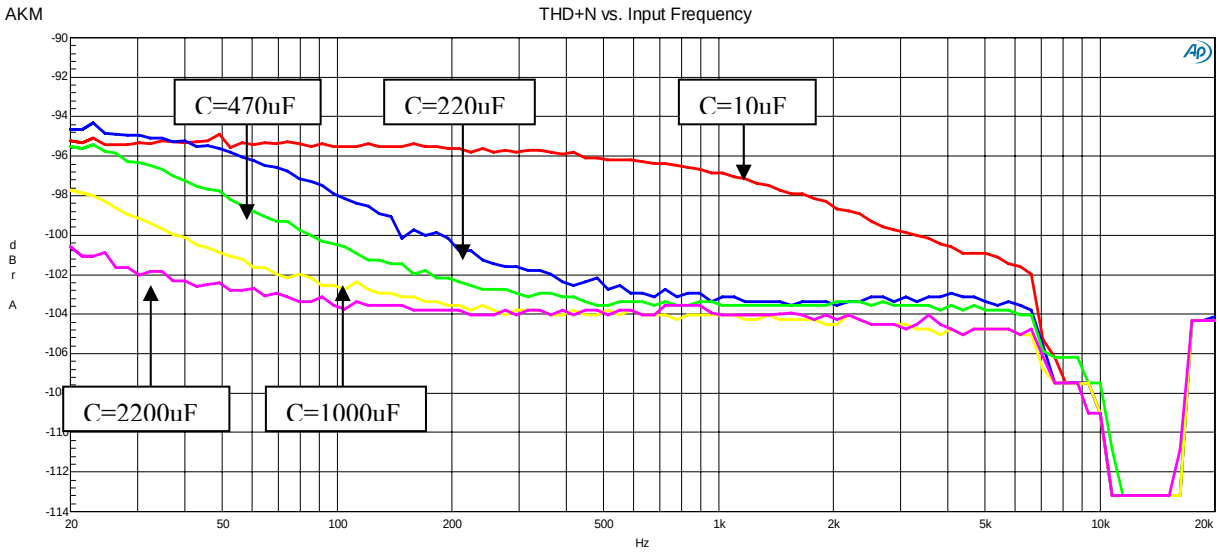
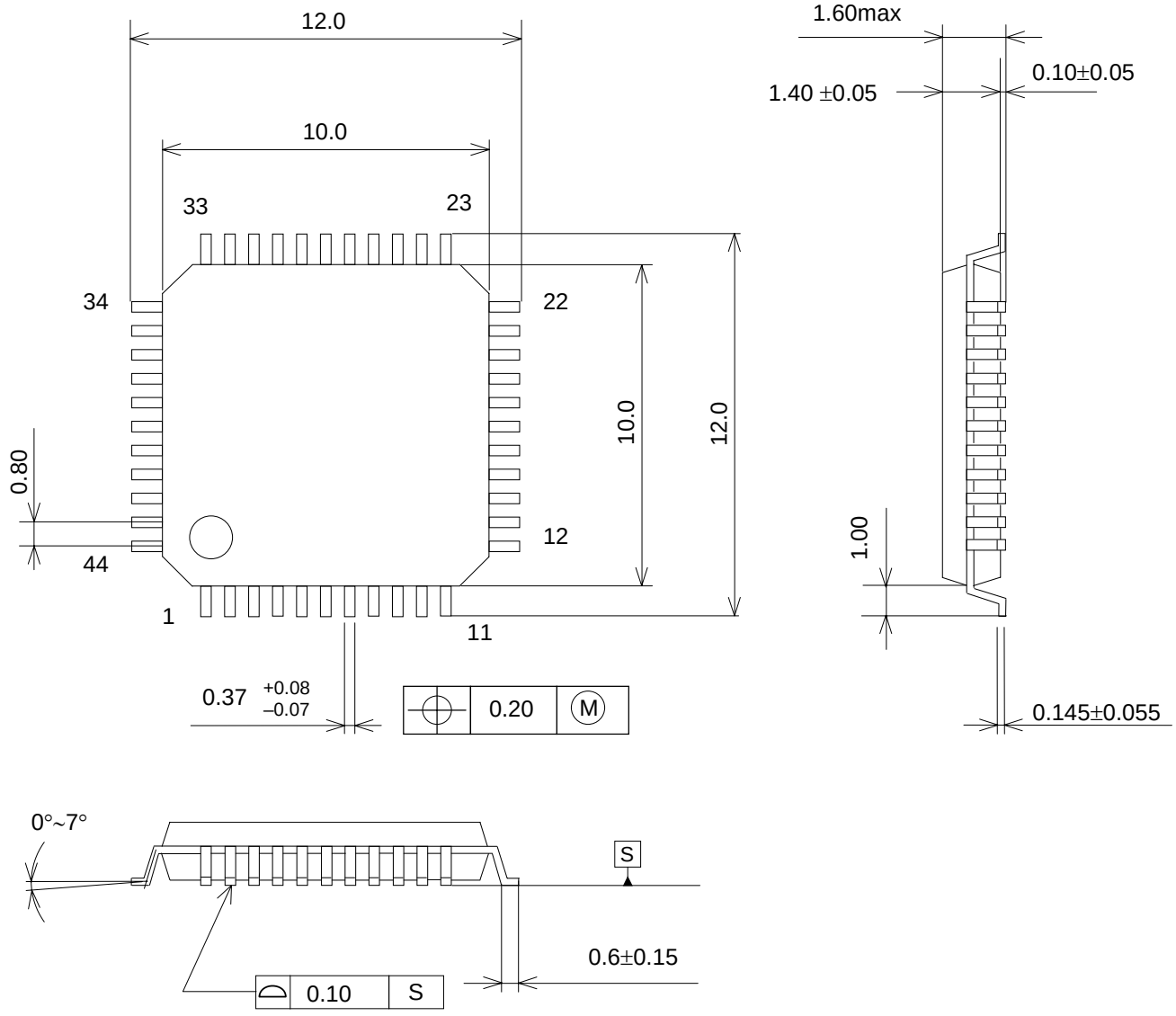


Figure 23. THD+N vs. Frequency

PACKAGE

44pin LQFP (Unit: mm)



■ Material & Lead finish

Package molding compound: Epoxy, Halogen (bromine and chlorine) free
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING

1) Pin #1 indication
2) AKM Logo
3) Date Code: XXXXXXX(7 digits)
4) Marking Code: AK4413
5) Audio 4 pro Logo

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
12/12/10	00	First Edition		
13/01/15	01	Error Correction	9	SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1/96/192kHz) Passband Ripple: "±0.005dB (max)" → "-0.0032dB (min), 0.0032 (max)" Note 12 was changed.
			10	SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1/96/192kHz) Passband Ripple: "±0.005dB (max)" → "-0.043dB (min), 0.043 (max)" Note 14 was changed.
			11	SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1/96/192kHz) Passband Ripple: "±0.005dB (max)" → "-0.0031dB (min), 0.0031 (max)"
			12	SHORT DELAY SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1/96/192kHz) Passband Ripple: "±0.005dB (max)" → "-0.05dB (min), 0.05 (max)"
			39	■ Register Definitions DEM1-0: The table number was corrected.
			42	A0H, Control 5 D3: The default value was changed. (0 → 1) D0: The default value was changed. (0 → 1) DEM3-2: Description was changed. PW2-1: Description was added.

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