

512MB DDR2 – SDRAM DIMM

240 Pin UDIMM

SEU06464H1CF1SA-25R

512MB PC2-6400 in FBGA Technology

RoHS compliant

Options:

- | | | |
|------------------------------|------|-------------|
| ▪ Data Rate / Latency | | Marking |
| DDR2 800 MT/s CL6 | | -25 |
| DDR2 667 MT/s CL5 | | -30 |
| ▪ Module Density | | |
| 512MB with 4 dies and 1 rank | | |
| ▪ Standard Grade | (tA) | 0°C to 70°C |
| | (tC) | 0°C to 85°C |

*) The refresh rate has to be doubled when 85°C < T_c < 95°C

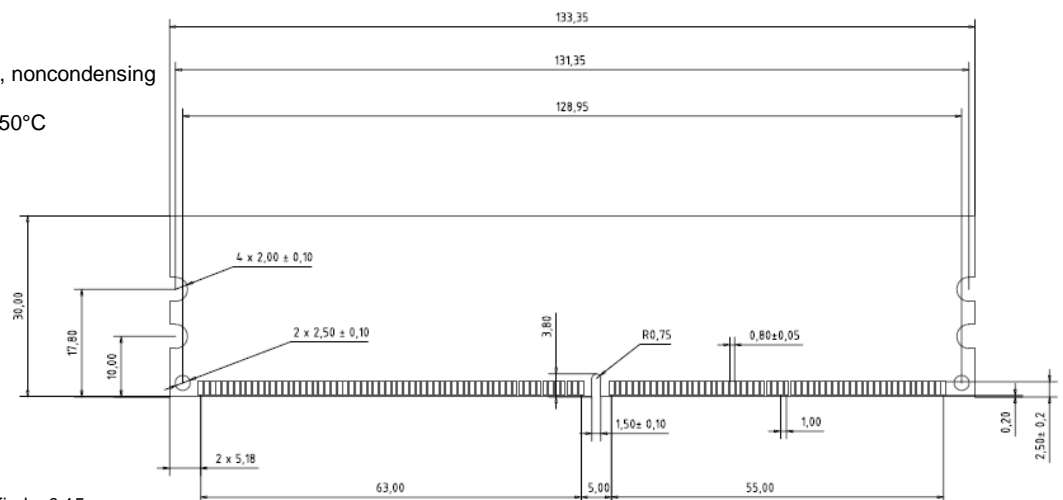
Environmental Requirements:

- Operating temperature (ambient)
standard Grade 0°C to 70°C
- Operating Humidity
10% to 90% relative humidity, noncondensing
- Operating Pressure
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
-55°C to 100°C
- Storage Humidity
5% to 95% relative humidity, noncondensing
- Storage Pressure
1682 PSI (up to 5000 ft.) at 50°C

Features:

- 240-pin 64-bit DDR2 Dual-In-Line Double Data Rate synchronous DRAM Module
- Module organization: single rank 64M x 64
- V_{DD} = 1.8V ±0.1V, V_{DDQ} 1.8V ±0.1V
- 1.8V I/O (SSTL_18 compatible)
- Serial Presence Detect (SPD) EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC PC2-6400 spec. and JEDEC- Standard MO-237. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- **DDR2 - SDRAM component Samsung K4T1G164QF-BCF7**
- 64Mx16 DDR2 SDRAM in FBGA-84 package
- Four bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Eight internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 4 or 8
- Adjustable data-output drive strength
- On-die termination (ODT)

Figure: mechanical dimensions¹



This Swissbit module is an industry standard 240-pin 8-byte DDR2 SDRAM Dual-In-line Memory Module (UDIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL_18 compatible.

The DDR2 SDRAM module uses the optional serial presence detect (SPD) function implemented via serial EEPROM using the standard I²C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
64M x 64bit	4 x 64M x 16bit (1024Mbit)	13	BA0, BA1, BA2	10	8k	S0#

Module Dimensions

in mm

133.35 (long) x 30(high) x 2,70 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SEU06464H1CF1SA-30R	512 MB	5.3 GB/s	3.0ns/667MT/s	5-5-5
SEU06464H1CF1SA-25R	512 MB	6.4 GB/s	2.5ns/800MT/s	6-6-6

Pin Name

A0 – 9, A11 – A12	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0 – DM7	Input Data Mask
DQS0 - DQS7	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
S0#	Chip Select
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0	Clock Enable
ODT0	On-Die Termination
CK0	Clock Inputs, positive line

CK0#	Clock Inputs, negative line
V _{DD}	Supply Voltage (1.8V±0.1V)
V _{REF}	Input / Output Reference
V _{SS}	Ground
V _{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0	On-Die Termination
NC	No Connection

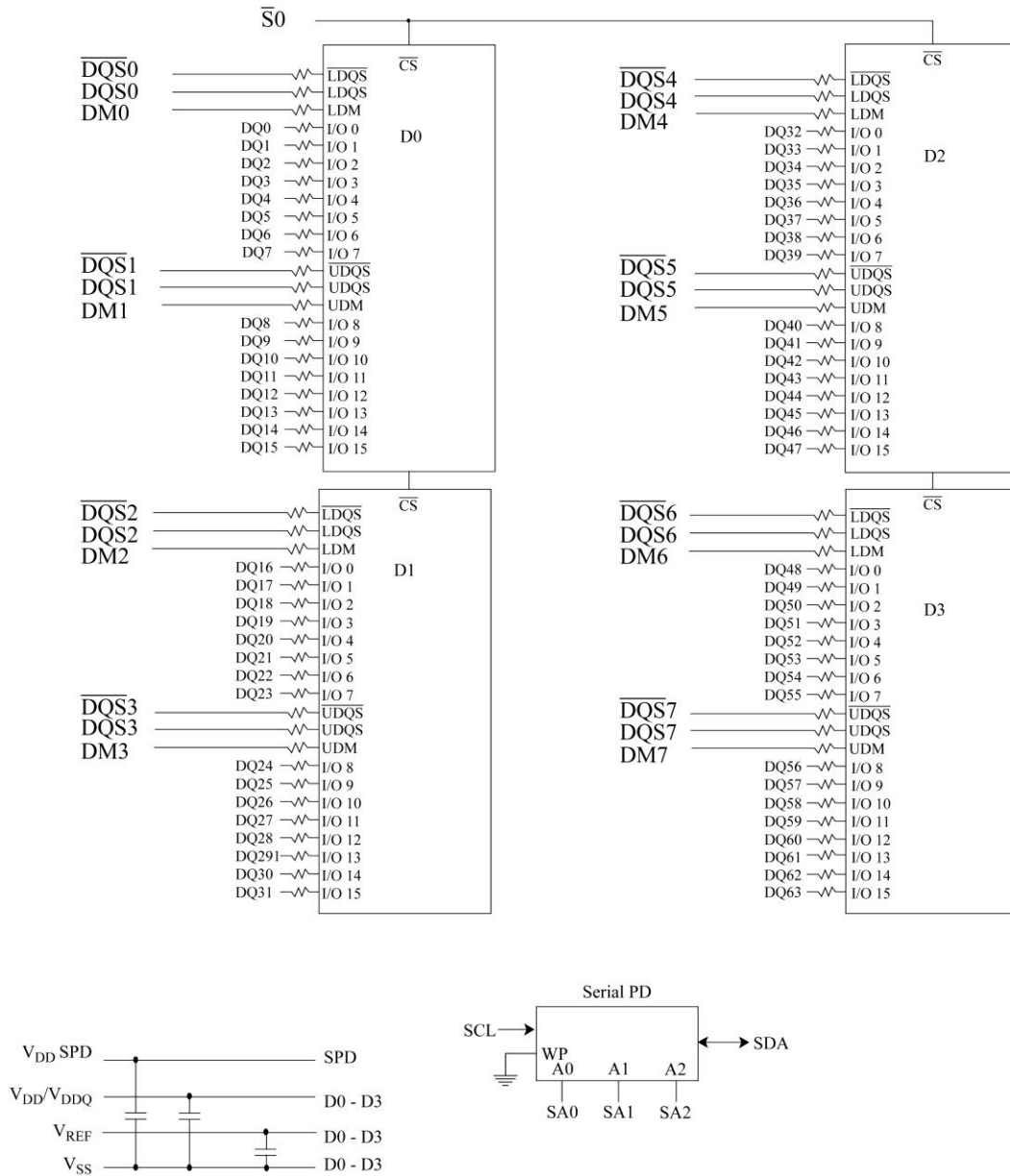
Pin Configuration

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	V _{REF}	121	V _{SS}	61	A4	181	V _{DDQ}
2	V _{SS}	122	DQ4	62	V _{DDQ}	182	A3
3	DQ0	123	DQ5	63	A2	183	A1
4	DQ1	124	V _{SS}	64	V _{DD}	184	V _{DD}
5	V _{SS}	125	DM0	65	V _{SS}	185	CK0
6	DQS0#	126	NC	66	V _{SS}	186	CK0#
7	DQS0	127	V _{SS}	67	V _{DD}	187	V _{DD}
8	V _{SS}	128	DQ6	68	NC(Par_In)	188	A0
9	DQ2	129	DQ7	69	V _{DD}	189	V _{DD}
10	DQ3	130	V _{SS}	70	A10/AP	190	BA1
11	V _{SS}	131	DQ12	71	BA0	191	V _{DDQ}
12	DQ8	132	DQ13	72	V _{DDQ}	192	RAS#
13	DQ9	133	V _{SS}	73	WE#	193	S0#
14	V _{SS}	134	DM1	74	CAS#	194	V _{DDQ}
15	DQS1#	135	NC	75	V _{DDQ}	195	ODT0
16	DQS1	136	V _{SS}	76	NC(CS1#)	196	A13
17	V _{SS}	137	NC(CK1)	77	NC(ODT1)	197	V _{DD}
18	NC(Reset)	138	NC(CK1#)	78	V _{DDQ}	198	V _{SS}
19	NC	139	V _{SS}	79	V _{SS}	199	DQ36
20	V _{SS}	140	DQ14	80	DQ32	200	DQ37
21	DQ10	141	DQ15	81	DQ33	201	V _{SS}
22	DQ11	142	V _{SS}	82	V _{SS}	202	DM4
23	V _{SS}	143	DQ20	83	DQS4#	203	NC
24	DQ16	144	DQ21	84	DQS4	204	V _{SS}
25	DQ17	145	V _{SS}	85	V _{SS}	205	DQ38
26	V _{SS}	146	DM2	86	DQ34	206	DQ39
27	DQS2#	147	NC	87	DQ35	207	V _{SS}
28	DQS2	148	V _{SS}	88	V _{SS}	208	DQ44
29	V _{SS}	149	DQ22	89	DQ40	209	DQ45
30	DQ18	150	DQ23	90	DQ41	210	V _{SS}
31	DQ19	151	V _{SS}	91	V _{SS}	211	DM5
32	V _{SS}	152	DQ28	92	DQS5#	212	NC

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
33	DQ24	153	DQ29	93	DQS5	213	V _{SS}
34	DQ25	154	V _{SS}	94	V _{SS}	214	DQ46
35	V _{SS}	155	DM3	95	DQ42	215	DQ47
36	DQS3#	156	NC	96	DQ43	216	V _{SS}
37	DQS3	157	V _{SS}	97	V _{SS}	217	DQ52
38	V _{SS}	158	DQ30	98	DQ48	218	DQ53
39	DQ26	159	DQ31	99	DQ49	219	V _{SS}
40	DQ27	160	V _{SS}	100	V _{SS}	220	NC(CK2)
41	V _{SS}	161	NC(CB4)	101	SA2	221	NC(CK2#)
42	NC(CB0)	162	NC(CB5)	102	NC(TEST)	222	V _{SS}
43	NC(CB1)	163	V _{SS}	103	V _{SS}	223	DM6
44	V _{SS}	164	NC(DM8)	104	DQS6#	224	NC
45	NC(DQS8#)	165	NC	105	DQS6	225	V _{SS}
46	NC(DQS8)	166	V _{SS}	106	V _{SS}	226	DQ54
47	V _{SS}	167	NC(CB6)	107	DQ50	227	DQ55
48	NC(CB2)	168	NC(CB7)	108	DQ51	228	V _{SS}
49	NC(CB3)	169	V _{SS}	109	V _{SS}	229	DQ60
50	V _{SS}	170	V _{DDQ}	110	DQ56	230	DQ61
51	V _{DDQ}	171	NC(CKE1)	111	DQ57	231	V _{SS}
52	CKE0	172	V _{DD}	112	V _{SS}	232	DM7
53	V _{DD}	173	NC(A15)	113	DQS7#	233	NC
54	BA2	174	NC(A14)	114	DQS7	234	V _{SS}
55	NC(Par_Out)	175	V _{DDQ}	115	V _{SS}	235	DQ62
56	V _{DDQ}	176	A12	116	DQ58	236	DQ63
57	A11	177	A9	117	DQ59	237	V _{SS}
58	A7	178	V _{DD}	118	V _{SS}	238	V _{DDSPD}
59	V _{DD}	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1

Signals in brackets (...) may be connected at the DIMM socket, but are not used on the DIMM

**FUNCTIONAL BLOCK DIAGRAM 512MB DDR2 SDRAM DIMM,
1 RANK AND 4 COMPONENTS**



- BA0 - BA2 → BA0-BA2: SDRAMs D0 - D3
- A0 - A15 → A0-A15: SDRAMs D0 - D3
- RAS → RAS: SDRAMs D0 - D3
- CAS → CAS: SDRAMs D0 - D3
- CKE0 → CKE: SDRAMs D0 - D3
- WE → WE: SDRAMs D0 - D3
- ODT0 → ODT: SDRAMs D0 - D3

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ, DM, DQS/DQS resistors: 22 Ohms ± 5%.
4. BAx, Ax, RAS, CAS, WE resistors: 10 Ohms ± 5%.
5. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-1.0	2.3	V
I/O Supply Voltage	V_{DDQ}	-0.5	2.3	V
V_{DDL} Supply Voltage	V_{DDL}	-0.5	2.3	V
Voltage on any pin relative to V_{SS}	V_{in}, V_{out}	-0.5	2.3	V
INPUT LEAKAGE CURRENT Any input $0V \leq V_{IN} \leq V_{DD}$, V_{REF} pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = $0V$)	I_I			μA
Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
CK, CK#		-20	20	
DM		-5	5	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$)	I_{OZ}	-5	5	μA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-16	16	μA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V
V_{DDL} Supply Voltage	V_{DDL}	1.7	1.8	1.9	V
I/O Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	V_{TT}	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.125$	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.25$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.25$	V

CAPACITANCE

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

 (0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

Parameter & Test Condition	Symbol	max.		Unit	
		5300-555	6400-666		
OPERATING CURRENT *) : One device bank Active-Precharge; t _{RC} = t _{RC} (I _{DD}); t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	200	220	mA	
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}); t _{RC} = t _{RC} (I _{DD}), t _{RAS} = t _{RAS} MIN (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I _{DD4W}	I _{DD1}	240	260	mA	
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD2P}	40	40	mA	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD2Q}	88	88	mA	
PRECHARGE STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD2N}	108	116	mA	
ACTIVE POWER-DOWN CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD3P}	Fast PDN Exit MR[12] = 0	96	100	mA
		Slow PDN Exit MR[12] = 1	80	80	
ACTIVE STANDBY CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD3N}	148	160	mA	
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4R}	380	420	mA	

Parameter & Test Condition	Symbol	max.		Unit
		5300-555	6400-666	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4W}	360	380	mA
BURST REFRESH CURRENT: t _{CK} = t _{CK} (I _{DD}); refresh command at every t _{RFC} (I _{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD5}	420	440	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V _{REF} ; DQ's are floating at V _{REF}	I _{DD6}	40	40	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = t _{RCD} (I _{DD}) - 1 x t _{CK} (I _{DD}); t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RRD} = t _{RRD} (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I _{DD7}	660	720	mA

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I _{DD} MEASUREMENT CONDITIONS			
SYMBOL	5300-555	6400-666	Unit
CL (I _{DD})	5	6	t _{CK}
t _{RCD} (I _{DD})	15	15	ns
t _{RC} (I _{DD})	60	60	ns
t _{RRD} (I _{DD})	10	10	ns
t _{CK} (I _{DD})	3.0	2.5	ns
t _{RAS} MIN (I _{DD})	45	45	ns
t _{RAS} MAX (I _{DD})	70,000	70,000	ns
t _{RP} (I _{DD})	15	15	ns
t _{RFC} (I _{DD})	127.5	127.5	ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$

AC CHARACTERISTICS			5300-555		6400-666		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
Clock cycle time	CL = 6		-	-	2.5	8.0	ns
	CL = 5	$t_{\text{CK}}(5)$	3.0	8.0	3.0	8.0	ns
	CL = 4	$t_{\text{CK}}(4)$	3.75	8.0	3.75	8.0	ns
	CL = 3	$t_{\text{CK}}(3)$	5.0	8.0	5.0	8.0	ns
CK high-level width		t_{CH}	0.48	0.52	0.48	0.52	t_{CK}
CK low-level width		t_{CL}	0.48	0.52	0.48	0.52	t_{CK}
Half clock period		t_{HP}	min ($t_{\text{CH}}, t_{\text{CL}}$)		min ($t_{\text{CH}}, t_{\text{CL}}$)		ps
Access window (output) of DQ _s from CK/CK#		t_{AC}	-0.45	+0.45	-0.40	+0.40	ns
Data-out high-impedance window from CK/CK#		t_{HZ}		+0.45 (= $t_{\text{AC max}}$)		+0.40 (= $t_{\text{AC max}}$)	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.45 (= $t_{\text{AC min}}$)	+0.45 (= $t_{\text{AC max}}$)	-0.40 (= $t_{\text{AC min}}$)	+0.40 (= $t_{\text{AC max}}$)	ns
DQ and DM input setup time relative to DQS		t_{DSa}	0.30		0.25		ns
DQ and DM input hold time relative to DQS		t_{DHa}	0.30		0.25		ns
DQ and DM input setup time relative to DQS		$t_{\text{DS(base)}}$	0.1		0.05		ns
DQ and DM input hold time relative to DQS		$t_{\text{DH(base)}}$	0.175		0.125		ns
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		t_{CK}
Data hold skew factor		t_{QHS}		0.34		0.30	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	$t_{\text{HP}} - t_{\text{QHS}}$		$t_{\text{HP}} - t_{\text{QHS}}$		ns
Data valid output window		t_{DVW}	$t_{\text{QH}} - t_{\text{DQSQ}}$		$t_{\text{QH}} - t_{\text{DQSQ}}$		ns
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}
DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK}
DQS output access time from CK/CK#		t_{DQSCK}	-0.40	+0.40	-0.35	+0.35	ns
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}
DQS -DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.24		0.20	ns
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
DQS write preamble		t_{WPRE}	0.35		0.35		t_{CK}
DQS write preamble setup time		t_{WPRES}	0		0		ns
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Write command to first DQS latching transition			WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	0.6		0.6		t_{CK}
Address and control input setup time		t_{ISa}	0.4		0.375		ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$

AC CHARACTERISTICS		5300-555		6400-666		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
Address and control input hold time	t_{IHa}	0.4		0.375		ns
Address and control input setup time	t_{ISb}	0.20		0.175		ns
Address and control input hold time	t_{IHb}	0.275		0.25		ns
CAS# to CAS# command delay	t_{CCD}	2		2		t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	60		60		ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	10		10		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		15		ns
Four bank Activate period	t_{FAW}	50		45		ns
ACTIVE to PRECHARGE command	t_{RAS}	40	70,000	40	70,000	ns
Internal READ to precharge command delay	t_{RTP}	7.5		7.5		ns
Write recovery time	t_{WR}	15		15		ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{\text{WR}} + t_{\text{RP}}$		$t_{\text{WR}} + t_{\text{RP}}$		ns
Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		ns
PRECHARGE command period	t_{RP}	15		15		ns
PRECHARGE ALL command period	t_{RPA}	$t_{\text{RP}} + t_{\text{CK}}$		$t_{\text{RP}} + t_{\text{CK}}$		ns
LOAD MODE command cycle time	t_{MRD}	2		2		t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	127.5		127.5		ns
Average periodic refresh interval						
$0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	t_{REFI}		7.8		7.8	μs
$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$			3.9		3.9	
Exit SELF REFRESH to non-READ command	t_{XSNR}	$t_{\text{RFC}}(\text{min}) + 10$		$t_{\text{RFC}}(\text{min}) + 10$		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		t_{CK}
Exit SELF REFRESH timing reference	t_{ISXR}	t_{IS}		t_{IS}		ps
ODT turn-on delay	t_{AOND}	2		2		t_{CK}
ODT turn-on	t_{AON}	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 700$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 600$	ps
ODT turn-on (power-down mode)	t_{AONPD}	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT to power-down entry latency	t_{ANPD}	3		3		t_{CK}

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ +85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		5300-555		6400-666		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
ODT power-down exit latency	t _{AXPD}	8		8		t _{CK}
ODT enable from MRS command	t _{MOD}	0	12	0	12	ns
Exit active power-down to READ command, MR [bit 12 = 0]	t _{XARD}	2		2		t _{CK}
Exit active power-down to READ command, MR [bit 12 = 1]	t _{XARDS}	7 – AL		8 – AL		t _{CK}
Exit precharge power-down to any non-READ command	t _{XP}	2		2		t _{CK}
CKE minimum high/low time	t _{CKE}	3		3		t _{CK}

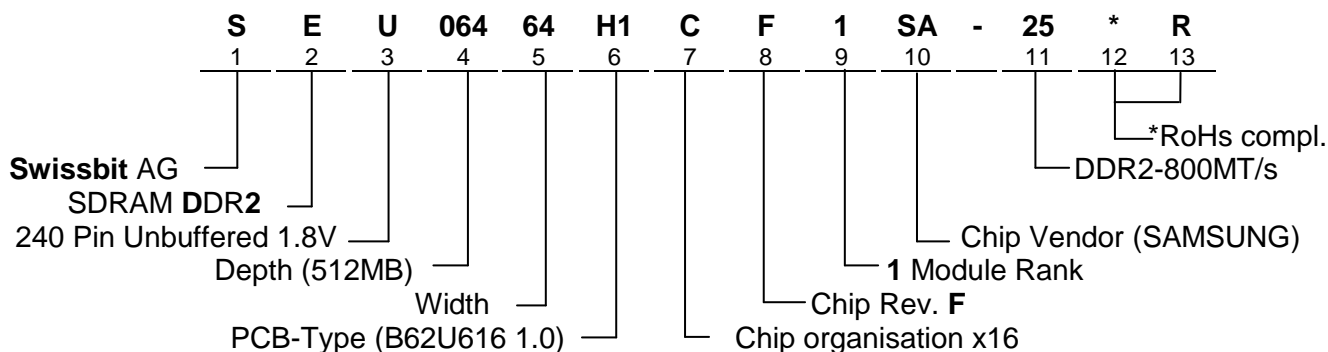
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	5300-555	6400-666
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x08	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0D	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A	
5	DIMM HIGHT AND MODULE RANKS	0x60	
6	MODULE DATA WIDTH	0x40	
7	MODULE DATA WIDTH (continued)	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS (V_{DDQ})	0x05	
9	SDRAM CYCLE TIME, (t_{CK}) [max CL] CAS LATENCY = 6 (6400), CL = 5 (5300)	0x30	0x25
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) [max CL] CAS LATENCY = 6 (6400); CL = 5 (5300)	0x45	0x40
11	MODULE CONFIGURATION TYPE	0x00	
12	REFRESH RATE / TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x10	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00	
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00	
16	BURST LENGTHS SUPPORTED	0x0C	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08	
18	CAS LATENCIES SUPPORTED	0x38	0x70
19	MODULE THICKNESS	0x01	
20	DDR2 DIMM TYPE	0x02	
21	SDRAM MODULE ATTRIBUTES	0x00	
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x07	
23	SDRAM CYCLE TIME, (t_{CK}) [max CL – 1] CAS LATENCY = 5 (6400), CL = 4 (5300)	0x3D	0x30
24	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 1] CAS LATENCY = 5 (6400), CL = 4 (5300)	0x50	0x45
25	SDRAM CYCLE TIME, (t_{CK}) [max CL – 2] CAS LATENCY = 4 (6400), CL = 3 (5300)	0x50	0x3D
26	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 2] CAS LATENCY = 4 (6400), CL = 3 (5300)	0x60	0x50
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3C	
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x28	
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3C	
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x2D	
31	MODULE BANK DENSITY	0x80	

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	5300-555	6400-666
32	ADDRESS AND COMMAND SETUP TIME, (t _{ISb})	0x20	0x17
33	ADDRESS AND COMMAND HOLD TIME, (t _{IHb})	0x27	0x25
34	DATA / DATA MASK INPUT SETUP TIME, (t _{DSb})	0x10	0x05
35	DATA / DATA MASK INPUT HOLD TIME, (t _{DHb})	0x17	0x12
36	WRITE RECOVERY TIME, (t _{WR})	0x3C	
37	WRITE to READ Command Delay, (t _{WTR})	0x1E	
38	READ to PRECHARGE Command Delay, (t _{RTP})	0x1E	
39	Mem Analysis Probe	0x00	
40	Extension for Bytes 41 and 42	0x06	
41	MIN ACTIVE AUTO REFRESH TIME, (t _{RC})	0x3C	
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t _{RFC})	0x7F	
43	SDRAM DEVICE MAX CYCLE TIME, (t _{CKMAX})	0x80	
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t _{DQSQ})	0x18	0x14
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t _{QHS})	0x22	0x1E
46	PLL Relock Time	0x00	
47-61	Optional Features, not supported	0x00	
62	SPD REVISION	0x13	
63	CHECKSUM FOR BYTES 0-62	0xA7	0x71
64-66	MANUFACTURER'S JEDEC ID CODE	0x7F	
67	MANUFACTURER'S JEDEC ID CODE (continued)	0Xda	
68-71	MANUFACTURER'S JEDEC ID CODE (continued)	0x00	
72	MANUFACTURING LOCATION	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
73-90	MODULE PART NUMBER (ASCII)	"SEU06464H1CF1SA-xxR"	
91	PCB IDENTIFICATION CODE	X	
92	IDENTIFICATION CODE (continued)	X	
93	YEAR OF MANUFACTURE IN BCD	X	
94	WEEK OF MANUFACTURE IN BCD	X	
95-98	MODULE SERIAL NUMBER	X	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	0x00	
128-255	Open for customer use	0xff	

Part Number Code



* optional / additional information

Locations

Swissbit AG

Industriestrasse 4 – 8
CH – 9552 Bronschhofen
Switzerland
Phone: +41 (0)71 913 03 03
Fax: +41 (0)71 913 03 15

Swissbit Germany GmbH

Wolfener Strasse 36
D – 12681 Berlin
Germany
Phone: +49 (0)30 93 69 54 – 0
Fax: +49 (0)30 93 69 54 – 55

Swissbit NA, Inc.

14 Willett Avenue, Suite 301A
Port Chester, NY 10573
USA
Phone: +1 914 935 1400
Fax: +1 914 935 9865

Swissbit NA, Inc.

3913 Todd Lane, Suite – 307
Austin, TX 78744
USA
Phone: +1 512 302 9001
Fax: +1 512 302 4808

Swissbit Japan, Inc.

3F Core Koenji,
2-1-24 Koenji-Kita, Sugunami-Ku,
Tokyo 166-0002
Japan
Phone: +81 3 5356 3511
Fax: +81 3 5356 3512