

# R2A20168NP/SA/SP

8-bit 8ch D/A Converter with Buffer Amplifiers

R03DS0019EJ0200  
Rev.2.00  
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## Description

The R2A20168 is an integrated circuit semiconductor of CMOS structure with 8 channels of built in D/A unnecessary and enabling configuration of a system with few component parts. Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD. Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc ( 0 to 5V ), making peripheral elements unnecessary and enabling configuration of a system with few component parts. Very small QFN package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

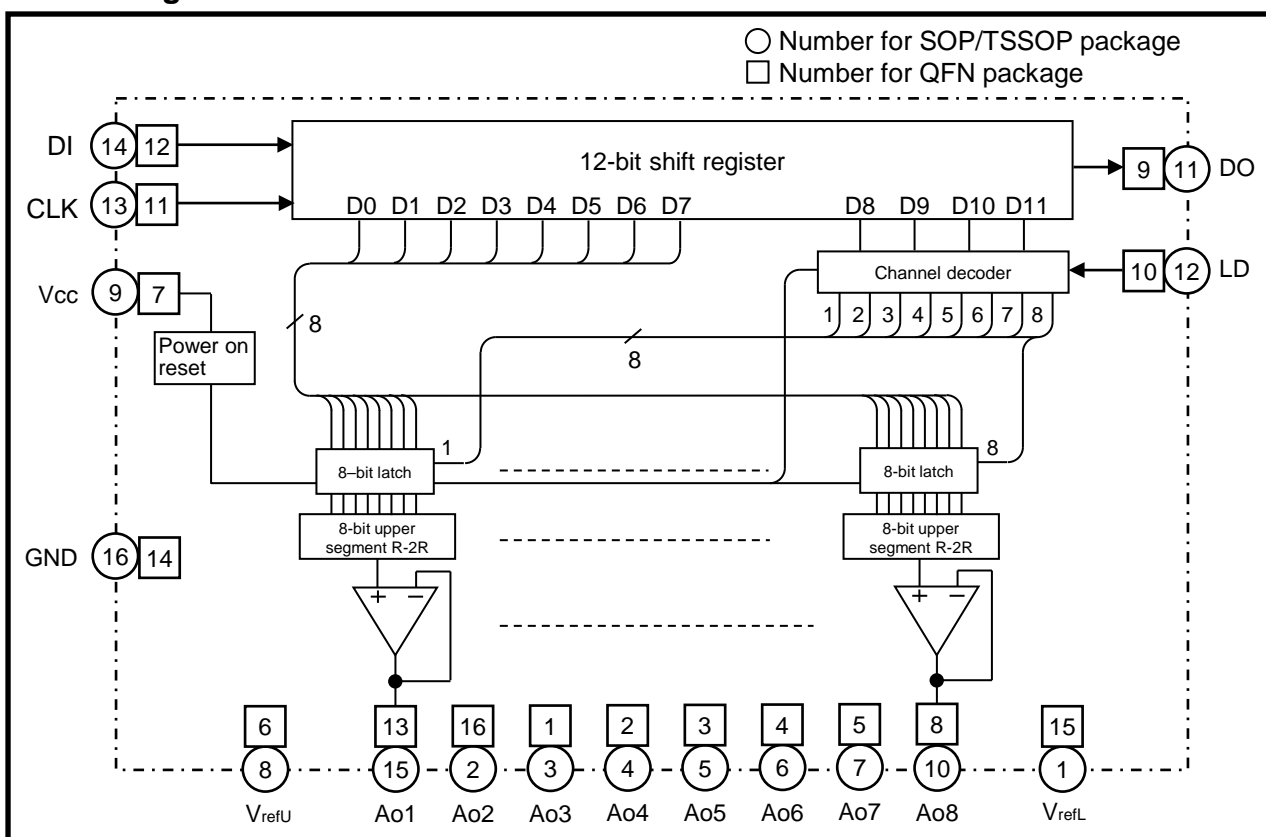
## Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Data transfer format: 12-bit serial data input type by 3 wire ( DI, SCK, LD )
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc ( 0 to 5V )
- Very small size package line-up: QFN-16(pin pitch: 0.5mm), TSSOP-16(pin pitch 0.65mm)

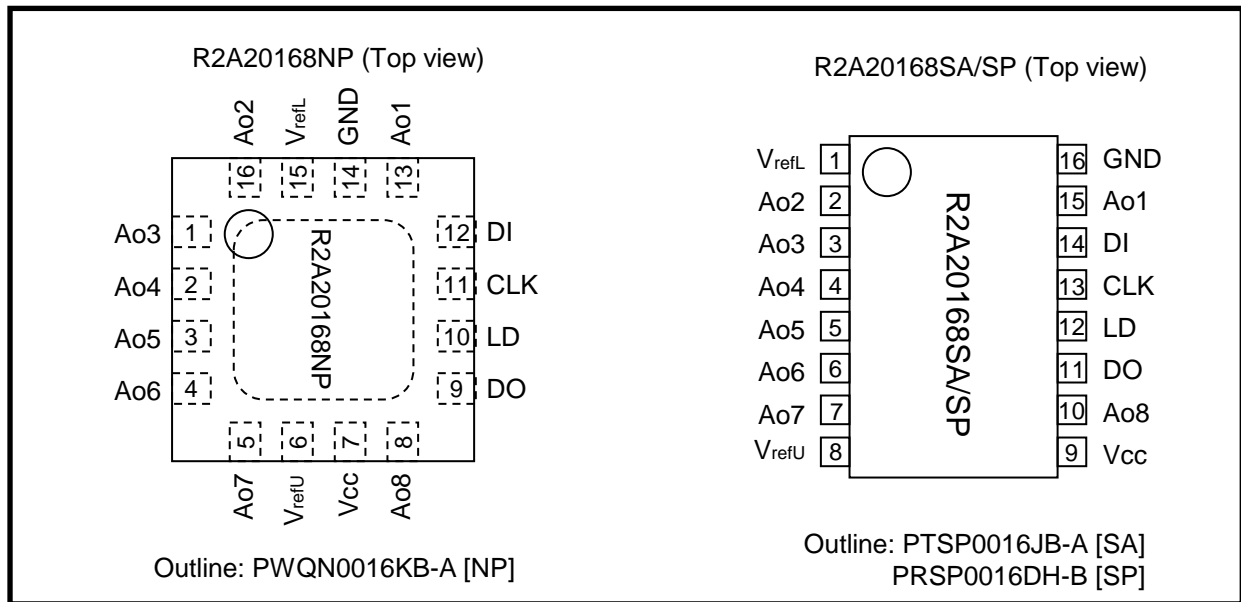
## Application

- Conversion from digital data to analog control data for home-use and industrial equipment.
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Blurring correction control or various control of the interchangeable lens of digital still camera.
- Automatic adjustment by combination with microcomputer and EEPROM.  
(substitution of half fixed resistance)

## Block Diagram



## Pin Arrangement



## Pin Description

Pin No.		Symbol	Function
[QFN]	[TSSOP /SOP]		
12	14	DI	Serial data input terminal. ( Input serial data with a 12-bit data length )
11	13	CLK	Serial clock input terminal (Input signal from DI terminal is input to 12-bit shift register at rise of serial clock.)
10	12	LD	Load terminal (When High level is input to LD terminal, value in 12-bit shift register is loaded into decoder and 8-bit latch.)
9	11	Do	Serial data output terminal (Data is sequentially output from the MSB bit.)
13	15	Ao1	8-bit resolution D/A converter output terminals (After power on, all channels are reset and DAC data 00h is output.)
16	2	Ao2	
1	3	Ao3	
2	4	Ao4	
3	5	Ao5	
4	6	Ao6	
5	7	Ao7	
8	10	Ao8	
7	9	Vcc	Power supply terminal
14	16	GND	GND terminal
6	8	VrefU	D/A converter upper reference voltage input terminal
15	1	VrefL	D/A converter lower reference voltage input terminal

**Absolute Maximum Ratings**

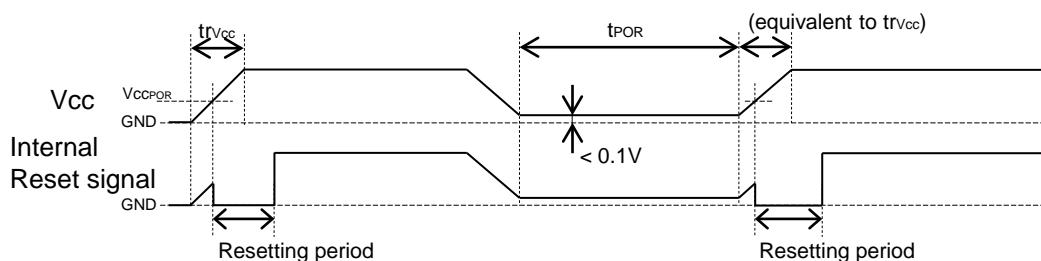
(Ta= +25deg unless otherwise noted)

Item	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>		-0.3 to +6.5	V
D/A converter upper reference voltage	V <sub>refU</sub>		-0.3 to +6.5	V
D/A converter lower reference voltage	V <sub>refL</sub>		-0.3 to +6.5	V
Buffer amplifier output current	I <sub>AO</sub>	Continuous	-2.0 to +2.0	mA
Input voltage	V <sub>in</sub>		-0.3 to V <sub>CC</sub> +0.3 <+6.5	V
Output voltage	V <sub>o</sub>		-0.3 to V <sub>CC</sub> +0.3 <+6.5	V
Power dissipation	P <sub>d</sub>	Ta= +85deg	290(NP) / 150(SA) / 300(SP)	mW
Thermal derating factor	K theta	Ta> +25deg	7.25(NP) / 3.75(SA) / 7.5(SP)	mW/deg
Operating temperature	Topr		-30 to +85	deg
Storage temperature	Tstg		-40 to +125	deg

**Electrical Characteristics**« Digital Part » (V<sub>CC</sub>, V<sub>refU</sub> = +5V +/-10%, V<sub>CC</sub>>V<sub>refU</sub>, GND, V<sub>refL</sub> =0V, Ta= -30 to +85deg, Unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Supply voltage	V <sub>CC</sub>		2.7	5.0	5.5	V
Supply current	I <sub>CC</sub>	CLK =1MHz, V <sub>CC</sub> =5V, I <sub>AO</sub> =0μA	-	0.4	1.2	mA
Input leak current	I <sub>LK</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-10	-	10	μA
Input low voltage	V <sub>IL</sub>		-	-	0.2V <sub>CC</sub>	V
Input high voltage	V <sub>IH</sub>	4.0V < V <sub>CC</sub>	0.55V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> £ 4.0V	0.8V <sub>CC</sub>	-	-	V
Output low voltage	V <sub>OL</sub>	4.0V < V <sub>CC</sub> , I <sub>OL</sub> = 2.0mA	-	-	0.4	V
		V <sub>CC</sub> < 4.0V, I <sub>OL</sub> = 1.5mA	-	-	0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400μA	V <sub>CC</sub> - 0.4	-	-	V
Supply voltage rise time *1	t <sub>rVCC</sub>	V <sub>CC</sub> = 0 to 2.7V	100	-	-	μs
Internal reset operating voltage *1	V <sub>CCPOR</sub>	V <sub>CC</sub> = 0 to 2.7V	-	1.5	1.9	V
Power supply restart interval (Power supply OFF à ON) *1	t <sub>POR</sub>	V <sub>CC</sub> < 0.1V	1	-	-	ms

\*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (t<sub>POR</sub>).



« Analog Part » (  $V_{CC}$ ,  $V_{refU} = +5V \pm 10\%$ ,  $V_{CC} > V_{refU}$ ,  $GND$ ,  $V_{refL} = 0V$ ,  $T_a = -30$  to  $+85$ deg, Unless otherwise noted )

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Current dissipation	$I_{refU}$	$V_{refU}=5V$ , $V_{refL}=0V$ , $I_{AO}=0\mu A$ , Data condition: at maximum current	-	1.0	2.0	mA
D/A converter upper reference voltage range *2	$V_{refU}$	$V_{CC} \geq 4.5V$	3.5	-	$V_{CC}$	V
		$V_{CC} < 4.5V$	$0.7V_{CC}$	-	$V_{CC}$	
D/A converter lower reference voltage range *2	$V_{refL}$	$V_{CC} \geq 4.5V$	GND	-	$V_{CC}-3.5$	V
		$V_{CC} < 4.5V$	GND	-	$0.3V_{CC}$	
Buffer amplifier output voltage range	$V_{AO}$	$I_{AO} = \pm 100 \mu A$	0.1	-	$V_{CC} - 0.1$	V
		$I_{AO} = \pm 500 \mu A$	0.2	-	$V_{CC} - 0.2$	V
Buffer amplifier output drive range	$I_{AO}$	Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V	-1.0	-	1.0	mA
Differential nonlinearity	$S_{DL}$	$V_{refU} = 4.79V$ , $V_{refL} = 0.95V$ , $V_{CC} = 5.5V$ (15mV/LSB), Without load ( $I_{AO} = 0\mu A$ )	-0.7	-	0.7	LSB
Nonlinearity	$S_L$		-1.0	-	1.0	LSB
Zero code error	$S_{ZERO}$		-2.0	-	2.0	LSB
Full scale error	$S_{FULL}$		-2.0	-	2.0	LSB
Output capacitive load	$C_o$		-	-	0.1	$\mu F$
Buffer amplifier output impedance	$R_o$		-	5.0	-	ohm

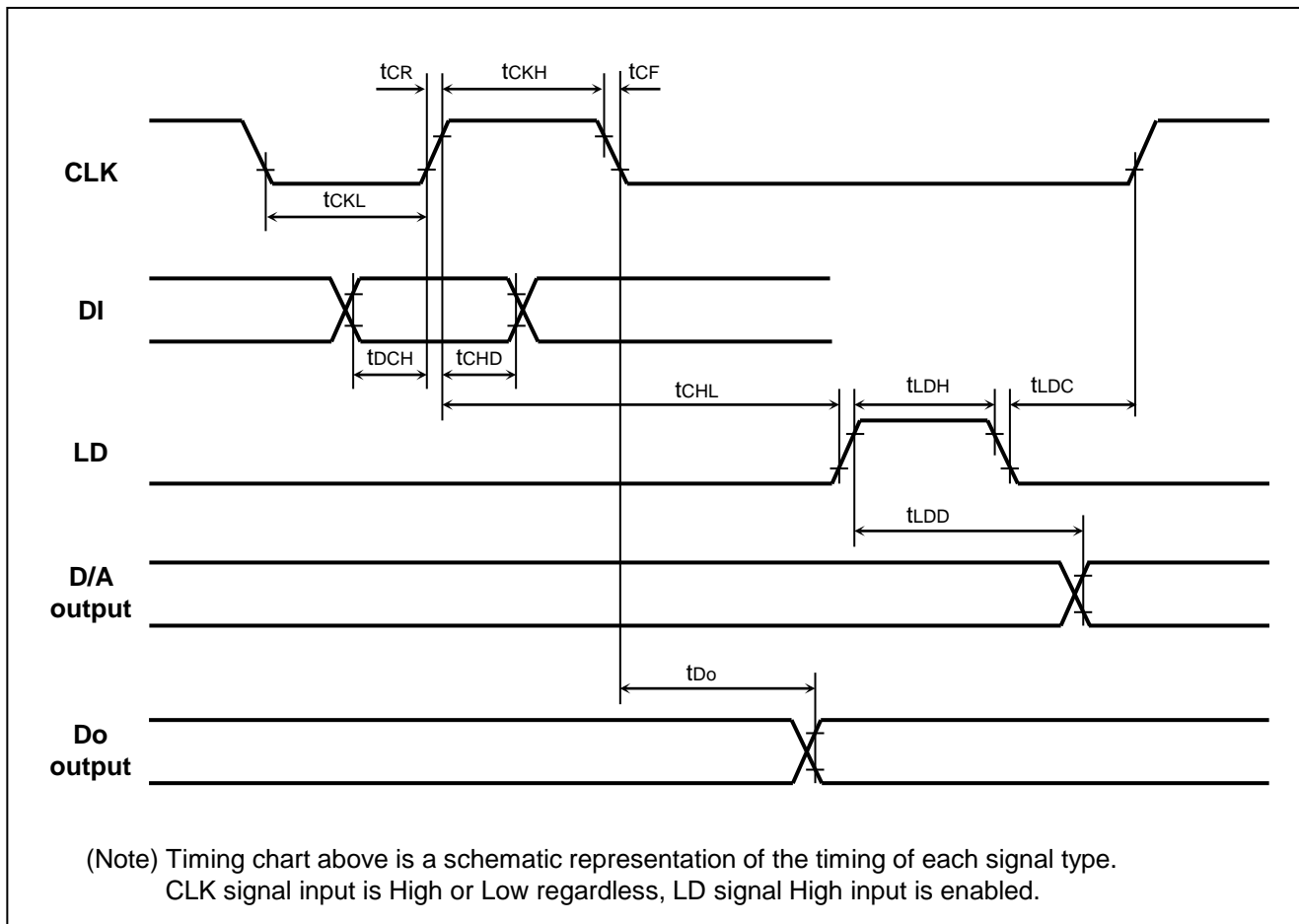
\*2 : The output does not necessary be the value with the reference voltage setting range.  
The output value is determined by the buffer amplifier output voltage range ( $V_{AO}$ ).

## AC Characteristics

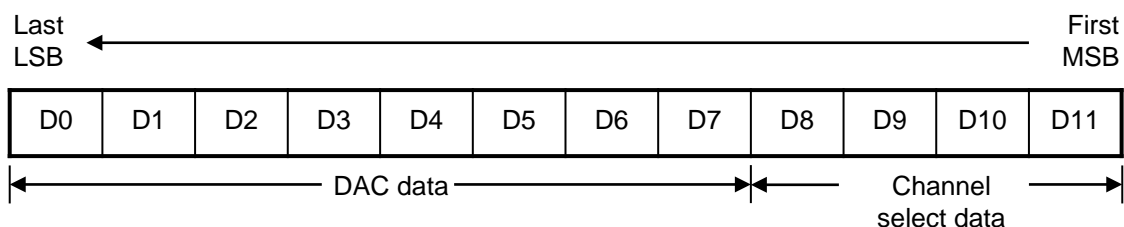
(  $V_{CC}, V_{refU} = +5V \pm 10\%$ ,  $V_{CC} \geq V_{refU}$ ,  $GND = V_{refL} = 0V$ ,  $T_a = -30$  to  $+85$ deg, unless otherwise noted )

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Clock frequency	f <sub>CLK</sub>		-	1.0	10	MHz
Clock low pulse width	t <sub>CKL</sub>		40	-	-	ns
Clock high pulse width	t <sub>CKH</sub>		40	-	-	ns
Clock rise time	t <sub>CR</sub>		-	-	200	ns
Clock fall time	t <sub>CF</sub>		-	-	200	ns
Data setup time	t <sub>DCH</sub>		4	-	-	ns
Data hold time	t <sub>CHD</sub>		30	-	-	ns
LD setup time	t <sub>CHL</sub>		40	-	-	ns </td
LD hold time	t <sub>LDC</sub>		40	-	-	ns
LD high pulse width	t <sub>LDH</sub>		40	-	-	ns
Data output delay time	t <sub>DO</sub>	$C_L < 100$ pF	-10	-	50	ns
D/A output settling time	t <sub>LDD</sub>	$T_a = 25$ deg, $C_L < 100$ pF, $V_{AO}: 0.5 \rightarrow 4.5V$ , The time until the output becomes the final value of 1/2 LSB.	-	-	150	μs

## Timing Chart



## Digital Data Format



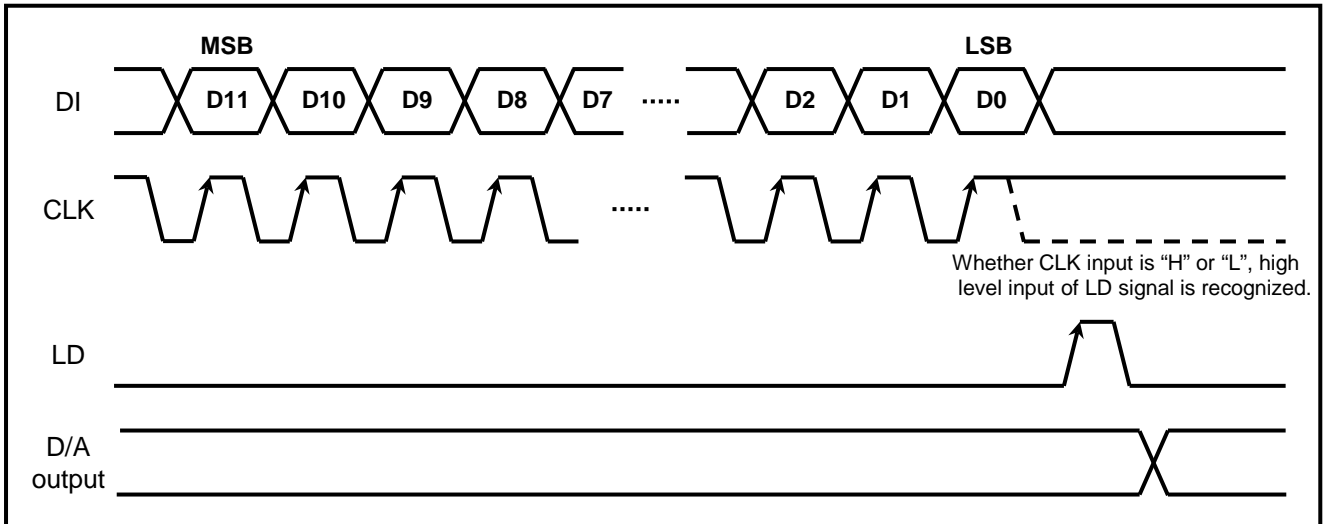
### Channel select data

D8	D9	D10	D11	Chanel Selection
0	0	0	0	Don't care
0	0	0	1	Ao1 select
0	0	1	0	Ao2 select
0	0	1	1	Ao3 select
0	1	0	0	Ao4 select
0	1	0	1	Ao5 select
0	1	1	0	Ao6 select
0	1	1	1	Ao7 select
1	0	0	0	Ao8 select
1	0	0	1	Don't care
:	:	:	:	:
1	1	1	0	Don't care
1	1	1	1	Don't care

### DAC data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	$(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 1 + V_{\text{refL}}$
1	0	0	0	0	0	0	0	$(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 2 + V_{\text{refL}}$
0	1	0	0	0	0	0	0	$(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 3 + V_{\text{refL}}$
1	1	0	0	0	0	0	0	$(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 4 + V_{\text{refL}}$
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 255 + V_{\text{refL}}$
1	1	1	1	1	1	1	1	$V_{\text{refU}}$

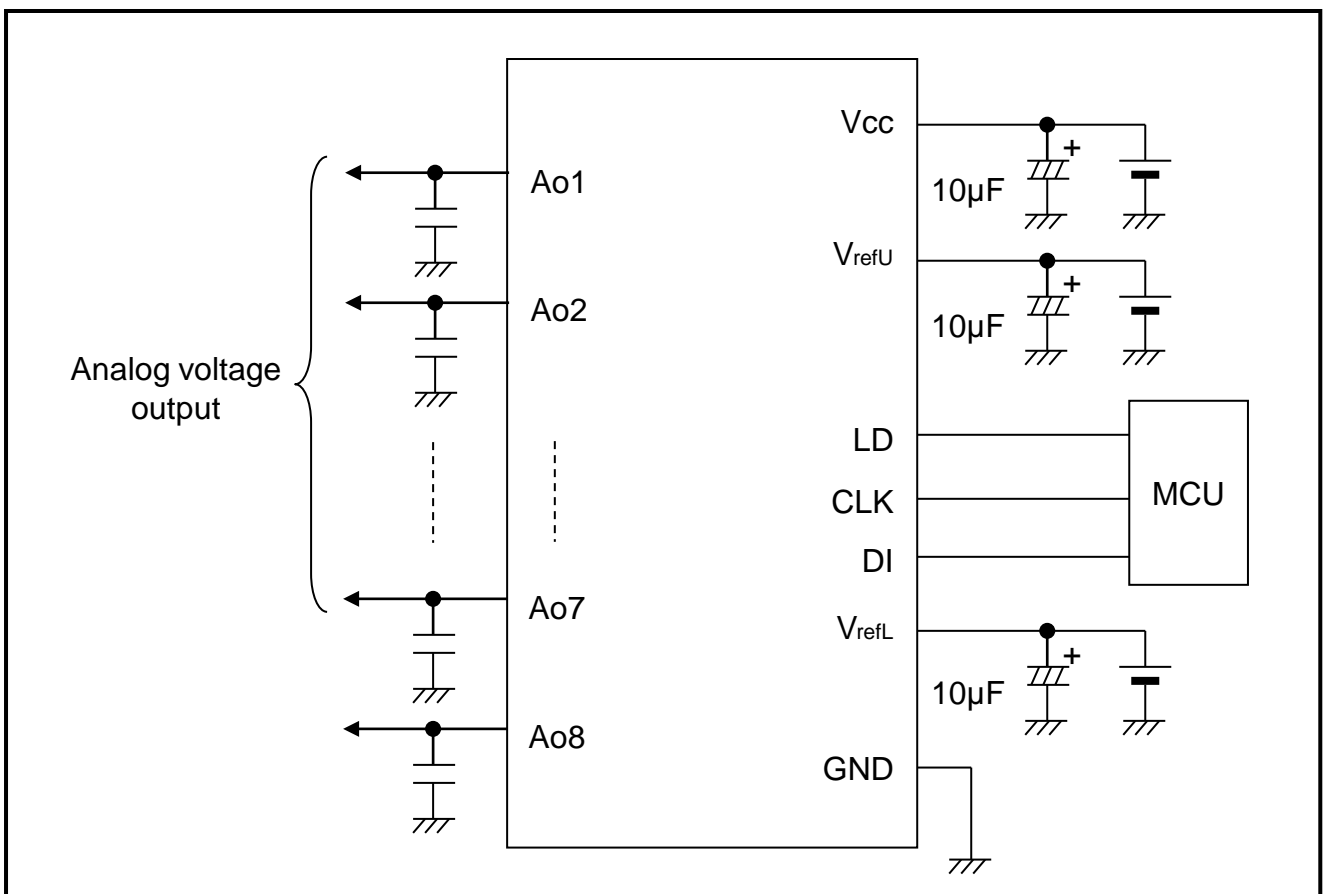
**Data Timing Chart ( Model )**



**Precaution For Use**

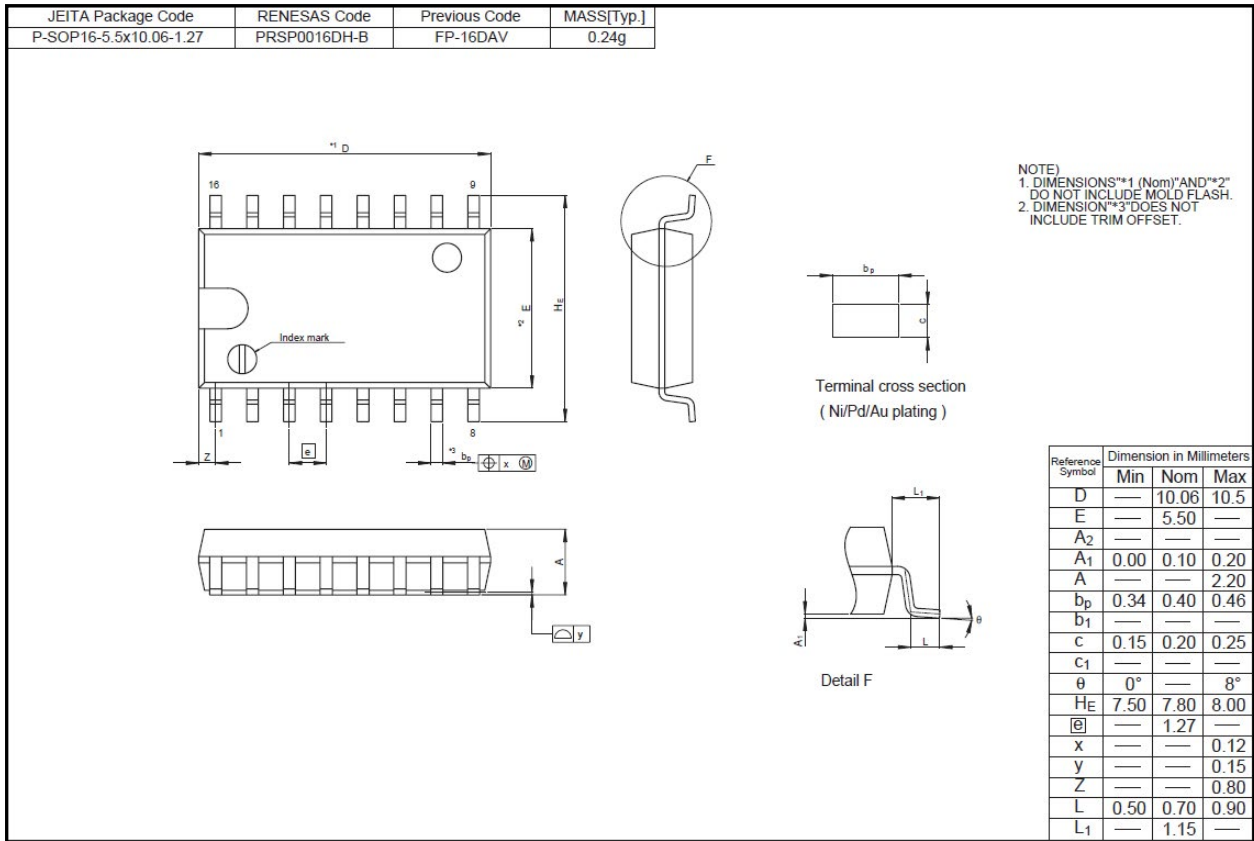
- There are three terminals ( $V_{CC}$ ,  $V_{refU}$ ,  $V_{refL}$ ) that should be impressed a constant voltage. When ripple or spike noise is input to this terminal, there is fear that the accuracy of D/A conversion becomes lower and this IC malfunction. So, when use this IC, please connect capacitor between these terminals ( $V_{CC}$ ,  $V_{refU}$ ,  $V_{refL}$ ) and GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor ( 0.1 $\mu$ F Max ) among output to GND for every noise elimination.

**Standard Application Circuit**

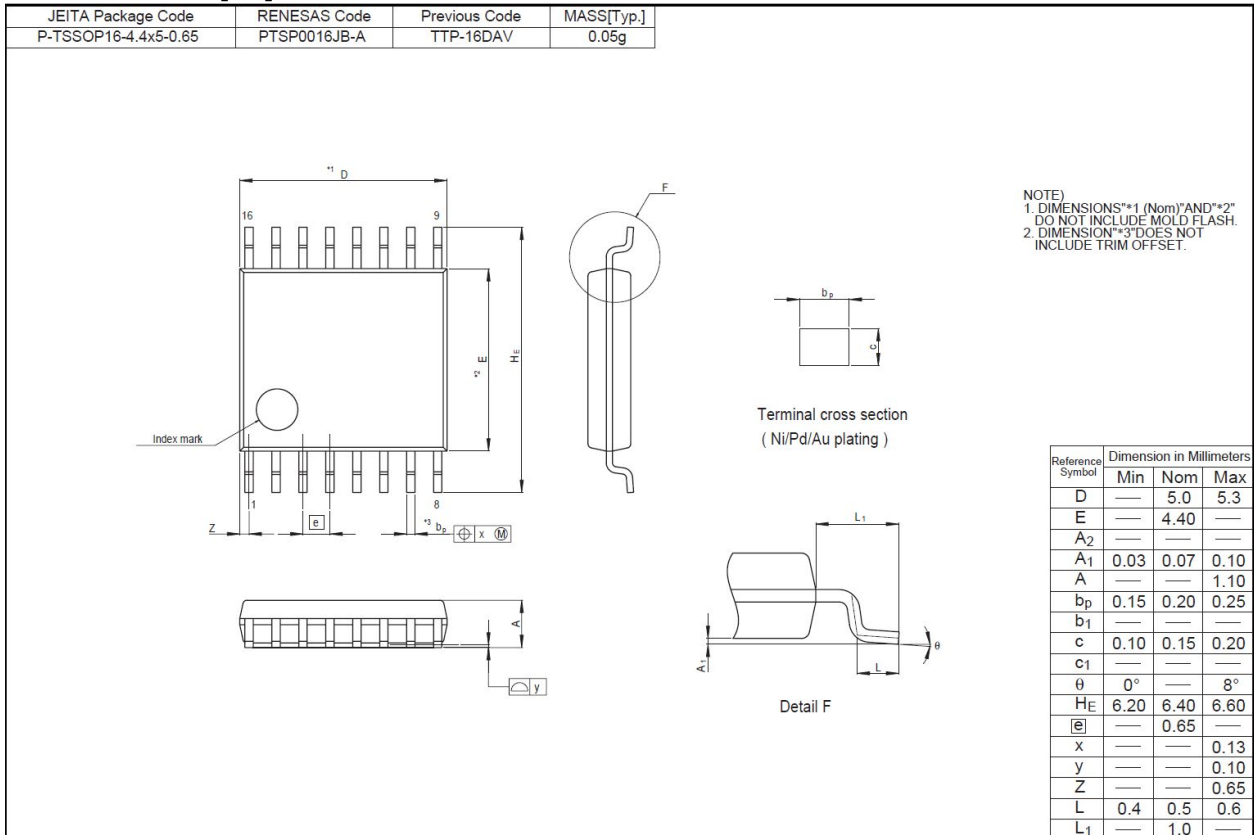


### Package Dimensions

#### PRSP0016DH-B [SP]

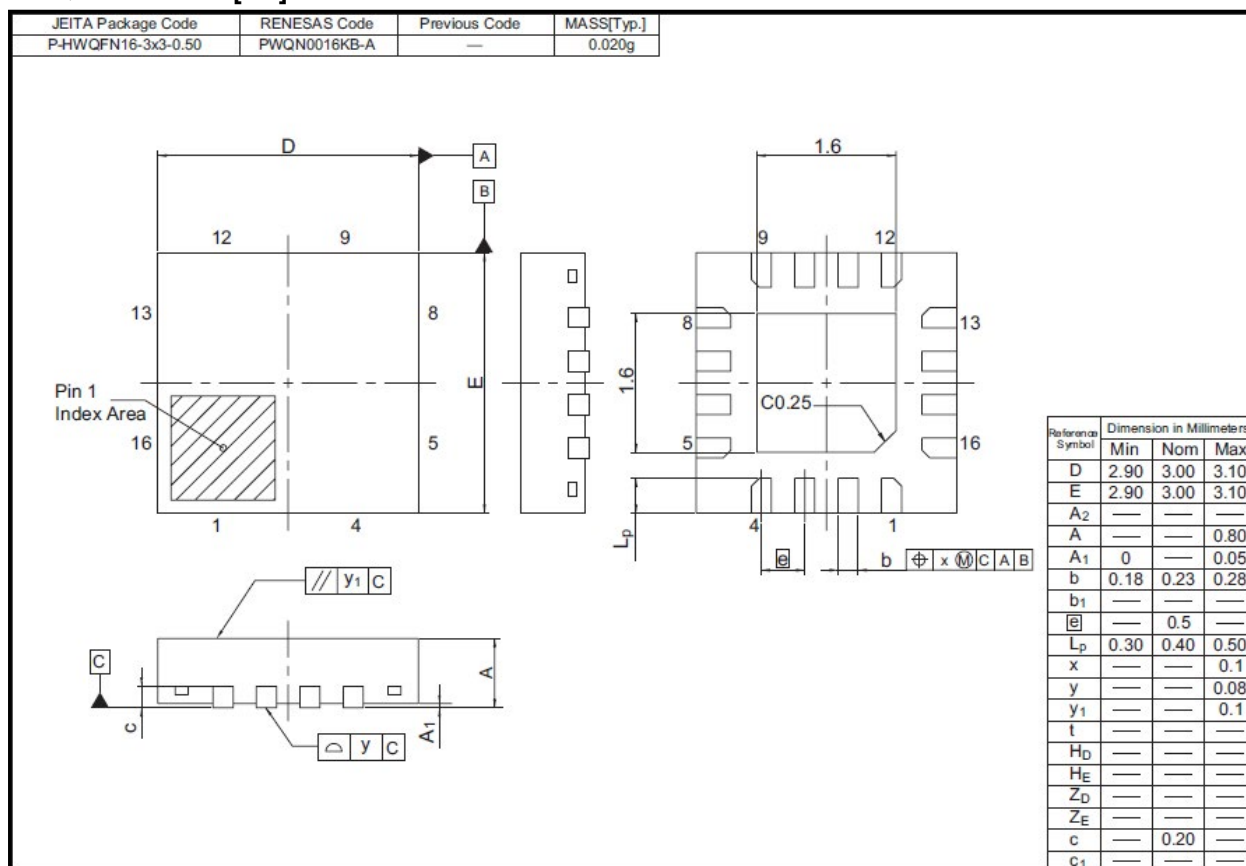


#### PTSP0016JB-A [SA]





## PWQN0016KB-A [NP]



## Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20168SP	SOP-16	PRSP0016DH-B	SP	Embossed Taping/2,000 pcs.
R2A20168SA	TSSOP-16	RTSP0016JB-A	SA	Embossed Taping/2,000 pcs.
R2A20168NP	QFN-16	PWQN0016KB-A	NP	Embossed Taping/3,000 pcs.

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