
ML610Q111/ML610Q112

8-bit Microcontroller

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as timers, PWM, UART, I²C bus interface (master/slave), synchronous serial port, voltage level supervisor analog comparators and 10-bit successive approximation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipe line architecture parallel processing. The Flash ROM that is installed as program memory, and the on-chip debug function that is installed, enable program debugging and programming on customer's board.

FEATURES

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set:
Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time:
 - 30.5us (@32.768kHz system clock)
 - 0.122us (@8.192MHz system clock)
- Internal memory
 - ML610Q111:
Flash memory :
 - Internal 24Kbyte Flash memory (12K x 16bit) for program including unusable 32byte test data area.
 - Internal 4Kbyte Flash memory (2K x 16bit) for data.SRAM :
 - Internal 2Kbyte data RAM (2K x 8bit)
 - ML610Q112:
Flash memory :
 - Internal 32Kbyte Flash memory (16K x 16bit) for program including unusable 32byte test data area.
 - Internal 4Kbyte Flash memory (2K x 16bit) for data.SRAM :
 - Internal 4Kbyte data RAM (4K x 8bit)
 - Flash Memory operating condition and specification
 - Refer to the chapter Electrical characteristics “FLASH MEMORY SPECIFICATION”.
- Interrupt controller
 - 1 non-maskable interrupt source (Internal source: 1(WDT))
 - 30 maskable interrupt sources (Internal sources: 23, External source: 7)
- Time base counter (TBC)
 - Low-speed time base counter: 1 channel
 - High-speed time base counter: 1 channel
(This time base counter is divided by 1-16, then it can be used as a clock of the Timer and PWM.)

- Watchdog timer (WDT)
 - Non-maskable interrupt and reset
(Non-maskable interrupt is generated by the first overflow, and reset is generated by the second overflow)
 - Free running
 - Overflow period: 7 types selectable by software (23.4ms, 31.25ms, 62.5ms, 125ms, 500ms, 2s, and 8s)
- Timer
 - 8-bit x 6 channels (16-bit configuration available, 16-bit x 3ch)
 - Supports auto reload timer mode/One shot timer mode
 - Timer count start/stop by software or external input trigger
(Timer function with external trigger input supports for only 2ch. Selectable external pins/analog comparator output as an external trigger.)
 - The effective minimum pulse width of the external trigger input: Timer clock 3 ϕ (about 183 ns @ 16.384 MHz)
 - Allows measurement of pulse width etc. using an external trigger input.
 - 8-selectable clock frequency as counter clock per channel
- PWM
 - Resolution 16-bit
 - Single output x 3ch, Multiple three outputs x 1ch
 - Allows an output of the PWM signal in a cycle of about 122ns (@PLLCLK = 16.384MHz) to 2s (@LSCLK = 32.768kHz)
 - Supports one shot PWM mode
 - PWM start/stop by software and external trigger input
(Selectable external pins, analog comparator output or timer interrupt as external trigger)
 - 3-selectable clock frequency as PWM clock per channel
- UART
 - TXD/RXD x 2ch
 - Half-Duplex Communication
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I²C bus interface
 - Master function: standard mode (100kbit/s@8MHz), Fast mode (400kbit/s@8MHz)
 - Slave function : standard mode (100kbit/s)
- Synchronous serial port (SSIO)
 - 1ch
 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- Successive approximation type A/D converter (SA-ADC)
 - 10-bit A/D converter
 - Analog Input
 - 6ch (ML610Q111)
 - 8ch (ML610Q112)

- Analog comparator
 - 2ch
 - ch0: Allows comparison of the voltage level of the two external pins or comparison of one external pin and internal reference voltage level.
 - ch1: Allows comparison of one external pin and internal reference voltage level
 - Input common mode voltage range : $V_{DD} = 0.1V$ to $V_{DD} - 1.5V$
 - Internal reference voltage : 0.1-0.8V (Selectable in 50mV increments)
 - Hysteresis (Comparator0 only): 20mV(Typ.)
 - Allows selection of with/without interrupt sampling and interrupt edge.
- General-purpose ports (GPIO)
 - Input/output port
 - 15ch (ML610Q111)
 - 25ch (ML610Q112)
- Reset
 - Reset by the RESET_N pin
 - Reset by power-on detection
 - Reset by the watchdog timer (WDT) 2nd overflow
 - Reset by the voltage level supervisor (VLS) function: Selectable by software
- Voltage level supervisor (VLS)
 - 2ch
 - ch0: It can be used for voltage level detection reset
 - ch1: It can be used for voltage level detection interrupt
 - Judgment accuracy: $\pm 3.0\%$ (Typ.)
- Clock
 - Low-speed clock:
 - Built-in RC oscillation (32.768kHz)
 - High-speed clock:
 - Built-in PLL oscillation (16.384MHz)
 - High-speed external clock (max. 8.192MHz)
 Maximum CPU clock is 8.192MHz.
 - Selection of high-speed clock mode by software:
 - Built-in PLL oscillation
 - External clock
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states)
 - STOP mode: Stop of oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock).
 - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
 - ML610Q111:
 - 20-pin TSSOP:
 - ML610Q111-xxxTD (blank product: ML610Q111-NNNTD)
 - ML610Q112:
 - 32-pin LQFP:
 - ML610Q112-xxxTC (blank product: ML610Q112-NNNTC)
- Guaranteed operating range
 - Operating temperature (ambience): -40°C to 105°C (Flash write/erase: -20°C to +85°C)
 - Operating voltage: VDD=2.7V to 5.5V

BLOCK DIAGRAM

The block diagram is shown in figure 1.

“*” means secondary function, tertiary function or quaternary function of each port.

“()^{*2}” means the function of ML610Q112.

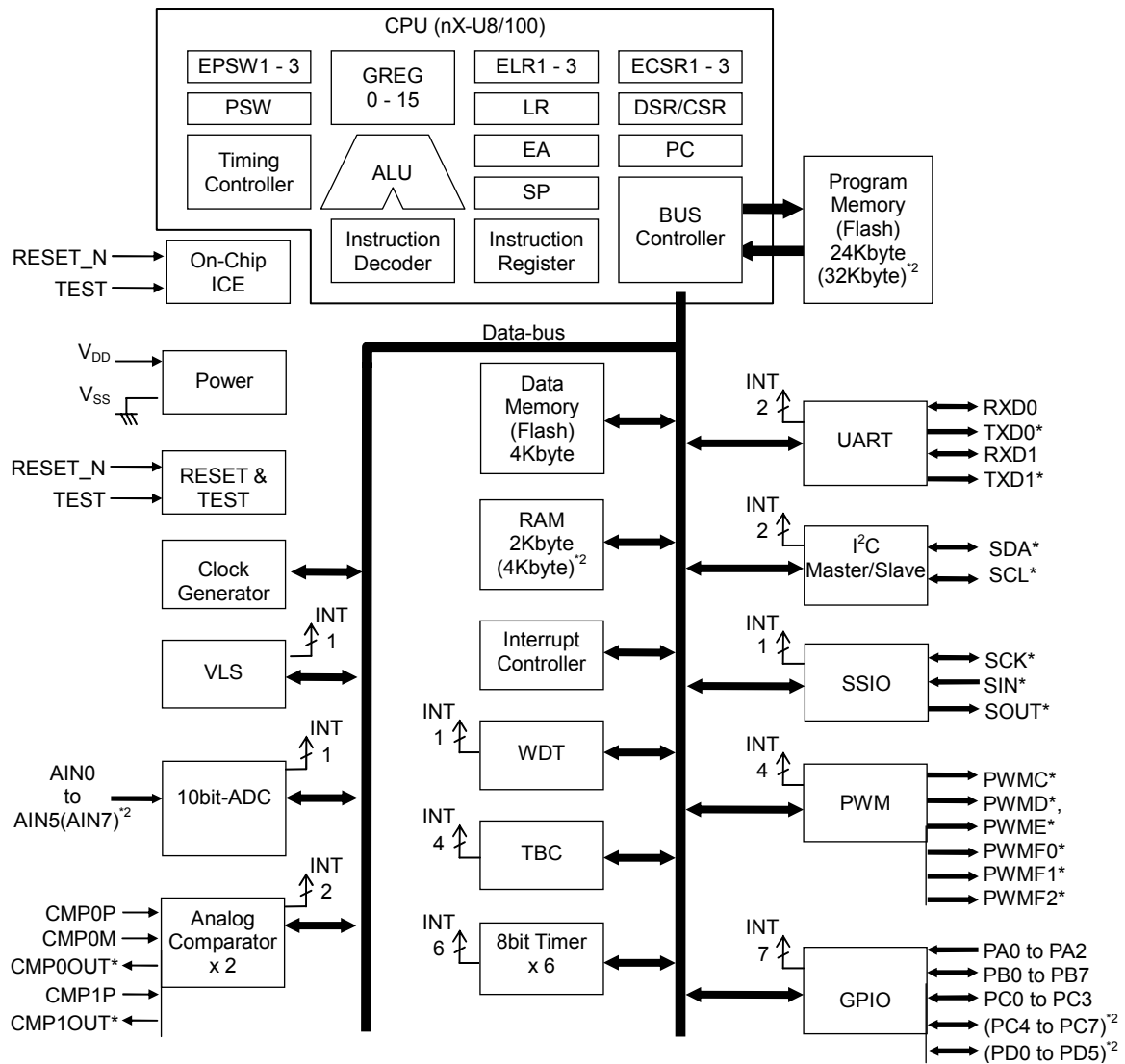
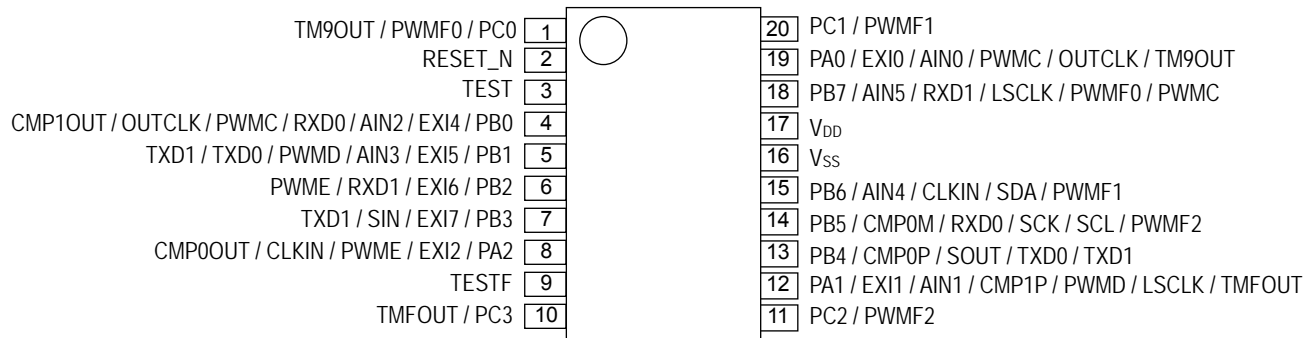


Figure 1. ML610Q111/ML610Q112 Block Diagram

PIN CONFIGURATION (TOP VIEW)

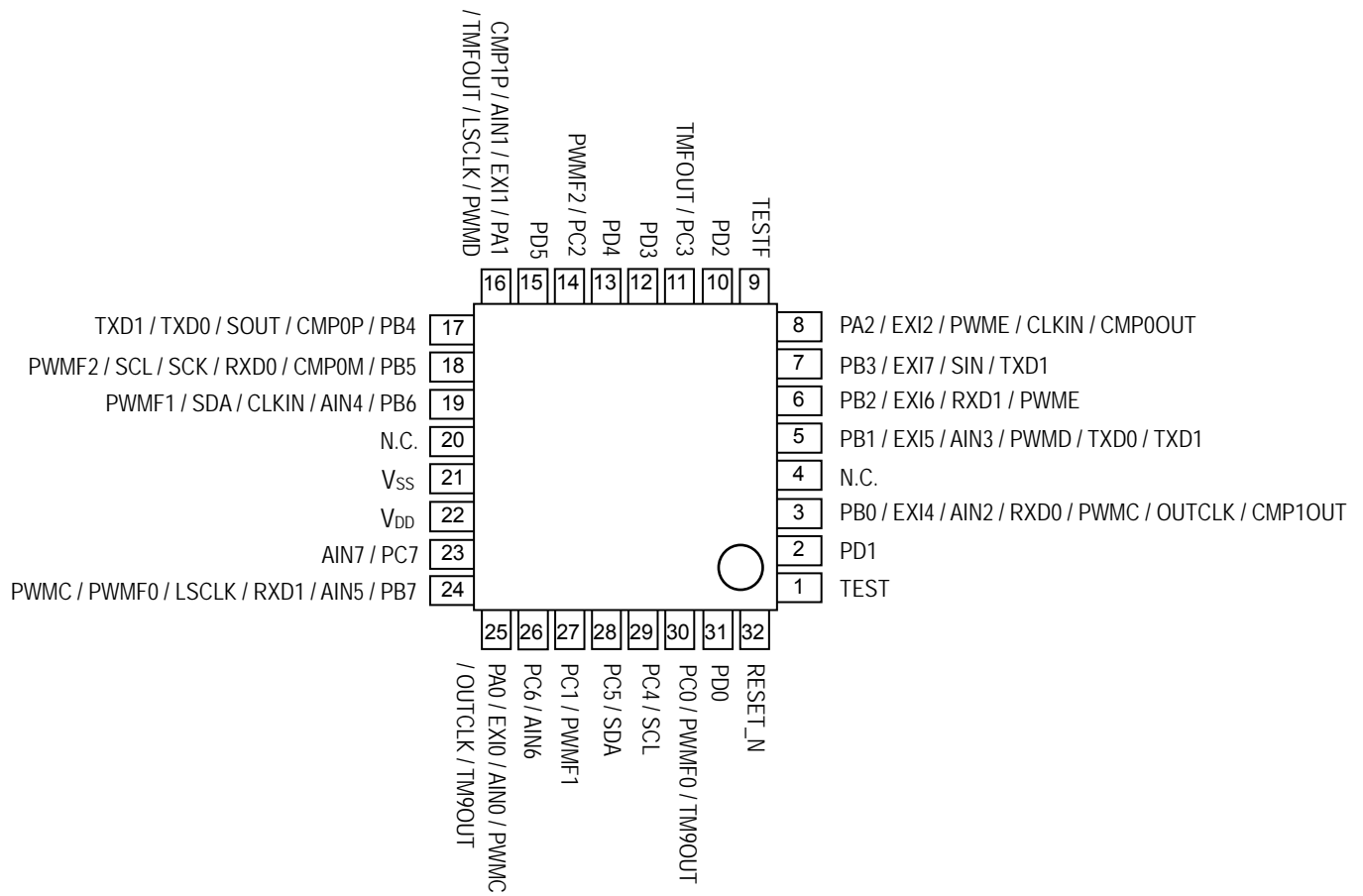
- ML610Q111-xxxTD
The pin layout is shown in figure 2.



* PIN No.4-8, 12-15, 18, 19 can be used as external trigger of the Timer E-F and PWMC-F.

Figure 2. ML610Q111 TSSOP20 Pin Configuration

- ML610Q112-xxxTC
The pin layout is shown in figure 3.



* PIN No.3, 5-8, 16-19, 24, 25 can be used as external trigger of the Timer E- F and PWMC-F.

Figure 3. ML610Q112 LQFP32 Pin Configuration

PIN LIST

Table 1. ML610Q111/ML610Q112 Pin List

| PIN No. | | Primary function | | | Secondary function | | | Tertiary function | | | Quaternary function | | |
|---------|----------|---|-----|--|--------------------|-----|----------|-------------------|-----|------------------|---------------------|-----|----------|
| 32 LQFP | 20 TSSOP | Name | I/O | Function | Name | I/O | Function | Name | I/O | Function | Name | I/O | function |
| 21 | 16 | V _{SS} | — | power supply | — | — | — | — | — | — | — | — | — |
| 22 | 17 | V _{DD} | — | power supply | — | — | — | — | — | — | — | — | — |
| 9 | 9 | TESTF | — | TEST | — | — | — | — | — | — | — | — | — |
| 32 | 2 | RESE T_N | I | SYSTEM | — | — | — | — | — | — | — | — | — |
| 1 | 3 | TEST | I/O | TEST | — | — | — | — | — | — | — | — | — |
| 25 | 19 | PA0/ EXI0/ AIN0/ TnTG ⁺ / PmTG ^{**} | I/O | GPIO/ EXINT/ SA-ADC/ TIMER/ PWM | PWMC | O | PWM | OUTCLK | O | SYSTEM | TM9OUT | O | TIMER |
| 16 | 12 | PA1/ EXI1/ AIN1/ CMP1P/ TnTG ⁺ / PmTG ^{**} | I/O | GPIO/ EXINT/ SA-ADC/ COMP/ TIMER/ PWM | PWMD | O | PWM | LSCLK | O | SYSTEM | TMFOUT | O | TIMER |
| 8 | 8 | PA2/ EXI2/ TnTG ⁺ / PmTG ^{**} | I/O | GPIO/ EXINT/ TIMER/ PWM | PWME | O | PWM | CLKIN | I | SYSTEM | CMP0OUT | O | COMP |
| 3 | 4 | PB0/ EXI4/ AIN2/ RXD0/ TnTG ⁺ / PmTG ^{**} | I/O | GPIO/ EXINT/ SA-ADC/ UART/ TIMER/ PWM | PWMC | O | PWM | OUTCLK | O | SYSTEM | CMP1OUT | O | COMP |
| 5 | 5 | PB1/ EXI5/ AIN3/ TnTG ⁺ / PmTG ^{**} | I/O | GPIO/ EXINT/ SA-ADC/ TIMER/ PWM | PWMD | O | PWM | TXD0 | O | UART | TXD1 | O | UART |
| 6 | 6 | PB2/ EXI6/ RXD1/ TnTG ⁺ / PmTG ^{**} | I/O | GPIO/ EXINT/ UART/ TIMER/ PWM | PWME | O | PWM | — | — | — | — | — | — |
| 7 | 7 | PB3/ EXI7/ TnTG ⁺ / PmTG ^{**} | I/O | GPIO/ EXINT/ TIMER/ PWM | SIN | I | SSIO | TXD1 | O | UART | — | — | — |
| 17 | 13 | PB4/ CMP0P | I/O | GPIO/ COMP | SOUT | O | SSIO | TXD0 | O | UART | TXD1 | O | UART |
| 18 | 14 | PB5/ RXD0/ CMP0M | I/O | GPIO/ UART/ COMP | SCK | I/O | SSIO | SCL | I/O | I ² C | PWMF2 | O | PWM |
| 19 | 15 | PB6/ AIN4 | I/O | GPIO/ SA-ADC | CLKIN | I | SYSTEM | SDA | I/O | I ² C | PWMF1 | O | PWM |
| 24 | 18 | PB7/ AIN5/ RXD1 | I/O | GPIO/ SA-ADC/ UART | LSCLK | O | SYSTEM | PWMF0 | O | PWM | PWMC | O | PWM |
| 30 | 1 | PC0 | I/O | GPIO | — | — | — | PWMF0 | O | PWM | TM9OUT | O | TIMER |
| 27 | 20 | PC1 | I/O | GPIO | — | — | — | PWMF1 | O | PWM | — | — | — |
| 14 | 11 | PC2 | I/O | GPIO | — | — | — | PWMF2 | O | PWM | — | — | — |
| 11 | 10 | PC3 | I/O | GPIO | — | — | — | — | — | — | TMFOUT | O | TIMER |

| PIN No. | | Primary function | | | Secondary function | | | Tertiary function | | | Quaternary function | | |
|---------|----------|------------------|-----|-----------------|--------------------|-----|------------------|-------------------|-----|----------|---------------------|-----|----------|
| 32 LQFP | 20 TSSOP | Name | I/O | Function | Name | I/O | Function | Name | I/O | Function | Name | I/O | function |
| 29 | — | PC4 | I/O | GPIO | SCL | I/O | I ² C | — | — | — | — | — | — |
| 28 | — | PC5 | I/O | GPIO | SDA | I/O | I ² C | — | — | — | — | — | — |
| 26 | — | PC6/ AIN6 | I/O | GPIO/ SA-ADC | — | — | — | — | — | — | — | — | — |
| 23 | — | PC7/ AIN7 | I/O | GPIO/ SA-ADC | — | — | — | — | — | — | — | — | — |
| 31 | — | PD0 | I/O | GPIO/ | — | — | — | — | — | — | — | — | — |
| 2 | — | PD1 | I/O | GPIO/ | — | — | — | — | — | — | — | — | — |
| 10 | — | PD2 | I/O | GPIO | — | — | — | — | — | — | — | — | — |
| 12 | — | PD3 | I/O | GPIO | — | — | — | — | — | — | — | — | — |
| 13 | — | PD4 | I/O | GPIO | — | — | — | — | — | — | — | — | — |
| 15 | — | PD5 | I/O | GPIO | — | — | — | — | — | — | — | — | — |

* : TnTG = TETG, TFTG.

** : PmTG = PCTG, PDTG, PETG, PFTG.

PIN DESCRIPTION

Table 2. ML610Q111/ML610Q112 Pin Description

| Pin name | I/O | Description | Primary Secondary Tertiary, Quaternary | Logic |
|--|-----|---|---|-----------------------|
| System | | | | |
| RESET_N | I | Reset input pin. When this pin is set to “L” level, system reset mode is set and the internal section is initialized. When this pin is set to “H” level subsequently, program execution starts. A pull-up resistor is internally connected. | Primary | Negative |
| CLKIN | I | High-speed clock input pin. This pin is used as the secondary function of PB6 pin and also as the tertiary function of PA2 pin. | Secondary, Tertiary | — |
| LSCLK | O | Low-speed clock output pin. This pin is used as the secondary function of PB7 pin and also as the tertiary function of the PA1. | Secondary, Tertiary | — |
| OUTCLK | O | High-speed clock output pin. This pin is used as the tertiary function of the PA0 and PB0 pin. | Tertiary | — |
| General Purpose Input/Output Port | | | | |
| PA0 to PA2 PB0 to PB7 PC0 to PC7 PD0 to PD5 | I/O | General-purpose input/output port. Since these pins have secondary, tertiary or quaternary functions, the pins cannot be used as a port when the secondary, tertiary or quaternary functions are used. | Primary | Positive |
| Synchronous Serial I/O | | | | |
| SIN | I | Synchronous serial data input pin. This pin is used as the secondary function of PB3 pin. | Secondary | Positive |
| SCK | I/O | Synchronous serial clock input/output pin. This pin is used as the secondary function of PB5 pin. | Secondary | — |
| SOUT | O | Synchronous serial data output pin. This pin is used as the secondary function of PB4 pin. | Secondary | Positive |
| UART | | | | |
| TXD0 | O | UART0 data output pin. This pin is used as the tertiary function of the PB1 and PB4 pin. | Tertiary | Positive |
| RXD0 | I | UART0 data input pin. This pin is used as the primary function of the PB0 and PB5 pin | Primary | Positive |
| TXD1 | O | UART1 data output pin. This pin is used as the tertiary function of the PB3 pin and also the quaternary function of the PB1 and PB4 pin. | Tertiary Quaternary | Positive |
| RXD1 | I | UART1 data input pin. This pin is used as the primary function of the PB2 and PB7 pin. | Primary | Positive |
| I²C Bus Interface | | | | |
| SCL | I/O | Serial clock input/output. This pin is used as the tertiary function of the PB5 and the secondary function of the PC4 pin. | Tertiary Secondary | Positive |
| SDA | I/O | Serial data input/output. This pin is used as the tertiary function of the PB6 and the secondary function of the PC5 pin. | Tertiary Secondary | Positive |
| PWM | | | | |
| PWMC | O | PWMC output pin. This pin is used as the secondary function of the PA0 and PB0 and also the quaternary function of the PB7 pin. | Secondary Quaternary | Positive/ Negative |
| PWMD | O | PWMD output pin. This pin is used as the secondary function of the PA1 and PB1 pin. | Secondary | Positive/ Negative |
| PWME | O | PWME output pin. This pin is used as the secondary function of the PA2 and PB2 pin. | Secondary | Positive/ Negative |
| PWMF0 | O | PWMF0 output pin. This pin is used as the tertiary function of the PB7 and PC0 pin. | Tertiary | Positive/ Negative |
| PWMF1 | O | PWMF1 output pin. This pin is used as the tertiary function of the PC1 and also the quaternary function of PB6 pin. | Tertiary/ Quaternary | Positive/ Negative |

| Pin name | I/O | Description | Primary Secondary Tertiary, Quaternary | Logic |
|--|-----|--|---|-----------------------|
| PWMF2 | O | PWMF2 output pin. This pin is used as the tertiary function of the PC2 and also the quaternary function of the PB5 pin. | Tertiary/ Quaternary | Positive/ Negative |
| External Interrupt | | | | |
| EXI0 to 2 | I | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PA0 – PA2 pins. | Primary | Positive/ negative |
| EXI4 to 7 | I | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PB0 – PB3 pins. | Primary | Positive/ negative |
| Timer | | | | |
| TETE, TFTG | I | External clock input pin used for both Timer E and Timer F. These pins are used as the primary function of the PA0-PA2, PB0-PB7 pins. | Primary | — |
| TM9OUT | O | Timer 9 output pin. This pin is used as the quaternary function of the PA0 and PC0 pin. | Quaternary | Positive |
| TMFOUT | O | Timer F output pin. This pin is used as the quaternary function of the PA1 and PC3 pin. | Quaternary | Positive |
| Successive approximation type A/D converter | | | | |
| AIN0 | I | Channel 0 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA0 pin. | Primary | — |
| AIN1 | I | Channel 1 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA1 pin. | Primary | — |
| AIN2 | I | Channel 2 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB0 pin. | Primary | — |
| AIN3 | I | Channel 3 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB1 pin. | Primary | — |
| AIN4 | I | Channel 4 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB6 pin. | Primary | — |
| AIN5 | I | Channel 5 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB7 pin. | Primary | — |
| AIN6 | I | Channel 6 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PC6 pin. | Primary | — |
| AIN7 | I | Channel 7 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PC7 pin. | Primary | — |
| Comparator | | | | |
| CMP0P | I | Non-inverting input for comparator0. This pin is used as the primary function of the PB4 pin. | Primary | — |
| CMP0M | I | Inverting input for comparator0. This pin is used as the primary function of the PB5 pin. | Primary | — |
| CMP0OUT | O | Output for comparator0. This pin is used as the quaternary function of the PA2 pin. | Quaternary | — |
| CMP1P | I | Non-inverting input for comparator1. This pin is used as the primary function of the PA1 pin. | Primary | — |
| CMP1OUT | O | Output for comparator1. This pin is used as the quaternary function of the PB0 pin. | Quaternary | — |
| TEST | | | | |
| TEST | I/O | Input/output pin for testing. A pull-down resistor is internally connected. | — | Positive |
| TESTF | — | Test pin for flash memory. A pull-down resistor is internally connected. | — | — |
| Power Supply | | | | |
| V _{SS} | — | Negative power supply pin. | — | — |
| V _{DD} | — | Positive power supply pin. | — | — |

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins for ML610Q111/ML610Q112

Table 3. Termination of Unused Pins

| Pin | Recommended pin termination |
|------------|-----------------------------|
| RESET_N | Open |
| TEST | Open |
| TESTF | Open |
| PA0 to PA2 | Open |
| PB0 to PB7 | Open |
| PC0 to PC7 | Open |
| PD0 to PD5 | Open |
| N.C. | Open |

Note:

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

● ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

| Parameter | Symbol | Condition | Rating | Unit |
|----------------------|------------------|-----------|------------------------------|------|
| Power supply voltage | V _{DD} | Ta = 25°C | -0.3 to +7.0 | V |
| Input voltage | V _{IN} | Ta = 25°C | -0.3 to V _{DD} +0.3 | V |
| Output voltage | V _{OUT} | Ta = 25°C | -0.3 to V _{DD} +0.3 | V |
| Output current | I _{OUT} | Ta = 25°C | -12 to +11 | mA |
| Power dissipation | PD | Ta = 25°C | 0.84 | W |
| Storage temperature | T _{STG} | — | -55 to 150 | °C |

● RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

| Parameter | Symbol | Condition | Range | Unit |
|----------------------------------|-----------------|-----------|-------------|------|
| Operating temperature (ambience) | T _{OP} | — | -40 to +105 | °C |
| Operating voltage | V _{DD} | — | 2.7 to 5.5 | V |

● FLASH MEMORY SPECIFICATION

(V_{SS}= 0V)

| Parameter | Symbol | Condition | Rating | Unit |
|----------------------------------|------------------|-------------------------------------|-------------------------------------|--------|
| Operating temperature (ambience) | T _{OPF} | At read | -40 to +105 | °C |
| | | At write/erase | -20 to +85 | °C |
| Rewrite counts ^{*1} | C _{EPD} | Data flash memory (4KB) | 6000 | cycles |
| | C _{EPP} | Program flash memory | 80 | |
| Erase unit | — | Chip-erase | Program flash and Data flash memory | — |
| | — | Block-erase (Program flash memory) | 8 | KB |
| | — | Block-erase (Data flash memory) | 4 | KB |
| | — | Sector-erase (Data flash memory) | 1 | KB |
| Erase time (max.) | — | Chip-erase/Block-erase/Sector-erase | 100 | ms |
| Write unit | — | — | 1word(2bytes) | — |
| Write time (max.) | — | 1word(2bytes) | 40 | μs |
| Data retention ^{*2} | Y _{DR} | — | 15 | years |

*¹: Rewrite counts is counted as one even if you erase suspend.

*²: However, keep active time of the LSI from exceeding ten years.

In addition, following capability of Flash memory is available;

- security function: providing security ID for the protection of program code implemented in Flash memory
- accidental-write protection: providing special sequence to protect accidental write data to Flash memory. By writing "0FAX" and "0F5x" sequentially, before write/erase, writing one word is available just only one time.
- erase interrupt function: in the case of external interrupt during erasing flash memory, erase execution is suspended. And then the interrupt is activated. Please re-erase after interrupt execution.

● DC CHARACTERISTICS (Supply Current)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|------------------|--------|--|--------|------|------|---------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Supply current 1 | IDD1 | CPU : In STOP state (All clock stop) $V_{DD}=5.0V$ | — | 1 | 50 | μA | 1 |
| Supply current 2 | IDD2 | CPU : In HALT state* ¹ (Only CR oscillation operates) $V_{DD}=5.0V$ | — | 240 | — | μA | |
| Supply current 3 | IDD3 | CPU : CR32.768kHz operating state* ² (Only CR oscillation operates) $V_{DD}=5.0V$ | — | 250 | — | μA | |
| Supply current 4 | IDD4 | CPU : CR8.192MHz operating state* ³ (CR and PLL oscillation operate) $V_{DD}=5.0V$ | — | 4 | 6 | mA | |

*¹ : LTBC and WDT are operating ,and significant bits of BLKCON0 to BLKCON7 registers are all "1".

*² : When the CPU operating rate is 100%. Minimum instruction execution time: Approx 30.52 μs (at 32.768kHz system clock)

*³ : When the CPU operating rate is 100%. Minimum instruction execution time: Approx 122 ns (at 8.192MHz system clock)

● DC CHARACTERISTICS (VLS, Comparator)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | | Rating | | | Unit | Measuring circuit |
|--|-------------|-------------------------------------|--------------|--------------|------|----------------|------|-------------------|
| | | | | Min. | Typ. | Max. | | |
| VLS0 threshold voltage ($V_{DD}=\text{fall}$) | V_{VLS0F} | $T_a=25^{\circ}C$ | | Typ -3.0% | 2.85 | Typ +3.0% | V | 1 |
| | | — | | Typ -5.0% | | Typ +5.0% | | |
| VLS0 threshold voltage ($V_{DD}=\text{rise}$) | V_{VLS0R} | $T_a=25^{\circ}C$ | | Typ -3.0% | 2.92 | Typ +3.0% | | |
| | | — | | Typ -5.0% | | Typ +5.0% | | |
| VLS1 threshold voltage ($V_{DD}=\text{fall}$) | V_{VLS1} | $T_a=25^{\circ}C$ | VLS1=0 | Typ -3.0% | 3.3 | Typ +3.0% | | |
| | | | VLS1=1 | | 3.6 | | | |
| | | | VLS1=2 | | 3.9 | | | |
| | | | VLS1=3 | | 4.2 | | | |
| | | — | Typ -5.0% | VLS1=0 | 3.3 | Typ +5.0% | | |
| | | | | VLS1=1 | 3.6 | | | |
| | | | | VLS1=2 | 3.9 | | | |
| | | | | VLS1=3 | 4.2 | | | |
| Comparator0 In-phase input voltage range | V_{CMR} | — | | 0.1 | — | $V_{DD} - 1.5$ | V | |
| Comparator0 hysteresis | V_{HYSP} | $T_a=25^{\circ}C$, $V_{DD} = 5.0V$ | | 10 | 20 | 30 | mV | |
| | | $V_{DD} = 5.0V$ | | 5 | 20 | 35 | | |
| Comparator0 Input offset voltage | V_{CMOF} | $T_a=25^{\circ}C$, $V_{DD} = 5.0V$ | | — | — | 7 | | |
| Comparator Reference-voltage error* ¹ | V_{CMREF} | $T_a=25^{\circ}C$ | | -25 | — | 25 | | |
| | | — | | -50 | — | 50 | | |

*¹: Comparator input offset voltage is included.

● DC CHARACTERISTICS (IO pins)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|--------|--|------------------|------|------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Output voltage1 (TEST, PA0-2, PB0-7, PC0-7, PD0-5) | VOH1 | IOH=-3.0mA, $V_{DD}=4.5V^{*1}$ Ta= -40 to 85°C | V_{DD} -0.7 | — | — | V | 2 |
| | | IOH=-3.0mA, $V_{DD}=4.5V^{*1}$ | V_{DD} -0.8 | — | — | | |
| | VOL1 | IOL=+8.5mA, $V_{DD}=4.5V^{*1}$ Ta= -40 to 85°C | — | — | 0.6 | | |
| | | IOL=+8.5mA, $V_{DD}=4.5V^{*1}$ | — | — | 0.7 | | |
| Output voltage2 (PB5, PB6 PC4, PC5) | VOL2 | IOL=+3.0mA | — | — | 0.4 | | |
| Output leakage (PA0-2, PB0-7, PC0-7, PD0-5) | IOOH | VOH = V_{DD} (in high-impedance state) | — | — | 1 | μA | 3 |
| | IOOL | VOL = V_{SS} (in high-impedance state) | -1 | — | — | | |
| Input current 1 (RESET_N) | IIH1 | VIH1 = V_{DD} | — | — | 1 | μA | 4 |
| | IIL1 | VIL1 = V_{SS} , $V_{DD} = 5.0V$ | -650 | -500 | -350 | | |
| Input current 2 (TEST) | IIH2 | VIH2= $V_{DD} = 5.0V$ | 20 | 115 | 200 | | |
| | IIL2 | VIL2 = V_{SS} | -1 | — | — | | |
| Input current 3 (PA0-2, PB0-7, PC0-7, PD0-5) | IIH3 | VIH3 = $V_{DD} = 5.0V$ (when pulled-down) | 20 | 115 | 200 | | |
| | IIL3 | VIL3 = V_{SS} , $V_{DD} = 5.0V$ (when pulled-up) | -200 | -100 | -20 | | |
| | IIH3Z | VIH3 = V_{DD} (in high-impedance stat) | — | — | 1 | | |
| | IIL3Z | VIL3 = V_{SS} (in high-impedance stat) | -1 | — | — | | |

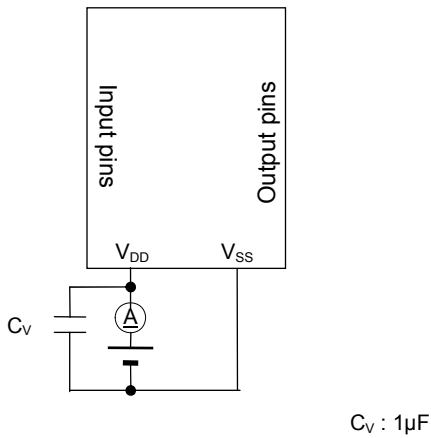
*1 : When the one terminal output state.

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

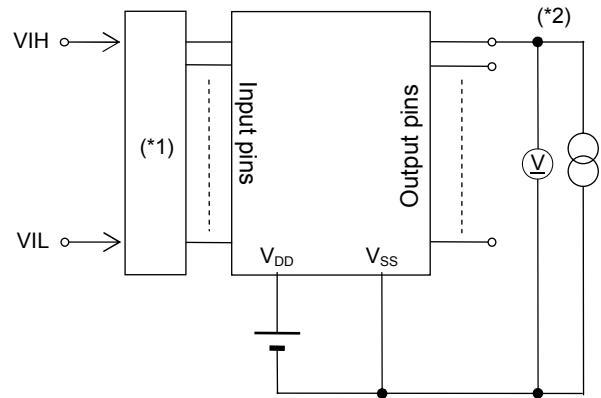
| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|--|--------|------------------------|------------------------|------|------------------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Input voltage 1 (RESET_N, TEST, PA0-2, PB0-7, PC0-7, PD0-5) | VIH1 | — | 0.7 $\times V_{DD}$ | — | V_{DD} | V | 2 |
| | VIL1 | — | 0 | — | 0.3 $\times V_{DD}$ | | |
| Input pin capacitance (PA0-2, PB0-7, PC0-7, PD0-5) | CIN | f = 10kHz Ta = 25°C | — | — | 20 | pF | — |

● MEASURING CIRCUITS

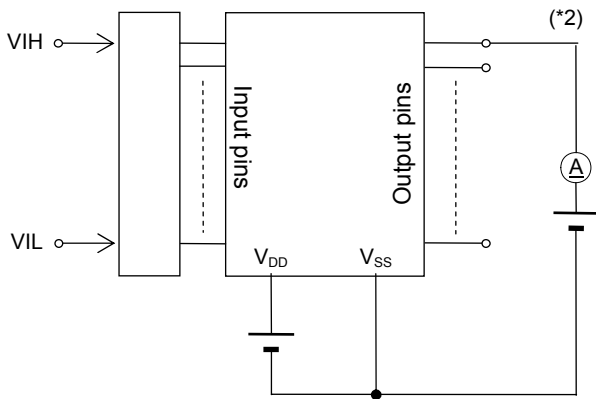
Measuring circuit 1



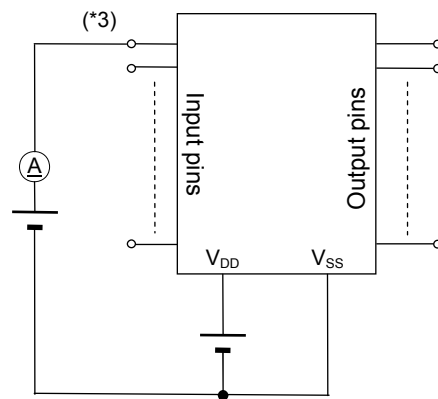
Measuring circuit 2



Measuring circuit 3



Measuring circuit 4



*1: Input logic circuit to determine the specified measuring conditions.

*2: Measured at the specified output pins.

*3: Measured at the specified input pins.

● AC CHARACTERISTICS (Clock)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

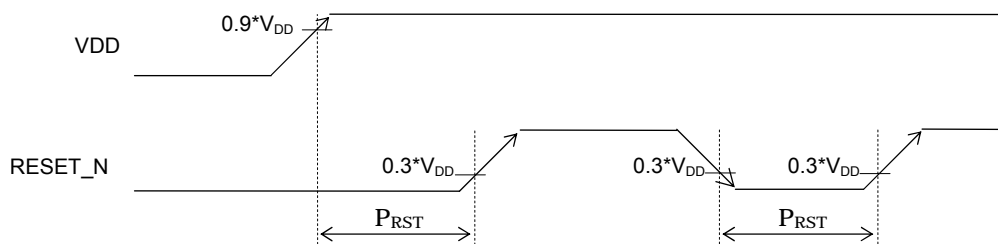
| Parameter | Symbol | Condition | Rating | | | Unit |
|--------------------------------|-----------|------------------------------|-------------|--------|-------------|------|
| | | | Min. | Typ. | Max. | |
| 32kHz RC oscillation frequency | f_{RCL} | $T_a = -20$ to $85^{\circ}C$ | Typ. -3% | 32.768 | Typ. +3% | kHz |
| | | — | Typ. -4% | | Typ. +4% | |
| PLL oscillation frequency *1 | f_{PLL} | $T_a = -20$ to $85^{\circ}C$ | Typ. -3% | 16.384 | Typ. +3% | MHz |
| | | — | Typ. -4% | | Typ. +4% | |

*1 : 1024 clock average. Maximum CPU clock frequency is $f_{PLL}/2$.

● AC CHARACTERISTICS (Power on / Reset sequence)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|------------|-----------|--------|------|------|---------|
| | | | Min. | Typ. | Max. | |
| Reset pulse width | P_{RST} | — | 100 | — | — | μs |
| Reset noise elimination pulse width | P_{NRST} | — | — | — | 0.4 | ms |
| Power-on reset activation power rise time | T_{POR} | — | — | — | 10 | |



External Reset sequence

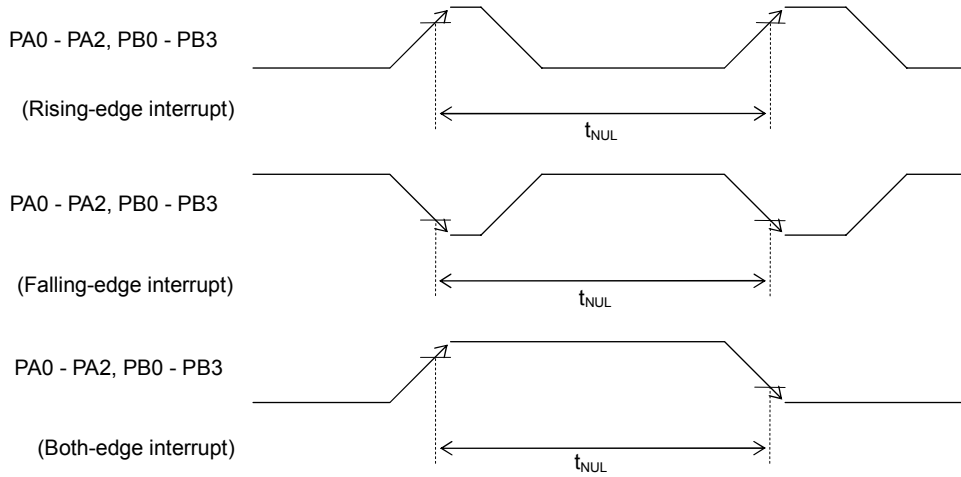


Power-on Reset sequence

● AC CHARACTERISTICS (External Interrupt)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|-----------------------------------|-----------|---|-----------------|------|-----------------|--------|
| | | | Min. | Typ. | Max. | |
| External interrupt disable period | T_{NUL} | Interrupt: Enabled (MIE = 1), CPU: NOP operation | 2.5 x sysclk | — | 3.5 x sysclk | ϕ |

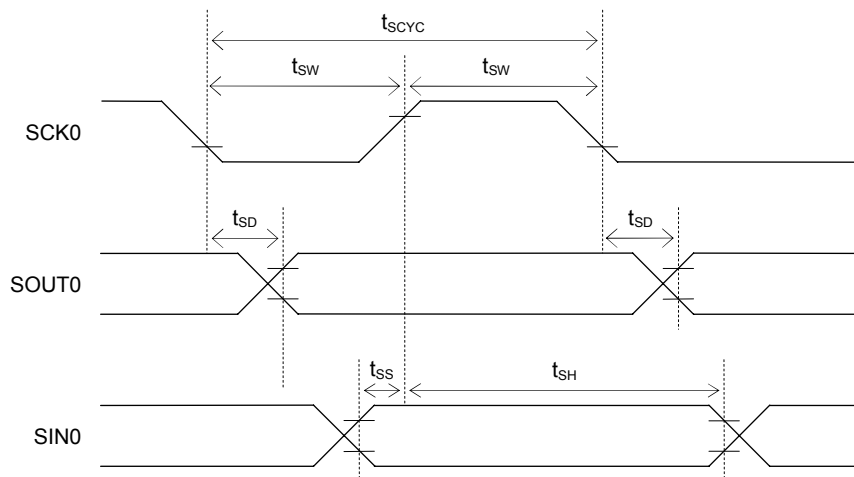


● AC CHARACTERISTICS (Synchronous Serial Port)

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--------------------------------------|------------|---|-----------------------|-----------------------|-----------------------|---------|
| | | | Min. | Typ. | Max. | |
| SCK input cycle (slave mode) | t_{scyc} | When high-speed oscillation is not active | 10 | — | — | μs |
| | | When high-speed oscillation is active | 500 | — | — | ns |
| SCK output cycle (master mode) | t_{scyc} | — | — | SCK* ¹ | — | s |
| SCK input pulse width (slave mode) | t_{sw} | When high-speed oscillation is not active | 4 | — | — | μs |
| | | When high-speed oscillation is active | 200 | — | — | ns |
| SCK output pulse width (master mode) | t_{sw} | — | $t_{scyc} \times 0.4$ | $t_{scyc} \times 0.5$ | $t_{scyc} \times 0.6$ | s |
| SOUT output delay (slave mode) | t_{sd} | — | — | — | 180 | ns |
| SOUT output delay (master mode) | t_{sd} | — | — | — | 80 | ns |
| SIN input setup time (slave mode) | t_{ss} | — | 50 | — | — | ns |
| SIN input hold time | t_{sh} | — | 50 | — | — | ns |

*¹: Clock period selected with S0CK3-0 of the serial port 0 mode register(SIO0MOD1)



● AC CHARACTERISTICS (I²C Bus Interface: Standard Mode 100kHz)

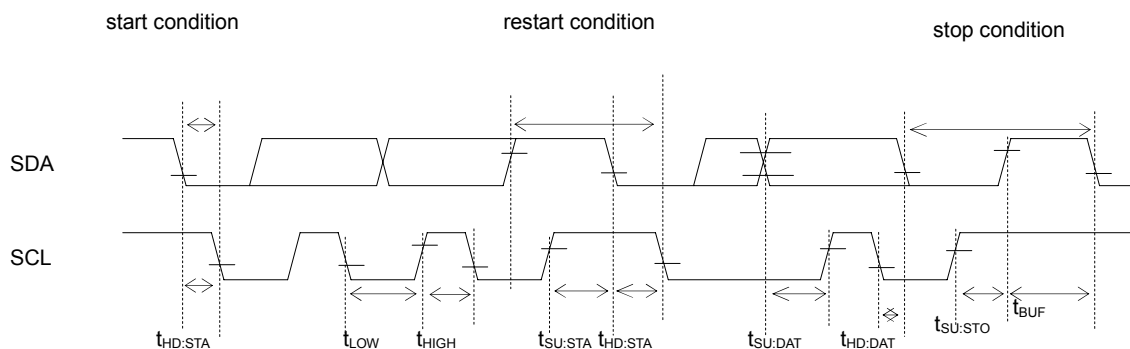
(V_{DD}=2.7 to 5.5V, V_{SS}=0V, T_a=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--|---------------------|-----------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | f _{SCL} | — | 0 | — | 100 | kHz |
| SCL hold time (start/restart condition) | t _{HD:STA} | — | 4.0 | — | — | μs |
| SCL "L" level time | t _{LOW} | — | 4.7 | — | — | μs |
| SCL "H" level time | t _{HIGH} | — | 4.0 | — | — | μs |
| SCL setup time (restart condition) | t _{SU:STA} | — | 4.7 | — | — | μs |
| SDA hold time | t _{HD:DAT} | — | 0 | — | — | μs |
| SDA setup time | t _{SU:DAT} | — | 0.25 | — | — | μs |
| SDA setup time (stop condition) | t _{SU:STO} | — | 4.0 | — | — | μs |
| Bus-free time | t _{BUF} | — | 4.7 | — | — | μs |

● AC CHARACTERISTICS (I²C Bus Interface: Fast Mode 400kHz)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, T_j=-40 to +105°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--|---------------------|-----------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | f _{SCL} | — | 0 | — | 400 | kHz |
| SCL hold time (start/restart condition) | t _{HD:STA} | — | 0.6 | — | — | μs |
| SCL "L" level time | t _{LOW} | — | 1.3 | — | — | μs |
| SCL "H" level time | t _{HIGH} | — | 0.6 | — | — | μs |
| SCL setup time (restart condition) | t _{SU:STA} | — | 0.6 | — | — | μs |
| SDA hold time | t _{HD:DAT} | — | 0 | — | — | μs |
| SDA setup time | t _{SU:DAT} | — | 0.1 | — | — | μs |
| SDA setup time (stop condition) | t _{SU:STO} | — | 0.6 | — | — | μs |
| Bus-free time | t _{BUF} | — | 1.3 | — | — | μs |

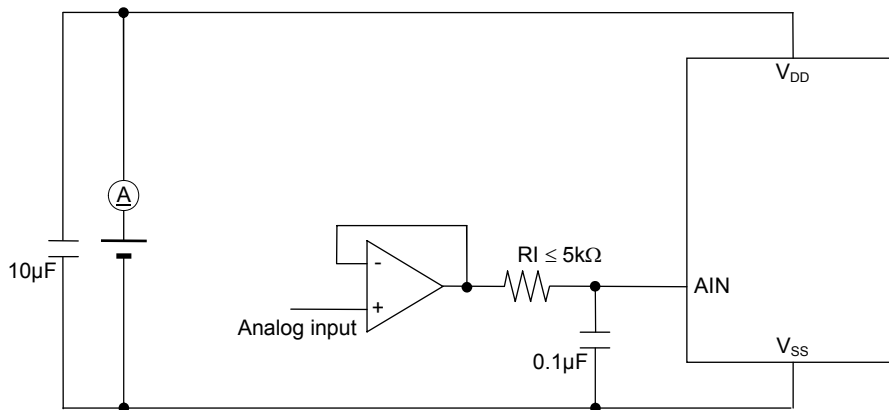


● Electrical Characteristics of Successive Approximation Type A/D Converter

($V_{DD}=2.7$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+105^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|----------------------------------|------------|-----------|--------|------|------|-----------|
| | | | Min. | Typ. | Max. | |
| Resolution | n | — | — | — | 10 | bit |
| Integral non-linearity error | INL | — | -4 | — | +4 | LSB |
| Differential non-linearity error | DNL | — | -3 | — | +3 | |
| Zero-scale error | V_{OFF} | — | -4 | — | +4 | |
| Full-scale error | FSE | — | -4 | — | +4 | |
| Conversion time | t_{CONV} | — | — | 102 | — | ϕ/CH |

Φ : period of OSCLK (more than 3MHz)



PACKAGE DIMENSIONS

- ML610Q111-xxxTD

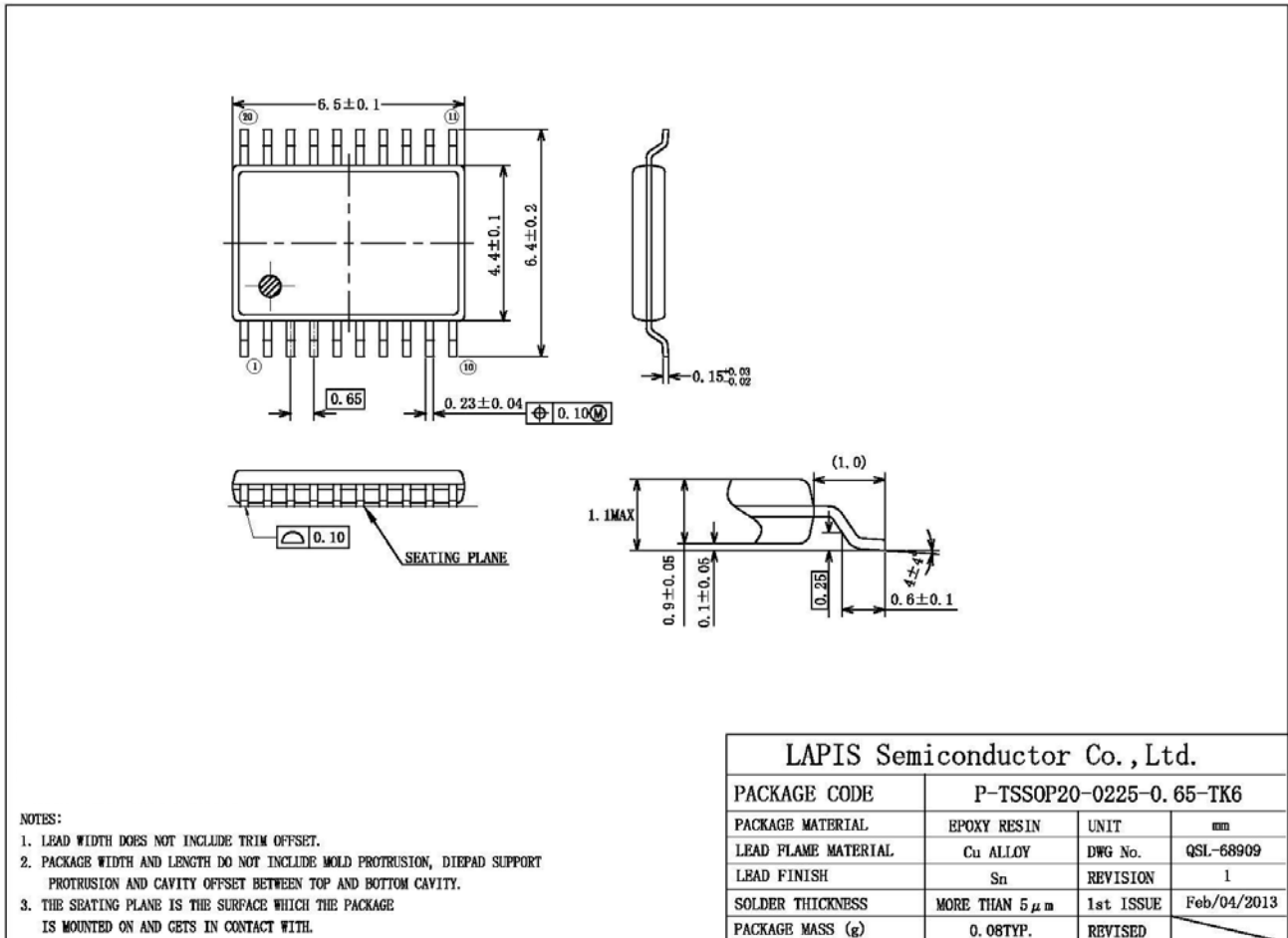


Figure 4 TSSOP20

● ML610Q112-xxxTC

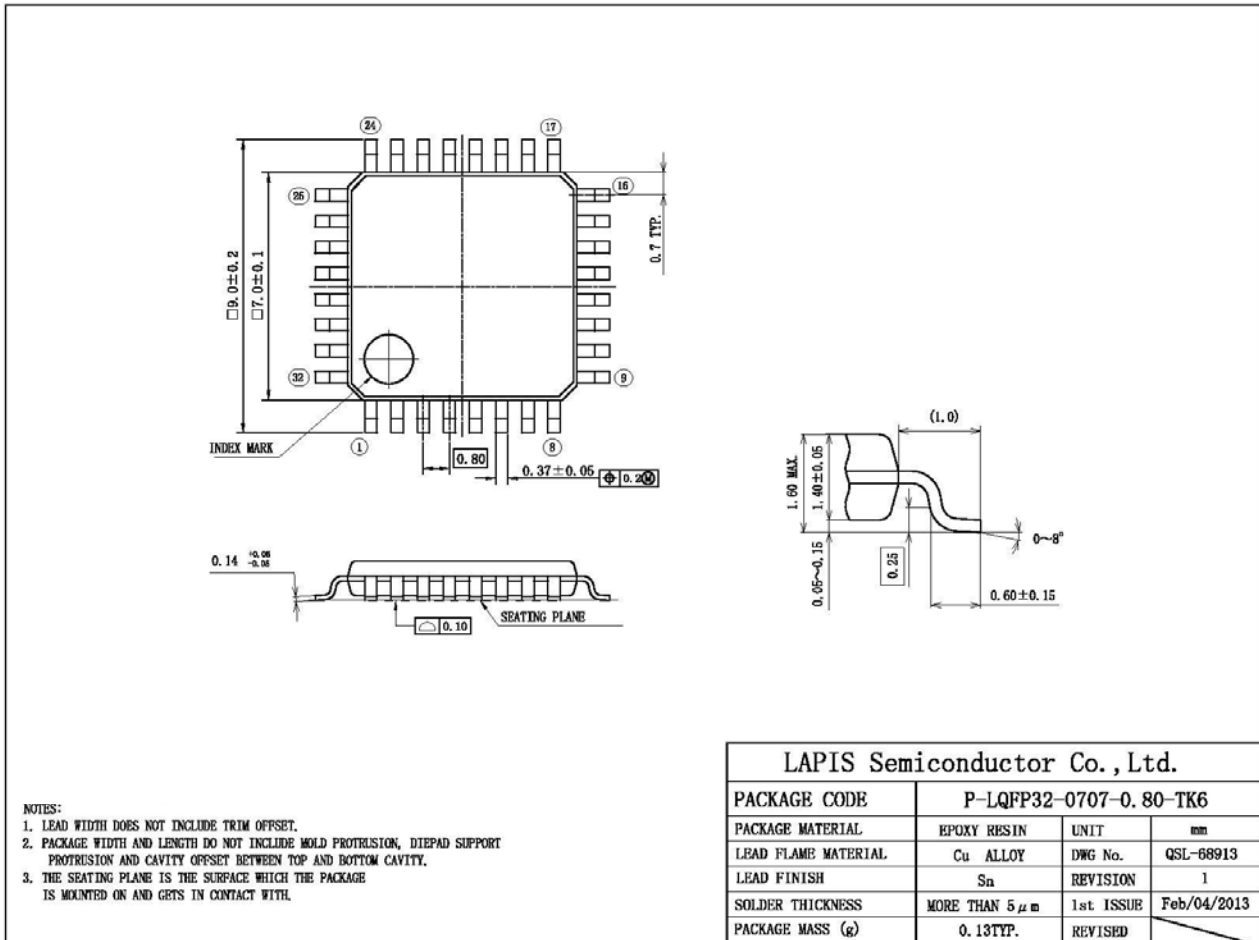


Figure 5 LQFP32

● Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|----------------|-----------|------------------|-----------------|-----------------|
| | | Previous Edition | Current Edition | |
| FEDL610Q111-01 | 2013.9.26 | — | — | Final edition 1 |
| | | | | |

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