TY Semicondutor®

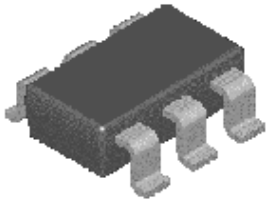
Product specification

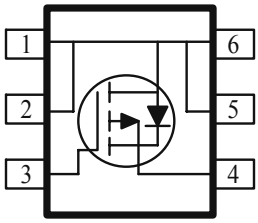
# AM3455P

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are power switch, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Low Gate Charge
- Fast Switch
- Miniature TSOP-6 Surface Mount Package Saves Board Space

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
| -30 | 0.112 @ $V_{GS}$ = 10 V | 3.4 |
| | 0.172 @ $V_{GS}$ = 4.5V | 2.7 |






| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C UNLESS OTHERWISE NOTED) | | | | |
|---|---|---|---|---|
| Parameter | | Symbol | Maximum | Units |
| Drain-Source Voltage | | $V_{DS}$ | -30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current[a] | $T_A$=25°C | $I_D$ | 3.4 | A |
| | $T_A$=70°C | | 2.6 | |
| Pulsed Drain Current[b] | | $I_{DM}$ | ±20 | |
| Continuous Source Current (Diode Conduction)[a] | | $I_S$ | 1.7 | A |
| Power Dissipation[a] | $T_A$=25°C | $P_D$ | 2.0 | W |
| | $T_A$=70°C | | 1.3 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 150 | °C |

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| Parameter | | Symbol | Maximum | Units |
| Maximum Junction-to-Ambient[a] | t <= 5 sec | $R_{THJA}$ | 62.5 | °C/W |
| | Steady-State | | 110 | |

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

| SPECIFICATIONS ($T_A$ = 25°C UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Limits** | | | **Unit** |
| | | | **Min** | **Typ** | **Max** | |
| **Static** | | | | | | |
| Gate-Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 uA | 1.0 | | | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -24 V, $V_{GS}$ = 0 V | | | 1 | uA |
| | | $V_{DS}$ = -24 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | | | 50 | |
| On-State Drain Current[A] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 10 V | 10 | | | A |
| Drain-Source On-Resistance[A] | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 3.4 A | | | 112 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 2.7 A | | | 172 | |
| Forward Tranconductance[A] | $g_{fs}$ | $V_{DS}$ = 4.5 V, $I_D$ = 3.4 A | | 6 | | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = 0.75 A, $V_{GS}$ = 0 V | | | 1.2 | V |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 30 V, $V_{GS}$ = 5 V, $I_D$ = 3.4 A | | 4.5 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 1.4 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 2.4 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 30 V, $R_L$ = 30 Ω, $I_D$ = 1 A, $V_{GEN}$ = 10 V | | 9 | | ns |
| Rise Time | $t_r$ | | | 12 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 25 | | |
| Fall-Time | $t_f$ | | | 14 | | |

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.