## Preliminary GaN Hybrid Power Amplifier HT2121-15A

#### **Product Features**

- GaN on SiC HEMT
- In/Out Impedance Matching
- Surface Mount Hybrid Type
- Small Size & Mass
- High Efficiency
- Low Cost
- 2W Average Output Power

#### Applications

- RF Sub-Systems
- Base Station
- Repeater
- LTE system







Package Type : NP-1E

#### Description

The HT2121-15A is designed for LTE Repeater & RF Sub-systems application frequencies from 2110 ~ 2170MHz This amplifier uses GaN HEMT technology which performs high breakdown voltage, high efficiency. High In/Output impedance, High power density.

#### Electrical Specifications @ Vds =28V, Ta=25°C

PARAMETER	UNIT	MIN	ТҮР	MAX	CONDITION
Frequency Range	MHz	2110	-	2170	ZS = ZL = 50 ohm
Power Gain		31.5	33	34.5	
Gain Flatness	dB	-	0.8	-	Amp : Idq1 = 47mA
Input Return Loss		-6	-10	-	Idq2 = 103mA
Pout @ Average	dBm	-	33	-	
Pout @ Psat	dBm	40.5	42	-	Pulse Width=20us, Duty10%
ACLR* @ BW 10MHz LTE (PAPR 7.5dB)	dD a	-	-36	-33	Non DPD
	dBc	-	-55	-	With DPD
Drain Efficiency	%	-	24.5	-	Deret @ Array
Ids	mA	-	290	-	Pout @ Average
Supply Voltage	V	-	-3.0	-2.0	Gate Bias (Vgs1 and Vgs2)
	V	-	28	-	Main Bias(Vds)

#### Caution

The drain voltage must be supplied to the device after the gate voltage is supplied

Turn on : Turn on the Gate Voltage supply and last turn On the Drain voltage supplies

Turn off : Turn off the Drain Voltage and last turn off the Gate voltage

#### Note

1. ACLR Measured Pout=33dBm @ fc± 10MHz / 9.015MHz

LTE 10MHz 1FA PAPR=7.5dB @ 0.01% probability on CCDF

2. HT Series have internal DC blocking capacitors at the RF input and output ports

#### **Mechanical Specifications**

PARAMETER	UNIT	ТҮР	REMARK
Mass	g	2	-
Dimension	mm	20.5 x 15 x 4.8	-

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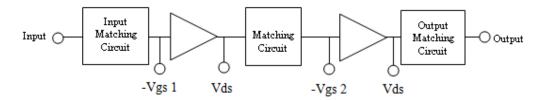
#### **Absolute Maximum Ratings**

PARAMETER	UNIT	RATING	SYMBOL
Gate-Source Voltage	v	-10 ~ 0	Vgs1 Vgs2
Drain-Source Voltage	V	50	Vds
Gate Current	mA	5.7	Ig
Operating Junction Temperature	°C	225	T <sub>J</sub>
Operating Case Temperature	°C	-30 ~ 85	T <sub>C</sub>
Storage Temperature	°C	-40 ~ 100	T <sub>STG</sub>

## **Operating Voltages**

PARAMETER	UNIT	MIN	ТҮР	MAX	SYMBOL
Drain Voltage	V	-	28	-	Vds
Gate Voltage (on-stage)	V	-	Vgs1@Idq1	-2	Vgs 1
Gate Voltage (on-stage)	V	-	Vgs2@Idq2	-2	Vgs 2
Gate Voltage (off-stage)	V	-	-8	-	Vgs 1
Gate Voltage (off-stage)	V	-	-8	-	Vgs 2

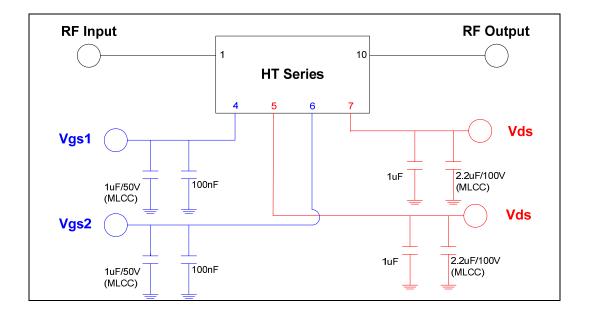
#### **Block Diagram**





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## **Application Circuit**



3/7

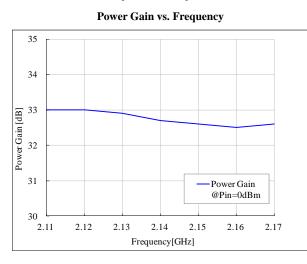


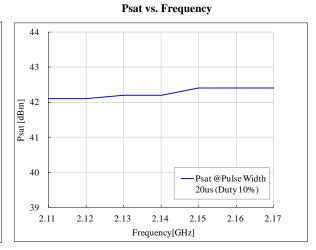
## Preliminary GaN Hybrid Power Amplifier HT2121-15A



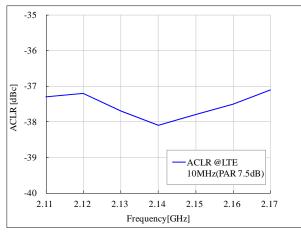
#### **Performance Charts**

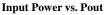
\* Bias condition @ Idq1= 47mA, Idq2= 103mA, Vds =+28V, Ta= $25\,^{\circ}$ C

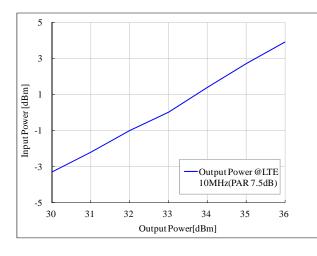


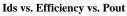


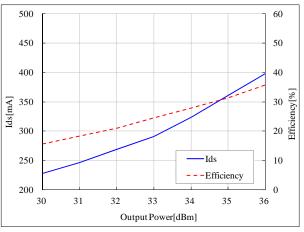
#### ACLR vs. Frequency



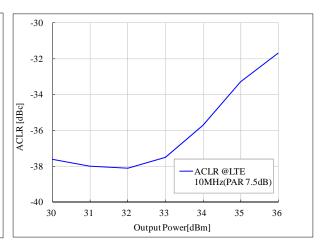








ACLR vs. Pout

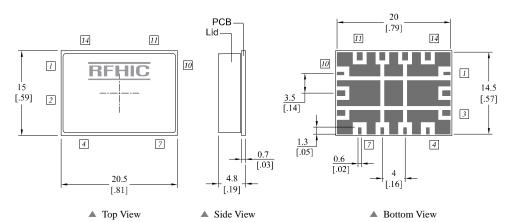


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## **RFHIC**

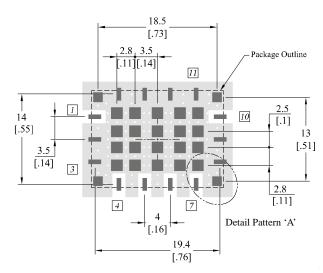
#### Package Dimensions (Type: NP-1E)

\* Unit: mm[inch] | Tolerance:  $\pm 0.15[.006]$ 

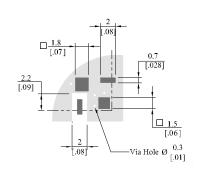


Pin Description								
Pin No	Function	Pin No	Function	Pin No	Function	Pin No	Function	
1	RF Input	4	Vgs1	8	GND	11	GND	
2	GND	5	Vds	9	GND	12	GND	
3	GND	6	Vgs2	10	RF Output	13	GND	
-	-	7	Vds	-	-	14	GND	

#### **Recommended Pattern**



### **Recommended Pattern Detail 'A'**



#### \* Mounting Configuration Notes

1. For the proper performance of the device, Ground / Thermal via holes must be designed to remove heat.

- 2. To properly use heatsink, ensure the ground/thermal via hole region to contact the heatsink. We recommend the mounting screws
- be added near the heatsink to mount the board
- 3. In designing the necessary RF trace, width will depend upon the PCB material and construction.
- 4. Use 1 oz. Copper minimum thickness for the heatsink.
- 5. Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink
- 6. We recommend adding as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

HT2121-15A



#### **Precautions**

This product is a Gallium Nitride Transistor.

The Gallium Nitride Transistor requires a Negative Voltage Bias which operates alongside a Positive Voltage Bias. These Biases are applied in accordance to the Sequence during Turn-On and Turn-Off.

The Pallet Amplifier does not have a built-in Bias Sequence Circuit. Therefore, users need to either apply positive voltages and negative voltages in the required sequence, or add an external Bias Circuit to this Amplifier.

The required sequence for power supply is as follows.

#### **During Turn-On**

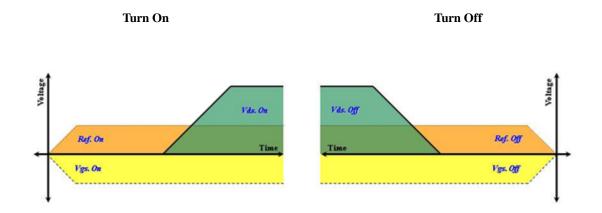
- 1. Connect GND.
- 2. Apply Vgs1 and Vgs2.
- 3. Apply Vds.
- 4. Apply the RF Power.

#### **During Turn-Off**

1. Turn off RF power.

2. Turn off Vds, and then, turn off the Vgs1 and Vgs2.

3. Remove all connections.



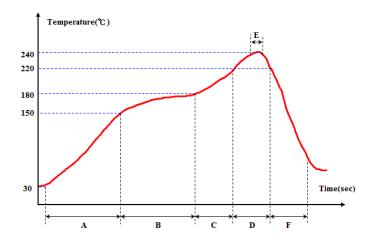
- Sequence Timing Diagram -

#### **Reflow Profile**

#### \* Reflow oven settings

Zone	Α	В	С	D	Е	F
Temperature(°C)	30∼150 °C	<b>150 ~ 180</b> ℃	180∼220 °C	220~220 °C	235 ~ 240 °C	$2 \sim 6$ °C / Sec Drop
Belt speed	55 ~ 115 sec	55 ~ 75 sec	30 ~ 50 sec	30 ~ 50 sec	5 ~ 10 sec	60 ~ 90 sec

#### \* Measured reflow profile



#### **Ordering Information**

Part Number	Package Design	
	-R (Reel)	
HT2121-15A	-B (Bulk)	
	-EVB (Evaluation Board)	

#### **Revision History**

Part Number	Release Date	Version	Modification	Data Sheet Status
HT2121-15A	2012.12.27	0.4	Changed Frequency & Model Number	Preliminary
HT2008-15A	2012.11.21	0.3	Changed Document	Preliminary
HT2008-15A	2012.09.10	0.2	Changed Quiescent current	Preliminary

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