HMC850LC3

28 GBPS, 1:2 FANOUT BUFFER WITH PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC850LC3 is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 28 Gbps
- Clock Buffering up to 20 GHz

Features

Inputs Terminated Internally to 50 Ohms

Differential Inputs are DC Coupled

Propagation Delay: 75 ps

Fast Rise and Fall Times: 16 / 15 ps

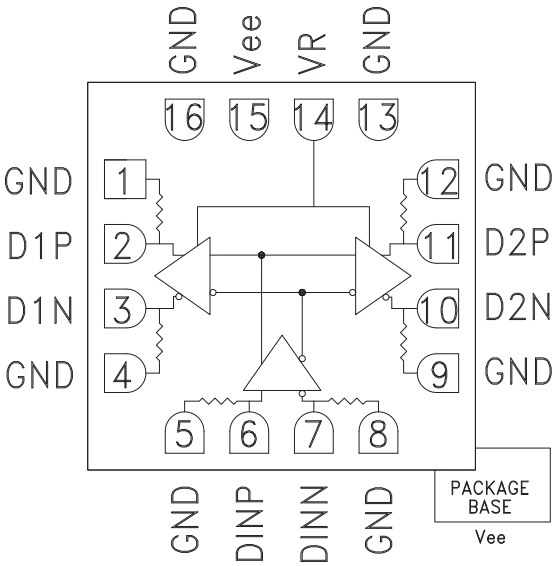
Programmable Differential

Output Voltage Swing: 600 - 1100 mV

Power Dissipation: 315 mW

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC850LC3 is a 1:2 Fanout Buffer designed to support data transmission rates up to 28 Gbps, and clock frequencies as high as 20 GHz. All differential inputs and outputs are DC coupled and terminated on chip with 50 Ohm resistors to the positive supply, ground. The outputs may be used in either single-ended or differential modes, and should be AC or DC coupled into 50 Ohm resistors connected to ground.

The HMC850LC3 also features an output level control pin, VR which allows for loss compensation or for signal level optimization. The HMC850LC3 operates from a single -3.3V DC supply and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vee = -3.3 V, VR = 0 V

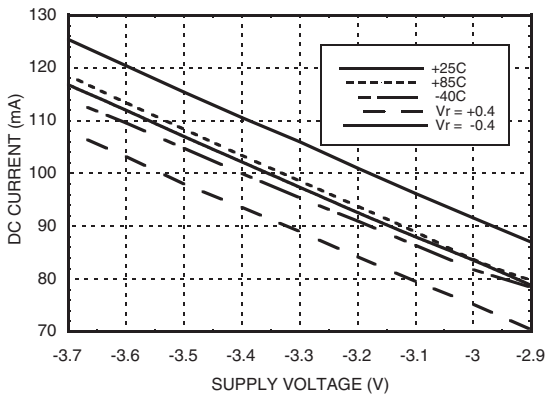
Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			95		mA
Maximum Data Rate			28		Gbps
Maximum Clock Rate			20		GHz
Input Voltage Range		-1.5		0.5	V
Input Voltage Differential		100		2000	mV
Input Return Loss	Frequency <20 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			-10		mV
Output Low Voltage			-550		mV
Output Rise / Fall Time	Single-Ended, 20% - 80%		16 / 15		ps

Electrical Specifications (continued)

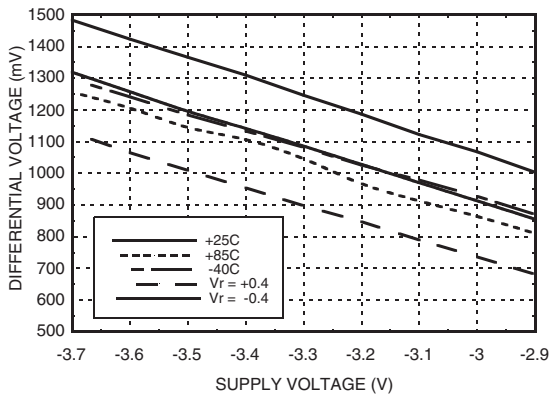
Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <20 GHz		10		dB
Small Signal Gain			28		dB
Random Jitter J_R	rms		0.2		ps rms
Deterministic Jitter, J_D	δ - δ, 2^{15}-1 PRBS input [1]		2	6	ps
Propagation Delay, td			75		ps
D1 to D2 Data Skew, t_{SKEW}			1	3	ps

[1] Deterministic jitter measured at 13 Gbps with a 300 mVpp, 2^{15}-1 PRBS input sequence.

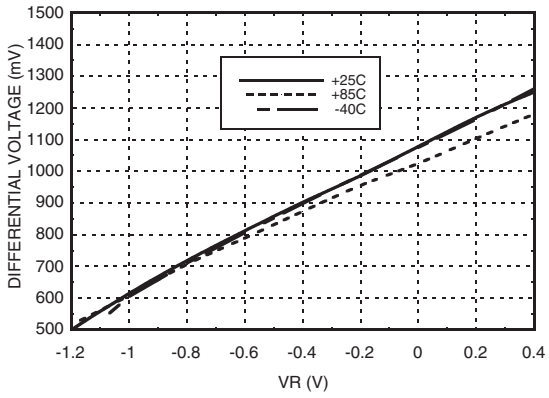
DC Current vs. Supply Voltage [1][2]



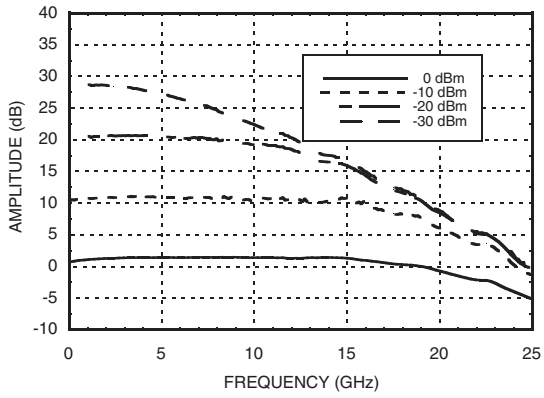
Output Differential vs. Supply Voltage [1][2]



Output Differential vs. VR [2][4]

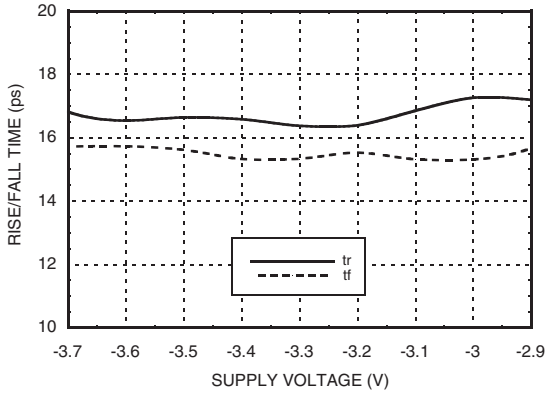


Amplitude vs. Input Power [1][3][4]

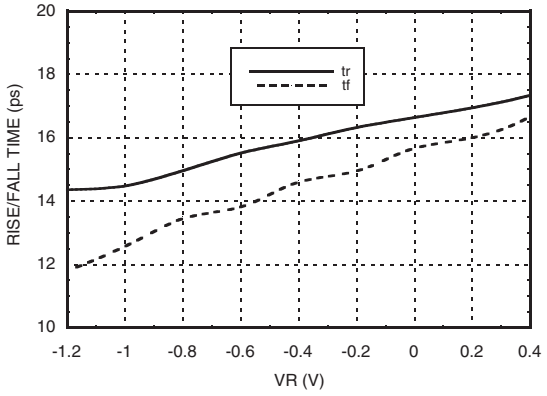


[1] VR = 0.0 V [2] Frequency = 13 Gbps [3] Device measured on evaluation board with port extensions [4] Vee = -3.3 V

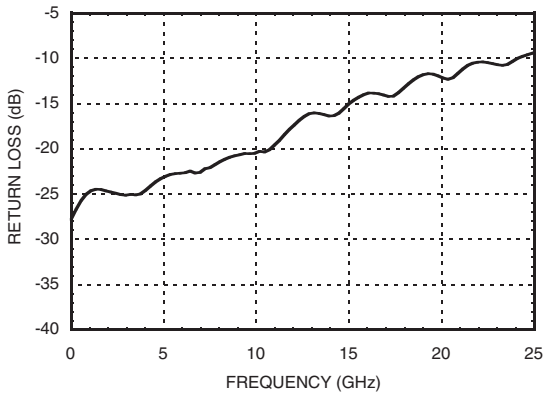
Rise / Fall Time vs. Supply Voltage [2][4]



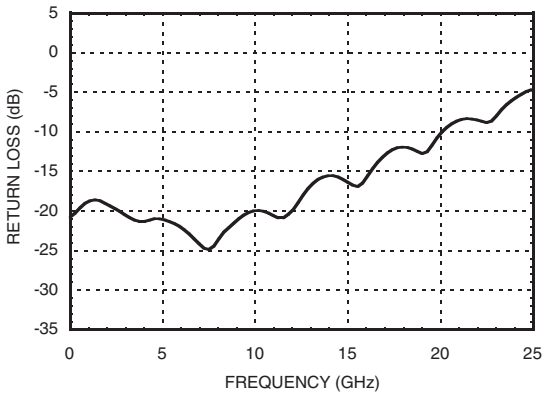
Rise / Fall Time vs. VR [2][4]



Input Return Loss vs. Frequency [1][3][4]

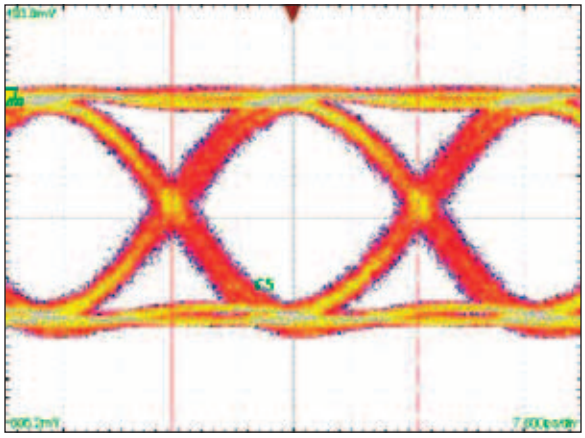


Output Return Loss vs. Frequency [1][3][4]



[1] VR = 0.0 V [2] Frequency = 13 Gbps [3] Device measured on evaluation board with port extensions [4] Vee = -3.3 V

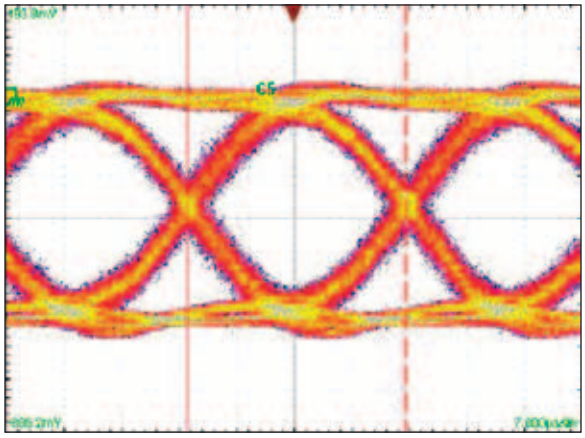
Eye Diagram @ 30 Gbps



Test Conditions:

Single-ended 550 mV data input. Pattern generated with four 2^{15} -1 PN patterns applied to the inputs resulting in a Quasi-Periodiic PRBS pattern at 30 Gbps. Measured using Tektronix CSA 8000.

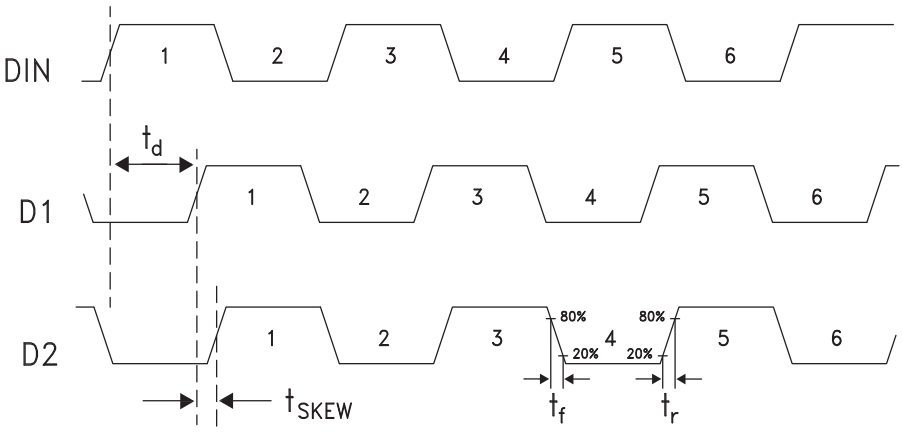
Eye Diagram @ 34 Gbps



Test Conditions:

Single-ended 550 mV data input. Pattern generated with four 2^{15} -1 PN patterns applied to the inputs resulting in a Quasi-Periodiic PRBS pattern at 34 Gbps. Measured using Tektronix CSA 8000.

Timing Diagram



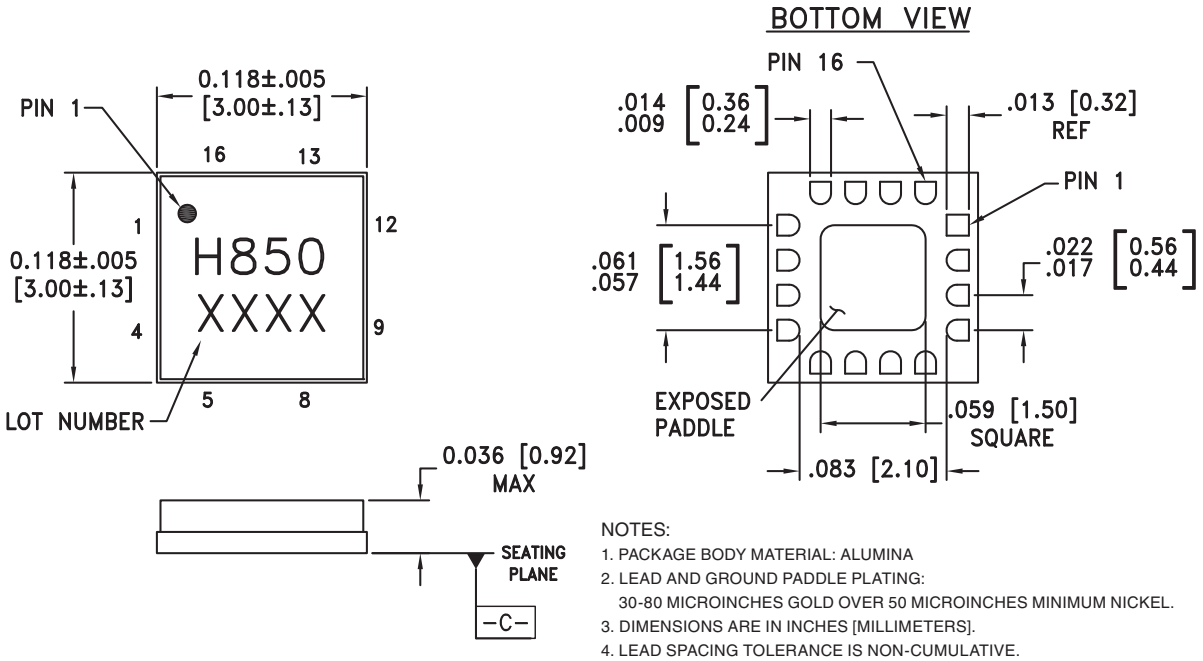
28 GBPS, 1:2 FANOUT BUFFER WITH PROGRAMMABLE OUTPUT VOLTAGE

Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +0.5 V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worse case device to package paddle	59 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

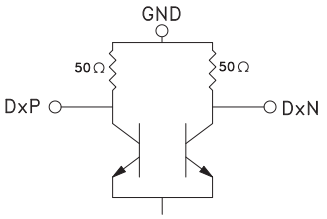
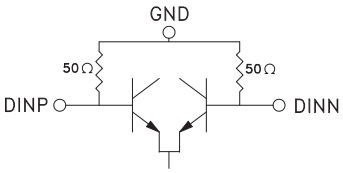
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing

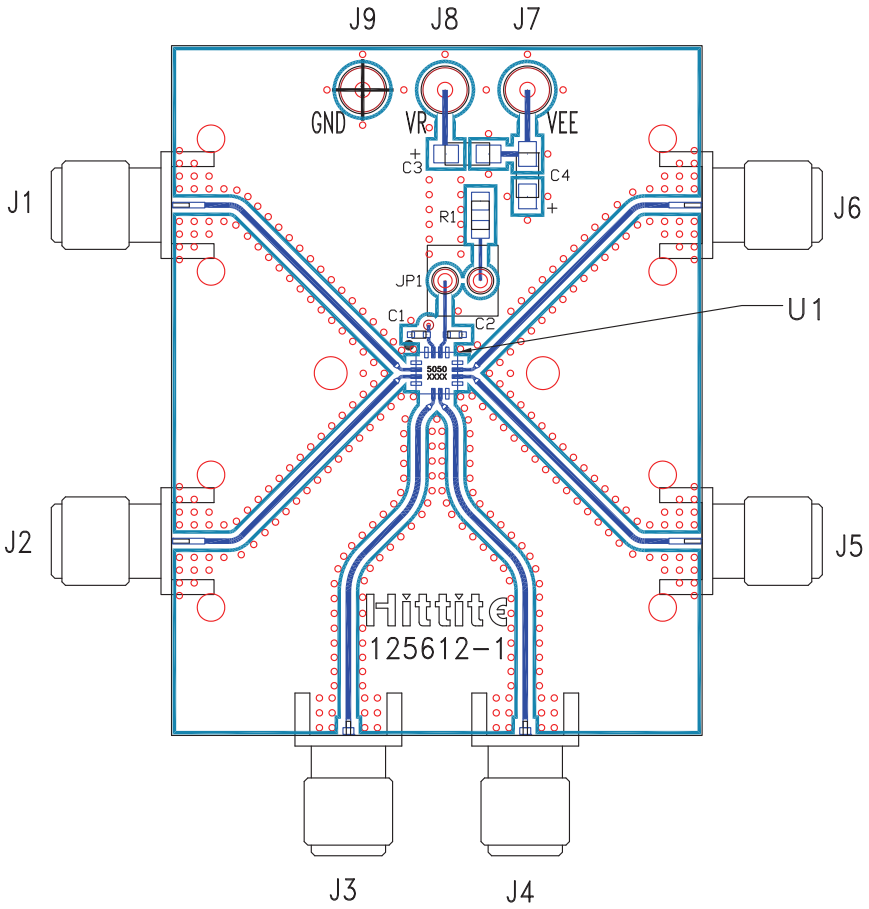


NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12, 13, 16	GND	These pins must be connected to a high quality RF/DC ground.	
2, 3, 10, 11	D1P, D1N, D2N, D2P	Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply.	
6, 7	DINP, DINN	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply	
14	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per “Output Differential vs. VR” plot.	
15 Package Base	Vee	These pins and the exposed paddle must be connected to the negative voltage supply.	

Evaluation PCB



List of Materials for Evaluation PCB 125614 [1]

Item	Description
J1 - J6	PCB Mount K RF Connectors
J7 - J9	DC Pin
C1, C2	100 pF Capacitor, 0402 Pkg.
C3, C4	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC850LC3 Fanout Buffer
PCB [2]	125612 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

Application Circuit