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# HD74HC4020

## 14-stage Binary Counter

REJ03D0645-0200 (Previous ADE-205-531) Rev.2.00 Mar 30, 2006

### **Description**

The HD74HC4020 is a 14 stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input.

#### **Features**

• High Speed Operation:  $t_{pd}$  (Clock to  $Q_1$ ) = 14 ns typ ( $C_L = 50 \text{ pF}$ )

• High Output Current: Fanout of 10 LSTTL Loads

• Wide Operating Voltage:  $V_{CC} = 2 \text{ to } 6 \text{ V}$ 

• Low Input Current: 1 μA max

• Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max (Ta = 25°C)

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC4020P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	_
HD74HC4020FPEL	D74HC4020FPEL SOP-16 pin (JEITA)		FP	EL (2,000 pcs/reel)

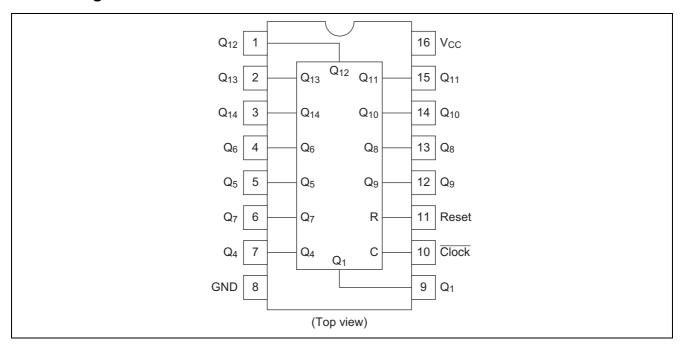
Note: Please consult the sales office for the above package availability.

#### **Function Table**

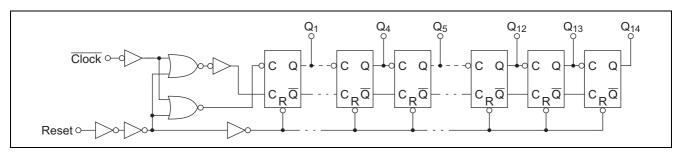
Clock	Reset	Outputs State
	L	No change
	L	Advance to next state
X	Н	All output are low

Note: 1. X: Don't care

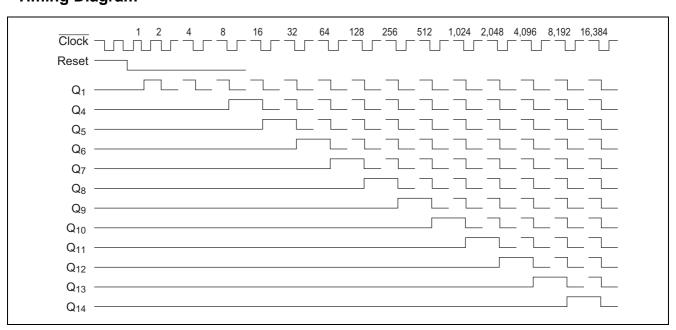
### **Pin Arrangement**



#### **Block Diagram**



## **Timing Diagram**



## **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
Input / Output voltage	V <sub>IN</sub> , V <sub>OUT</sub>	–0.5 to V <sub>CC</sub> +0.5	V
Input / Output diode current	I <sub>IK</sub> , I <sub>OK</sub>	±20	mA
Output current	I <sub>OUT</sub>	±25	mA
V <sub>CC</sub> , GND current	I <sub>CC</sub> or I <sub>GND</sub>	±50	mA
Power dissipation	P <sub>T</sub>	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## **Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to V <sub>CC</sub>	V	
Operating temperature	Та	-40 to 85	°C	
		0 to 1000		V <sub>CC</sub> = 2.0 V
Input rise / fall time*1	t <sub>r</sub> , t <sub>f</sub>	0 to 500	ns	V <sub>CC</sub> = 4.5 V
		0 to 400		V <sub>CC</sub> = 6.0 V

Note: 1. This item guarantees maximum limit when one input switches. Waveform: Refer to test circuit of switching characteristics.

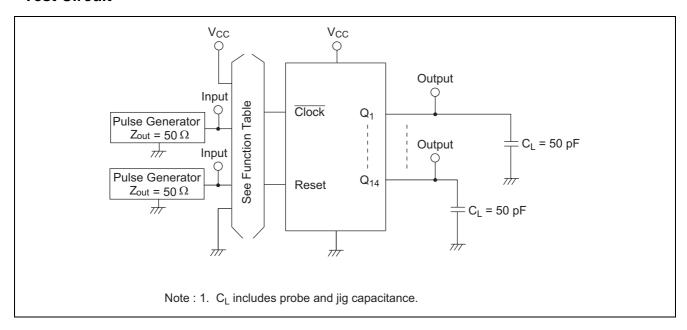
#### **Electrical Characteristics**

			Ta = 25°C Ta = -40 to+85°C		to+85°C					
Item	Symbol	V <sub>cc</sub> (V)	Min	Тур	Max	Min	Max	Unit	Test Con	ditions
Input voltage	V <sub>IH</sub>	2.0	1.5	_	_	1.5	_	V		
		4.5	3.15	_		3.15	_			
		6.0	4.2	_	_	4.2	_			
	$V_{IL}$	2.0	_	_	0.5	_	0.5	V		
		4.5	_	_	1.35	_	1.35			
		6.0	_	_	1.8	_	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0		1.9	_	V	$Vin = V_{IH} or V_{IL}$	$I_{OH} = -20 \mu A$
		4.5	4.4	4.5	_	4.4	_			
		6.0	5.9	6.0	_	5.9	_			
		4.5	4.18	_	_	4.13	_			$I_{OH} = -4 \text{ mA}$
		6.0	5.68	_	_	5.63	_			$I_{OH} = -5.2 \text{ mA}$
	V <sub>OL</sub>	2.0	_	0.0	0.1	_	0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu A$
		4.5	_	0.0	0.1	_	0.1			
		6.0	_	0.0	0.1	_	0.1			
		4.5	_	_	0.26	_	0.33			$I_{OH} = 4 \text{ mA}$
		6.0	_	_	0.26	_	0.33			$I_{OH} = 5.2 \text{ mA}$
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	Vin = V <sub>CC</sub> or GN	D
Quiescent supply current	Icc	6.0	_	_	4.0		40	μΑ	Vin = V <sub>CC</sub> or GN	D, lout = $0 \mu A$

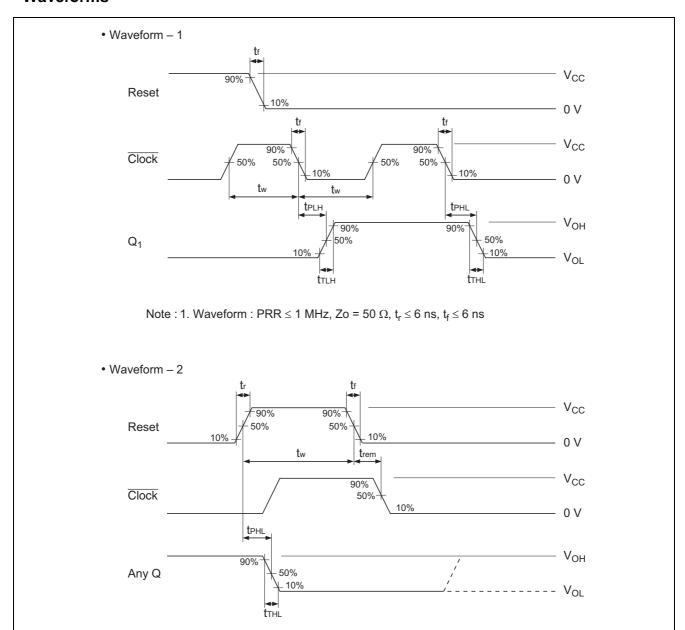
# **Switching Characteristics** ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

			Т	a = 25°	С	Ta = -40	to +85°C		
Item	Symbol	V <sub>cc</sub> (V)	Min	Тур	Max	Min	Max	Unit	Test Conditions
Maximum clock	f <sub>max</sub>	2.0	_	_	5	_	4	MHz	
frequency		4.5	_	_	25	_	20		
		6.0	_	_	29	_	24		
Propagation delay	t <sub>PLH</sub>	2.0	_	_	175	_	220	ns	Clock to Q <sub>1</sub>
time	t <sub>PHL</sub>	4.5	_	14	35	_	44		
		6.0	_	_	30	_	37		
	t <sub>PLH</sub>	2.0	_	_	175	_	220	ns	Clock to Q <sub>1</sub>
	t <sub>PHL</sub>	4.5	_	14	35	_	44		
		6.0	_	_	30	_	37		
	t <sub>PLH</sub>	2.0	_	_	200	_	250	ns	Reset to output
	t <sub>PHL</sub>	4.5	_	18	40	_	50		
		6.0	_	_	34	_	43		
	t <sub>PLH</sub>	2.0	_	_	100	_	125	ns	$Q_n$ to $Q_{n-1}$
	t <sub>PHL</sub>	4.5	_	_	20	_	25		
		6.0	_	_	17	_	21		
Removal time	t <sub>rem</sub>	2.0	100	_	_	125	_	ns	
		4.5	20	6	_	25	_		
		6.0	17	_	_	21	_		
Pulse width	t <sub>w</sub>	2.0	80		_	100		ns	
		4.5	16	4	_	20	_		
		6.0	14	_	_	17	_		
Output rise/fall	t <sub>TLH</sub>	2.0	_	_	75	_	95	ns	
time	t <sub>THL</sub>	4.5	_	5	15	_	19		
		6.0	_	_	13	_	16		
Input capacitance	Cin	_	_	5	10	_	10	pF	

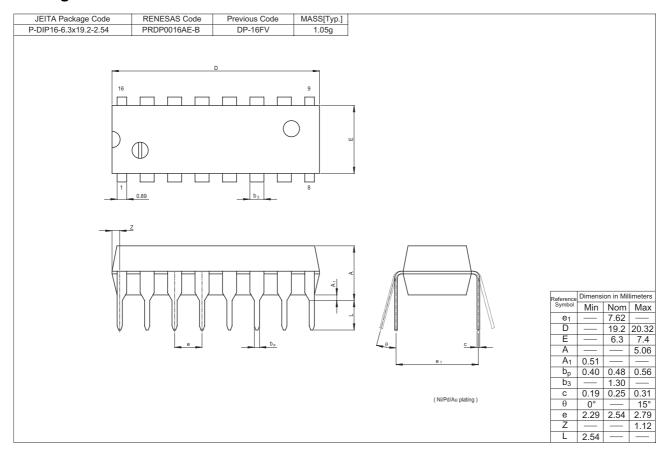
## **Test Circuit**

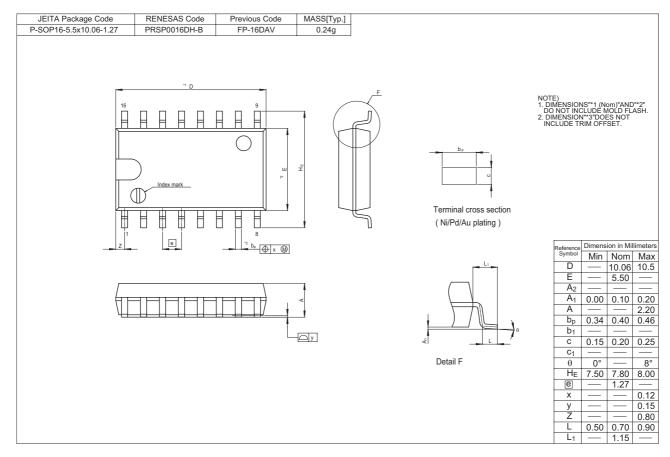


### **Waveforms**



### **Package Dimensions**





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