AND8353/D

Implementing Cost Effective and Robust Power Factor Correction with the NCP1607

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APPLICATION NOTE

Introduction

The NCP1607 is a voltage mode power factor correction (PFC) controller designed to drive cost−effective converters to meet input line harmonic regulations. The device operates in Critical Conduction Mode (CRM) for optimal performance in applications up to about 300 W. Its voltage mode scheme enables it to obtain unity power factor without the need for a line sensing network. The output voltage is accurately controlled with a built in high precision error amplifier. The controller also implements a comprehensive array of safety features for robust designs.

This application note describes the design and implementation of a 400 V, 100 W, CRM Boost PFC converter using the NCP1607. The converter exhibits high power factor, low standby power dissipation, high active mode efficiency, and a variety of protection features.

The Need for PFC

Most electronic ballasts and switching power supplies use a diode bridge rectifier and a bulk storage capacitor to produce a dc voltage from the utility ac line. This produces a non−sinusoidal current draw and increases the demand on the power delivery infrastructure. Government regulations and utility requirements often necessitate control over line current harmonic content.

Active PFC circuits have become the most popular way to meet these harmonic content requirements. They consist of inserting a PFC pre−regulator between the rectifier bridge and the bulk capacitor (Figure 1). The boost (or step−up) converter is the most popular topology for active power factor correction. With the proper control, it can be made to produce a constant output voltage while maintaining a sinusoidal input current from the line.

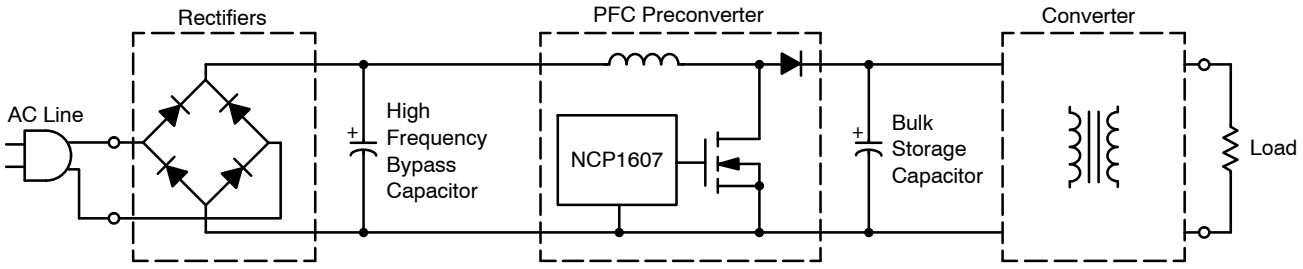

Figure 1. Active PFC Stage with the NCP1607

Basic Operation of a CRM Boost Converter

For medium power (<300 W) applications, critical conduction mode (CRM) is the preferred control method. Critical conduction mode occurs at the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In CRM, the next driver on time is initiated when the boost inductor current reaches zero. Hence, CRM combines the lower peak currents of CCM operation with the zero current switching of DCM operation. This control method causes the frequency to vary with the line input voltage and the output load. The operation and waveforms of a PFC boost converter are illustrated in Figure 2. For detailed information on the operation of a CRM Boost Converter for PFC applications, please refer to AND8123 at www.onsemi.com.

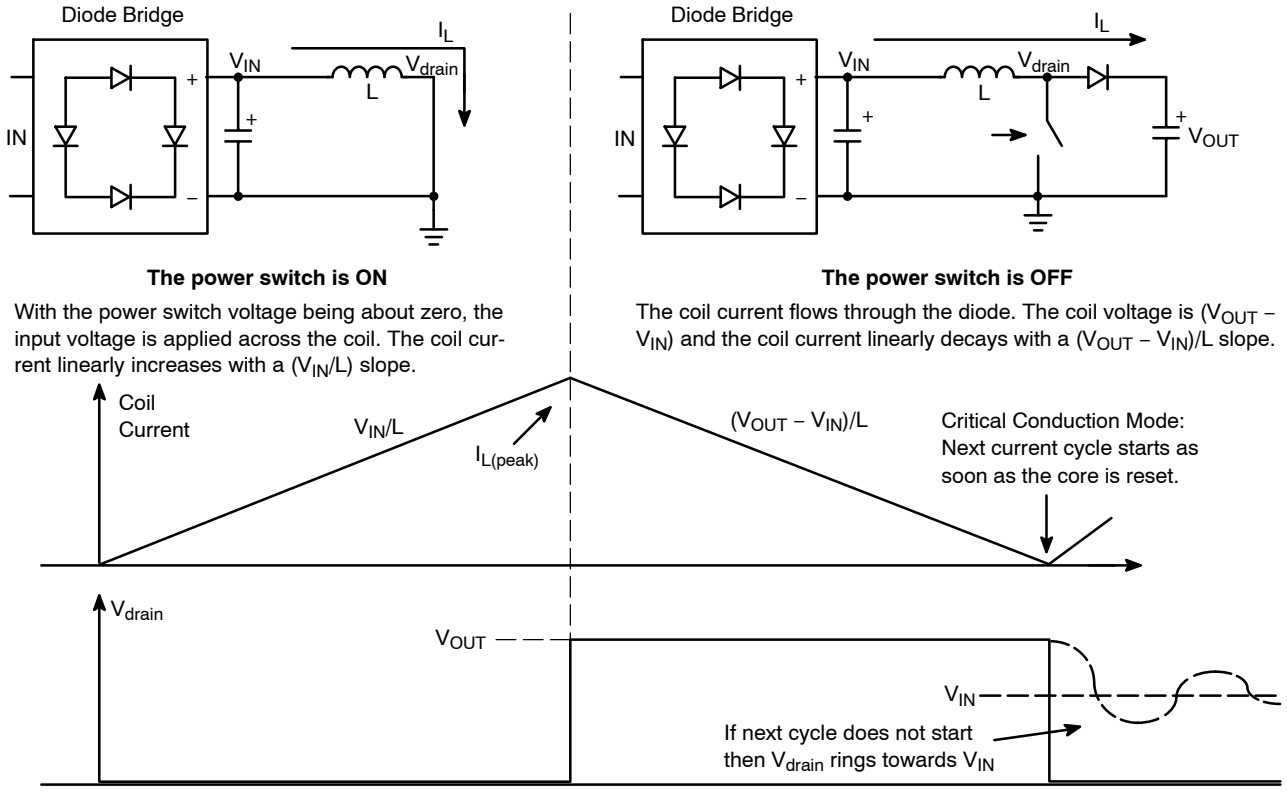

Figure 2. Schematic and Waveforms of an Ideal CRM Boost Converter

Features of the NCP1607

The NCP1607 offers an ideal controller for medium power CRM boost PFC applications. A simple CRM Boost pre−converter featuring the NCP1607 is shown in Figure 3.

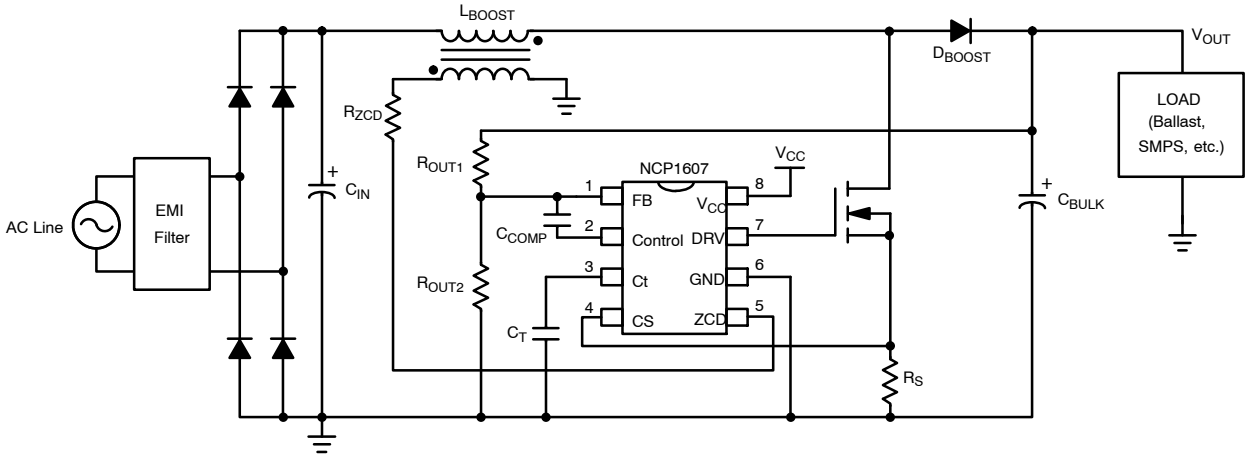

Figure 3. CRM Boost PFC Stage Featuring the NCP1607

Pin 1 (FB) senses the boost output voltage through the resistor divider formed by R_{OUT1} and R_{OUT2}. This pin is the input to an error amplifier, whose output is pin 2 (Control). A combination of resistors and capacitors between pin 1 and pin 2 form a compensation network that limits the bandwidth of the converter. For high power factor, the bandwidth is generally below 20 Hz. A capacitor connected to pin 3 (Ct) sets the on time for a given Control voltage.

CS (pin 4) gives cycle by cycle over current protection. This is accomplished with an internal comparator which compares the voltage generated by the switch current and R_{SENSE} to an internal 0.5 V reference.

Pin 5 (ZCD) senses the demagnetization of the boost inductor. The driver on time begins when the voltage at this pin rises above 2.1 V (typ) and then drops below 1.6 V (typ). A resistor in series with the zero current detection (ZCD) winding limits the current into this pin. Additionally, by pulling this pin to ground, the drive pulses are disabled and the controller is placed in a low current standby mode.

The NCP1607 features a powerful output driver on pin 7. This driver is capable of switching the gates of large MOSFETs in an efficient manner. The driver incorporates both active and passive pulldown circuitry to prevent the output from floating high when V_{CC} is off.

Pin 8 (V_{CC}) powers the controller. When V_{CC} is below the turn on level ($V_{CC(on)}$, typically 11.8 V), the current consumption of the part is limited to < 40 μA. This gives allows for fast startup times and reduced standby power losses. Alternatively, V_{CC} can also be directly supplied from another controller, such as the NCP1230. This approach can further improve standby power performance in a two stage SMPS system.

Open Feedback Loop Protection

The NCP1607 features comprehensive protection against open feedback loop conditions by implementing OVP, UVP, and Floating Pin Protection (FPP). There are three conditions in which the feedback loop can be opened.

1. UVP Protection: The connection from resistor ROUT1 to the FB pin is opened. ROUT2 pulls the FB pin down to ground. The UVP comparator detects a UVP fault and disables thus disabling the drive.
2. OVP Protection: The connection from resistor ROUT2 to the FB pin is open. ROUT1 pulls the FB pin up to the output voltage. The ESD diode clamps the FB voltage to 10 V and ROUT1 limits the current into the FB pin. The VEAL clamp detects a static OVP fault and the drive is disabled.
3. FPP Protection: The FB pin is floating. The internal pull down resistor, R_{FB}, pulls the FB voltage down below the UVP threshold. The UVP comparator detects a UVP fault and disables the drive.

UVP and OVP protect the system from low bulk voltages and rapid operating point changes respectively, while the FPP protects the system against floating feedback pin conditions. Without FPP, if a manufacturing error causes the feedback pin to float, the feedback voltage is dependent on the coupling within the system and the surrounding environment. The coupled feedback voltage may be within the regulation limits (i.e. above the UVP threshold, but below V_{ref}) and cause the controller to deliver excessive power. The result is that the output voltage rises until a component fails due to overvoltage stress.

For detailed information on the operation of the NCP1607, please refer to NCP1607/D at www.onsemi.com.

Design Procedure

The design of a CRM Boost PFC circuit is discussed in many ON Semiconductor application notes (see Table 1). This application note describes the design procedure for a 400 V, 100 W converter using the features of the NCP1607. A design aid that allows users to quickly determine component values is available at www.onsemi.com.

Table 1.

AND8123	Power Factor Correction Stages Operating in Critical Conduction Mode
AND8016	Design of Power Factor Correction Circuits Using the MC33260
AND8154	NCP1230 90 W, Universal Input Adapter Power Supply with Active PFC
HBD853	Power Factor Correction Handbook

*Additional resources for the design and understanding of CRM Boost PFC circuits available at www.onsemi.com.

DESIGN STEP 1: Define the Required Boost Parameters

Minimum AC Line Voltage	Vac_{LL}	85	V_{ac}
Maximum AC Line Voltage	Vac_{HL}	265	V_{ac}
Line Frequency	f_{line}	47−63	Hz
Boost PFC Output Voltage	V_{OUT}	400	V
Maximum Output Voltage	$V_{OUT(OVP)}$	440	V
Boost Output Power	P_{OUT}	100	W
Minimum Switching Frequency	$f_{SW(MIN)}$	50	kHz
Estimated Efficiency	η	92	%

DESIGN STEP 2: Calculate the Boost Inductor

The boost inductor is calculated with Equation 1:

$$L \le \frac{Vac^2 \cdot \left(\frac{V_{OUT}}{\sqrt{2}} - Vac\right) \cdot \eta}{V_{OUT} \cdot P_{OUT} \cdot f(min) \cdot \sqrt{2}} \quad \text{(eq. 1)}$$

To ensure that the switching frequency exceeds the minimum frequency, the boost inductor is evaluated at both the minimum and maximum RMS line voltage:

- $L \le 465\ \mu H$ for Vac_{LL}
- $L \le 408\ \mu H$ for Vac_{HL}

A value of 400 μH is selected. Equation 2 is used to calculate the resultant minimum frequency at full load.

$$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L \cdot P_{OUT}} \cdot \left(1 - \frac{Vac \cdot \sqrt{2}}{V_{OUT}}\right) \quad \text{(eq. 2)}$$

f_{SW} is equal to 58 kHz at 85 V_{ac} and 51 kHz at 265 V_{ac}.

DESIGN STEP 3: Size the Ct Capacitor

The Ct capacitor must be large enough to provide the maximum on time at low line and full power. The maximum on time is given by:

$$t_{on(MAX)} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot Vac_{LL}^{\ 2}} = 12.0\ \mu s \quad \text{(eq. 3)}$$

However, delivering an on tiem that is too long causes the application to deliver excessive power and also reduces the control range at high line or light loads. The Ct capacitor is best sized slightly larger then that calcultated by Equation 4:

$$Ct > \frac{I_{CHARGE} \cdot t_{on(MAX)}}{V_{CTMAX}} = \frac{2 \cdot P_{OUT} \cdot L \cdot I_{CHARGE}}{\eta \cdot Vac^2 \cdot V_{CTMAX}} \quad \text{(eq. 4)}$$

Where I_{CHARGE} and V_{CTMAX} are found in the NCP1607 datasheet. To ensure that the controller is capable of delivering the maximum on time, use the maximum I_{CHARGE} and the minimum V_{CTMAX} in the calculations for Ct. From the NCP1607 datasheet:

- $V_{CTMAX} = 2.9$ V (min)
- $I_{CHARGE} = 297\ \mu A$ (max)

Ct is equal to 1.2 nF. A normalized value of 1.5 nF (±10%) provides adequate.

DESIGN STEP 4: Determine the ZCD Turns Ratio

A winding taken off of the boost inductor providess the zero current detection (ZCD) signal. When the switch is on, the ZCD voltage is calculated using Equation 5:

$$V_{ZCD(on)} = \frac{-V_{in}}{N_B : N_{ZCD}} \quad \text{(eq. 5)}$$

where V_{IN} is the instantaneous ac line voltage.

When the switch is off, the ZCD voltage is calculated using Equation 6:

$$V_{ZCD(off)} = \frac{V_{OUT} - V_{in}}{N_B : N_{ZCD}} \quad \text{(eq. 6)}$$

To activate the zero current detection comparators of the NCP1607 (see Figure 5), the ZCD turns ratio is sized such that at least V_{ZCDH} (2.1 V typ) is applied to the ZCD pin during all operating conditions. The turns ratio is calculated using Equation 7.

$$N_B : N_{ZCD} \le \frac{V_{OUT} - Vac_{HL} \cdot \sqrt{2}}{V_{ZCDH}} = 11 \quad \text{(eq. 7)}$$

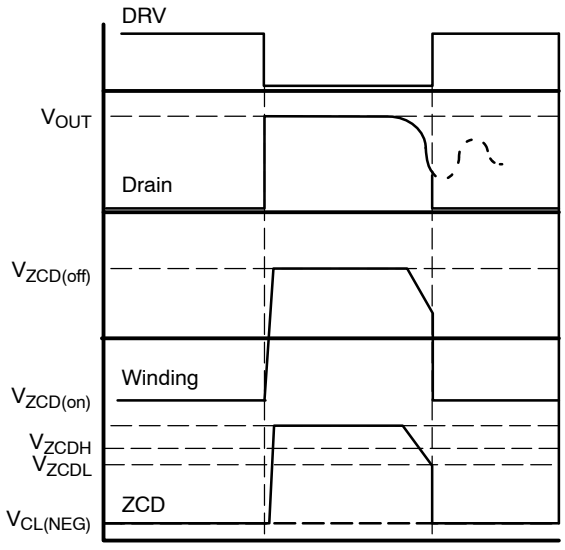

Figure 4. Voltage Waveforms for Zero Current Detection

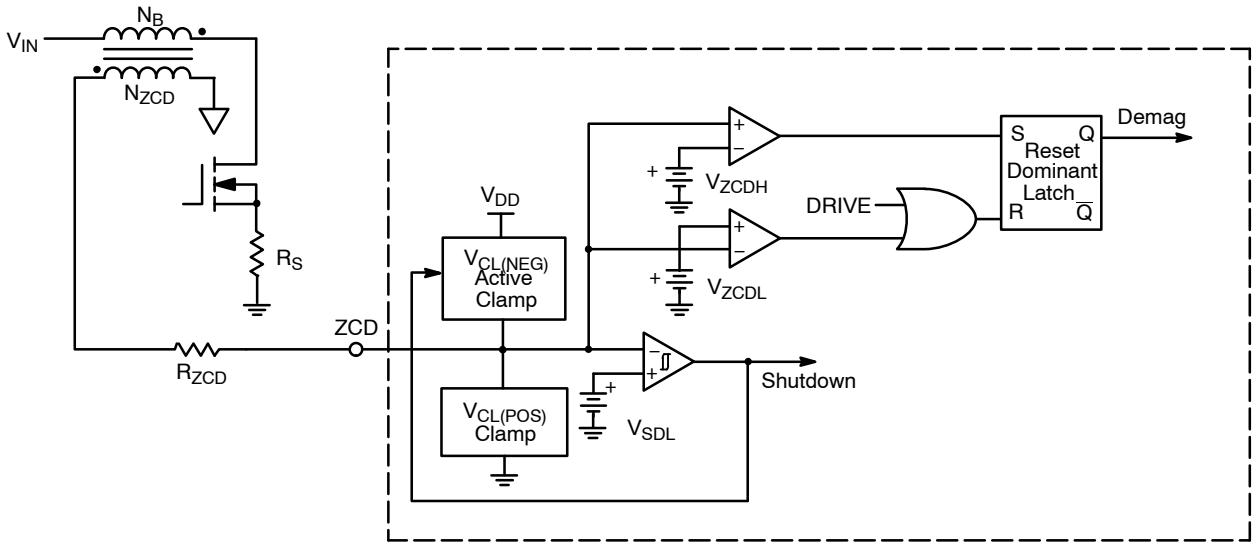

Figure 5. ZCD Winding and Internal Logic Arrangement

A turns ratio of 10 is selected for this design. R_{ZCD} is added between the ZCD winding and pin 5 to limit the current into or out of the pin. This current must be low enough so as to not trigger the ZCD shutdown feature. R_{ZCD} is calculated using Equation 8:

$$R_{ZCD} \geq \frac{Vac_{HL} \cdot \sqrt{2}}{I_{CL(NEG)} \cdot (N_B : N_{ZCD})} = 15.0\ k\Omega \quad \text{(eq. 8)}$$

where $I_{CL(NEG)}$ = 2.5 mA (from the NCP1607 datasheet)

The value of R_{ZCD} and the small parasitic capacitance of the ZCD pin determines when the ZCD winding signal is detected and the next drive pulse begins. Ideally R_{ZCD} turns on the drive at the drain voltage valley to minimize switching losses. The value of R_{ZCD} large cause minimum drain voltage switching is fournd experimentally. Too large of a value creates a significant delay in detecting the ZCD event. In this case, the controller operates in discontinuous conduction mode (DCM) and the power factor is reduced. If R_{ZCD} is too small, then the next driver on time starts when the voltage is high and switching efficiency is reduced.

DESIGN STEP 5: Set the FB, OVP, and UVP Levels

The low bandwidth of the PFC stage causes overshoots during transient loads or at startup. The NCP1607 incorporates an adjustable overvoltage protection (OVP) circuit to protect against overshoots. The OVP activation level is set by R_{OUT1}. A derivation in the NCP1607 datasheet results in Equation 9:

$$V_{OUT(OVP)} = V_{OUT(OVP)} + R_{OUT1} \cdot I_{OVP} \quad \text{(eq. 9)}$$

Where I_{OVP} = 10 μA.

R_{OUT1} is calculated using Equation 10:

$$R_{OUT1} = \frac{V_{OUT(OVP)} - V_{OUT}}{I_{OVP}} \quad \text{(eq. 10)}$$

R_{OUT1} is equal to 4.0 MΩ.

R_{OUT2} is sized to maintain 2.5 V on the FB pin when Vout is at the targeted level. The FPP feature introduces an error into the output voltage.

The output voltage including the error casued by R_{FB} ($\overline{V_{OUT}}$) is calculated using Equation 11.

$$\overline{V_{OUT}} = V_{OUT} + R_{OUT1} \cdot \frac{V_{REF}}{R_{FB}} \quad \text{(eq. 11)}$$

$$\overline{V_{OUT}} = 400 + 4\ M \cdot \frac{2.5}{4.7\ M} = 402\ V$$

The error caused by R_{FB} is compensated by adjusting R_{OUT2}. The parallel combination of R_{FB} and R_{OUT2} form an equivalent resistor R_{EQ} that is calculated using Equation 12.

$$R_{EQ} = R_{OUT1} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad \text{(eq. 12)}$$

$$R_{EQ} = 4\ M \cdot \frac{2.5}{400 - 2.5} = 25.16\ k\Omega$$

R_{EQ} is used to calculate R_{OUT2}.

$$R_{OUT2} = \frac{R_{EQ} \cdot R_{FB}}{R_{FB} - R_{EQ}} \quad \text{(eq. 13)}$$

$$R_{OUT2} = \frac{25.16\ k \cdot 4.7\ M}{4.7\ M - 25.16\ k} = 25.29\ k\Omega$$

For this design, a 25.5 kΩ resistor is used for R_{OUT2}. The compensated output voltage is calculated using Equation 14.

$$V_{OUT} = V_{REF} \cdot \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}} + R_{OUT1} \cdot \frac{V_{REF}}{R_{FB}} \quad \text{(eq. 14)}$$

$$V_{OUT} = 2.5 \cdot \frac{4\ M + 25.5\ k}{25.5\ k} + 4\ M \cdot \frac{2.5}{4.7\ M} = 397\ V$$

When determining the maximum output voltage level, care must be exercised so as not to interfere with the natural line frequency ripple on the output capacitor. This ripple is caused by the averaging effect of the PFC stage: the current charging the bulk cap is sinusoidal and in phase with the input line, but the load current is not. The resultant ripple voltage is calculated using Equation 15:

$$V_{ripple(pk-pk)} = \frac{P_{OUT}}{C_{BULK} \cdot 2 \cdot \pi \cdot f_{line} \cdot V_{OUT}} \quad \text{(eq. 15)}$$

where f_{line} = 47 Hz (worst case for ripple)

A bulk capacitor value of 68 μF results in a peak−to−peak ripple of 12.5 V. This corresponds to a peak output voltage of 406.25 V, which is below the peak output overvoltage level (440 V).

The NCP1607 also incorporates undervoltage protection (UVP). Under normal conditions, the boost output capacitor charges to the peak of the ac line. If it does not charge to some minimum voltage, the NCP1607 enters undervoltage protection. The voltage on the output that triggers a UVP fault is calculated using Equation 16:

$$V_{OUT(UVP)} = \frac{R_{OUT1} + R_{OUT2}}{R_{OUT2}} \cdot V_{UVP} = 48\ V \quad \text{(eq. 16)}$$

$$V_{OUT(UVP)} = \frac{4\ M + 25.5\ k}{25.5\ k} \cdot 300\ mV = 48\ V$$

Note that this feature also provides protection against open loop conditions in the feedback path. If Pin 1 is inadvertently floating (perhaps due to a bad solder joint), the controller senses that V_{FB} is low and responds by delivering maximum power. The output voltage increases and over stresses the components. The NCP1607 incorporates two features to protect the application if FB is floating. The internal pull−down resistor, R_{FB}, ensures that the FB pin is pulled low if it is floating. Additionally, an internal timer adds a 180 μs delay during startup prior to the first drive pulse. Since the built in error amplifier normally pulls FB to V_{REF}, the NCP1607 disables the error amplifier during this time (Figure 6). If the V_{FB} remains less than UVP (300 mV typ), the driver and the error amplifier remain disabled. The combination of R_{FB} and the start timer protects the application if the feedback loop is open during startup.

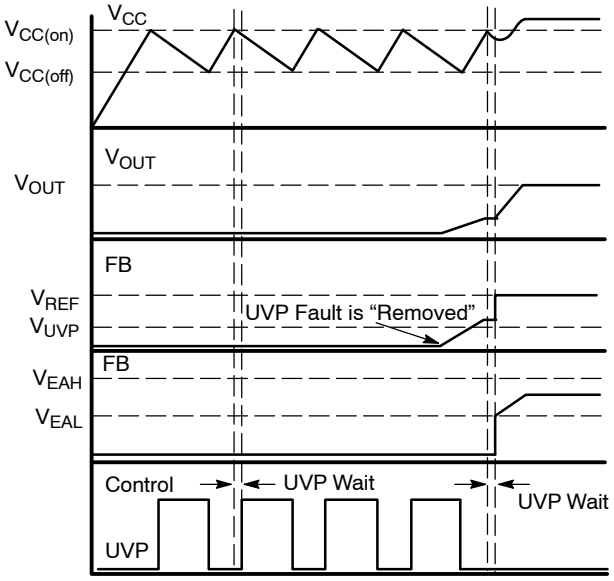

Figure 6. Timing Diagram Showing UVP and Recovery from UVP

If the FB pin floats during operation, V_{FB} begins decreasing from V_{ref}. The rate of decrease depends on R_{FB} and the FB pin parasitic capacitance. As V_{FB} decreases, the control pin voltage the on time increase until $V_{FB} < V_{UVP}$. When the FB voltage drops below the UVP threshold, then the undervoltage fault will be entered. The situation is depicted in Figure 7.

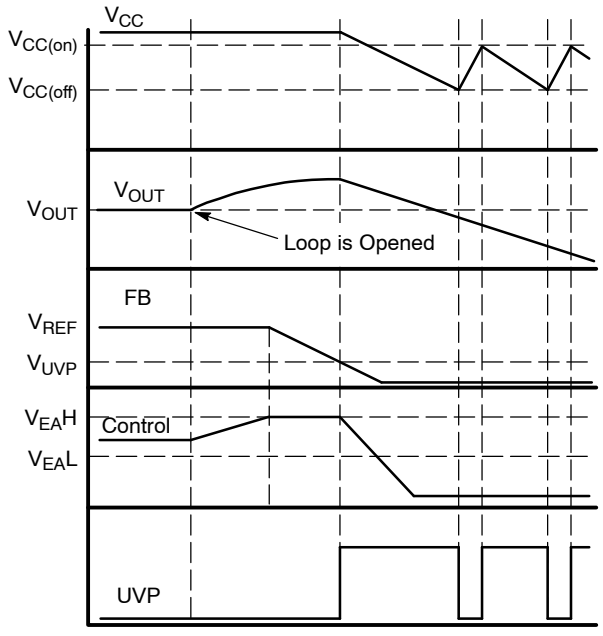

Figure 7. UVP Operation if Loop is Opened After Startup

DESIGN STEP 6: Size the Power Components

The power components are properly sized for the current and voltages applied to them. The stresses are greatest at full load and low line.

1. The Boost inductor, L

$$I_{L(peak)} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{\eta \cdot Vac_{LL}} = 3.62\ A \quad \text{(eq. 17)}$$

$$I_{L(RMS)} = \frac{2 \cdot P_{OUT}}{\sqrt{3} \cdot Vac_{LL} \cdot \eta} = 1.48\ A \quad \text{(eq. 18)}$$

2. The Boost Diode, D_{BOOST}

$$I_{D(RMS)} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi}} \cdot \frac{P_{OUT}}{\eta \cdot \sqrt{Vac_{LL} \cdot V_{OUT}}} = 0.75\ A \quad \text{(eq. 19)}$$

3. The MOSFET, Q1

$$I_{M(RMS)} = \frac{2}{\sqrt{3}} \cdot \frac{P_{OUT}}{\eta \cdot Vac_{LL}} \quad \text{(eq. 20)}$$

$$\sqrt{1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot V_{OUT}}\right)} = 1.27\ A$$

The MOSFETa maximum voltage is equal to the V_{OUT} overvoltage level (440 V for this example). If an 80% derating is used for the MOSFET's BV_{DSS}, a 550 V FET provides adequate margin.

4. The sense resistor, R_S

$$R_S = \frac{V_{CS(limit)}}{I_{peak}} = 0.14\ \Omega \quad \text{(eq. 21)}$$

$$P_{RS} = I_{M(RMS)}{}^2 \cdot R_S = 0.22\ W \quad \text{(eq. 22)}$$

$V_{CS(limit)} = 0.5$ V (typ)

5. The bulk capacitor, C_{BULK}

$$I_{C(RMS)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{OUT}{}^2}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{OUT} \cdot \eta^2} - (I_{LOAD(rms)})^2} = 0.70\ A \quad \text{(eq. 23)}$$

The bulk capacitor value is calculated in Step 5 to give an acceptable ripple voltage that does not trigger the output over voltage protection. This value may need to be increased so that the RMS current is within the capacitor's ratings.

The voltage rating of C_{BULK} is greater than the maximum V_{OUT} level. Since this design has an output overvoltage level of 440 V, a 450 V capacitor is selected.

DESIGN STEP 7: Supply V_{CC}

Generally, a resistor connected between the ac input and pin 8 charges up the V_{CC} cap to the $V_{CC(on)}$ level. Because of the very low consumption of the NCP1607 during this stage, most of the current goes directly to charging up the V_{CC} capacitor. This provides faster startup times and reduced standby power dissipation. The startup time is approximated with the following equation:

$$t_{START} = \frac{C_{VCC} \cdot V_{CC(on)}}{\frac{Vac \cdot \sqrt{2}}{R_{START}} - I_{CC(startup)}} \quad \text{(eq. 24)}$$

Where $I_{CC(startup)} = 40\ \mu A$ (max)

When the V_{CC} voltage exceeds the $V_{CC(on)}$ level (12 V typical), the internal references and logic of the NCP1607 turn on. The controller has an undervoltage lockout (UVLO) feature that keeps the part active until V_{CC} drops below about 9.5 V. This hysteresis allows ample time for another supply to take over and provide the necessary power to V_{CC}. The ZCD winding is an excellent candidate, but the voltage generated on the winding can be well below the desired V_{CC} level. Therefore, a small charge pump must be constructed to supply V_{CC}. Such a schematic is illustrated in Figure 8.

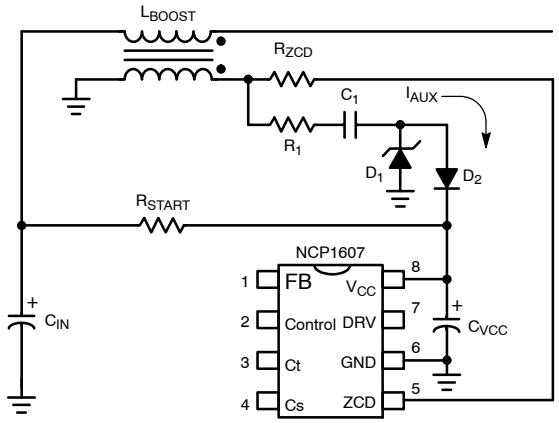

Figure 8. The ZCD Winding can Supply V_{CC} through a Charge Pump Circuit

C1 stores the energy for the charge pump. R1 limits the current by reducing the rate of voltage change. D1 supplies current to C1 when its cathode is negative. When its cathode is positive it limits the maximum voltage applied to V_{CC}. When the ZCD winding is switching, the voltage change across C1 over one period is:

$$\Delta V_{C1} = \frac{V_{OUT} - V_{CC}}{N_B : N_{ZCD}} \quad \text{(eq. 25)}$$

Therefore, the current available for charging V_{CC} is:

$$I_{AUX} = C1 \cdot f_{SW} \cdot \Delta V_{C1} = C1 \cdot f_{SW} \cdot \frac{V_{OUT} - V_{CC}}{N_B : N_{ZCD}} \quad \text{(eq. 26)}$$

For off line ac−dc applications which require PFC, a 2 stage approach is generally used. The first stage is the CRM boost PFC. This supplies the 2nd stage−−traditionally an isolated flyback or forward converter. This solution exhibit excellent performance at a low cost. However, during light load operations, the input current is low and the PFC stage is not necessary. In fact, leaving it on only degrades the efficiency of the system. Advanced controllers, such as the NCP1230 and NCP1381, detect this light load case and instruct the PFC to shut down (Figure 9). The NCP1607 is compatible with this type of topology, provided that the supplied V_{CC} is initially greater than the NCP1607's $V_{CC(on)}$ level.

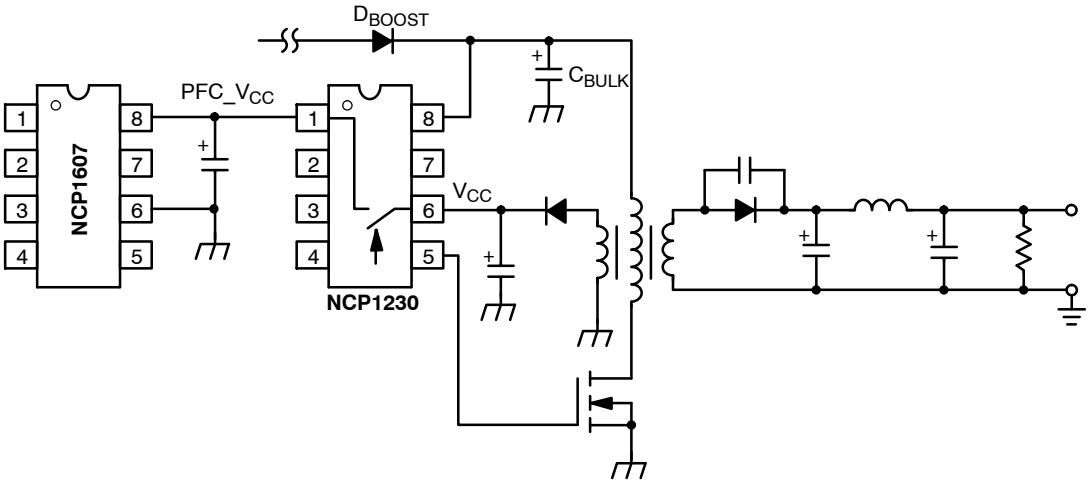

Figure 9. Using the SMPS Controller to Supply Power to the NCP1607

DESIGN STEP 8: Limit the Inrush Current

The sudden application of the mains to the PFC converter causes the circuit to experience an inrush current and a resonant voltage overshoot that is several times normal values. To resize the power components to handle this is cost prohibitive. Furthermore, the controller cannot do anything to protect against this. Turning on the boost switch makes the issue worse. There are two primary ways to solve this issue:

1. Startup Bypass Rectifier

A rectifier can be added from the input voltage to the output voltage (Figure 10). This bypasses the inductor and diverts the startup current directly to the bulk capacitor. The bulk capacitor is then charged to the peak ac line voltage without resonant overshoot and without excessive inductor current. After startup, D_{BYPASS} is reverse biased and does not interfere with the boost converter.

2. External Inrush Current Limiting Resistor

An NTC (negative temperature coefficient) thermistor in series with the boost inductor can limit the inrush current (Figure 11). The resistance value drops from a few ohms to a few milliohms as the device is heated by the I^2R power dissipation. Alternatively, this NTC can be placed in series with the boost diode. This improves the active efficiency as the resistor only conducts the output current instead of the input current. However, an NTC resistor may not be able to adequately protect the inductor and bulk capacitor against inrush current during a brief interruption of the mains, such as during line drop out and recovery.

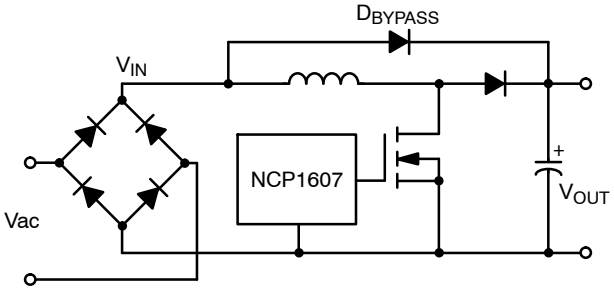

Figure 10. Use a Second Diode to Route the Inrush Current Away from the Inductor

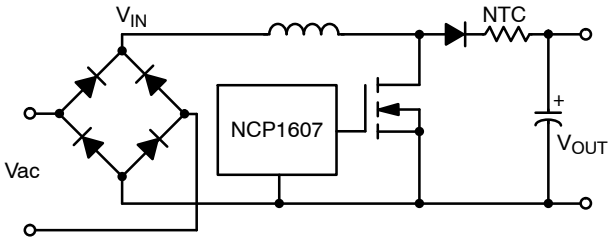

Figure 11. Use an NTC to Limit the Inrush Current Through the Inductor

DESIGN STEP 9: Develop the Compensation Network

As stated earlier, due to the natural output voltage ripple, the bandwidth of the PFC feedback loop is generally kept below 20 Hz. For a simple type 1 compensation network, only a capacitor is placed between FB and Control. The gain, G(s), of the feedback network is then given by:

$$G(s) = \frac{1}{s \cdot R_{OUT1} \cdot C_{COMP}} \qquad \text{(eq. 27)}$$

Therefore, the capacitor necessary to attenuate the bulk voltage ripple is given by:

$$C_{COMP} = \frac{10^{G/20}}{4 \cdot \pi \cdot f_{line} \cdot R_{OUT1}} \qquad \text{(eq. 28)}$$

where G is the attenuation level in dB (commonly 60 dB) and f_{line} is the minimum AC line frequency (47 Hz).

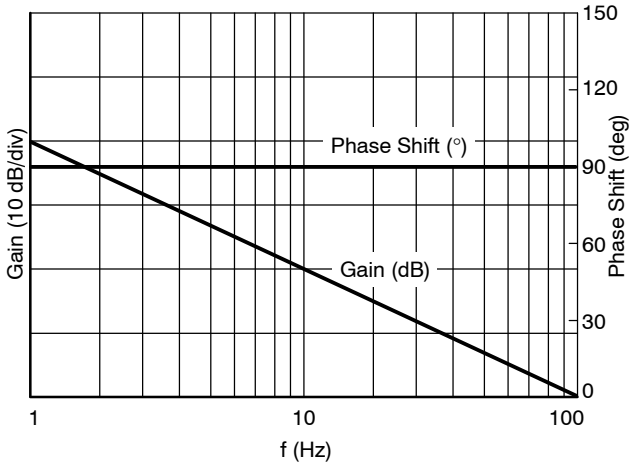

Figure 12. Gain and Phase for a Type 1 Feedback Network

As shown in Figure 12, a type 1 compensation network provides no phase boost to improve stability. For resistive loads, this may be sufficient (Figure 13). But for constant power loads, such as SMPS stages, the phase margin is reduced (Figure 14).

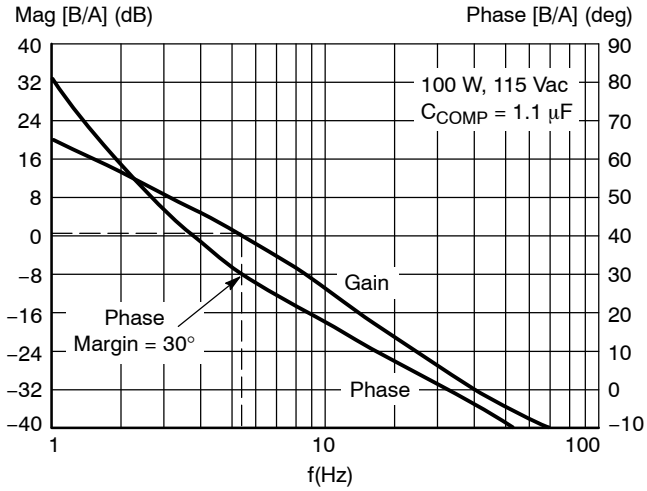

Figure 13. Boost demo board with a resistive load. Phase margin = 30 deg.

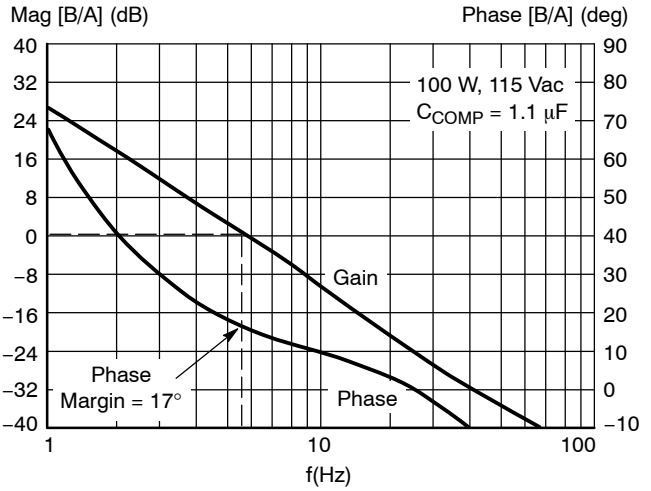

Figure 14. Boost demo board with a constant power load. Phase margin is reduced to 17 deg.

If greater system stability is required, then a type 2 compensation network is implemented. In this setup, a resistor and capacitor are placed in parallel with C_{COMP} (Figure 15).

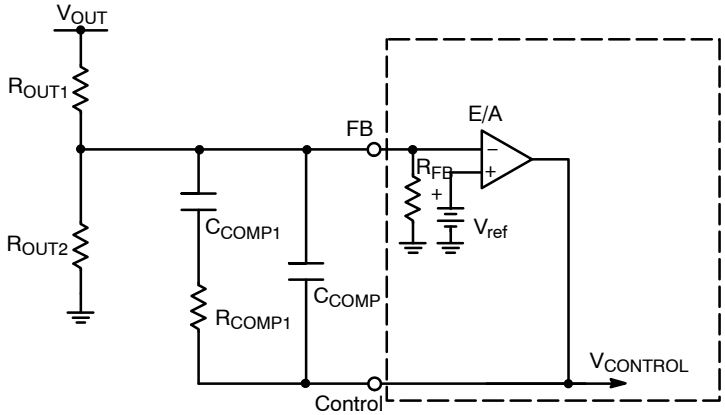

Figure 15. Type 2 compensation network

The transfer function for the type 2 error amplifier is now:

$$G(s) = \frac{1 + s \cdot R_{COMP1} \cdot C_{COMP1}}{s \cdot R_{OUT1} \cdot (C_{COMP} + C_{COMP1}) \cdot \left(1 + s \cdot R_{COMP1} \cdot \left(\frac{C_{COMP} \cdot C_{COMP1}}{C_{COMP} + C_{COMP1}}\right)\right)} \quad \text{(eq. 29)}$$

This gives a pole at 0 Hz, a zero at f_Z (eq 30), and another pole at f_P (eq 31).

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_{COMP1} \cdot C_{COMP1}} \quad \text{(eq. 30)}$$

$$f_P = f_Z \cdot \left(\frac{C_{COMP} + C_{COMP1}}{C_{COMP}}\right) \quad \text{(eq. 31)}$$

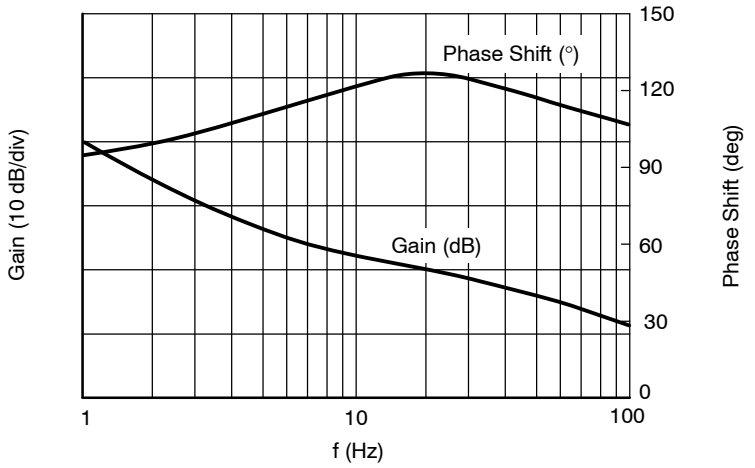

Figure 16. Representative Gain and Phase for a Type 2 Feedback Network. Note the Phase Boost

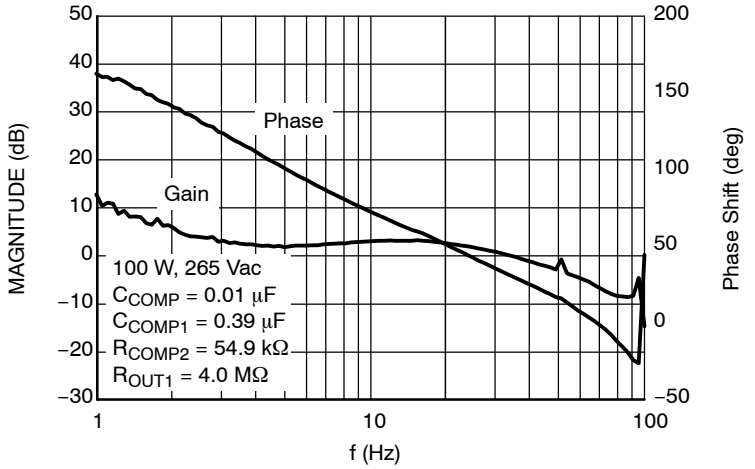

Figure 17. Improved Stability with a Type 2 Compensation Network. Phase Margin = 50 deg.

The poor stability observed with the type 1 compensation in Figure 14 improved (with the same total compensation capacitance) to Figure 17.

The phase margin and cross over frequency will change with the line voltage. Therefore, it is critical that any design has the gain−phase measured under all operating conditions. This is accomplished with a simple setup (Figure 18) and a network analyzer.

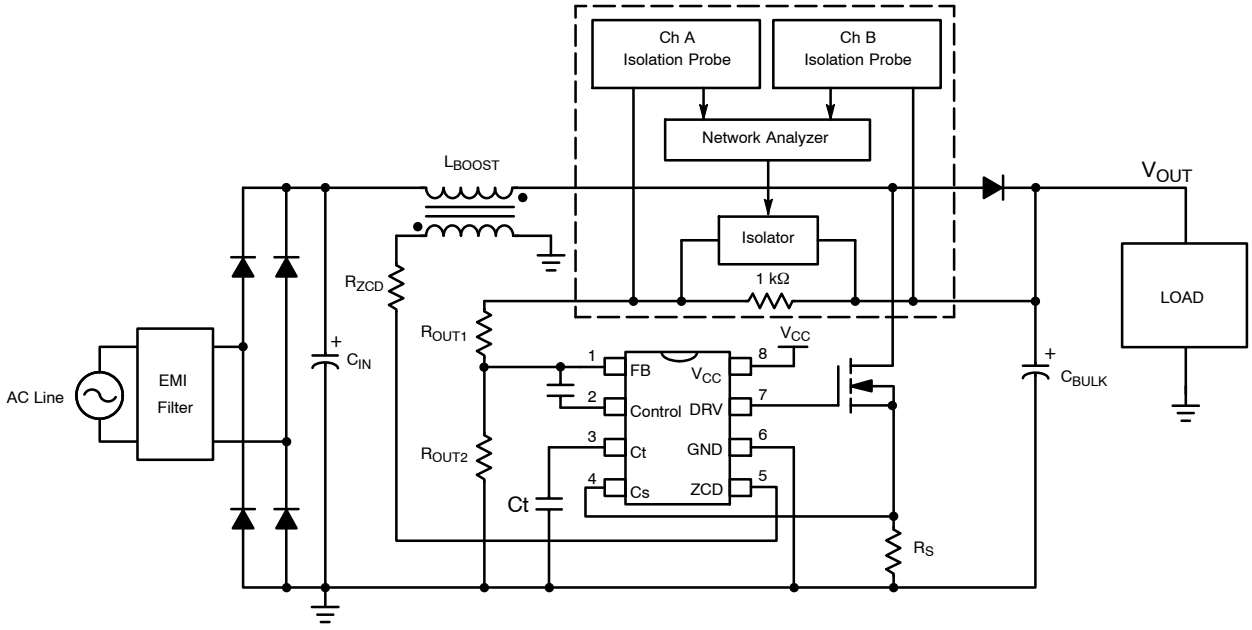

Figure 18. Gain−Phase Measurement Setup for Boost PFC Pre−converters

Simple Improvements for Additional THD Reduction

The NCP1607, with its constant on time architecture, provides a good deal of flexibility in optimizing each design. If further power factor performance is necessary, consider the following design guidelines.

1. Improve the THD/PF at Full Load by Increasing the On Time at the Zero Crossing:

One issue with CRM control is that at the zero crossing of the AC line, the voltage is not large enough to significantly charge the boost inductor during the fixed on time. Little energy is processed and some “zero crossover distortion” (Figure 19) is produced.

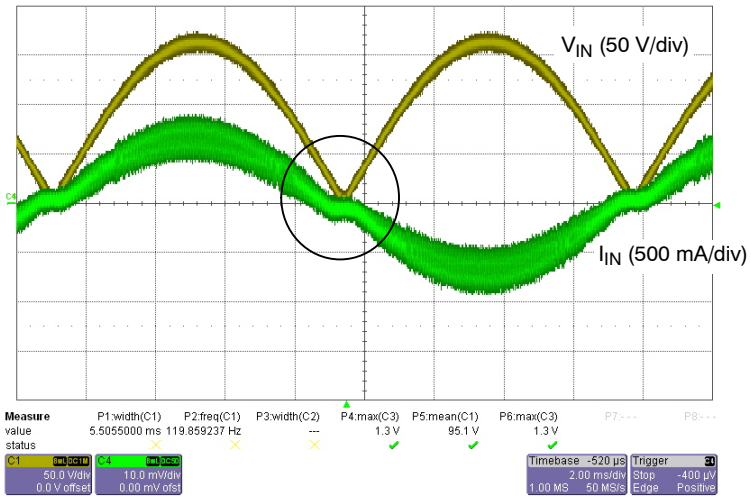

Figure 19. Zero Crossover Distortion

This raises the THD and lowers the lowers the PF of the pre−converter. To meet IEC1000 requirements, this is generally not an issue, as the NCP1607 delivers more than an ample reduction in current distortion. If improved THD or PF is required, then this zero crossover distortion can be reduced. The key is to increase the on time when the input voltage is low. This allows more time for the inductor to charge up and reduces the voltage level at which the distortion begins.

Fortunately, such a method is easy to implement on the NCP1607. If a resistor is connected from pin 3 (Ct) to the input voltage, then a current proportional to the instantaneous line voltage is injected into Ct (Figure 20). This current is higher at the peak of the line and has nearly no effect at low input voltages.

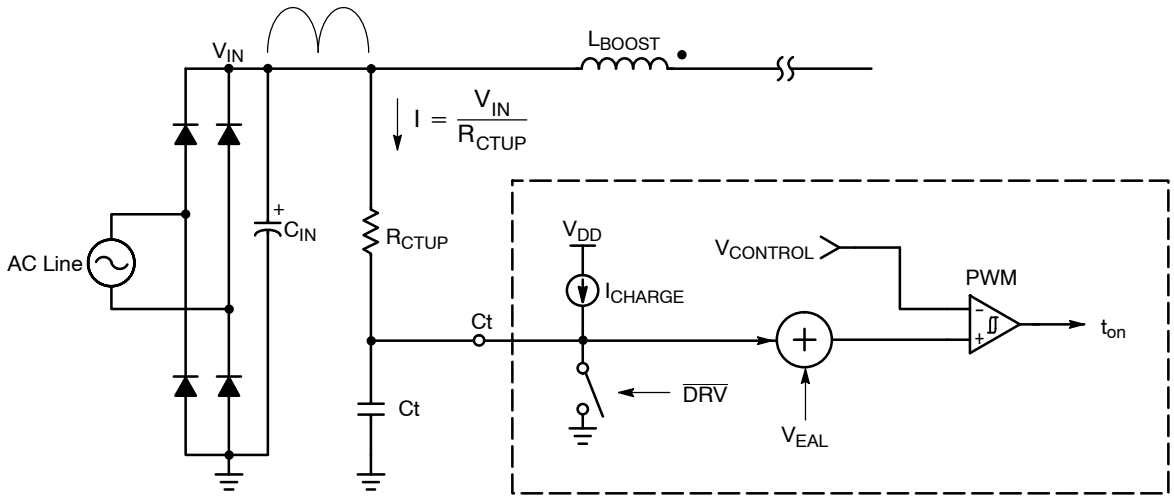

Figure 20. Add R_{CTUP} to Modify the On Time and Reduce the Zero Crossing Distortion

The Ct capacitor is increased in size so that the on time is longer near the zero crossing (Figure 21). This also reduces the frequency variation over the ac line cycle. The tradeoff to this approach is the increased no load power dissipation created by R_{CTUP}. The designer must balance the desired THD and PF performance with the no load power dissipation requirements.

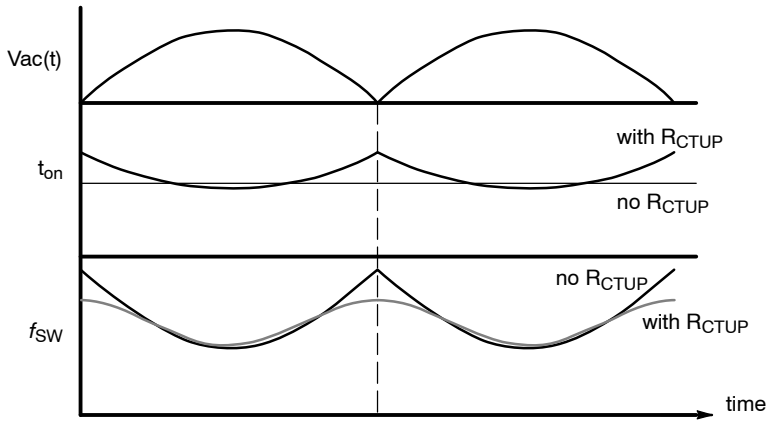

Figure 21. On Time and Switching Frequency With and Without R_{CTUP}

The effect of this resistor on THD and power factor is illustrated in Figure 22.

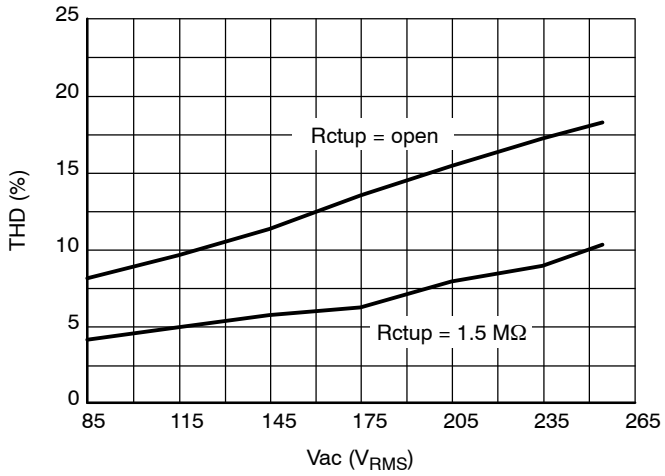

Figure 22. Effect of Rctup on Full Load (100 W) THD

2. Improve the THD/PF at Light Load or High Line:

If the required on time at light load or high line is less than the minimum on time, then the controller delivers too much power. This causes the control voltage to fall to its lowest level (V_{EAL}). The controller then disables the drive (static OVP) to prevent the output voltage from rising too high. Once the output drops lower, the control voltage rises and the cycle repeats. This adds to the distortion of the input current and output voltage ripple. There are two solutions to improve THD/PF at light load or high line:

1. Properly size the Ct capacitor. As mentioned above, the capacitor must be large enough to deliver the required on time at full load and low line. However, sizing it too large means that the range of control levels at light load or high line is reduced.
2. Compensate for propagation delays. If optimizing the Ct capacitor does not achieve the desired performance, then it may be necessary to compensate for the PWM propagation delay. When the Ct voltage exceeds the $V_{CONTROL}$ setpoint, the PWM comparator sends a signal to end the on time of the driver (Figure 23).

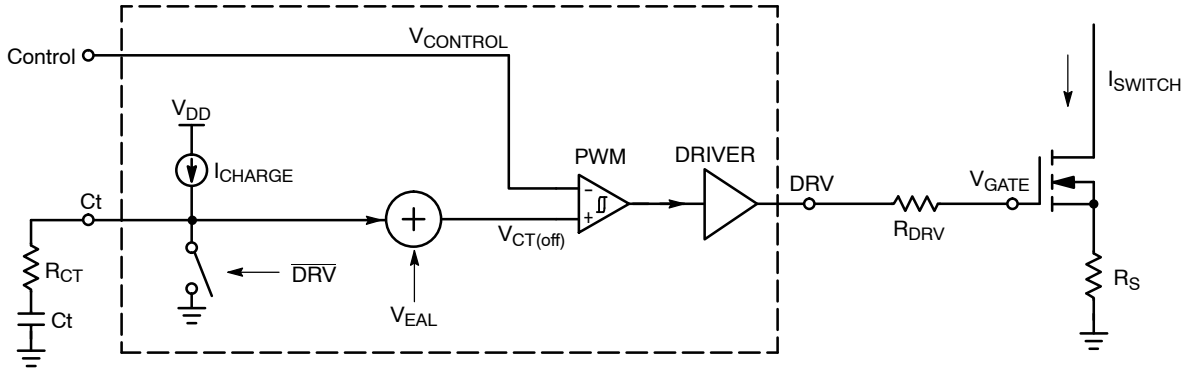

Figure 23. Block Diagram of the Propagation Delay Components

However, there is a delay before the MOSFET fully turns off. This delay is created by the propagation delay of the PWM comparator and the time to bring the MOSFET's gate voltage to zero (Figure 24).

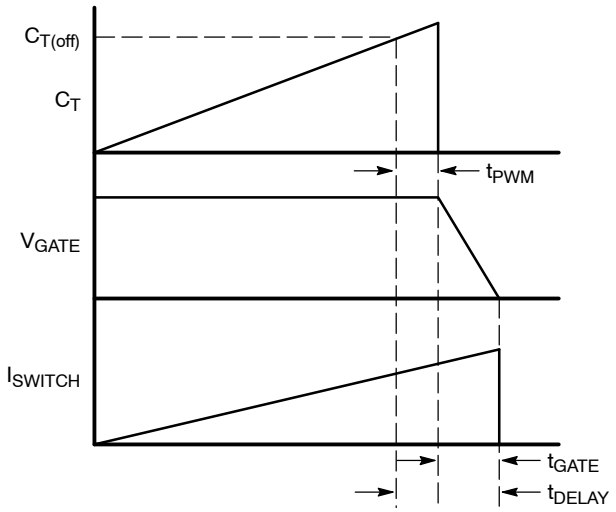

Figure 24. Driver Turn Off Propagation Delay

The total delay, t_{DELAY}, is summarized in eq 32:

$$t_{DELAY} = t_{PWM} + t_{GATE} \quad \text{(eq. 32)}$$

This delay adds to the effective on time of the controller. If a resistor (R_{CT}) is inserted in series with the Ct capacitor, then the total on time is reduced by:

$$\Delta t = Ct \cdot \frac{\Delta V_{RCT}}{\Delta I_{RCT}} = Ct \cdot R_{CT}$$

Therefore, to compensate for the propagation delay, R_{CT} is calculated using Equation 33:

$$R_{CT} = \frac{t_{DELAY}}{Ct} \quad \text{(eq. 33)}$$

The NCP1607 datasheet gives a typical t_{PWM} of 100 ns. The t_{GATE} delay is a function of the MOSFET's gate charge and the resistor "R_{DRV}." For this demo board, the gate delay is measured at about 150 ns. A value of R_{CT} = 300 Ω is sufficient to compensate for the propagation delays. This improves PF and THD. At light load and high line (Figure 25).

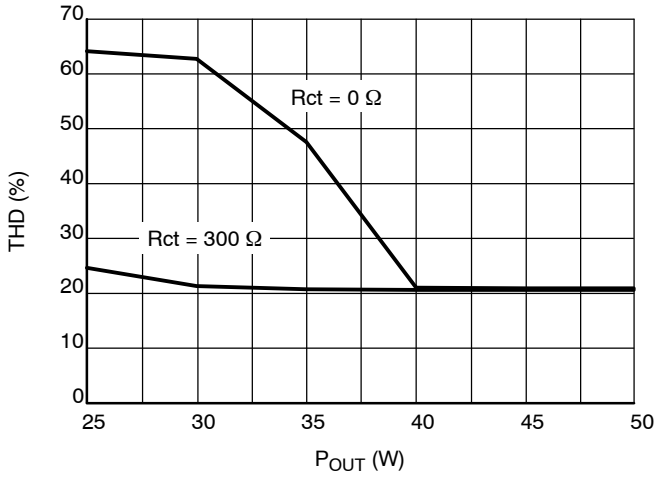

Figure 25. Effect of Rct on Light Load THD at 265 Vac / 50 Hz (Rctup = open)

Design Results

The completed demo board schematic using the NCP1607 is shown in Figure 26.

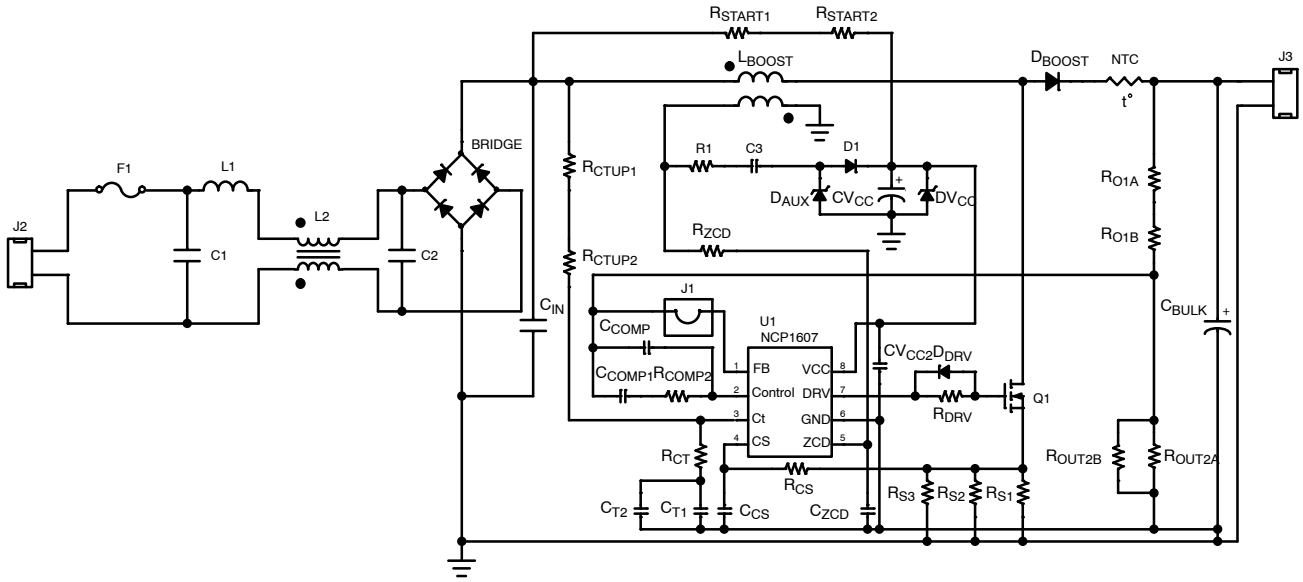

Figure 26. 100 W PFC Pre−Converter Using the NCP1607

The bill of materials (BOM) and layout drawings are shown in Appendix 1 and 2, respectively. This pre−converter exhibits excellent THD (Figures 27 and 28), PF (Figure 29), and efficiency (Figure 30).

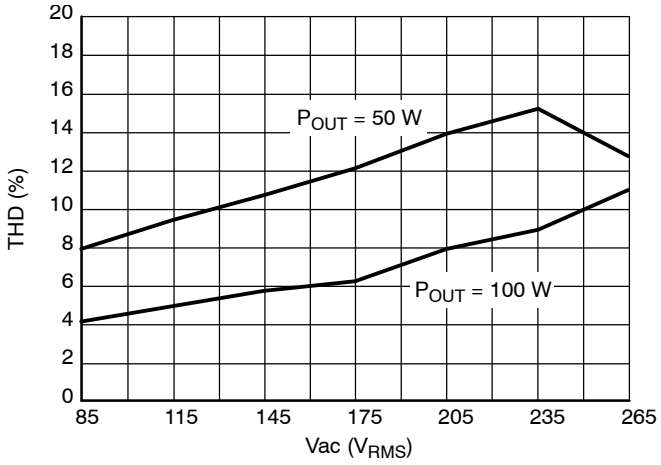

Figure 27. THD vs. Input Voltage at Full Load and 50% Load

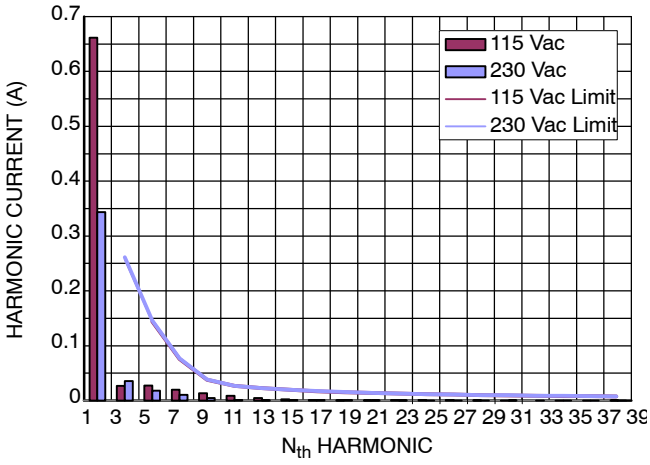

Figure 28. Individual Harmonic Current at 115 Vac and 230 Vac

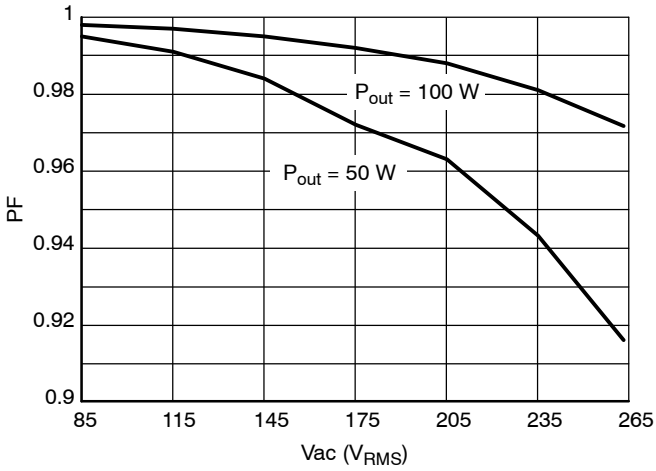

Figure 29. PF vs. Input Voltage at Full Load and 50% Load

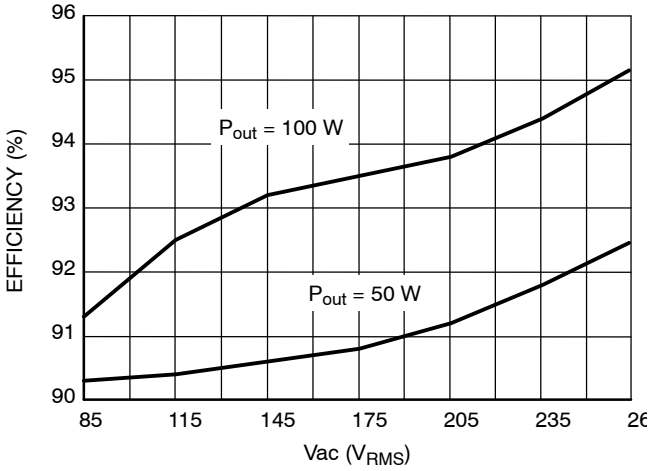

Figure 30. Efficiency vs. Input Voltage at Full Load and 50% Load

The input current and resultant output voltage ripple is shown in Figure 31. The overvoltage protection scheme can be observed by starting up the pre−converter with a light load on the output (Figure 32). The OVP activates at about 440 V and restarts at about 410 V.

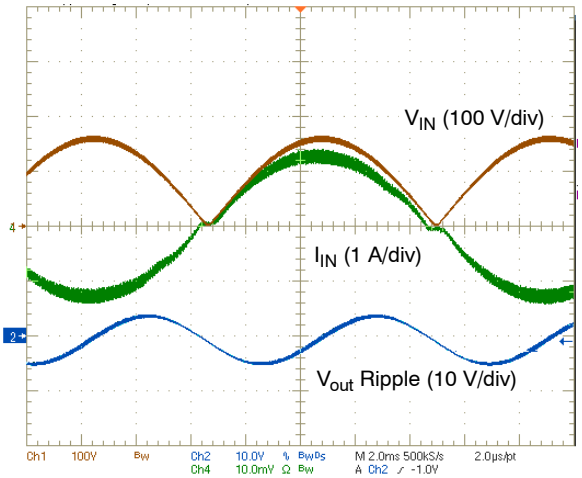

Figure 31. Full Load Input Current at 115 Vac/60 Hz

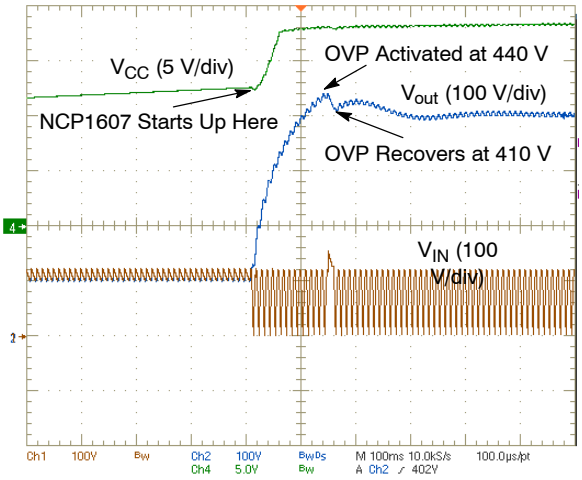

Figure 32. Startup Transient Showing OVP Activation and Recovery

FPP Jumper

This demo board is equipped with a jumper between Pin 1 of the controller and the feedback network to demonstrate the FPP feature of the NCP1607. If the jumper is removed prior to applying input power, the drive is disabled (Figures

33, 34). If the jumper is removed at any time during operation, the drive is disabled within 1 ms (Figures 35, 36). This jumper is for FPP demonstration only and is not required in the end application.

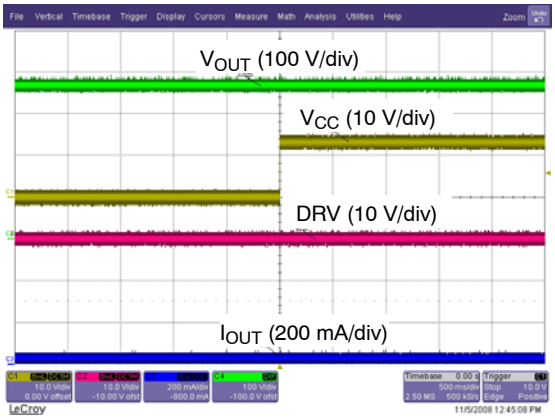

Figure 33. Startup with Jumper Removed at 265 Vac/50 Hz, I_{OUT} = 0 mA, V_{CC} = 13 V, and T_J = −40°C

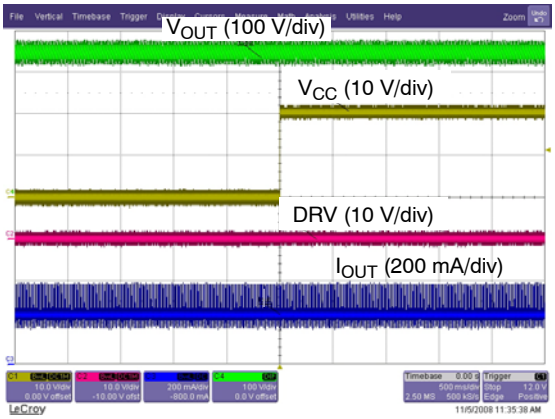

Figure 34. Startup with Jumper Removed at 265 Vac/50 Hz, I_{OUT} = 250 mA, V_{CC} = 20 V, and T_J = −40°C

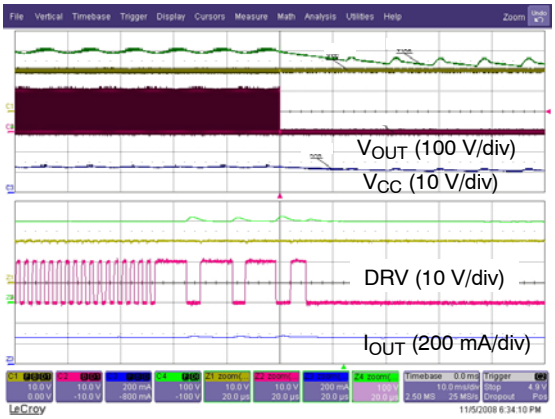

Figure 35. Removing Jumper During Operation at 265 Vac/50 Hz, I_{OUT} = 250 mA, V_{CC} = 20 V, and T_J = −40°C

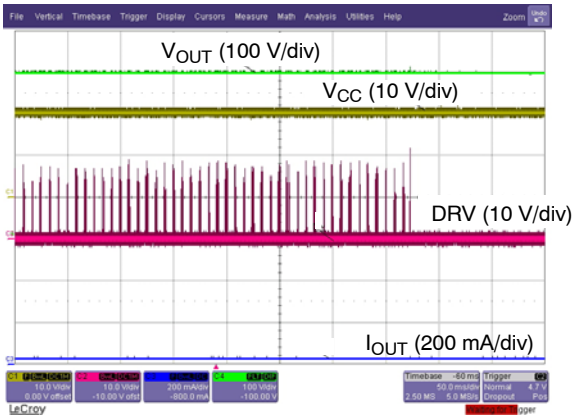

Figure 36. Removing Jumper During Operation at 265 Vac/50 Hz, I_{OUT} = 0 mA, V_{CC} = 13 V, and T_J = −40°C

This demo board can be configured in a variety of ways to optimize performance. Table 2 shows results of a few of these configurations.

Table 2. Summary of key parameters for different variations of the demo board.

RCTUP	Ct	Shutdown (V_{ZCD} = 0 V) Pdiss @ 265 Vac	Efficiency @ 100 W		THD @ 100 W	
			115 Vac 60 Hz	230 Vac 50 Hz	115 Vac 60 Hz	230 Vac 50 Hz
open	1.5 nF	225 mW	92.5%	94.6%	9.5%	16.7%
1.5 MEG	1.8 nF	295 mW	92.5%	94.4%	4.9%	8.9%

Safety Concerns

Since the FPP feature is only intended to protect the circuit in the case of a floating FB pin, care must be taken when removing the jumper. **Do not attach any wires to the jumper pins with the jumper removed.** Doing so injects noise into the FB pin and prevents the correct operation of FPP thus causing maximum power to be delivered to the output. This can cause C_{BULK} to vent. **Always wear proper eye protection when the jumper is removed.**

The jumper is located next to several high-voltage components. Do not remove the jumper during operation with bare fingers or non-insulated metal tools.

Layout Considerations

As with many switching power supplies, careful consideration must be given to the placement of critical components during layout. Noise from the high peak currents of the main power switch are easily coupled into sensitive inputs of the NCP1607. To reduce this noise, be sure to follow these guidelines:

1. Locate critical components as physically close to the controller as possible with the following priority:
   a. Ct capacitor
   b. V_{CC} Decoupling Capacitor
   c. Other Compensation Components
2. Minimize the length of all signal traces.
3. Locate R_S adjacent to the source pin of Q1.
4. Locate the ground connections for C_{IN}, BRIDGE, R_S, and C_{BULK} as close together as possible.
5. Add decoupling capacitors to the ZCD and CS pin if needed.
   a. If a capacitor is added to these pins, R_{ZCD} and R_{CS} may need to be adjusted to ensure proper timing.
   d. Although the demo board does not require C_{ZCD} and C_{CS}, it contains unpopulated footprints for both so that the user may add them if needed.

Appendix 1: Bill of Materials (BOM)

Designator	Qty	Description	Value	Tolerance	Foot−Print	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
U1	1	NCP1607	NCP1607	−	SOIC−8	ON Semiconductor	NCP1607BDR2G	No	Yes
D1	1	Diode, General Purpose	100 V	−	SOD123	ON Semiconductor	MMSD4148T1G	No	Yes
DAUX	1	Diode, Zener	18 V	−	SOD123	ON Semiconductor	MMSZ4705T1G	No	Yes
DBOOST	1	Diode, Ultrafast	4 A, 600 V	−	Axial	ON Semiconductor	MUR460RLG	No	Yes
BRIDGE	1	Diode, Bridge Rectifier	4A, 600 V	−	KBL	Vishay	KBL06−E4/51	Yes	Yes
DVCC, DDRV	2	Diode, General Purpose	open	−	SOD123	−	−	−	−
F1	1	Fuse, SMD	2 A, 600 V	−	SMD	Littelfuse	0461002.ER	Yes	Yes
LBOOST	1	Inductor, Boost, Nboost:Nzcd = 10:1	400 μH, 10:1	−	Custom	Coilcraft	FA2890−CL	No	Yes
L1	1	Inductor, Radial	180 uH	10%	Through Hole	Coilcraft	PCV−2−184−05L	No	Yes
L2	1	Inductor, Common−Mode Choke	4.7 mH, 2.7 A	−	Through Hole	Panasonic	ELF−20N027A	Yes	Yes
Q1	1	MOSFET, N−Channel	11.6 A, 560 V	−	TO−220	Infineon	SPP12N50C3	Yes	Yes
NTC	1	Thermistor, Inrush Current Limiter	4.7 Ω	20%	Radial	EPCOS	B57238S479M	Yes	Yes
RCOMP1	1	Resistor, SMD	54.9 kΩ	1%	1206	Yageo	RC1206FR−0754K9L	Yes	Yes
R1	1	Resistor, SMD	100 Ω	1%	1206	Yageo	RC1206FR−07100RL	Yes	Yes
RCT	1	Resistor, SMD	0 Ω	1%	1206	Yageo	RC1206FR−070RL	Yes	Yes
RDRV	1	Resistor, SMD	10.0 Ω	1%	1206	Yageo	RC1206FR−0710RL	Yes	Yes
ROUT2A	1	Resistor, SMD	25.5 kΩ	1%	1206	Yageo	RC1206FR−0725K5L	Yes	Yes
RO1A,RO1B	2	Resistor, SMD	2.00 MΩ	1%	1206	Yageo	RC1206FR−072ML	Yes	Yes
RS1	1	Resistor, SMD	0.100 Ω, 1 W	1%	2512	KOA	SR733ATTER100F	Yes	Yes
RS2,RS3	2	Resistor, SMD	open	−	2512	−	−	−	−
ROUT2B	1	Resistor, SMD	open	−	1206	−	−	−	−
RCS	1	Resistor, 1/4 W Axial	510 Ω	5%	Axial	Yageo	CFR−25JB−510R	Yes	Yes
RCTUP1, RCTUP2	2	Resistor, 1/4 W Axial	750 kΩ	5%	Axial	Yageo	CFR−25JB−750K	Yes	Yes
RZCD	1	Resistor, 1/4 W Axial	51 kΩ	5%	Axial	Yageo	CFR−25JB−51K	Yes	Yes
RSTART1, RSTART2	2	Resistor, 1/4 W Axial	330 kΩ	5%	Axial	Yageo	CFR−25JB−330K	Yes	Yes
C1,C2	2	X Capacitor	0.47u	20%	Radial	EPCOS	B32923C3474M	Yes	Yes
CIN	1	X Capacitor	0.1u	20%	Radial	EPCOS	B32921A2104M	Yes	Yes
CVCC	1	Capacitor, Electrolytic	47 uF, 25 V	20%	Radial	Panasonic	EEU−FC1E470	Yes	Yes

Appendix 1: Bill of Materials (BOM)

Designator	Qty	Description	Value	Tolerance	Foot−Print	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free
CBULK	1	Capacitor, Electrolytic	68 μF, 450 V	20%	Radial	NCC	EKXG451ELL680MM N3S	Yes	Yes
CVCC2,CCOMP	2	Capacitor, Ceramic, SMD	0.1 μF, 25 V	10%	1206	Vishay	VJ1206Y104KXX	Yes	Yes
CCOMP1	1	Capacitor, Ceramic, SMD	0.39 μF, 25 V	10%	1206	Vishay	VJ1206Y394KXX	Yes	Yes
CT1	1	Capacitor, Ceramic, SMD	1.5 nF, 25 V	10%	1206	Vishay	VJ1206Y152KXX	Yes	Yes
CT2	1	Capacitor, Ceramic, SMD	330 pF, 25 V	10%	1206	Vishay	VJ1206Y331KXX	Yes	Yes
C3	1	Capacitor, Ceramic, SMD	22 nF, 25 V	10%	1206	Vishay	VJ1206Y223KXX	Yes	Yes
CZCD,CCS	2	Capacitor, Ceramic, SMD	open	−	1206	−	−	−	−
J1	1	Header	1 Row of 3, 1 Row of 2	−	2.54 mm	3M	929400−01−36	Yes	Yes
J2,J3	2	Connector, 156 mil 3 pin	−	−	156 mil	MOLEX	26−60−4030	Yes	Yes
MECHANICAL	1	Jumper, Shorting	−	−	−	3M	929955−06	Yes	Yes
MECHANICAL	1	Heatsink	−	−	TO220	Aavid	590302B03600	Yes	Yes
MECHANICAL	1	Screw	4−40 1/4" screw	−	−	Building Fasteners	PMSSS 440 0025 PH	Yes	Yes
MECHANICAL	1	Nut	4−40 screw nut	−	−	Building Fasteners	HNSS440	Yes	Yes
MECHANICAL	1	Nylon Washer	Shoulder washer #4	−	−	Keystone	3049	Yes	Yes
MECHANICAL	1	TO220 Thermal Pad	9 mil	−	−	Wakefield	173−9−240P	Yes	Yes
MECHANICAL	4	Standoffs	Hex 4−40, Nylon 0.75"	−	−	Keystone	4804K	Yes	Yes
MECHANICAL	4	Nylon Nut	Hex 4−40	−	−	Building Fasteners	NY HN 440	Yes	Yes

Appendix 2: Layout Drawings

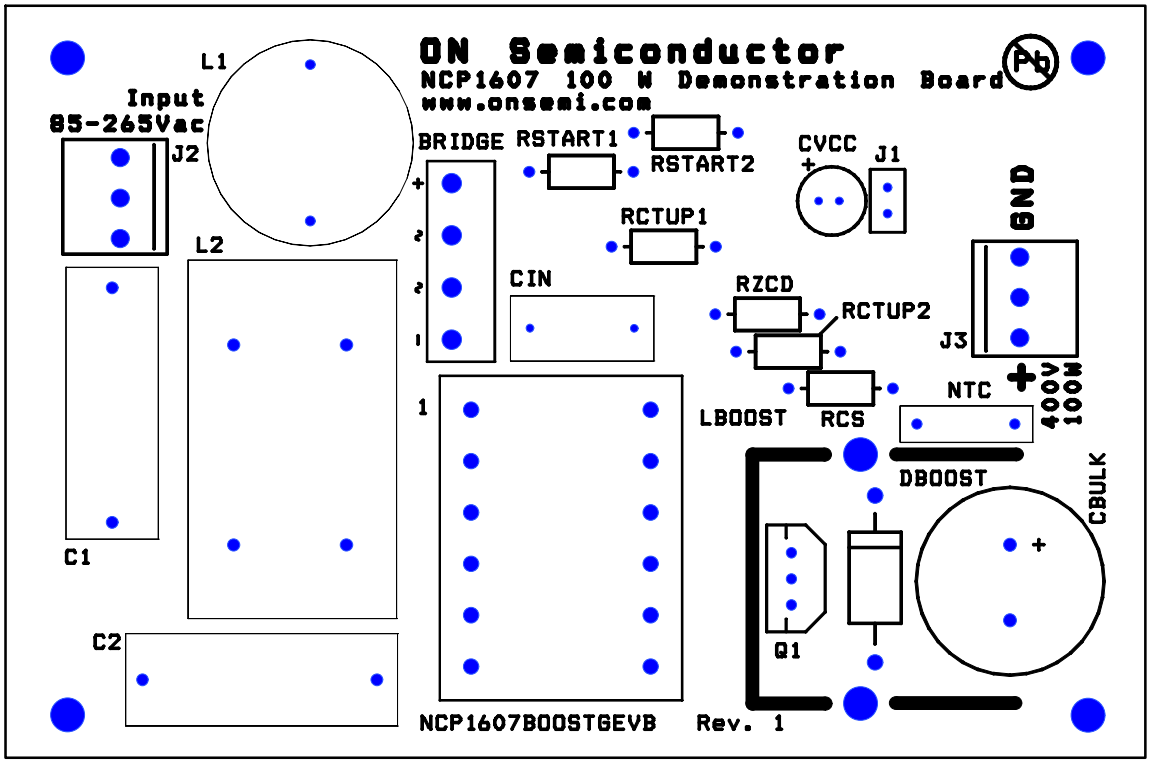

Figure 38. Top View of 100 W Board Layout

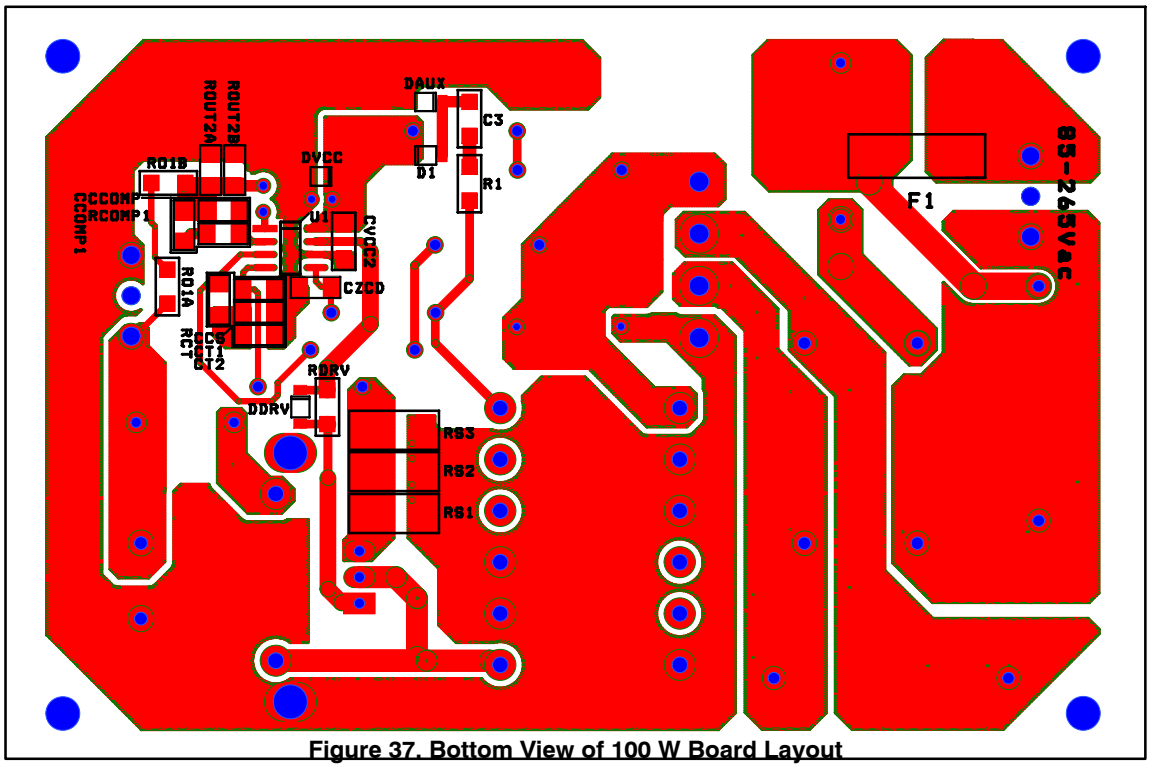

Figure 37. Bottom View of 100 W Board Layout

Appendix 3: Summary of Boost Equations for the NCP1607

RMS Input Current	$I_{ac} = \frac{P_{OUT}}{\eta \cdot V_{ac}}$	η (the efficiency of only the Boost PFC stage) is generally in the range of 90 – 95%
Maximum Inductor Peak Current	$I_{pk(MAX)} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{\eta \cdot Vac_{LL}}$	Where Vac_{LL} is the minimum line input voltage. $I_{pk(MAX)}$ occurs at the lowest line voltage.
Inductor Value	$L \leq \frac{2 \cdot Vac^2 \cdot \left(\frac{V_{OUT}}{\sqrt{2}} - Vac\right)}{V_{OUT} \cdot Vac \cdot I_{pk(MAX)} \cdot f_{SW(MIN)}}$	$f_{SW(MIN)}$ is the minimum desired switching frequency. The maximum L must be calculated at low line and high line.
Maximum On Time	$t_{on(MAX)} = \frac{2 \cdot L \cdot P_{OUT}}{\eta \cdot Vac_{LL}^2}$	The maximum on time occurs at the lowest line voltage and maximum output power.
Off Time	$t_{off} = \frac{t_{on}}{\frac{V_{OUT}}{Vac \cdot \lvert\sin(\theta)\rvert \cdot \sqrt{2}} - 1}$	The off time is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.
Frequency	$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L \cdot P_{OUT}} \cdot \left(1 - \frac{Vac \cdot \lvert\sin\theta\rvert \cdot \sqrt{2}}{V_{OUT}}\right)$	
Pin 3 Capacitor	$Ct \geq \frac{2 \cdot P_{OUT} \cdot L \cdot I_{CHARGE}}{\eta \cdot Vac^2 \cdot V_{CTMAX}}$	I_{CHART} and V_{CTMAX} are given in the NCP1607 specification table.
Boost Turns to ZCD Turns Ratio	$N_B : N_{ZCD} \leq \frac{V_{OUT} - Vac_{HL} \cdot \sqrt{2}}{V_{ZCDH}}$	Where V_{acHL} is the maximum line input voltage. The turns ratio must be low enough so as to trigger the ZCD comparators at high line.
Resistor from ZCD winding to the ZCD pin (pin 5)	$R_{ZCD} \geq \frac{Vac_{HL} \cdot \sqrt{2}}{I_{CL(NEG)} \cdot (N_B : N_{ZCD})}$	R_{ZCD} must be large enough so that the shutdown comparator is not inadvertently activated.
Boost Output Voltage	$V_{OUT} = V_{REF} \cdot \frac{R_{OUT1} + R_{EQ}}{R_{EQ}}$ $R_{EQ} = \frac{R_{OUT2} \cdot R_{FB}}{R_{OUT2} + R_{FB}}$	
Maximum V_{OUT} voltage prior to OVP activation and the necessary R_{OUT1} and R_{OUT2}.	$V_{OUT(OVP)} = V_{OUT} + R_{OUT1} \cdot I_{OVP}$ $R_{OUT1} = \frac{V_{OUT(OVP)} - V_{OUT}}{I_{OVP}}$ $R_{EQ} = R_{OUT1} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$ $R_{OUT2} = \frac{R_{EQ} + R_{FB}}{R_{FB} - R_{EQ}}$	I_{OVP} is given in the NCP1607 specification table.
Minimum output voltage necessary to exit undervoltage protection (UVP)	$V_{OUT(UVP)} = \frac{R_{OUT1} + R_{EQ}}{R_{EQ}} \cdot V_{UVP}$	V_{UVP} is given in the NCP1607 specification table.
Bulk Cap Ripple	$V_{ripple(pk-pk)} = \frac{P_{OUT}}{C_{BULK} \cdot 2 \cdot \pi \cdot f_{line} \cdot V_{OUT}}$	Use f_{line} = 47 Hz for worst case at universal lines. The ripple must not exceed the OVP level for V_{OUT}.
Inductor RMS Current	$I_{L(RMS)} = \frac{2 \cdot P_{OUT}}{\sqrt{3} \cdot Vac_{LL} \cdot \eta}$	
Boost Diode RMS Current	$I_{D(RMS)MAX} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot \sqrt{2}}{\pi}} \cdot \frac{P_{OUT}}{\eta \cdot \sqrt{Vac_{LL} \cdot V_{OUT}}}$	

Appendix 3: Summary of Boost Equations for the NCP1607

MOSFET RMS Current	$I_{M(RMS)MAX} = \frac{2}{3} \cdot \frac{P_{OUT}}{\eta \cdot Vac_{LL}^{2}} \cdot \sqrt{1 - \left(\frac{8 \cdot \sqrt{2} \cdot Vac_{LL}}{3 \cdot \pi \cdot V_{OUT}}\right)}$	
MOSFET Sense Resistor	$R_S = \frac{V_{CS(limit)}}{I_{pk(MAX)}}$ $P_{RS} = I_{M(RMS)}^{2} \cdot R_S$	$V_{CS(limit)}$ is given in the NCP1607 specification table.
Bulk Capacitor RMS Current	$I_{C(RMS)MAX} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{OUT}^{2}}{9 \cdot \pi \cdot Vac_{LL} \cdot V_{OUT} \cdot \eta^{2}} - (I_{LOAD(RMS)})^{2}}$	
C_{COMP} for Type 1	$C_{COMP} = \frac{10^{G/20}}{4 \cdot \pi \cdot f_{line} \cdot R_{OUT1}}$	G is the desired attenuation in decibels (dB). Typically it is 60 dB.

The product described herein (NCP1607), may be covered by the following U.S. patents: 5,073,850 and 6,362,067. There may be other patents pending.

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