AN1751
APPLICATION NOTE

EMI Filters: Recommendations and measurements

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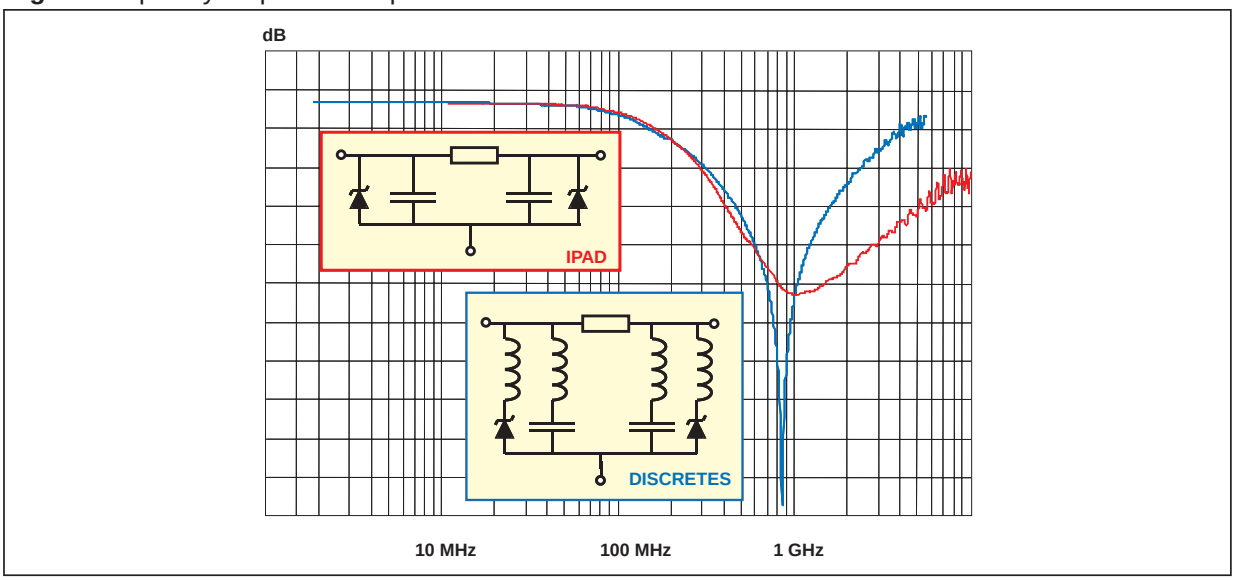
With the development of wireless telecommunications, consumer products and cellular phones are subjected to Radio Frequency Interference and may generate ElectroMagnetic Interference. This is in addition to ElectroStatic Discharge the user can apply when touching a connector like a bottom connector on a cellular phone.
In the past, filtering was achieved by discrete devices (capacitors, resistors) and ESD protection was done by discretes diodes. Cellular phone size drop and enhanced features require faster signals and more and more integrated devices which are becoming very sensitive to ESD or EMI/RFI.

Discretes devices impose a well designed layout to minimize parasitic effect of PCB inductances while Integrated Passive and Active Devices suppress most of these inductances due to very short tracks between passives on the die itself.

Fig. 1: Frequency response comparison between discrete and IPAD™ filter.



Discrete filter will behave like a rejection filter but the rejection frequency will be depending on parasitic inductances while the IPAD filter will act like a low pass filter.

EMIF filters have three main functions, the first is of course to filter EMI/RFI, the second is to protect inputs and outputs against ESD and the third one is to transmit data from inputs to outputs. EMIF datasheets provide data and curve measured in specific conditions. The goal of this note is to explain test conditions for EMIF devices.

1-Frequency response

EMIF target is to pass low frequency signals and to reject frequency higher than 800MHz especially 900MHz, 1.8 and 2.4GHz.

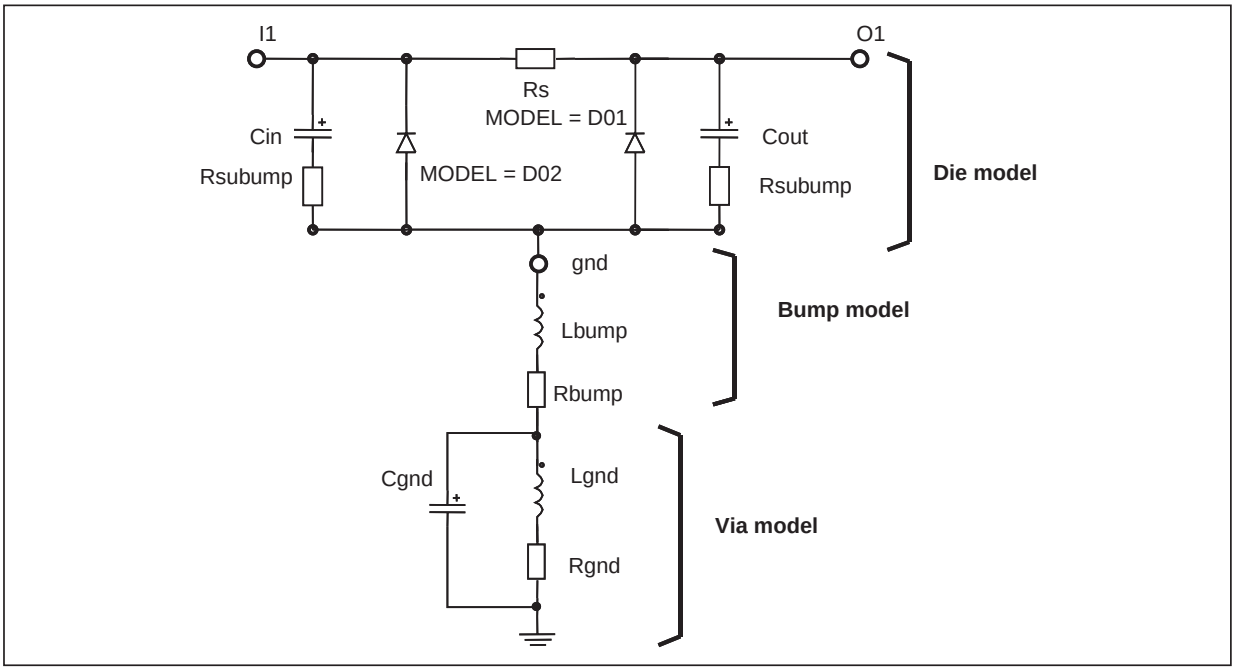
Attenuation curve provided in specification shows :

- Simulation thanks to the Aplac (or P-Spice) tool. This is done before the die design to be sure the device will fit customer requirements
- Measurement done on demonstration board.

Aplac models take into account of die, bumps and via for the ground connections. It does not consider PCB track in the application.

Figure 2 represents an example of Aplac model for one filtering cell.

Fig. 2: Aplac model for die, bumps and PCB via.



P-Spice is probably the most wellknown simulation software in electronic industry. Limits of P-Spice is reached when trying to simulate RF signals because of the time it takes for each simulation. It is also impossible to simulate crosstalk phenomena. Aplac has been developed to avoid all these P-Spice limitations.

Concerning measurements, the first step is to calibrate the equipment. This is why demoboards are delivered with a calibration kit shown in *figure 3* while the IPAD™ device is on another board (*figure 4*).

Fig. 3: Calibration board.

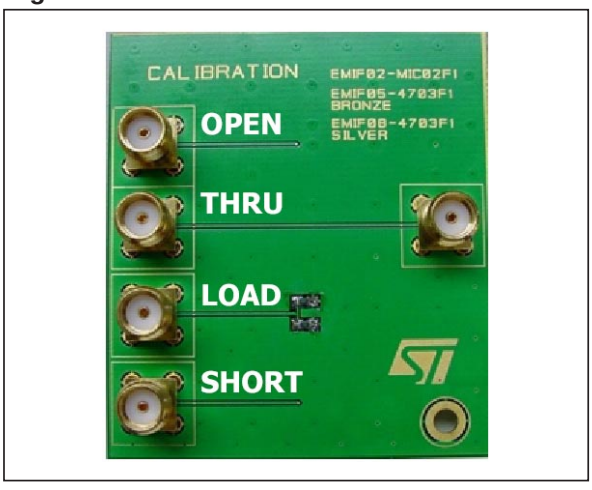
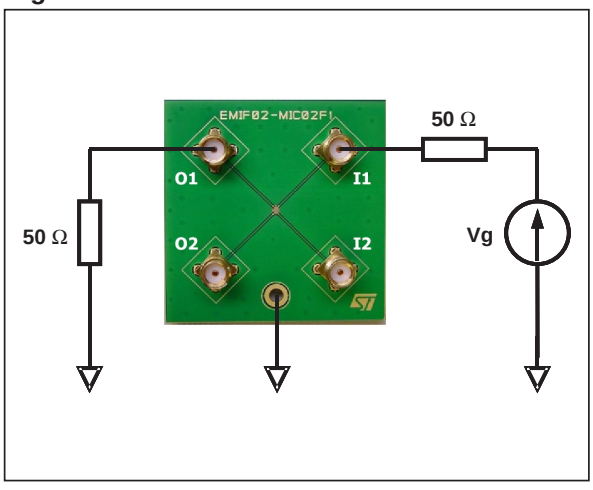


Fig. 4: Measurement condition on demoboard.

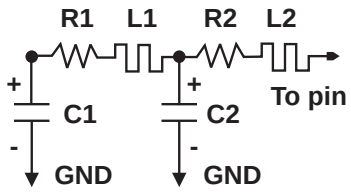


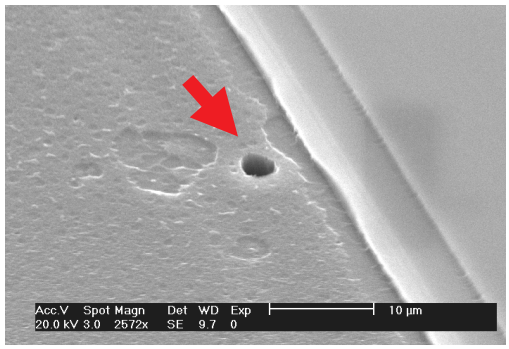
If test equipment is not calibrated, non negligible error can occur as the attenuation measurement will correspond to the one of the IPAD™ + board + connections. Furthermore measurement is done with a 50 Ω load while some applications may have other impedances.

2- ESD and latch-up measurements

I/O lines of a cellular phone must be protected against ESD. Most popular ESD standard is the IEC61000-4-2 having a surge generator defined in *figure 5*.

Fig. 5: IEC61000-4-2 generator and the result on a non protected integrated circuit die.





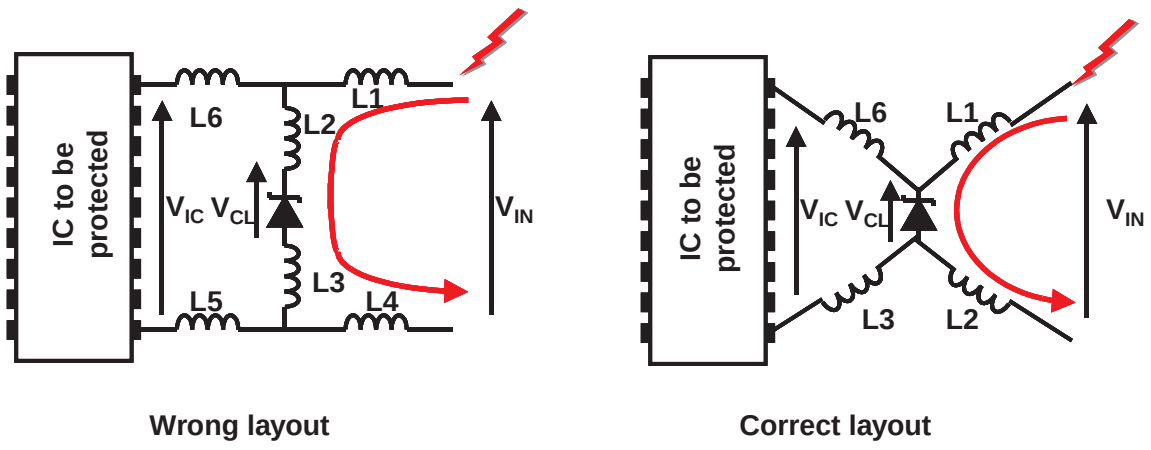
IEC61000-4-2 specifies C1 charged up to 8kV (contact) and 15kV (air discharge). The MIL-STD 883E Method 3015.7 is also a reference.

All external pins (bottom connectors, microphone jack…) may be subjected to these kinds of surges. If no protection is used, result will be the destruction of the internal silicon chip. Destroyed I/O is generally a short circuit as silicon melt on a very small area as shown in *figure 5*.

If ESD protection device is the minimun to prevent failure, layout is also very important as very high dI/dt of surge will generate a high LdI/dt.

This means even with a protection device, an integrated circuit can be destroyed because of layout problem. *Figure 6* explains differences between 2 layouts.

Fig. 6: Two layouts for two very different results.



Knowing all PCB tracks are equivalent to an inductance, in the first case the IC will see a voltage:
$V_{IC} = (L1+L2+L3+L4) \times dI/dt + V_{CL}$

With a track lengh, for protection device connection, of 2 cm (1cm from side to side), 35µ thickness, 0.5mm wide (microstrip track) then L2+L3 = 8nH

Considering a 15kV ESD surge surge having dI/dt = 50A/0.7ns

The result is V_{IC} = 570V

Overvoltage being directly linked to track lengh, voltage across IC may be much higher with few more centimeters. Most of IC will not like it.

With the correct layout, no high current is flowing through L6 and L3, then $V_{IC} = V_{CL}$
In the first case, IC can be destroyed while with the second layout IC is perfectly protected.

Figure 7 gives input and output voltages of an EMI filter with the suitable layout. The demoboard shows the ESD is applied on input (V_{IN}), while EMIF output (V_{OUT}) is connected to the IC to be protected.

Fig. 7: ESD demoboard and measurements on EMIF10-1K010F1.

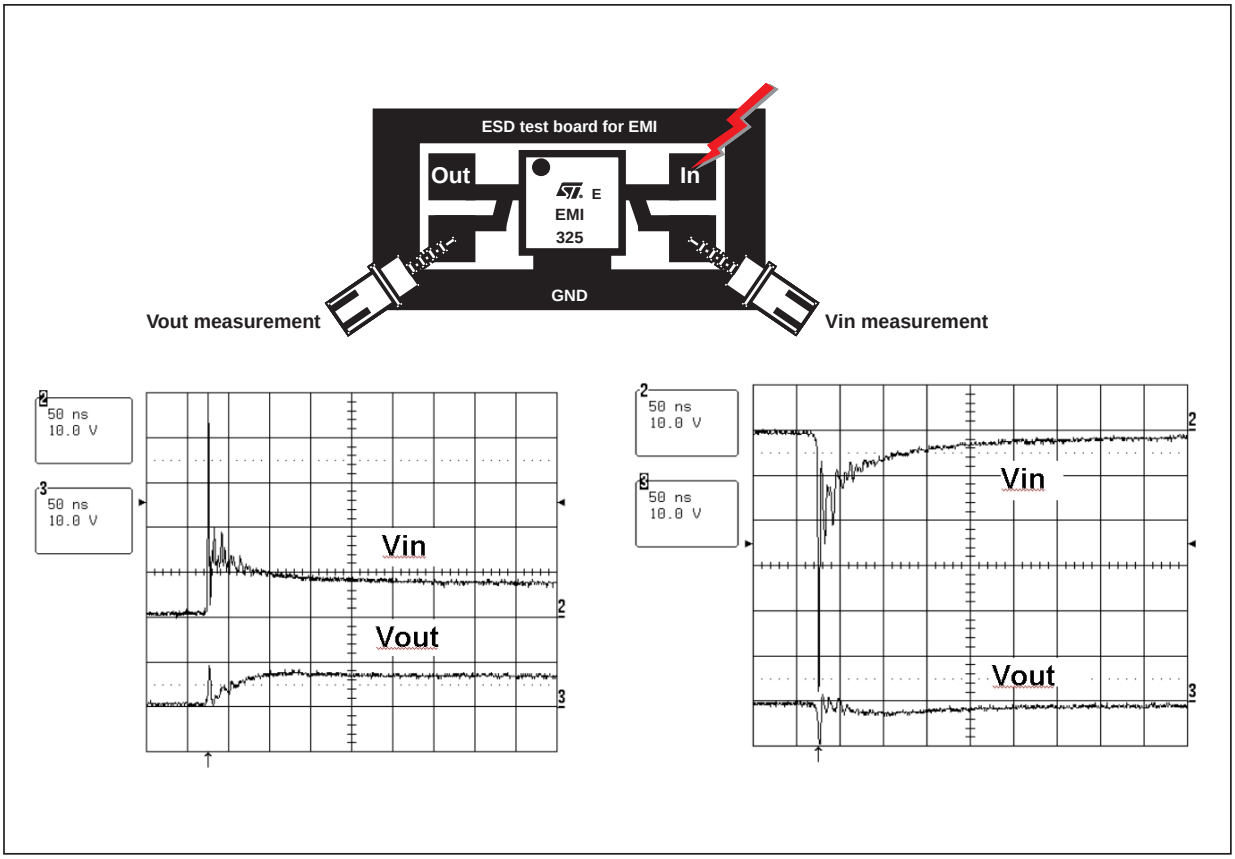
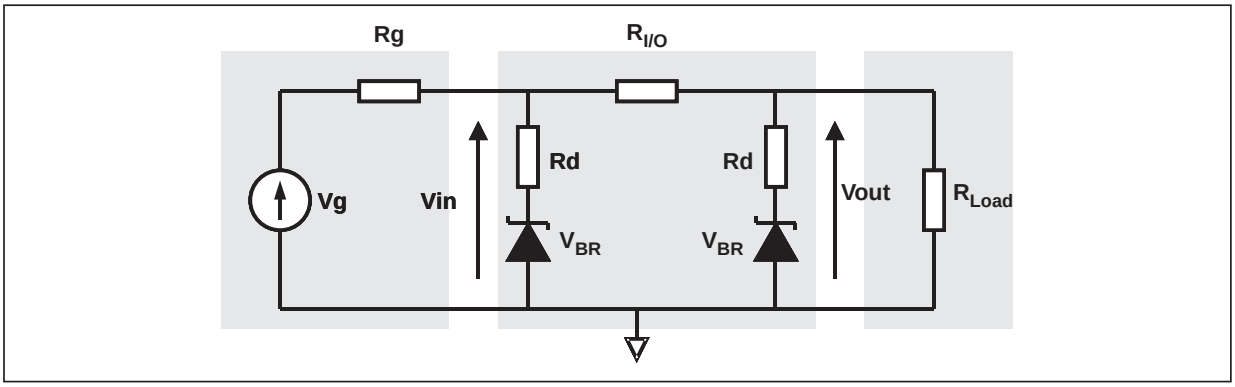


Figure 8 shows the equivalent schematic with the ESD surge generator, the EMI Filter and the load which corresponds to the device to be protected.

Fig. 8: Equivalent schematic of EMI filter connected to ESD surge generators.



Using EMI filter, protection is done in two steps. The first ESD diode will limit the V_{IN} voltage to:

$$V_{IN} = \frac{Rg \times V_{BR} + Rd \times Vg}{Rg + Rd}$$

$$V_{OUT} = \frac{R \times V_{BR} + Rd \times V_{IN}}{R_{I/O} + Rd}$$

Taking into account of : R >> Rd, Rg >> Rd and Rload >> Rd (open circuit on the test board).

With Vg = 15kV, Rg = 330Ω applied to the EMIF10-1K010F1 board (Rd = 1Ω , V_{BR} = 8V and $R_{I/O}$ = 1kΩ)

V_{IN} = 53V and V_{OUT} = 8.4V

With a correct layout, maximum output voltage is closed to V_{BR}.

Early ageing and destruction of IC is often due to latch-up phenomena which is mainly induced by dV/dt. Thanks to its RC structure, EMI filters provide high immunity to latch-up by integration of fast edges. Measurements done on *figure 7* show very clearly the high efficiency of the structure.

3- Crosstalk measurements

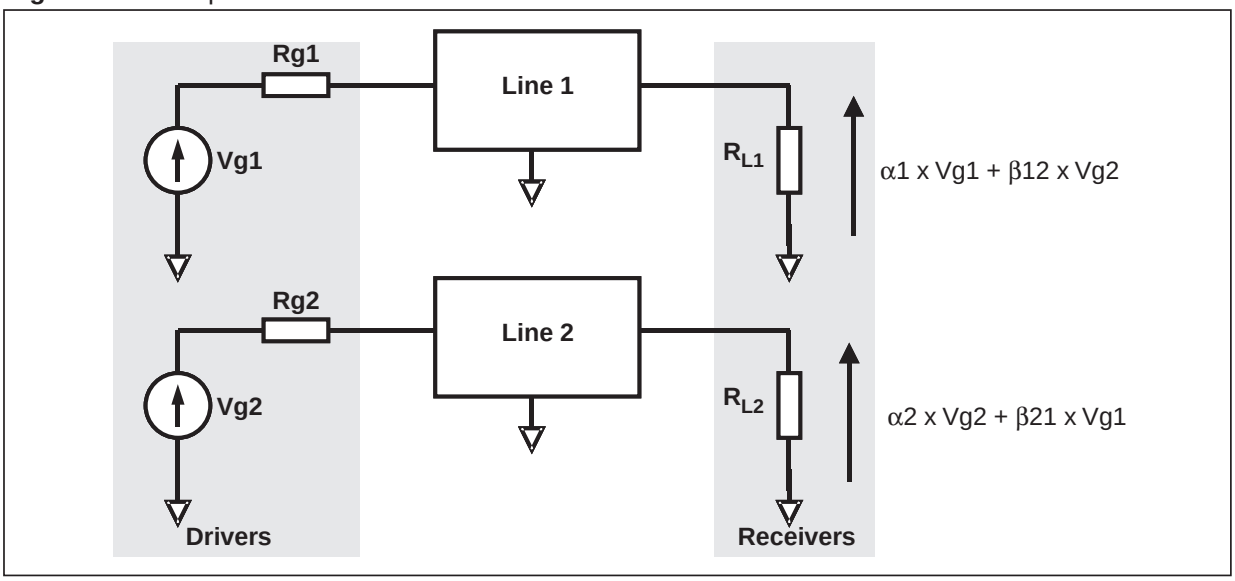
3a - Digital crosstalk

Crosstalk phenomena are due to coupling between 2 lines (2 filters in our case). Coupling factors (β12 and β21) shown in *figure 9* increase when distance between lines decreases, particularly in silicon dice where distances between components are very short.

In the example above the expected signal on load RL2 is α2 x Vg2, in fact the actual voltage at this point has got an extra value β21 x Vg1. This part of the Vg1 signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2.

This phenomenon has to be taken into account when drivers impose fast digital data or high frequency analog signals. The disturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Fig. 9: Crosstalk phemonema.



For digital crosstalk, test is done thanks to a square pulse generator connected in Vg1 through a 74HC04 gate. An oscilloscope is connected to Vg2.

Figure 10 shows the measurement circuit used to quantify crosstalk effect in a classical digital application.

Fig. 10: Digital crosstalk measurement circuit.

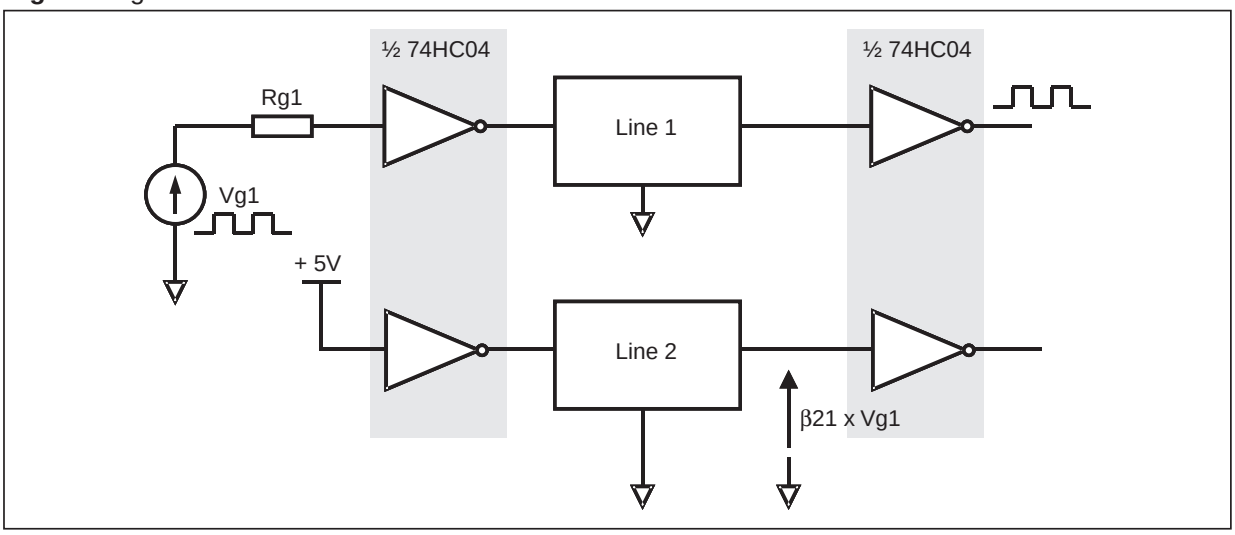
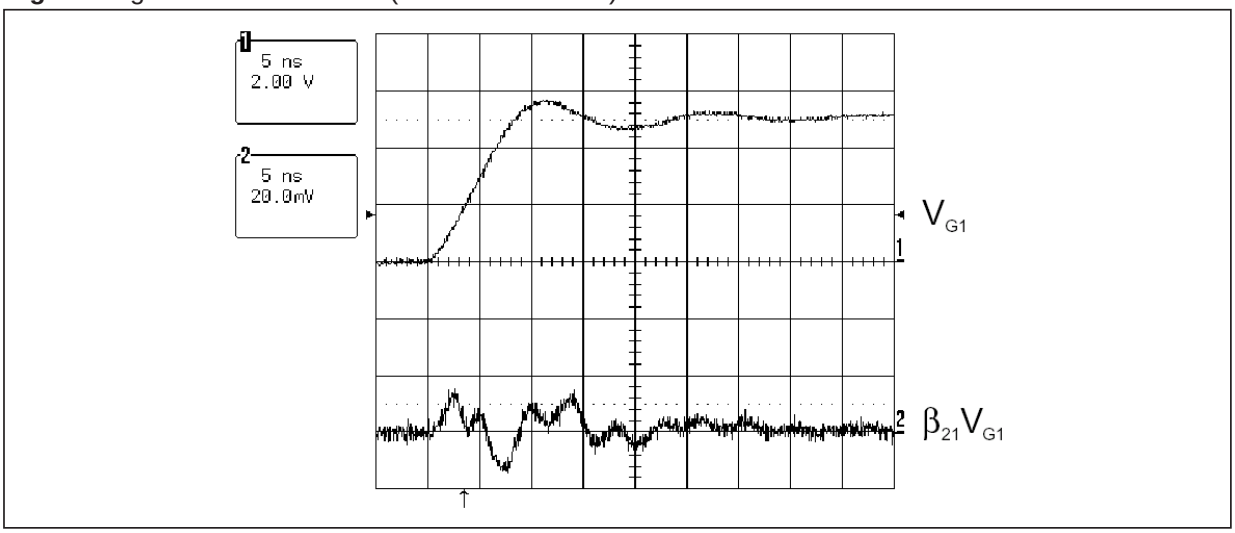


Figure 11 shows with a signal from 0 to 5V and rise time of few ns, the impact on the disturbed line is less than 40mV peak to peak: no data disturbance was noted on the concerned line. The measurements performed with falling edges gives an impact within the same range.

Fig. 11: Digital crosstalk results (EMIF10-1K010F1).



3b - Analog crosstalk

Figure 12 gives the measurement circuit for analog crosstalk. In *figure 13*, the curve shows the effect of cell on filter I1/O1 on cell I2/O2 for the EMIF10-1K010F1. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -47 dB

Fig. 12: Analog crosstalk measurement circuit.

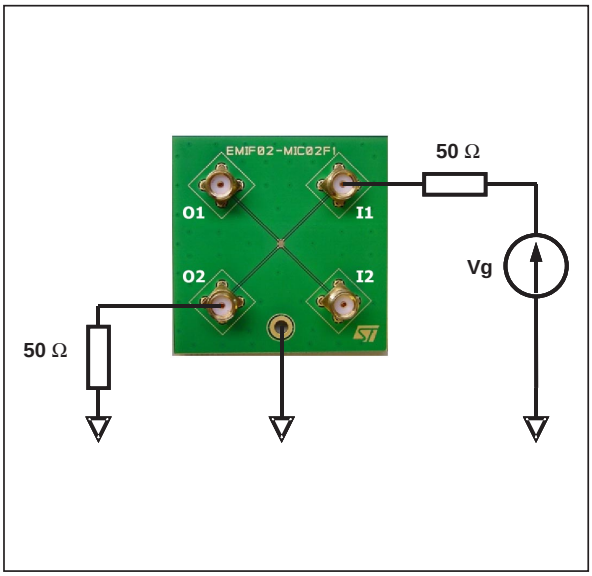
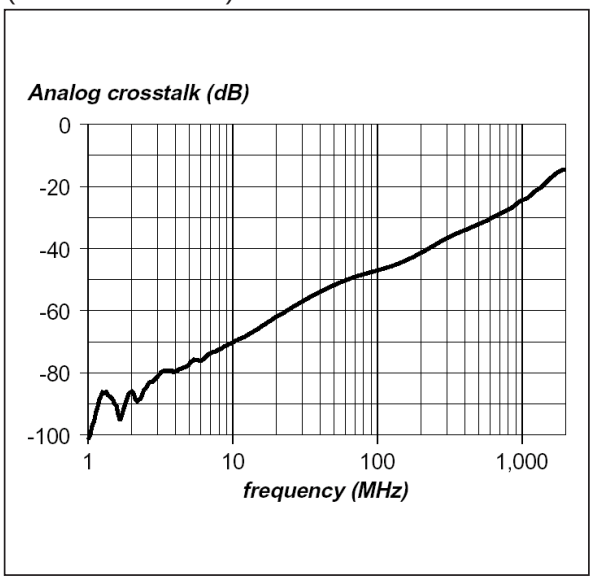


Fig. 13: Typical analog crosstalk result (EMIF10-1K010F1).



4- Conclusion

EMI filter are designed to suppress EMI and RFI noises and are also used to protect sensitive systems against electro-static discharges. The use of an Z-R-Z structure provides a very stable voltage on the output during ESD discharge when layout has been correctly routed.

RF measurement must be done carefully after using calibration board provided with EMIF demoboards.

EMI filters on flipchip are the most efficient topology to filter and protect integrated circuit by saving PCB area.