AN1723
Application note

Designing with the L5973AD high efficiency DC-DC converter

Introduction

The L5973AD is a step-down monolithic power switching regulator capable of delivering up to 2 A at output voltages from 1.235 V to 35 V. The operating input voltage ranges from 4.4 V to 36 V. It is realized in BCDV technology and the power switching element is realized by a P-channel D-MOS transistor. It doesn't require a bootstrap capacitor, and the duty cycle can range up to 100%. An internal oscillator fixes the switching frequency at 500 kHz which minimizes the LC output filter. The synchronization pin is available in case a higher frequency is required. Pulse-by-pulse and frequency foldback overcurrent protection offer an effective short-circuit protection. Other features include voltage feed-forward, protection against feedback disconnection, and inhibit and thermal shutdown. The device is housed in a HSOP8 package with exposed pad that helps to reduce the thermal resistance junction to ambient ($R_{Thj\text{-}a}$) down to approximately 40 °C/W.

Figure 1. EVAL5973AD demonstration board

Contents

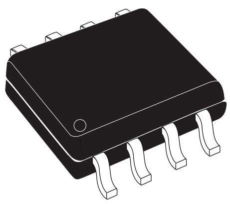
List of figures

1 Pin description

Table 1. Pin functions

N.	Name	Description
1	OUT	Regulator output
2	SYNC	Master/slave synchronization. When open, a signal synchronous with the turn-off of internal power is present at the pin. When connected to an external signal at a frequency higher than the internal signal, the device is synchronized by the external signal. When connecting the SYNC pins of two devices together, the one with the higher frequency works as master and the other as slave.
3	INH	A logical signal (active high) disables the device. With IHN higher than 2.2 V the device is OFF and with INH lower than 0.8 V, the device is ON. If INH is not used, the pin must be grounded. When it is open, an internal pull-up disables the device.
4	COMP	E/A output to be used for frequency compensation.
5	FB	Step-down feedback input. Connecting the output voltage directly to this pin results in an output voltage of 1.235 V. An external resistor divider is required for higher output voltages (the typical value for the resistor connected between this pin and ground is 4.7 kΩ).
6	V_{REF}	Reference voltage of 3.3 V. No filter capacitor is needed for stability.
7	GND	Ground
8	V_{CC}	Unregulated DC input voltage.

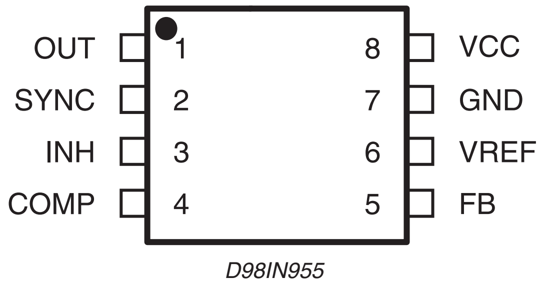
Figure 2. Package



HSOP8-exposed pad

AM11311v1

Figure 3. Pin connection



AM11310v1

2 Application information

In *Figure 4* the demonstration board application circuit is shown, where the input supply voltage, V_{CC}, can range from 4.4 V to 25 V due to the rated voltage of the input capacitor, and the output voltage is adjustable from 1.235 V to V_{CC}.

Figure 4. Demonstration board application circuit

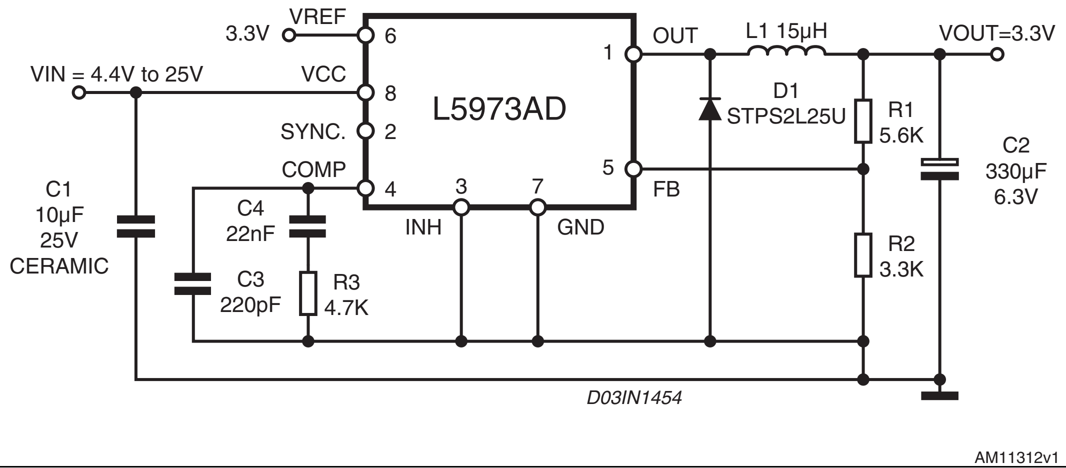
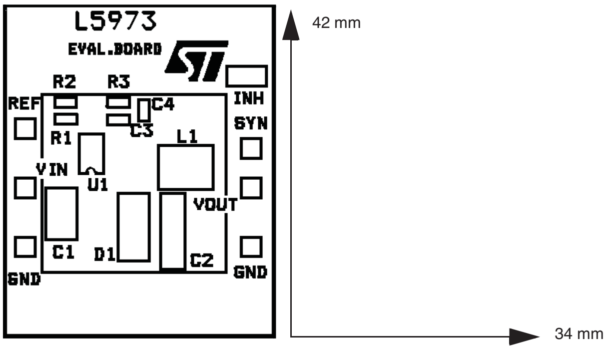


Table 2. Component list

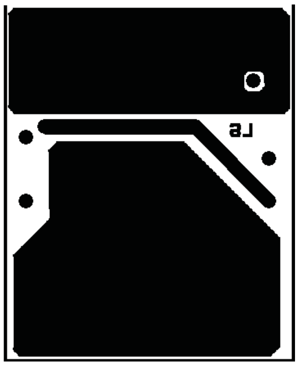
Reference	Part number	Description	Manufacturer
C1		10 µF, 25 V	Tokin
C2	POSCAP 6TPB330M	330 µF, 6.3 V	Sanyo
C3	C1206C221J5GAC	220 pF, 5%, 50 V	KEMET
C4	C1206C223K5RAC	22 nF, 10%, 50 V	KEMET
R1		5.6 kΩ, 1%, 0.1 W 0603	Neohm
R2		3.3 kΩ, 1%, 0.1 W 0603	Neohm
R3		4. 7 kΩ, 1%, 0.1 W 0603	Neohm
D1	STPS2L25U	2 A, 25 V	ST
L1	DO3316P-153	15 µH, 3 A	Coilcraft

Figure 5. PCB layout (component side)



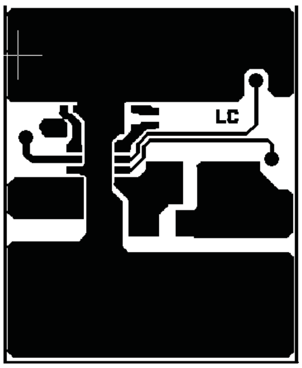
AM11313v1

Figure 6. PCB layout (bottom side)



AM11314v1

Figure 7. PCB layout (front side)



AM11315v1

The graphs that follow show the T_j versus output current in different input and output voltage conditions, and some efficiency measurements.

Figure 8. Junction temperature vs. output current at V_{IN} = 5 V

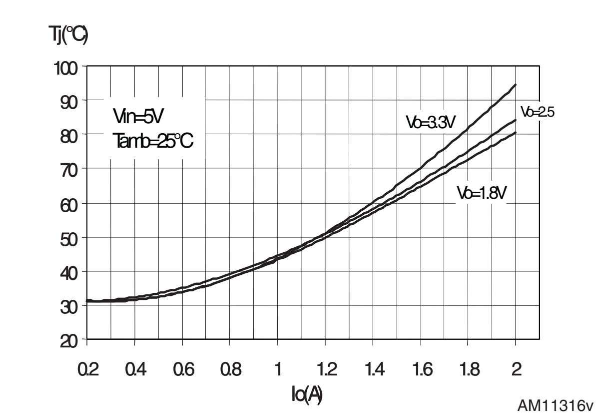


Figure 9. Junction temperature vs. output current at V_{IN} = 12 V

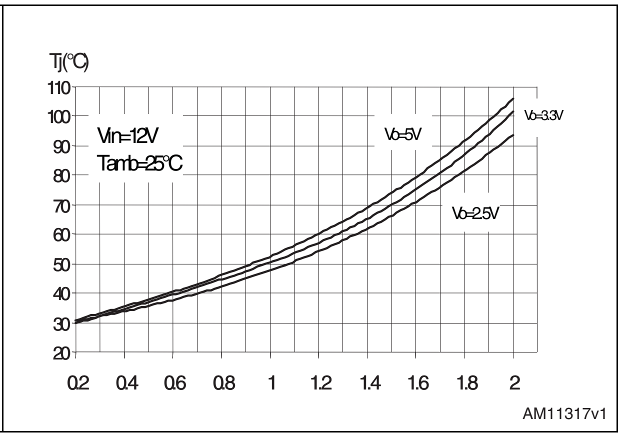


Figure 10. Efficiency vs. output current at V_{IN} = 5 V

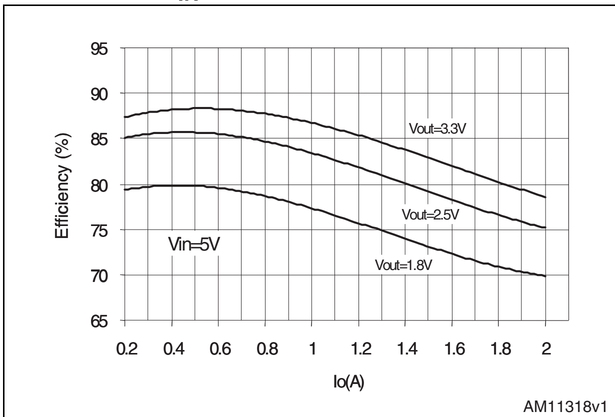
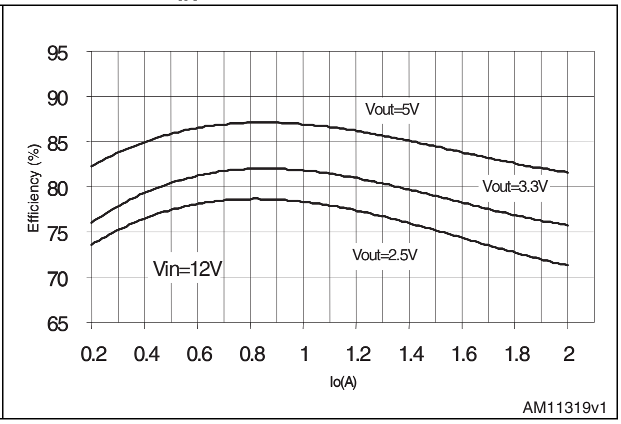


Figure 11. Efficiency vs. output current at V_{IN} = 12 V



The following points are analyzed:

- Component selection
- Closing the loop
- Board layout
  - Thermal considerations
  - Short-circuit protection
- Application ideas.

3 Component selection

3.1 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor must absorb all this switching current which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency.

The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 1

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

where η is the expected system efficiency, D is the duty cycle and I_O the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2 (considering $\eta = 1$).

The maximum and minimum duty cycles are:

Equation 2

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

Equation 3

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}} \quad \text{and} \quad D = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX} it is possible to determine the max. I_{RMS} flowing through the input capacitor. Different capacitors can be considered:

- Electrolytic capacitors

  These are the most commonly used due to their low cost and wide range of RMS current ratings. The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.
- Ceramic capacitors

  If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is their high cost.
- Tantalum capacitor

  Small, good quality tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge. Therefore, it is better to avoid this type of capacitor for the input filter of the device. They can, however, be subjected to high surge current when connected to the power supply.

4 Output capacitor

The output capacitor is very important in order to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to every high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided. Tantalum and electrolytic capacitors are usually a good choice for this purpose. A list of some tantalum capacitor manufacturers is provided in *Table 3*.

Table 3. Recommended output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
AVX	TPS	100 to 470	4 to 35	50 to 200
KEMET	T494/5	100 to 470	4 to 20	30 to 200
Sanyo POSCAP (1)	TPA/B/C	100 to 470	4 to 16	40 to 80
Sprague	595D	220 to 390	4 to 20	160 to 650

1. POSCAP capacitors have characteristics very similar to tantalum capacitors.

4.1 Inductor

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20-40% of I_{Omax}, which is 0.3-0.6 A with I_{Omax} = 1.5 A. The approximate inductor value is obtained using the following formula:

Equation 4

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \cdot T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T. For example, with V_{OUT} = 3.3 V, V_{IN} = 12 V and ΔI_O = 0.45 A, the minimum inductor value is about 12 µH.

The peak current through the inductor is given by:

Equation 5

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

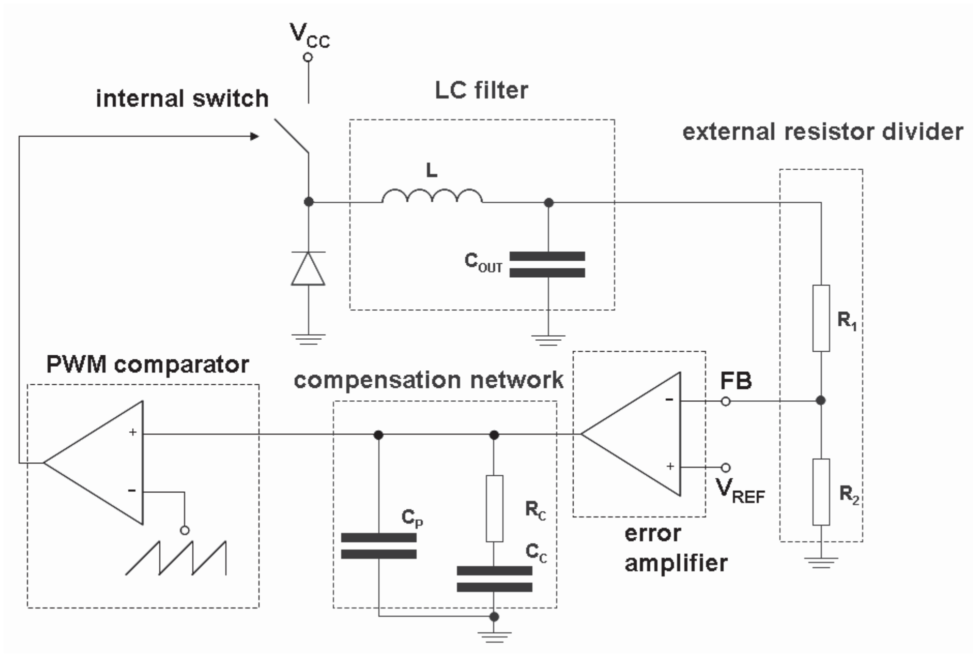
and it can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In *Table 4*, some inductor manufacturers are listed.

Table 4. Recommended inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	DO3316	15 to 33	2.0 to 3.0
Coiltronics	UP1B	22 to 33	2.0 to 2.4
BI	HM76-3	15 to 33	2.5 to 3.3
Epcos	B82476	33 to 47	1.6 to 2
Wurth elektronik	744561	33 to 47	1.6 to 2

5 Closing the loop

Figure 12. Block diagram



5.1 Error amplifier and compensation network

The output L-C filter of a step-down converter contributes with a 180 degree phase shift in the control loop. For this reason a compensation network between the COMP pin and GROUND is added. The simplest compensation network together with the equivalent circuit of the error amplifier are shown in *Figure 13*. RC and CC introduce a pole and a zero in the open loop gain. CP does not significantly affect real system stability, but is useful to reduce the noise of the COMP pin.

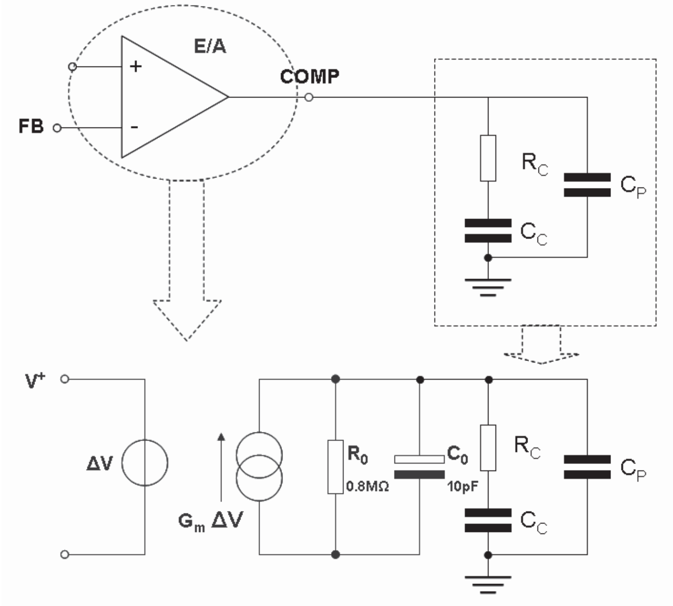
The transfer function of the error amplifier and its compensation network is:

Equation 6

$$A_o(s) = \frac{A_{vo} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_C \cdot C_C + s \cdot (R_0 \cdot C_C + R_0 \cdot (C_0 + C_p) + R_C \cdot C_C) + 1}$$

where $A_{vo} = G_m \cdot R_0$.

Figure 13. Error amplifier equivalent circuit and compensation network



The poles and zeroes of this transfer function are (if $C_C >> C_0 + C_P$):

Equation 7

$$F_{P1} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 8

$$F_{P2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 9

$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

F_{P1} is the low frequency pole that sets the bandwidth, while the zero F_{z1} is usually put close to the frequency of the double pole of the L-C filter (see *Section 5.2*). F_{P2} is usually at a very high frequency.

5.2 LC filter

The transfer function of the L-C filter is given by:

Equation 10

$$A_{LC}(s) = \frac{R_{LOAD} \cdot (1 + ES(R \cdot C_{OUT} \cdot s))}{s^2 \cdot L \cdot C_{OUT} \cdot (ESR + R_{LOAD}) + s \cdot (ESR \cdot C_{OUT} \cdot R_{LOAD} + L) + R_{LOAD}}$$

where R_{LOAD} is defined as the ratio between V_{OUT} and I_{OUT}.

If R_{LOAD}>>ESR, the previous expression of A_{LC} can be simplified and becomes:

Equation 11

$$A_{LC}(s) = \frac{1 + ESR \cdot C_{OUT} \cdot s}{L \cdot C_{OUT} \cdot s^2 + ESR \cdot C_{OUT} \cdot s + 1}$$

The zero of this transfer function is given by:

Equation 12

$$F_0 = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}}$$

F_0 is the zero introduced by the ESR of the output capacitor and is very important to increase the phase margin of the loop.

The poles of the transfer function can be calculated through the following expression:

Equation 13

$$F_{PLC1,\,2} = \frac{-(ESR \cdot C_{OUT} \pm \sqrt{(ESR \cdot C_{OUT})^2 - (4 \cdot L \cdot C_{OUT})})}{2 \cdot L \cdot C_{OUT}}$$

In the denominator of A_{LC}, the typical second order system equation can be recognized:

Equation 14

$$s^2 + 2 \cdot \delta \cdot \omega_h \cdot s + \omega_n^2$$

If the damping coefficient δ is very close to zero, the roots of the equation become a double root whose value is ω_h.

Similarly for A_{LC}, the poles can usually be defined as a double pole whose value is:

Equation 15

$$F_{PLC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}}$$

5.3 PWM comparator

The PWM gain is given by the following formula:

Equation 16

$$G_{PWM}(s) = \frac{V_{CC}}{(V_{OSCMAX} - V_{OSCMIN})}$$

where V_{OSCMAX} is the maximum value of a sawtooth waveform, and V_{OSCMIN} is the minimum value. A voltage feed-forward is implemented to ensure a constant G_{PWM}. This is obtained generating a sawtooth waveform directly proportional to the input voltage V_{CC}.

Equation 17

$$V_{OSCMAX} - V_{OSCMIN} = (K \cdot V_{CC})$$

where K is equal to 0.152. Therefore the PWM gain is also equal to:

Equation 18

$$G_{PWM}(s) = \frac{1}{K} = \text{const}$$

This means that even if the input voltage changes, the error amplifier does not change its value to keep the loop in regulation, therefore ensuring better line regulation and line transient response. In summary, the open loop gain can be written as:

Equation 19

$$G(s) = G_{PWM}s \cdot \frac{R_2}{R_1 + R_2} \cdot A_0((s) \cdot A_{LC}(s))$$

Example 1:

Considering R_C = 2.7 kΩ, C_C = 22 nF and C_P = 220 pF, the poles and zeroes of A_0 are:

- F_{P1} = 9 Hz
- F_{P2} = 256 kHz
- F_{Z1} = 2.68 kHz

If L = 22 µH, C_{OUT} = 100 µF and ESR = 80 mΩ, the poles and zeroes of A_{LC} becomes:

- F_{PLC} = 3.39 kHz
- F_0 = 19.89 kHz

Finally R_1 = 5.6 kΩ and R_2 = 3.3 kΩ

The gain and phase bode diagrams are plotted respectively in *Figure 14* and *Figure 15*.

Figure 14. Module plot

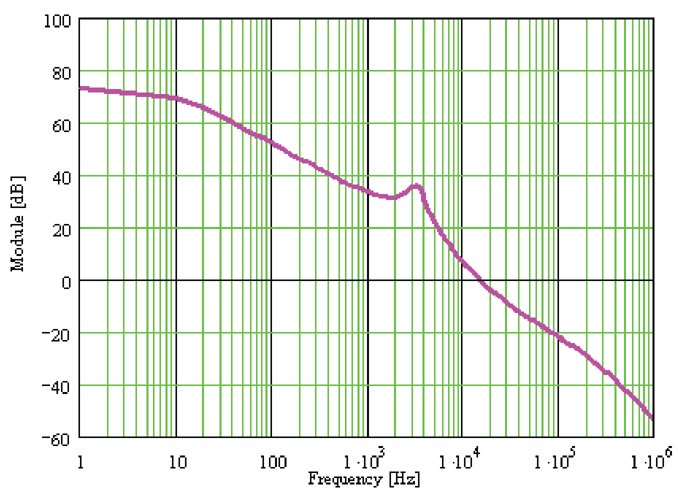
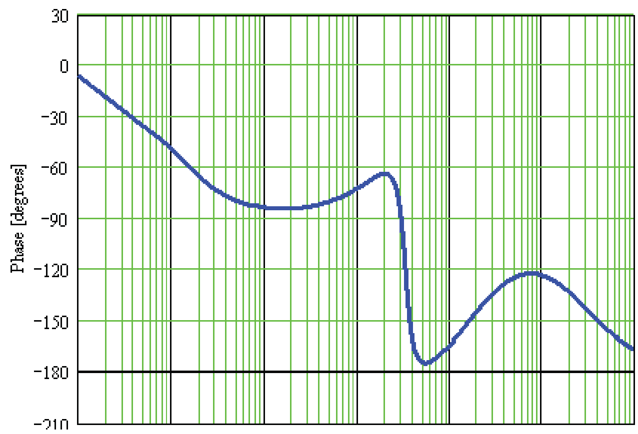


Figure 15. Phase plot



The cutoff frequency and the phase margin are:

- F_C = 14.9 kHz
- Phase margin = 29 °.

6 Layout considerations

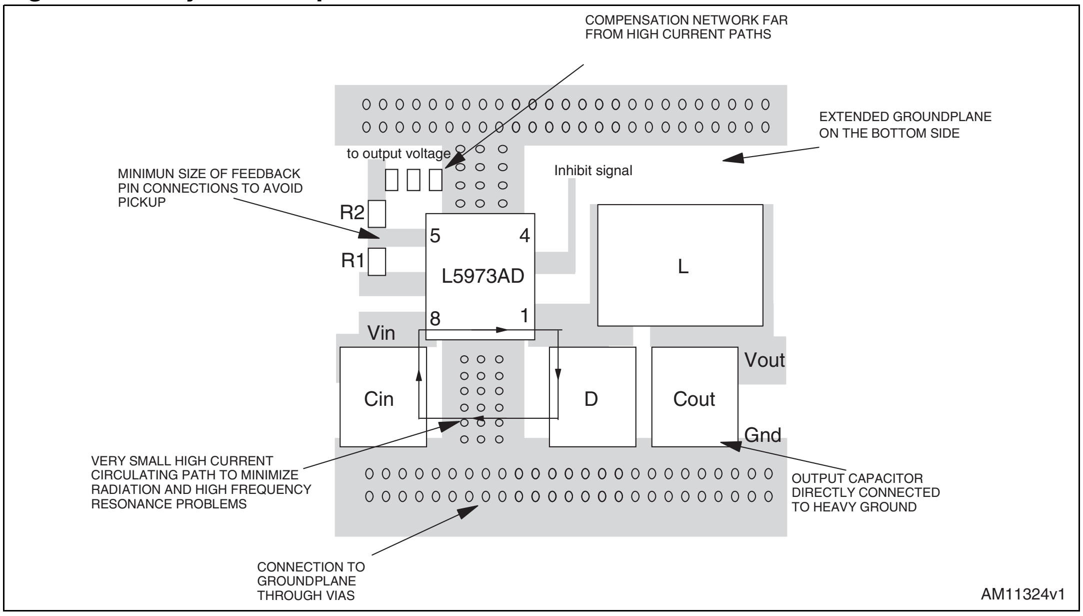
The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible. High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths.

A layout example is provided in *Figure 16*.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pickup noise.

Another important issue is the groundplane of the board. Since the package has an exposed pad, it is very important to connect it to an extended groundplane to reduce the thermal resistance junction to ambient.

Figure 16. Layout example



6.1 Thermal considerations

The dissipated power of the device is related to three different sources:

- Switching losses due to the not negligible R_{DSON}. These are equal to:

Equation 20

$$P_{ON} = R_{DSON} \cdot (I_{OUT})^2 \cdot D$$

where D is the duty cycle of the application. Note that the duty cycle is theoretically derived from the ratio between V_{OUT} and V_{IN}, but in practice it is quite higher than this value to compensate for the losses of the overall application. For this reason, the switching losses related to the R_{DSON} increase compared to an ideal case.

Equation 21

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{ON} + T_{OFF})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

where T_{ON} and T_{OFF} are the overlap times of the voltage across the power switch and the current flowing into it during the turn-on and turn-off phases. T_{SW} is the equivalent switching time.

- Quiescent current losses

Equation 22

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current.

Example 2:

- $V_{IN} = 5$ V
- $V_{OUT} = 3.3$ V
- $I_{OUT} = 1.5$ A.

The R_{DSON} has a typical value of 0.25 Ω @ 25 °C and increases up to a maximum value of 0.5 Ω @ 150 °C. We can consider a value of 0.4 Ω

- T_{SW} is approximately 70 ns
- I_Q has a typical value of 5 mA @ $V_{IN} = 12$ V.

The overall losses are:

Equation 23

$$P_{TOT} = R_{DSON} \cdot (I_{OUT})^2 \cdot D \cdot V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} \cdot V_{IN} \cdot I_Q =$$
$$= 0.4 \cdot 1.5^2 \cdot 0.7 \cdot 5 \cdot 1.5 \cdot 70 \cdot 10^{-9} \cdot 500 \cdot 10^3 + 5 \cdot 5 \cdot 10^{-3} \cong 0.9W$$

The junction temperature of the device is:

Equation 24

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

where T_A is the ambient temperature and Rth_{J-A} is the thermal resistance junction to ambient.

Considering that the device, if mounted on the board with a good groundplane, has a thermal resistance junction to ambient (Rth_{J-A}) of about 42 °C/W, and considering an ambient temperature of about 70 °C:

Equation 25

$$T_J = 70 + 0.9 \cdot 42 \cong 108^\circ C$$

6.2 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit, the device reduces the T_{ON} down to its minimum value (approximately 250 ns) and the switching frequency to approximately one third of its nominal value (see the L5973AD device datasheet).

In these conditions, the duty cycle is strongly reduced and, in most applications, this is enough to limit the current to I_{lim}. In any case, if there is a heavy short-circuit at the output ($V_{OUT} = 0$ V) and depending on the application conditions (V_{CC} value and parasitic effect of external components) the current peak could reach values higher than I_{lim}.

This can be understood by considering the inductor current ripple during the ON and OFF phases:

- ON phase

Equation 26

$$\Delta I_L = \frac{V_{IN} - V_{out} - DCR_L \cdot I}{L} \cdot T_{ON}$$

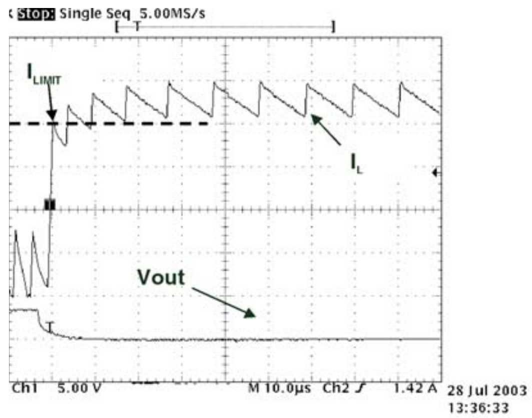
- OFF phase

Equation 27

$$\Delta I_L = \frac{V_D + V_{out} + DCR_L \cdot I}{L} \cdot T_{OFF}$$

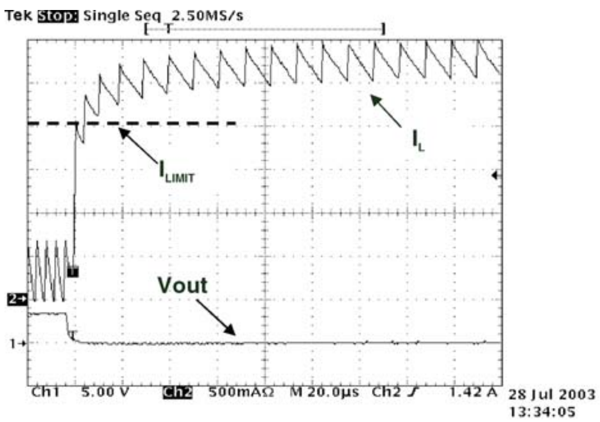
where V_D is the voltage drop across the diode and DCR_L is the series resistance of the inductor. In short-circuit conditions, V_{OUT} is negligible. So, during T_{OFF}, the voltage applied to the inductor is very small and it is possible that the current ripple in this phase does not compensate for the current ripple during T_{ON}. The maximum current peak can be easily measured through the inductor with V_{OUT} = 0 V (short-circuit) and V_{CC}=V_{INmax}. If the application must sustain the short-circuit condition for an extended period, the external components (mainly inductor and diode) must be selected accordingly.

Figure 17. Short-circuit current V_{IN} = 25 V



AM11333v1

Figure 18. Short-circuit current V_{IN} = 30 V



AM11332v1

For example, in *Figure 17* and *Figure 18* it can be observed that, for a given component list, increasing the input voltage causes the current peak to increase also. The current limit is immediately triggered but the current peak increases until the current ripple during T_{OFF} is equal to the current ripple during T_{ON}.

7 Application ideas

7.1 Positive buck-boost regulator

The device can be used to design an up-down converter with a positive output voltage. In *Figure 19*, the schematic circuit of this topology for an output voltage of 12 V is shown.

The input voltage can range from 5 V to 35 V.

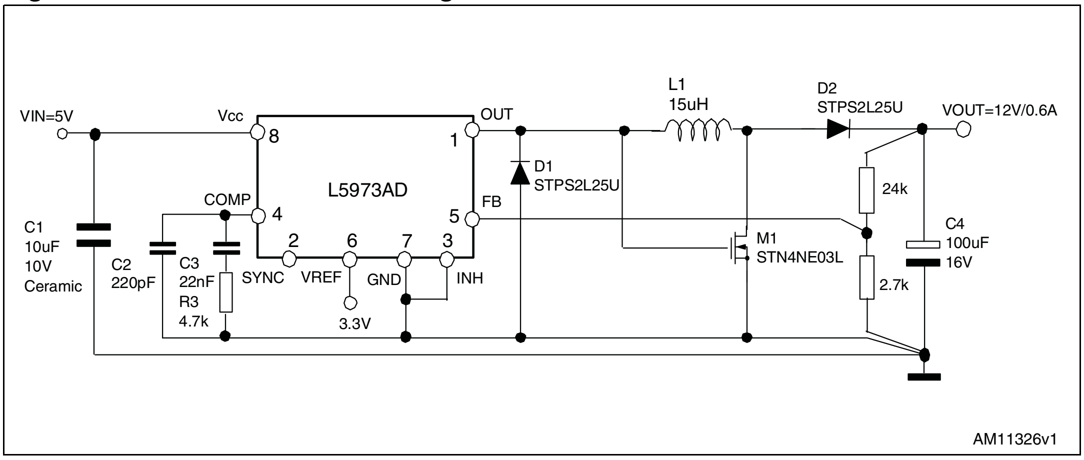
The output voltage is given by $V_O = V_{IN} \cdot D/(1\text{-}D)$, where D is the duty cycle.

The maximum output current is given by $I_{OUT} = 1 \times (1\text{-}D)$.

The current capability is reduced by the term (1-D) and so, for example, with a duty cycle of 0.5, and considering an average current flowing through the switch of 1.5 A, the maximum deliverable output current to the load is 0.75 A.

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

Figure 19. Positive buck-boost regulator



7.2 Buck-boost regulator

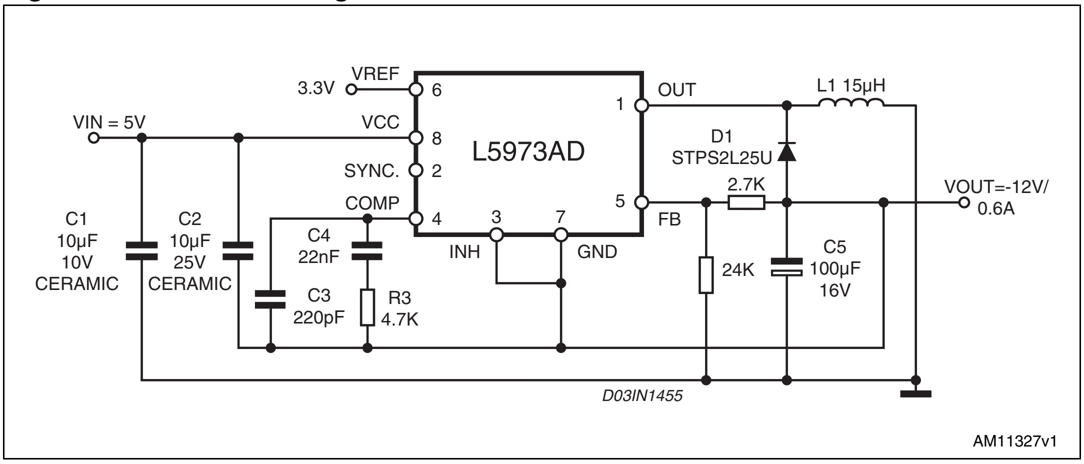
In *Figure 20* the schematic circuit to design a standard buck-boost topology is provided.

The output voltage is given by $V_O = -V_{IN} \cdot D/(1\text{-}D)$.

The maximum output current is equal to $I_{OUT} = 1 \cdot (1\text{-}D)$, for the same reason as that of the up-down converter.

It is important to note that the GND pin of the device is connected to the negative output voltage. Therefore, the device is subject to a voltage equal to $V_{IN}\text{-}V_O$, which must be lower than 36 V (maximum operating input voltage).

Figure 20. Buck-boost regulator



7.3 Dual output voltage with auxiliary winding

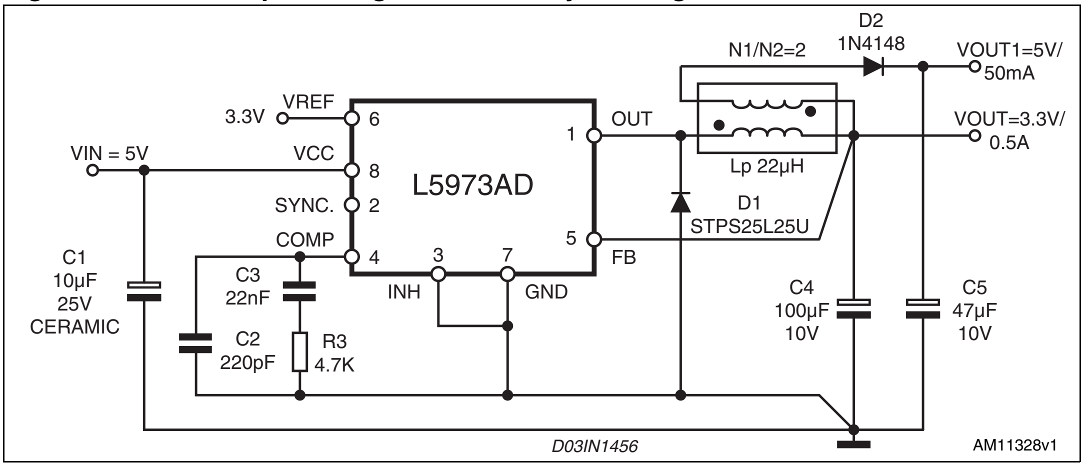
When two output voltages are required, it is possible to implement a dual output voltage converter by using a coupled inductor.

During the ON phase, the current is delivered to V_{OUT} while D2 is reverse-biased.

During the OFF phase, the current is delivered through the auxiliary winding to the output voltage V_{OUT1}.

This is possible only if the magnetic core has stored sufficient energy. So, to be sure that the application is working properly, the load related to the second output V_{OUT1} should be much lower than the load related to V_{OUT}.

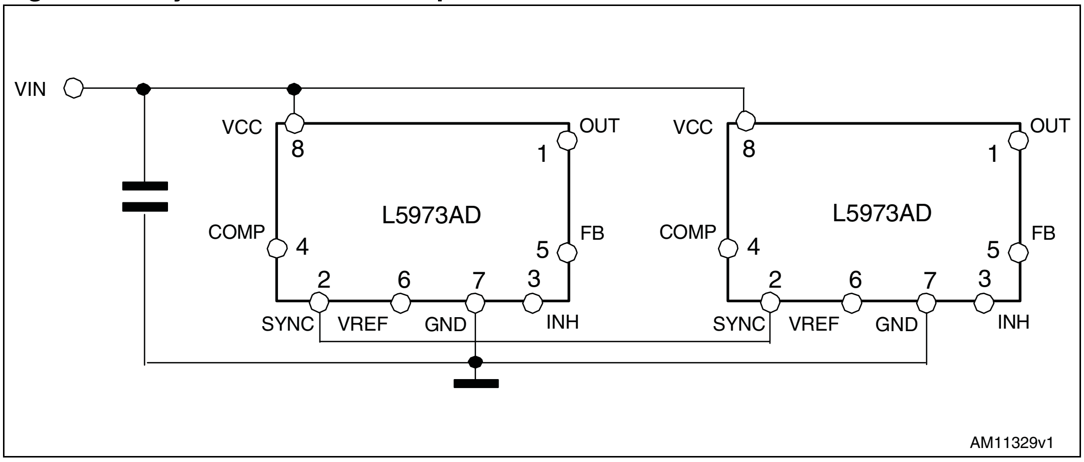
Figure 21. Dual output voltage with auxiliary winding



7.4 Synchronization example

Two or more devices (up to 6) can be synchronized by simply connecting together the synchronization pins. In this case, the device with a slightly higher switching frequency value works as master and those with slightly lower switching frequency values work as slaves.The device can also be synchronized from an external source. In this case, the logic signal must have a frequency higher than the internal switching frequency of the device (500 kHz).

Figure 22. Synchronization example



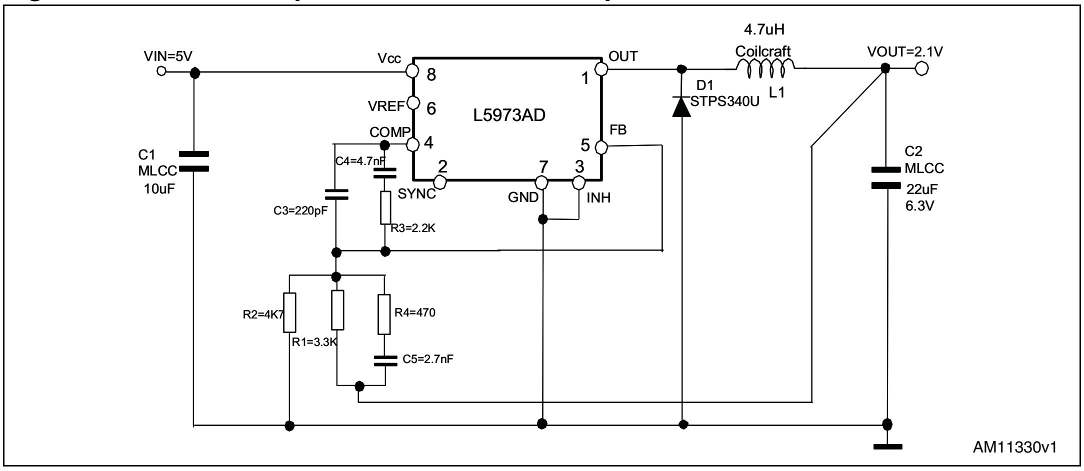
7.5 Compensation network with MLCC (multiple layer ceramic capacitor) at the output

MLCC with values in the range of 10 µF - 22 µF and rated voltages in the range of 10 V - 25 V are available today at relatively low cost from many manufacturers.

These capacitors have very low ESR values (a few mΩ), so they are sometimes used for the output filter to reduce the voltage ripple and the overall size of the application.

However, the very low ESR value affects the compensation of the loop (see *Section 5*) and in order to keep the system stable, a more complicated compensation network may be required. *Figure 23* shows an example of a compensation network which stabilizes the system using ceramic capacitors at the output (the optimum component values depend on the application).

Figure 23. MLCC compensation network example

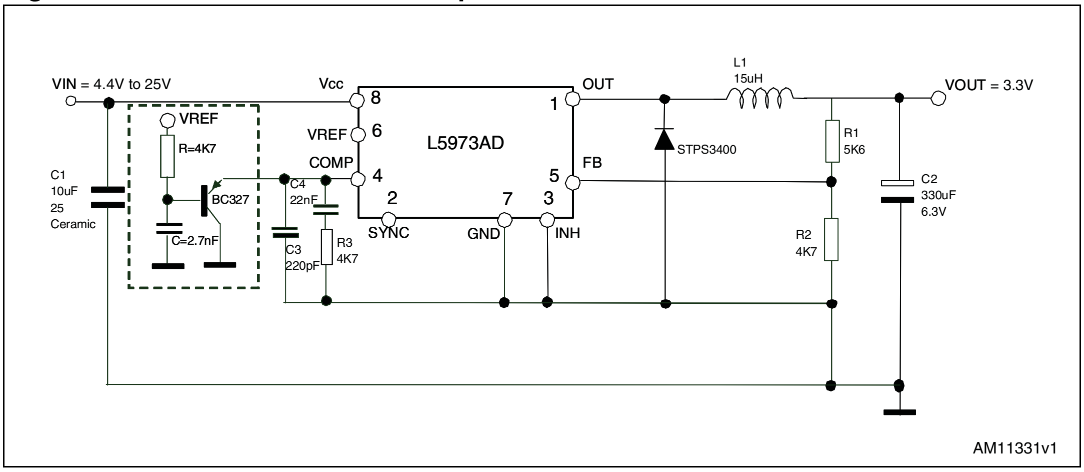


7.6 External soft-start network

At startup, the device can quickly increase the current up to the current limit in order to charge the output capacitor. If a soft ramp-up of the output voltage is required, an external soft-start network can be implemented as shown in *Figure 24*.

The capacitor C is charged up to an external reference (through R), and the BJT clamps the COMP pin. This clamps the duty cycle, limiting the slew rate of the output voltage.

Figure 24. Soft-start network example



8 Revision history

Table 5. Document revision history

Date	Revision	Changes
18-Oct-2006	2	Initial electronic version
09-Jun-2009	3	– *Section 5: Closing the loop* modified – Minor text changes throughout the document
07-Jun-2012	4	Equations: *4*, *5*, *20*, *21*, *22*, *23*, *24*, *25*, *26* and *27* have been updated.