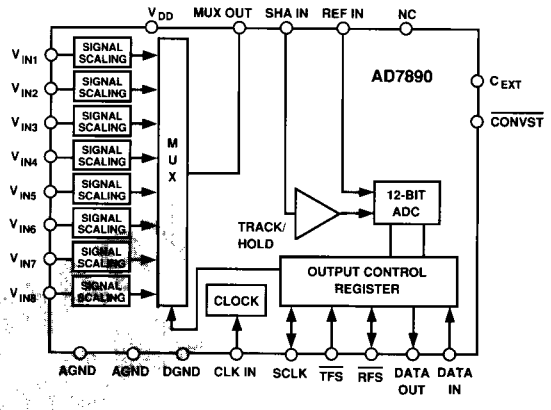
LC²MOS 8-Channel, 12-Bit Serial, Data Acquisition System

AD7890

FEATURES

Fast 12-Bit ADC with 10 μs Conversion Time
Eight Single-Ended Analog Input Channels
±10 V Input Range
Allows Separate Access to Multiplexer and ADC
On-Chip Track/Hold Amplifier
High Speed, Flexible, Serial Interface
Single Supply Operation
Low Power, 50 mW max in Normal Operation
Power-Down Mode

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7890 is an eight-channel 12-bit data acquisition system. The part contains an input multiplexer, an on-chip track/hold amplifier, a high speed 12-bit ADC and a high speed serial interface. The part operates from a single +5 V supply and accepts an analog input range of ±10 V.

The multiplexer on the part is independently accessible. This allows the user to insert an antialiasing filter, if required, between the multiplexer and the ADC. This means that one antialiasing filter can be used for all eight channels. Connection of an external capacitor allows the user to adjust the time given to the multiplexer settling to include any external delays in this antialiasing filter.

Output data from the AD7890 is provided via a high speed bidirectional serial interface port. The part contains an on-chip control register, allowing control of channel selection, conversion start, power-down, etc., via the serial port. Versatile, high speed logic ensures easy interfacing to serial ports on microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7890 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is low at 30 mW typ, and the part can be placed in a standby (power-down) mode if it is not required to performed conversions. The AD7890 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package or in a 24-pin small outline package (SOIC).

PRODUCT HIGHLIGHTS

1. Complete 12-Bit Data Acquisition System on a Chip
   The AD7890 is a complete monolithic ADC combining an eight-channel multiplexer, 12-bit ADC and a track/hold amplifier on a single chip.
2. Separate Access to Multiplexer and ADC
   The AD7890 provides access to the output of the multiplexer allowing the user to insert an antialiasing filter between the multiplexer and the ADC. This allows one antialiasing filter for eight channels—a considerable saving over the eight antialiasing filters required if the multiplexer was internally connected to the ADC.
3. High Speed Serial Interface
   The part provides a high speed serial interface for easy connection to serial ports of microcontrollers and DSP processors. An on-chip control register is programmed via this bidirectional serial port.

AD7890—SPECIFICATIONS

(V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V, f_{CLKIN} = 2.5 MHz external, MUX OUT connected to SHA IN. All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	A Version[1]	B Version	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					Any Channel
Signal-to-Noise Ratio @ +25°C	70	72	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion	−80	−80	−80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Peak Harmonic or Spurious Noise	−81	−81	−81	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 83 kHz
2nd Order Terms	−80	−80	−80	dB typ	
3rd Order Terms	−80	−80	−80	dB typ	
Channel-to-Channel Isolation	−80	−80	−80	dB max	f_{IN} = 1 kHz Sine Wave
DC ACCURACY					Any Channel
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±1	±1	±1	LSB max	
Negative Full-Scale Error[2]	±1	±1	±1	LSB max	
Full-Scale Error Match[2]	1	1	1	LSB max	
Bipolar Zero Error	±1	±1	±1	LSB max	
Bipolar Zero Error Match	1	1	1	LSB max	
ANALOG INPUTS					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	μA max	
MUX OUT OUTPUT					
Output Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Output Resistance	2.9/4.2	2.9/4.2	2.9/4.2	kΩ min/ kΩ max	
SHA IN INPUT					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	50	50	50	nA max	
REFERENCE INPUT					
Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	4	4	4	mA max	Varies with ADC Code
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
Serial Data Output Coding	2s COMPLEMENT				
CONVERSION RATE					
Conversion Time	10	10	10	μs max	$f_{CLK\ IN}$ = 2.5 MHz, MUX OUT Connected to SHA IN
Track/Hold Acquisition Time	2	2	2	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD} (Normal Mode)	10	10	10	mA max	
I_{DD} (Standby Mode)	500	500	500	μA max	Logic Inputs = 0 V or V_{DD}
Power Dissipation (Normal Mode)	50	50	50	mW max	Typically 30 mW
Power Dissipation (Standby Mode)	2.5	2.5	2.5	mW max	Typically 1 mW

NOTES

[1]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.

[2]Measured with respect to 4 × REF IN voltage and is calculated after the bipolar zero error has been adjusted out.

[3]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Description
V_{IN1}-V_{IN8}	Analog Input Channels. These input channels provide eight single-ended inputs. The analog input range on each channel is ±10 V. The channel to be converted is selected using the A0, A1 and A2 bits in the control register. The multiplexer has guaranteed break-before-make operation.
MUX OUT	Multiplexer Output. The output of the multiplexer appears at this pin. The output voltage range from this output is 0 to +2.5 V for a ±10 V analog input to the selected channel. The output impedance of this output is nominally 3.5 kΩ. If no external antialiasing filter is required, MUX OUT should be connected to SHA IN.
SHA IN	Track/Hold Input. The input to the on-chip track/hold is applied to this pin. It is a high impedance input, and the input voltage range is 0 V to +2.5 V.
REF IN	Voltage Reference Input. The reference voltage for the part is applied to this pin. The input impedance of this reference input varies with the analog input voltage and REF IN should, therefore, be driven from a low impedance source. The nominal reference voltage for correct operation of the AD7890 is +2.5 V.
V_{DD}	Positive supply voltage, +5 V ± 5%.
AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
DGND	Digital Ground. Ground reference for digital circuitry.
SCLK	Serial Clock Input. In the external clocking (slave) mode (see DIGITAL INTERFACE section) this is an externally applied serial clock which is used to load serial data to the control register and to access data from the output register. In the self-clocking (master) mode, the internal serial clock, which is derived from the clock input (CLK IN), appears on this pin. Once again, it is used to load serial data to the control register and to access data from the output register.
$\overline{TFS}$	Transmit Frame Synchronization Pulse. Active low logic input with serial data expected after the falling edge of this signal.
DATA IN	Serial Data Input. Serial data to be loaded to the control register is provided at this input. The first six bits of serial data are loaded to the control register on the first six falling edges of SCLK after $\overline{TFS}$ goes low. Serial data on subsequent SCLK edges is ignored while $\overline{TFS}$ remains low.
$\overline{RFS}$	Receive Frame Synchronization Pulse. In the external clocking mode, this pin is an active low logic input with $\overline{RFS}$ provided externally as a strobe or framing pulse to access serial data from the output register. In the self-clocking mode, it is an active low output which is internally generated and provides a strobe or framing pulse for serial data from the output register. For applications which require that data be transmitted and received at the same time, $\overline{RFS}$ and $\overline{TFS}$ should be connected together.
DATA OUT	Serial Data Output. Sixteen bits of serial data are provided with one leading zero, preceeding the three address bits of the Control register and the 12-bits of conversion data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{RFS}$ goes low. Output coding from the ADC is 2s complement.
$\overline{CONVST}$	Convert Start. Edge-triggered logic input. A low to high transition on this input puts the track/hold into hold and initiates conversion provided that the internal one-shot has timed out (see Control Register section). If the internal pulse is active when the $\overline{CONVST}$ goes high, the track/hold will not go into hold until the pulse times out. If the internal pulse has timed out when $\overline{CONVST}$ goes high, the rising edge of $\overline{CONVST}$ drives the track/hold into hold and initiates conversion.
CLK IN	Clock Input. An external TTL-compatible clock is applied to this input pin to provide the clock source for the conversion sequence. In the self-clocking serial mode, the SCLK output is derived from this CLK IN pin.
C_{EXT}	External Capacitor. An external capacitor is connected to this pin to determine the length of the internal one-shot pulse (see $\overline{CONVST}$ input and Control Register section). Larger capacitances on this pin extend the pulse to allow for settling-time delays through an external antialiasing filter or signal conditioning circuitry.
NC	No Connect. Do not connect anything to this pin.

CONTROL REGISTER

A2	A1	A0	CONV	SC/EC	STBY

A2 Address Input. This input is the most significant address input for multiplexer channel selection.

A1 Address Input. This is the 2nd most significant address input for multiplexer channel selection.

A0 Address Input. Least significant address input for multiplexer channel selection. When the address is written to the control register, an internal one-shot is initiated, the pulse width of which is determined by the value of capacitance on the C_{EXT} pin. When this pulse is active, it ensures the conversion process cannot be activated. This allows an external antialiasing filter (the output of which appears at SHA IN) to settle before the track/hold goes into hold and conversion is initiated. When this pulse times out, the track/hold goes into hold and conversion is initiated.

CONV Conversion Start. Writing a 1 to this bit initiates a conversion in a similar manner to the $\overline{CONVST}$ input. Continuous conversion starts do not take place when there is a 1 in this location. The internal one-shot and the conversion process are initiated on the next clock edge after a 1 is written to this bit. With a 1 in this bit, the hardware conversion start, i.e., the $\overline{CONVST}$ input, is disabled. Writing a 0 to this bit enables the hardware $\overline{CONVST}$ input.

SC/EC Master/Slave Selection. Writing a 0 to this bit puts the AD7890 into its self-clocking (master) mode where the SCLK and $\overline{RFS}$ pins are outputs and the AD7890 effectively acts as a master in a serial system. This self-clocking mode is useful for connection to shift registers and the serial ports of DSP processors. Writing a 1 to this bit puts the AD7890 serial interface into its external clocking (slave) mode where the SCLK and $\overline{RFS}$ pins are both inputs and the AD7890 effectively acts as a slave to a microprocessor in a serial system. This external clocking mode is useful for connection to the serial port of microcontrollers such as the 8XC51 and the 68HCXX and for connection to the serial ports of DSP processors. The AD7890 powers up in its external clocking mode.

STBY Standby Mode Input. Writing a 1 to this bit places the device in its standby or power-down mode. Writing a 0 to this bit places the device in its normal operating mode.

CIRCUIT DESCRIPTION

The AD7890 is an eight-channel, 12-bit serial data acquisition system. It provides the user with signal scaling, multiplexer, track/hold, A/D converter and versatile serial logic functions on a single chip. The signal scaling allows the part to handle ±10 V input signals while operating from a single +5 V supply. The part requires an external +2.5 V external reference.

Unlike other single chip solutions, the AD7890 provides the user with separate access to the multiplexer and the A/D converter. This means that the flexibility of separate multiplexer and ADC solutions is not sacrificed with the one-chip solution. With access to the multiplexer output, the user can implement external signal conditioning between the multiplexer and the track/hold. It means that one antialiasing filter can be used to on the output of the multiplexer to provide the antialiasing function for all eight channels. The extra settling time introduced into the circuit by the external circuitry can be allowed for by the AD7890 by connecting a single capacitor to the C_{EXT} pin. If no external signal conditioning is required, the multiplexer output (MUX OUT) can simply be connected directly to the track/hold input (SHA IN).

A serial write to the control register selects the input channel to be converted. When the three address bits are written to the control register, an internal pulse is initiated. This disables the track/hold from going into hold and also disables conversion from being initiated. The duration of the internal pulse allows for the settling time of the on-chip multiplexer. By connecting different values of capacitor for the C_{EXT} pin, this internal pulse can be stretched to cater for the settling time of external components between the MUX OUT and SHA IN pins.

Once the pulse has been timed out, conversion can be initiated on the A/D converter. The conversion can be initiated by pulsing the $\overline{CONVST}$ input or by writing to the CONV bit of the Control Register. If the conversion start command is coincident with the multiplexer write or occurs while the internal pulse is active, the track/hold will not go into hold and conversion will not be initiated until the internal pulse has timed out.

The AD7890 provides separate channel select and conversion start control. This allows the user to optimize the throughput rate of the system. Once the track/hold has gone into hold mode the input channel can be updated and the input voltage can settle to the new value while the present conversion is in progress.

DIGITAL INTERFACE

The AD7890's serial communications port provides a flexible arrangement to allow easy interfacing to industry standard microprocessors, microcontrollers and digital signal processors. A serial read to the AD7890 accesses data from the output register via the DATA OUT line. A serial write to the AD7890 writes data to the Control Register via the DATA IN line.

Two different modes of operation are available, optimized for different types of interface where the AD7890 can either act as master in the system (it provides the serial clock and data framing signal) or act as slave (an external serial clock and framing signal can be provided to the AD7890). These two modes, labelled self-clocking mode and external clocking mode, are discussed in detail in the following sections. Note, the AD7890 powers up in its external clocking mode. A Logic 0 must be written to the SC/EC bit of the control register to place the part in its self-clocking mode.

Self-Clocking Mode

The AD7890 is configured for its self-clocking mode by writing a 0 to the SC/EC bit of the control register. In this mode, the AD7890 provides the serial clock signal and the serial data framing signal used for the transfer of data from the AD7890. This self-clocking mode can be used with processors which allow an external device to clock their serial port including most digital signal processors.

Read Operation

Figure 1 shows a timing diagram for reading from the AD7890 in the self-clocking mode. At the end of conversion, $\overline{RFS}$ goes low and the serial clock (SCLK) and serial data (DATA OUT) outputs become active. Sixteen bits of data are transmitted with one leading zero, followed by the three address bits of the Control Register, followed by the 12 bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. The $\overline{RFS}$ output remains low for the duration of the sixteen clock cycles. When $\overline{RFS}$ returns high, the serial clock and serial data outputs are disabled.

Write Operation

Figure 2 shows a write operation to the Control Register of the AD7890. The $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. $\overline{TFS}$ going low initiates the SCLK output, and this is used to clock data out of the processors serial port and into the Control Register of the AD7890. The AD7890 Control Register requires only six bits of data. These are loaded on the first six clock cycles of the serial clock with data on all subsequent clock cycles being ignored. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

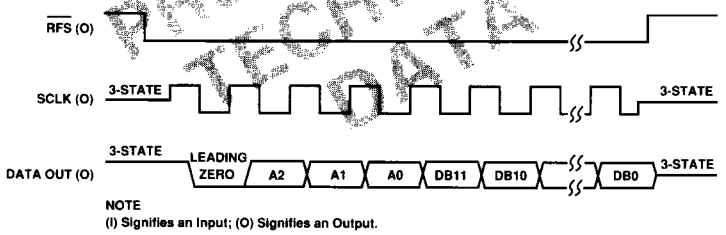


Figure 1. Self-Clock (Master) Mode Output Register Read

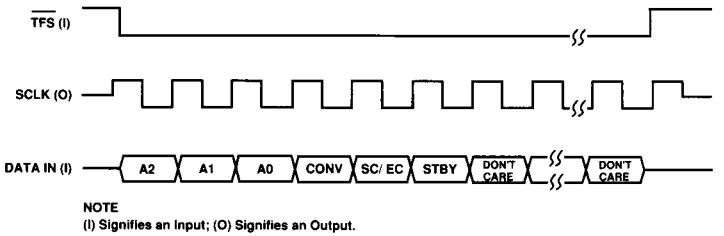


Figure 2. Self-Clocking (Master) Mode Control Register Write

External Clocking Mode

The AD7890 is configured for its external clocking mode by writing a 1 to the SC/EC bit of the Control Register. In this mode, SCLK and $\overline{RFS}$ of the AD7890 are configured as inputs. This external-clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Read Operation

Figure 3 shows the timing diagram for reading from the AD7890 in the external clocking mode. $\overline{RFS}$ goes low to access data from the AD7890. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However, $\overline{RFS}$ must remain low for the duration of the data transfer operation. Once again, sixteen bits of data are transmitted with one leading zero, followed by the three address bits in the Control Register, followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK and is valid on the falling edge of SCLK. If a serial read from the output register is in progress when conversion is complete, the updating of the output register is deferred until the serial data read is complete.

Write Operation

Figure 4 shows a write operation to the Control Register of the AD7890. As with the self-clocking mode, the $\overline{TFS}$ input goes low to indicate to the part that a serial write is about to occur. The AD7890 control register requires only six bits of data. These are loaded on the first six clock cycles of the serial clock with data on all subsequent clock cycles being ignored. Serial data to be written to the AD7890 must be valid on the falling edge of SCLK.

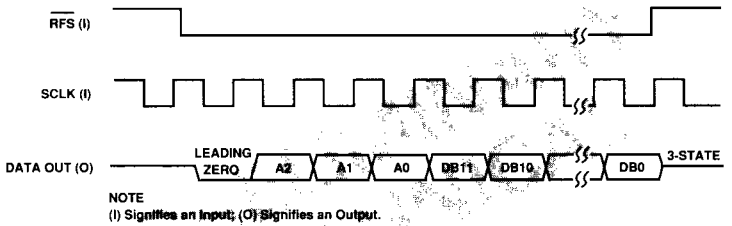


Figure 3. External Clocking (Slave) Mode Output Register Read

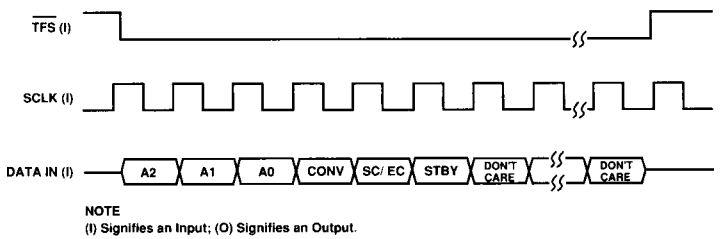


Figure 4. External Clocking (Slave) Mode Control Register Writer