UM1556
User manual

VIPower M0-5 and M0-5Enhanced high-side drivers

Introduction

The aim of this document is to give the design engineer a comprehensive “tool kit” to better understand the behavior of VIPower high side switches, allowing easier design and saving time and money.

Today’s VIPower high side switches represent the 5th generation of smart power drivers (the so called M0-5). In this latest generation of drivers, all the experience and know-how derived from previous generations have been implemented in order to improve robustness, increase functionality and raise package density while maintaining lower prices.

The complexity of a modern High Side Driver (HSD) is still relatively low compared to many other logic ICs. However, the combination of digital logic functions with analog power structures supplied by an unstabilized automotive battery system across a wide temperature range is very challenging for such a device.

The M0-5 components today meet all the above criteria, providing an optimal price/performance ratio by offering the highest performance and robustness at excellent prices.

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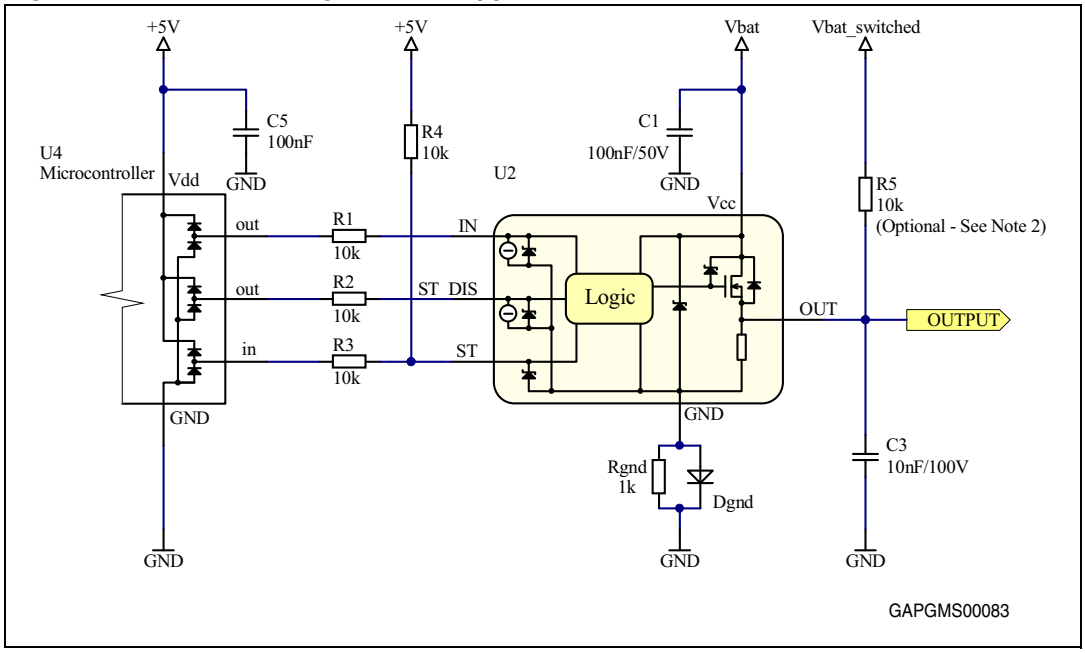
1.1 Application schematic (monolithic digital, monolithic and hybrid analogue HSD)

Figure 1. Monolithic digital HSD - application schematic



1. If status disable function is not required, ST_DIS pin should be left open or connected to ground through a resistor (~10 kΩ). Direct connection to ground is not safe (ISO pulses clamped through ST_DIS pin can damage the device).
2. Pull-up R5 is optional (for open load detection in off-state).
3. No pull-down resistors are necessary on IN and ST_DIS pins due to the internal pull-down structure.

Figure 2. Monolithic analogue HSD - application schematic

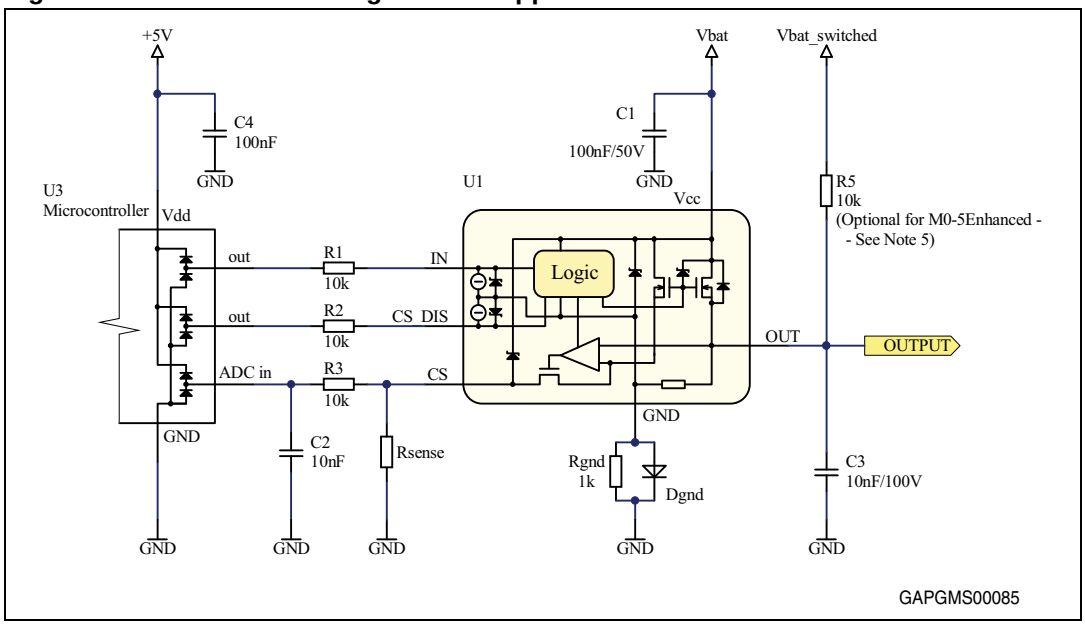
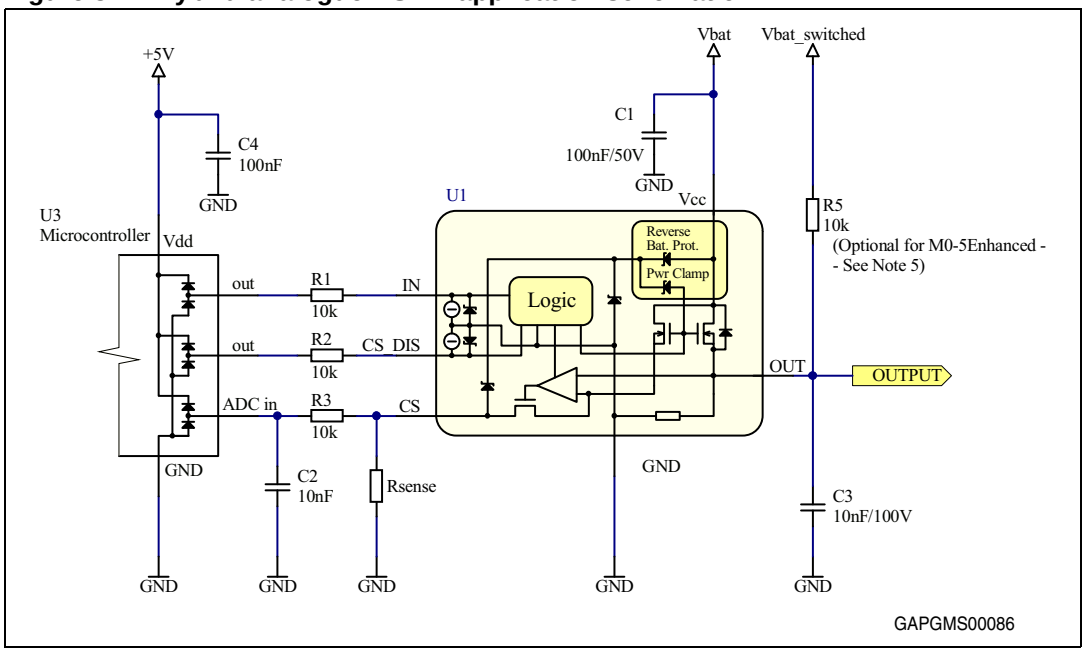


Figure 3. Hybrid analogue HSD – application schematic



4. If current sense disable function is not required, CS_DIS pin should be left open or connected to ground through a resistor (~10 kΩ). Direct connection to ground is not safe (ISO pulses clamped through CS_DIS pin can damage the device).

   ISO pulses refered to ISO 7637-2: 2004(E).

5. Pull-up R5 is optional (open load detection in off-state capability in case of M0-5Enhanced).

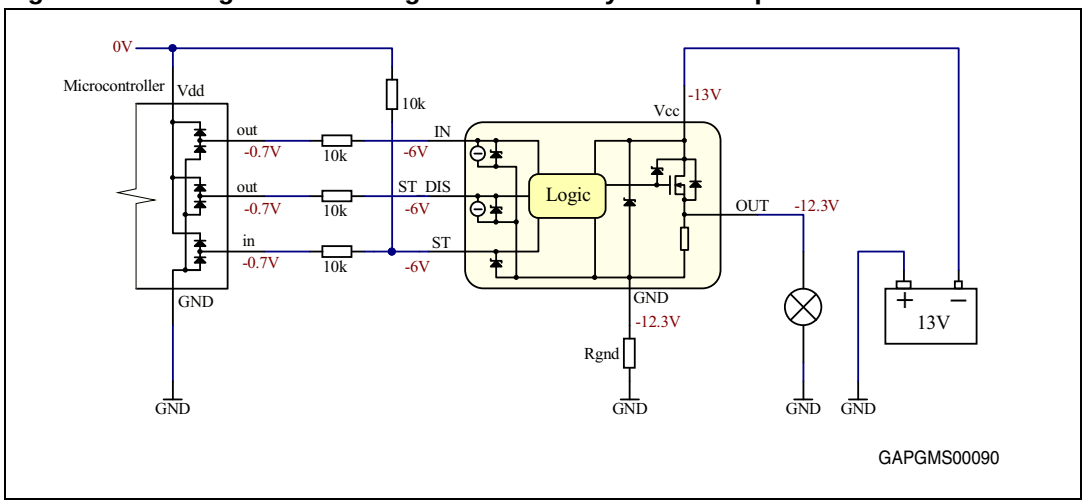
1.2 Reverse battery protection

1.2.1 Reverse battery protection of monolithic HSDs

The reverse battery protection is inserted to the GND terminal of the driver. There are three possible solutions: resistor only, resistor plus diode and MOSFET. There is a relatively low current in the GND path and therefore no high power components are needed. However, this protection circuit still must be able to handle the clamped ISO pulse current, as well as the ISO pulse voltage. We also have to consider the fact that this simple "ground" circuitry doesn't provide any protection to the connected load. If a reverse battery condition occurs, the load is supplied in reverse polarity through internal body diode of the HSD and the power dissipation on the HSD can become critical (depending on connected load and thermal connection of the HSD). With a typical voltage drop on the internal body diode of about 0.7 V, the resulting power dissipation = 0.7 I_{LOAD} [W].

Reverse battery protection using resistor

Figure 4. Voltage levels during reverse battery – resistor protection



A resistor R_{gnd} in the GND line prevents a short circuit through the internal substrate diode of the HSD during a reverse battery condition. The minimum resistor value is limited by the DC reverse ground pin current of the HSD. The maximum resistor value is limited by the drop voltage, caused by the on-state supply current (I_S) of the HSD. The voltage drop across this resistor elevates the minimum input High threshold and normally should not exceed 1 V (depending on microcontroller I/O levels).

Equation 1

$$R_{GND} \leq \frac{V_{GND}}{I_{S(on)max}}$$

Equation 2

$$R_{GND} \geq \frac{V_{BAT}}{I_{GND(reverse)max}}$$

Equation 3

$$P_D = \frac{(V_{BAT})^2}{R_{GND}}$$

This resistor can be shared amongst several different HSDs. In this case, *Equation 1* $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices. When the microprocessor ground is not common with the device ground, the R_{GND} produces a shift ($I_{S(on)max} \times R_{GND}$) in the input thresholds and (in case of a digital HSD) also the status output values. This shift varies depending on how many devices are ON in the case of several HSDs sharing the same R_{GND}. This can lead to a very low value of R_{GND} (needed to comply with *Equation 1* and *Equation 2*) not being fulfilled. To overcome this problem, ST suggests the use of another solution with diode or MOSFET.

Resistor calculation – example (reverse battery requirement – 14 V@60 s):

1. Define maximum acceptable (safe) ground shift level V_{GND}:

Figure 5. Logical levels check

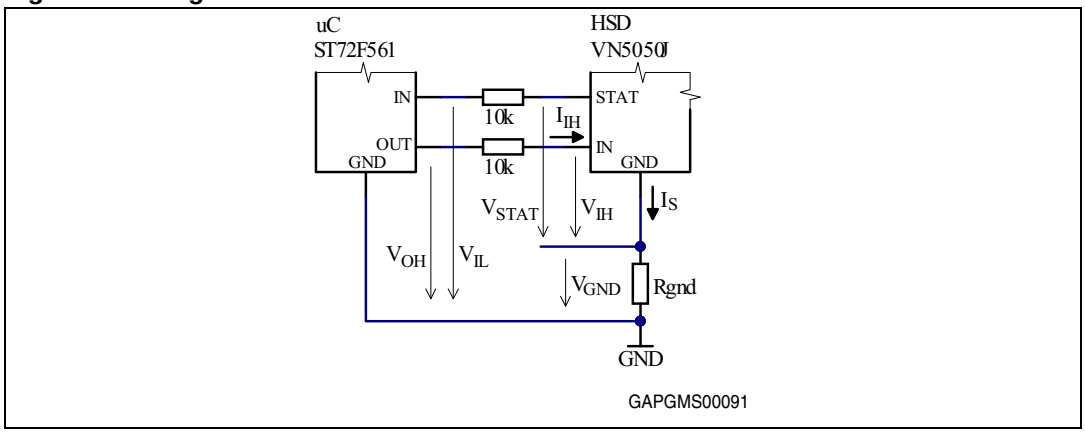


Table 1. Datasheet values

Symbol	Parameter	Value
VN5050J		
V_{IH}	Input high-side voltage (min)	2.1 V
I_{IH}	High level input current (max)	10 µA
I_{GND}	DC reverse GND current (max)	-200 mA
$I_{S(ON)}$	On-state supply current (max)	3 mA
V_{STAT}	Low level status voltage (max)	0.5 V at 1.6 mA
ST72F561		
V_{OH}	Output high level voltage (min)	4.3 V at -2 mA
V_{IL}	Input low level voltage (max)	0.3 V_{DD}

The maximum acceptable ground shift level is the maximum drop voltage on R_{GND} that does not influence the communication between HSD and µC.

- STATUS signal level check: as seen in *Table 1*, the microcontroller can safely recognize log. “L” when the input voltage is below V_{IL} = 0.3 V_{DD} = 0.3 × 5 = 1.5 V. The maximum low level voltage on the HSD status pin V_{STAT} = 0.5 V. This means there is a 1.5 V – 0.5 V = 1 V safety margin for voltage drop on R_{GND}.
- INPUT signal level check: as seen in *Table 1*, the microcontroller output high level (4.3 V) is clearly above the HSD minimum input high level (2.1 V). The voltage drop on the protection serial resistor is relatively small: $R_{PROT} \times I_{IH}$ = 10 k × 10 µA = 0.1 V. Hence, there is a 4.3 V – 0.1 V – 2.1 V = 2.1 V safety margin.
- Result: the maximum acceptable drop voltage on R_{GND} is 1 V. For safety reasons, we consider $\mathbf{V_{GND} = 0.8\ V}$ for the following calculations.

2. Calculate resistor value

$$\left.\begin{aligned} R_{GND} \leq \frac{V_{GND}}{I_{S(on)max}} = \frac{0.8V}{3mA} \leq 266.67\Omega \\ R_{GND} \geq \frac{V_{BAT}}{I_{GND}} = \frac{14V}{200mA} \geq 70\Omega \end{aligned}\right\} \Rightarrow R_{GND} = 220\Omega$$

3. Check power dissipation in reverse mode => select resistor package

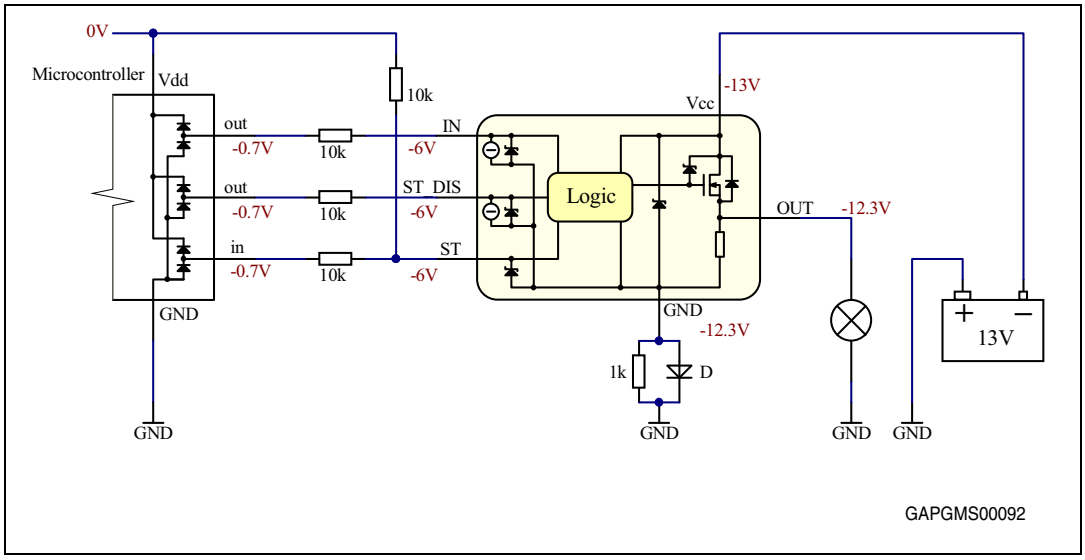
$$P_D = \frac{(V_{BAT})^2}{R_{GND}} = \frac{14V^2}{220\Omega} = 0.89W \Rightarrow Package = 2512$$

Power rating@70 °C of 2512 is 1 W

Note: The device with only a resistor at the GND terminal doesn't clamp ISO pulses on the supply line. Positive ISO pulses (> 50 V) and negative ISO pulses pass the GND and logic terminals. Therefore a serial protection resistor should be used between the µC and HSD. Resistor values should be calculated according to the maximum injected current to the I/O pin of the microcontroller used.

Reverse battery protection using diode plus resistor

Figure 6. Voltage levels during reverse battery using diode-resistor protection network



A diode at the GND terminal prevents a short circuit through the internal substrate diode of the HSD during reverse mode. A resistor (1 kΩ - package 0805) should be inserted in parallel to the diode if the device drives an inductive load (to clean up negative voltage peaks at GND terminal in case of inductive load switch-off). This ground network can be safely shared amongst several different HSDs. The presence of the ground networkalso produces a shift (~ 600 mV) in the input threshold and in the status output values. This shift does not vary if more than one HSD share the same diode/resistor.

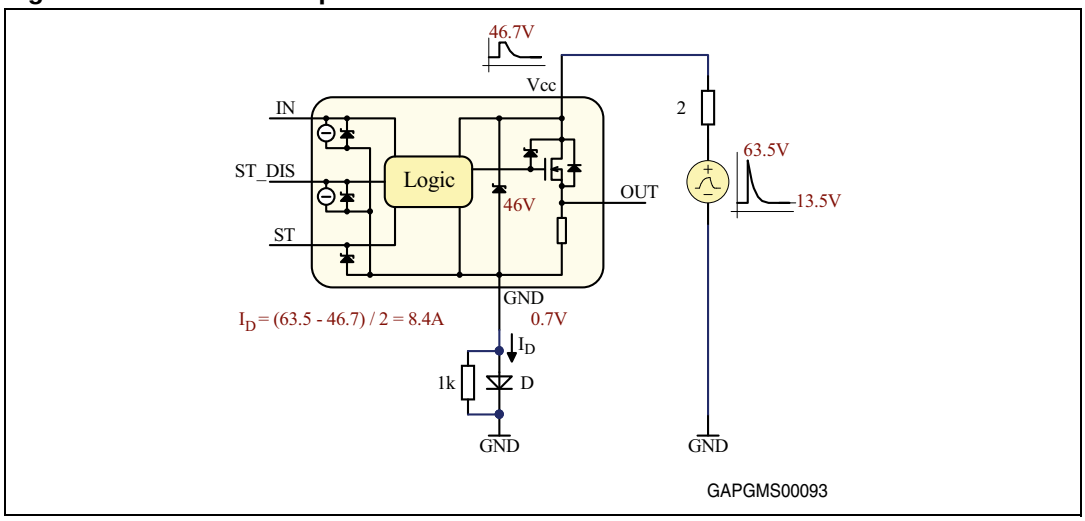
A diode at the GND terminal allows the HSD to clamp positive ISO pulses above 50 V (clamping voltage of the HSD). Negative ISO pulses still pass GND and logic terminals. The diode should withstand clamped ISO currents in case of positive ISO pulses, and reverse voltages in case of negative ISO pulses.

Dimensioning of the diode [(a)]:

The most severe positive ISO pulse to consider is test pulse 2 at level IV (50 V @ 50 µs). This voltage is considered on top of the nominal supply voltage of 13.5 V, so total voltage is 63.5 V. The VIPower has a clamping voltage of typ. 46 V (minimum 41 V/maximum 52 V). In a typical device, the remaining voltage is 63.5 V - 46 V - 0.7 V = 16.8 V. The ISO pulse generator interior resistance is given with 2 Ω. Hence the resulting peak current through the diode is 8.4 A for a duration of 50 µs.

a. Result:
maximum peak forward current: 8.4 A @ 50 µs
maximum reverse voltage: -100 V

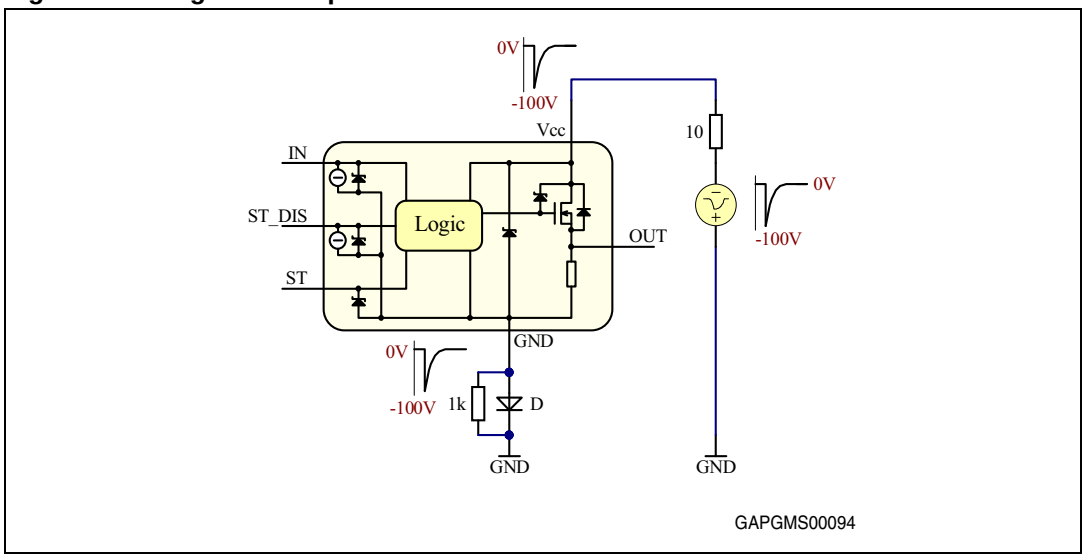
Figure 7. Positive ISO pulse



The most severe negative ISO pulse to consider is test pulse 1 at level IV (-100 V@2 ms). This pulse is directly transferred to the GND pin. The maximum peak reverse voltage of the diode should therefore be at least 100 V.

Note: The diode works in avalanche mode if pulse level is above the rated reverse voltage.

Figure 8. Negative ISO pulse

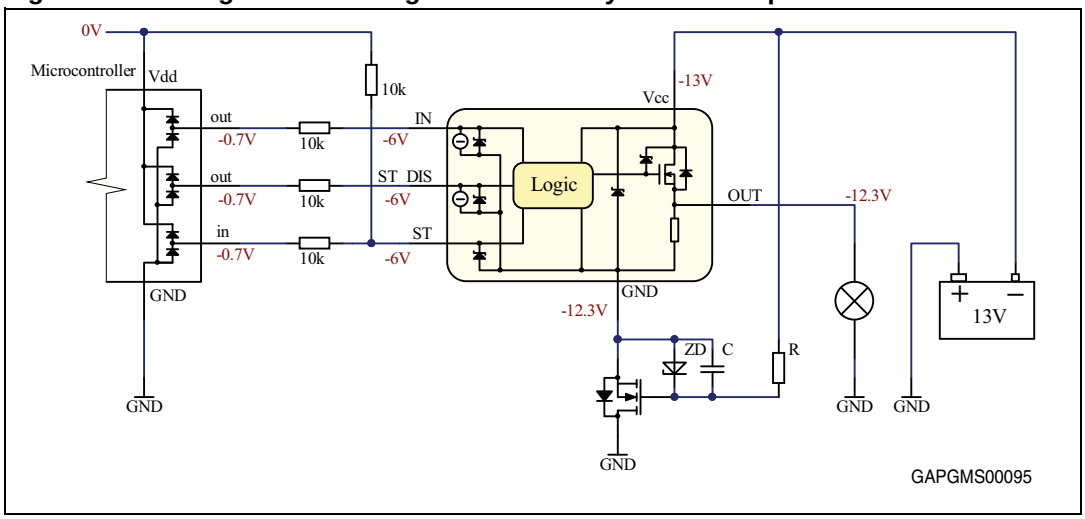


Note: As seen from the above explanation, the HSD with diode protection in the GND pin doesn't clamp negative ISO pulses at supply line. Therefore an appropriate serial protection resistor should be used between the µC and HSD.The resistor value should be calculated according to maximum injected current to the I/O pin of the used microcontroller.

Note: Diode parameters can be lower if an external clamping circuitry is used (e.g. HSD module is supplied from a protected power supply line).

Reverse battery protection using MOSFET

Figure 9. Voltage levels during reverse battery – MOSFET protection



The HSD is protected by a MOSFET which is switched-off during reverse battery conditions. This MOSFET circuitry also provides full ISO pulse clamping at supply line and causes no ground level shift. A capacitor between gate and source keeps the gate charged during negative ISO pulses as well. The time constant given by RC values should be longer than 2 ms (duration of reverse battery protection (monolithic HSDs only) - comparison of negative ISO7637 pulse 1).

Table 2. Reverse battery protection (of monolithic HSDs only) – comparison

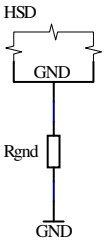
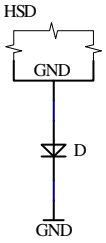
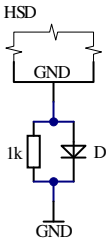
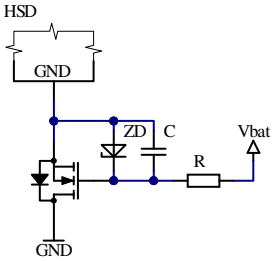
Protection type (monolithic HSD)	+	-
Resistor 	– Any type of load.	– Voltage drop fluctuation. – Calculation of R value necessary. – Positive and negative ISO-pulse transfer to input and diagnostics pin (serial protection resistors necessary). – Relatively high power dissipation on the R_{GND} (~1 W) during reverse conditions ⇒ higher price of the resistor – Device turns-off in case of positive ISO pulses
Diode 	– Fixed voltage drop. – Positive ISO-pulse clamping (> 50 V).	– Resistive load only. – Negative ISO-pulse transfer to input and diagnostics pin (serial protection resistors necessary).

Table 2. Reverse battery protection (of monolithic HSDs only) – comparison (continued)

Protection type (monolithic HSD)	+	-
Resistor and diode 	– Fixed voltage drop – Positive ISO-pulse clamping (> 50 V). – Any type of load.	– Negative ISO-pulse transfer to input and diagnostics pin (serial protection resistors necessary).
MOSFET 	– Any type of load. – No voltage drop. – No ISO-pulse transfer to input and diagnostics pin.	– Higher cost (more external components needed).

1.2.2 Reverse battery protection of hybrid HSDs

In contrast to monolithic devices, all hybrid VIPower HSD do not need any external components to protect the internal logic in case of a reverse battery condition. The protection is provided by internal structures (see "Reverse Battery Protection" in the block diagram of *Figure 10*).

In addition, due to the fact that the output MOSFET turns on even in reverse battery mode thus providing the same low ohmic path as in regular operating conditions, no additional power dissipation has to be considered.

Furthermore, if for example, a diode is connected to the GND of a hybrid HSD, the output MOSFET is unable to turn on and thus the unique feature of the driver is disabled (see *Figure 11*).

Figure 10. Hybrid HSD - reverse battery protection with self switch-on of the MOSFET

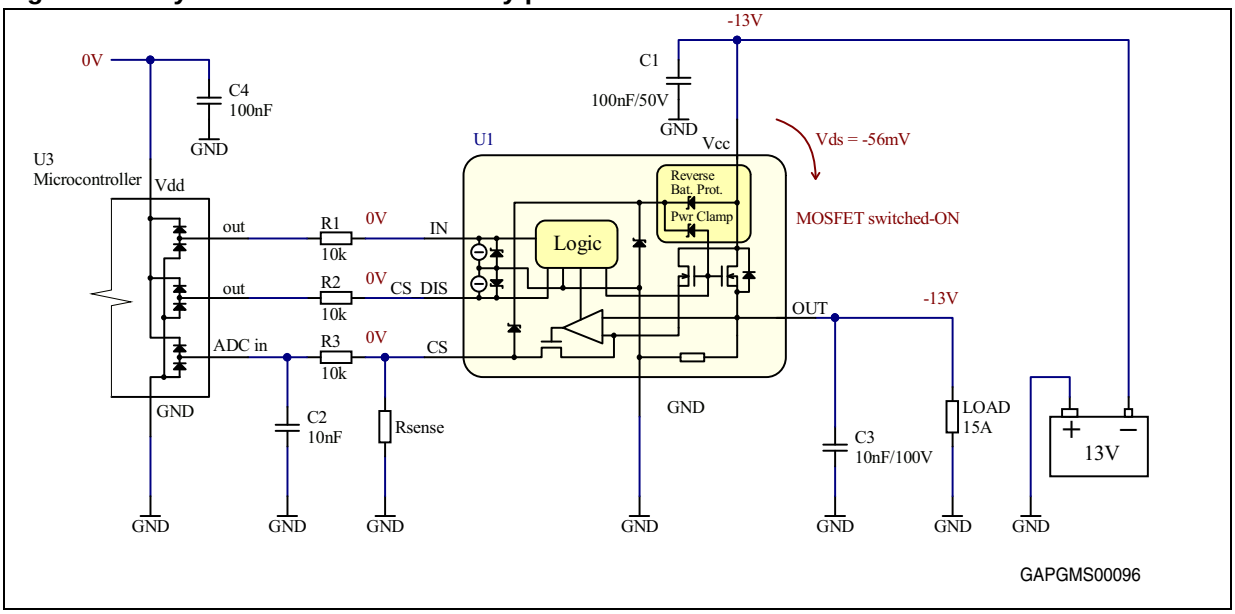
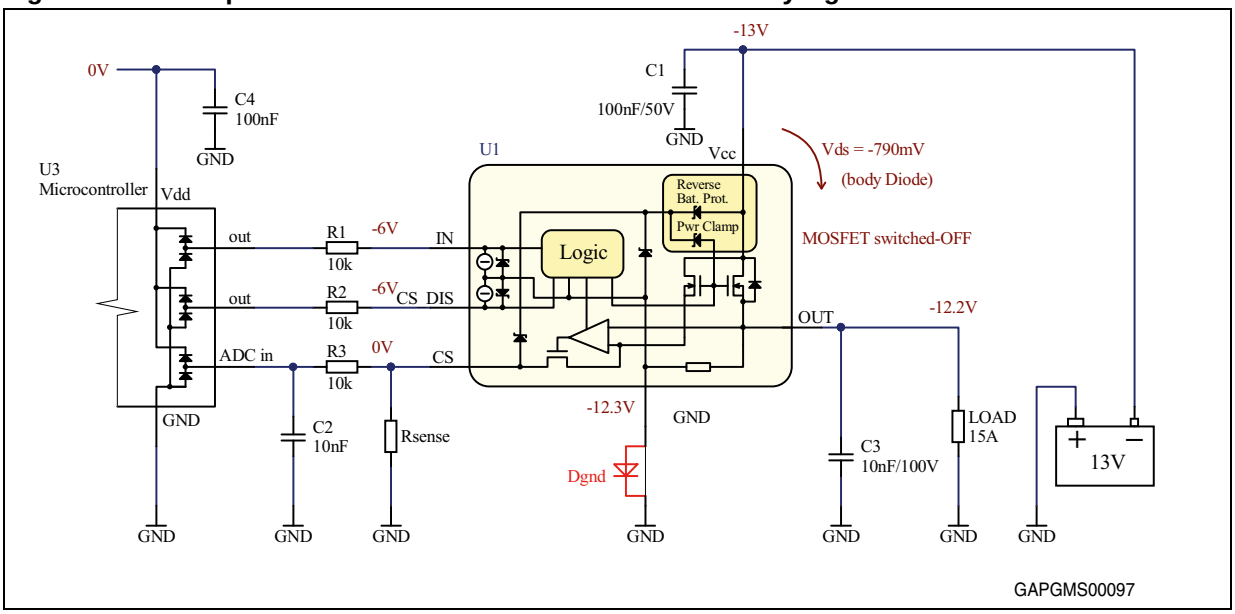


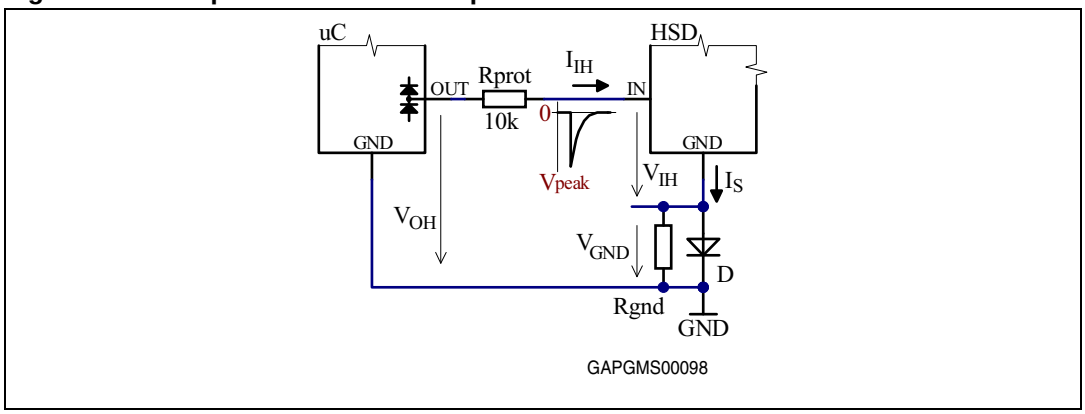
Figure 11. Example - Self switch-on of MOSFET eliminated by Dgnd



1.3 Microcontroller protection

If ISO pulses or reverse battery conditions appear, the HSD control pins are pulled to dangerous voltage levels due to the internal HSD structure and ground protection network (see *Section 1.2: Reverse battery protection* for further details).

Figure 12. ISO-pulse transfer to I/O pin



Therefore, each microcontroller I/O pin connected to a HSD must be protected by a serial resistor to limit the injected current. The value of R_{PROT} must be high enough to ensure that injected current is always below the latch-up limit of the microcontroller I/O. We should also consider the voltage drop on R_{PROT} because the current required by the HSD input is typically 10 µA. The following condition must be fulfilled:

$$\frac{V_{PEAK}}{I_{(\mu C)LATCHUP}} \leq R_{PROT} \leq \frac{V_{OH} - (V_{IH} + V_{GND})}{I_{IH}}$$

Example:

$$\frac{100V}{20mA} \leq R_{PROT} \leq \frac{4.3V - (2.1V + 1V)}{10\mu A}$$

$$5k\Omega \leq R_{PROT} \leq 120k\Omega$$

Recommended R_{PROT} value is 10 kΩ (safe value for most automotive microcontrollers).

1.4 Introduction of M0-5Enhanced products

In addition to the established M0-5 drivers, STMicroelectronics has introduced a new set of products called M0-5Enhanced. As the name indicates, these new drivers are based on the ST proprietary M0-5 technology, but have some more sophisticated features.

The new features of the M0-5Enhanced family are aimed at improving the load handling as well as the overload diagnostics capabilities.

1.4.1 New features overview

- Improved diagnostics on analogue current sense devices:
  - Open load/short to Vbat indication in off-state
- Improved compatibility with higher variety of loads
  - Optimized current limitation range
- Faster detection of overload and short to GND through
  - Indication of power limitation

  Analogue: stable indication by pulling the CS pin to V_{SENSEH} (as for TSD)

  Digital: stable indication by pulling low the status pin (as for TSD)

1.4.2 Open load in off-state/short to Vbat

- Now also featured on analogue M0-5Enhanced high side drivers (already implemented for digital high side drivers)
- Open load detection in off-state through external pull up resistor
- Differentiation between open load and short to Vbat by disconnecting the optional pull up resistor

Figure 13. Open load/short to Vcc condition

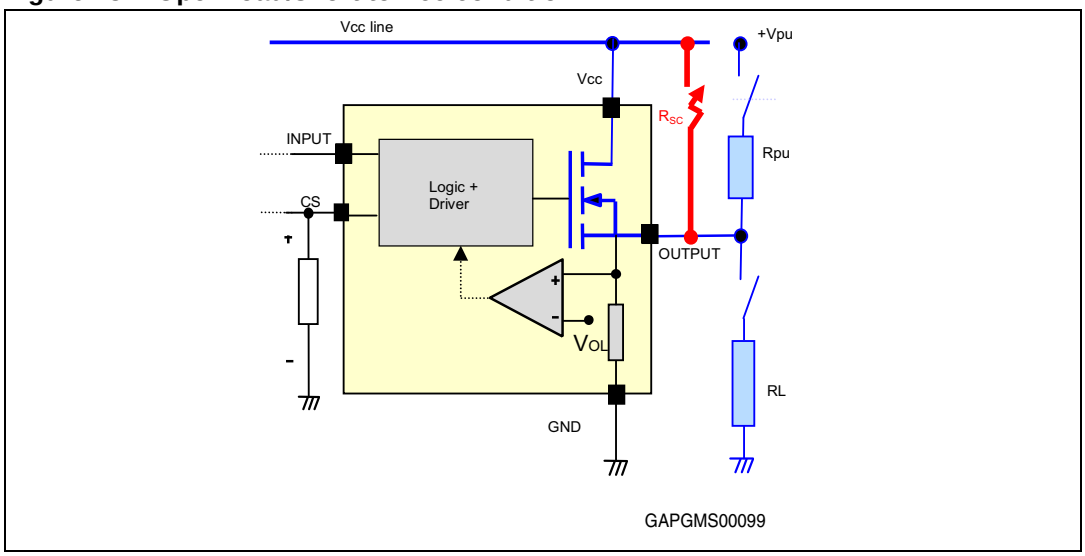


Figure 14. Open load/short to Vcc condition

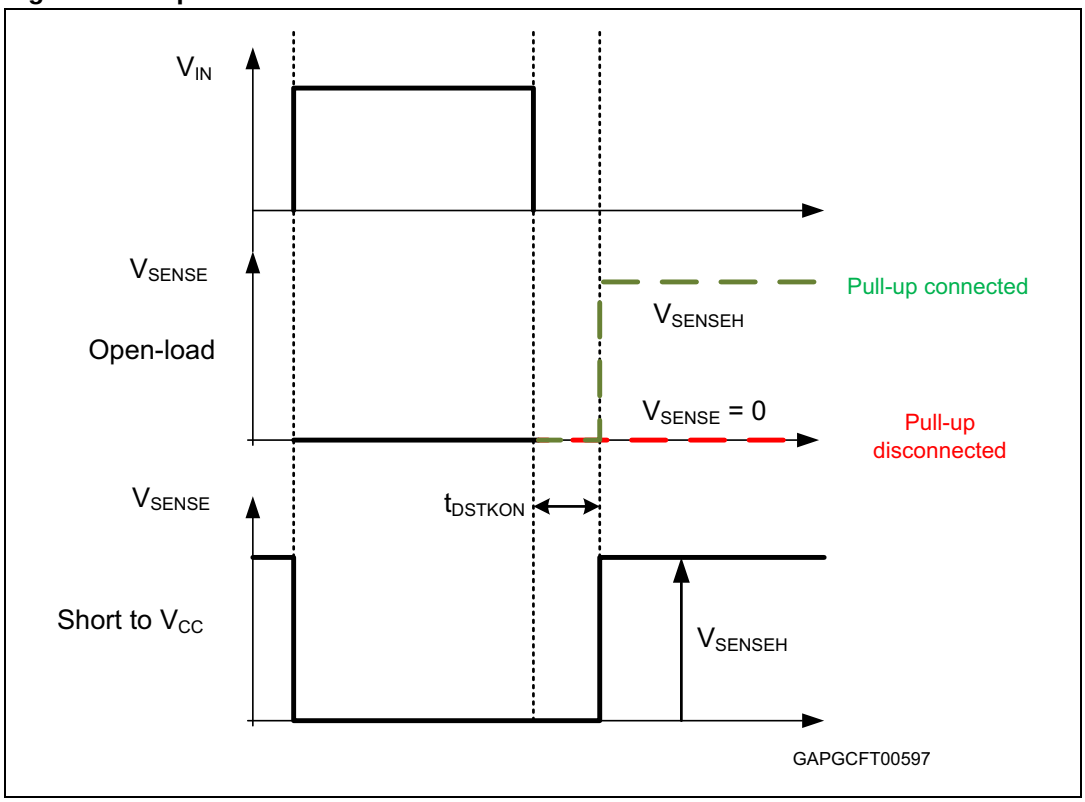


Table 3. CS pin levels in off-state

	Pull up	CS
Open load	Yes	VsenseH
	No	0
Short to Vcc	Yes	VsenseH
	No	VsenseH
Nominal	Yes	0
	No	0

1.4.3 Indication of power limitation

The principle:

- Diagnostics reacts as soon as power limitation is reached without waiting for thermal shut down (in digital as well as in analogue HSDs)
- No ambiguity of diagnostics between open load and overload
- Fast and secure detection of short circuit/overload also for intermittent loads (for example turn-indicator lamps or loads driven with PWM)
- Intermittent short circuit detection covered as well

1.4.4 Indication of power limitation – example for analogue driver

Figure 15. M0-5 – “Soft” short to GND

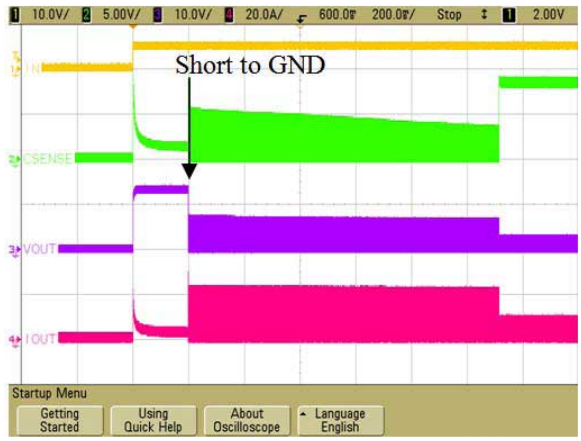


Figure 16. M0-5 – “Hard” short to GND

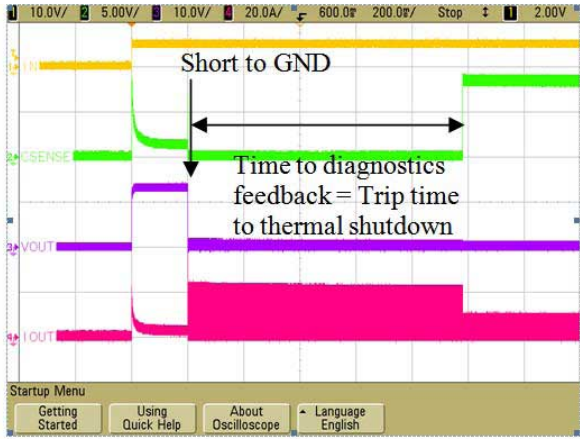


Figure 17. M0-5Enhanced – “Soft” short to GND

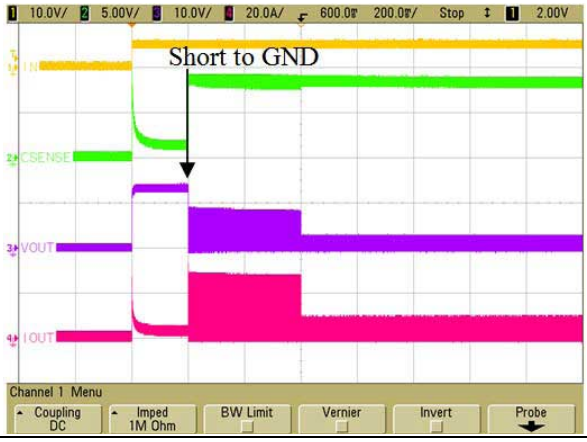
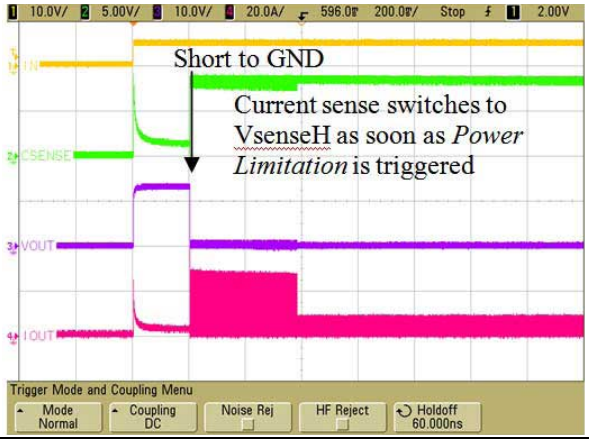


Figure 18. M0-5Enhanced – “Hard” short to GND



1.4.5 Indication of power limitation – example for digital driver

Figure 19. M0-5 – “Soft” short to GND

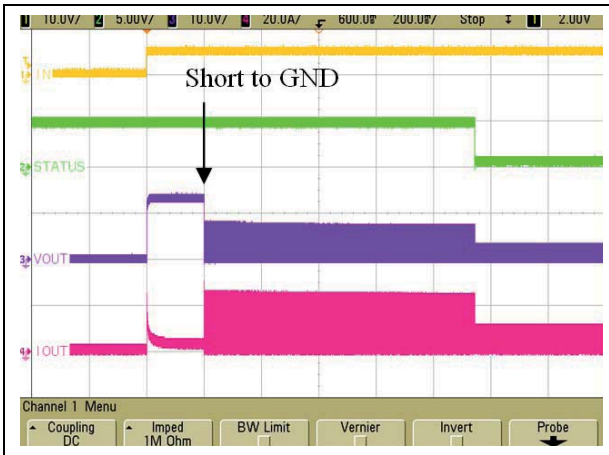


Figure 20. M0-5 – “Hard” short to GND

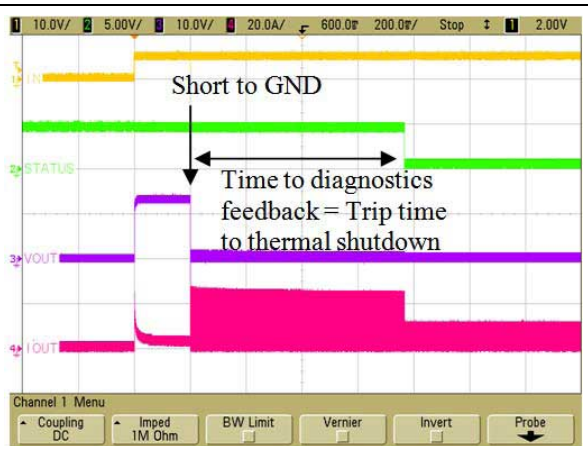


Figure 21. M0-5Enhanced – “Soft” short to GND

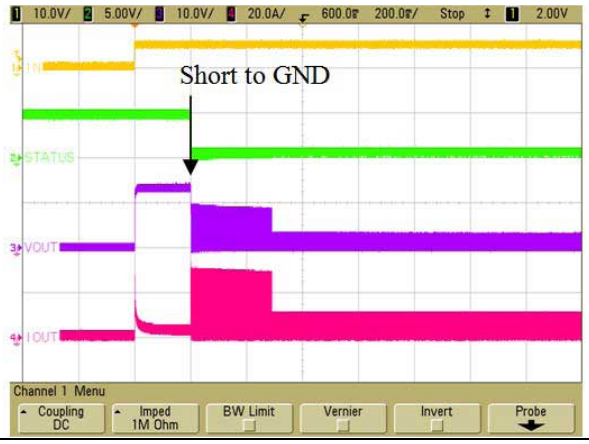
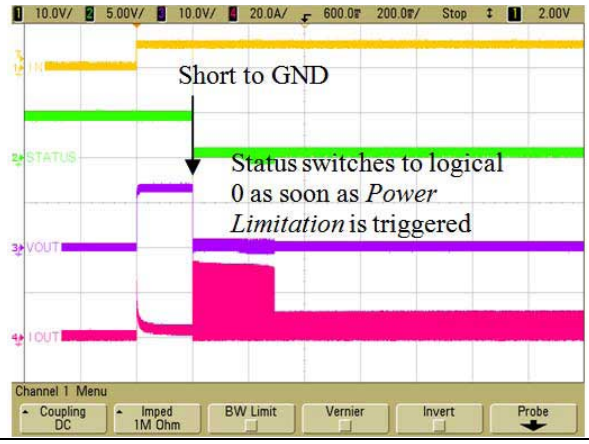


Figure 22. M0-5Enhanced – “Hard” short to GND



1.4.6 M0-5Enhanced: analogue current sense truth table

Table 4. Analogue driver-truth table (OFF-state)

Operation mode	Input level	Output level	Current sense
Normal operation	L	L	0 V
Short to Vbat		Vbat	V_{SENSEH}
Open load		H (with external pull up)	V_{SENSEH}
		L (without external pull up)	0 V
Short to GND		L	0 V
Overtemperature		L	0 V

Table 5. Analogue driver-truth table (ON-state)

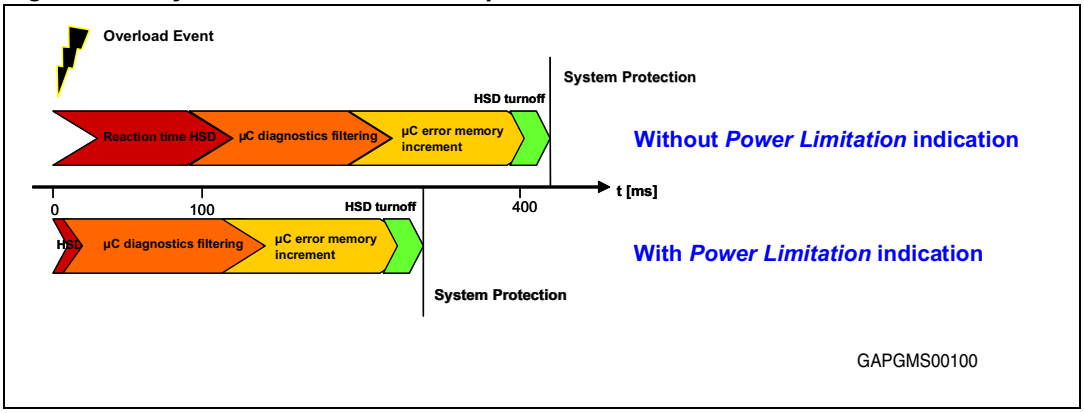
Operation mode	Input level	Output level	Current sense
Normal operation	H	Vbat	I_{OUT}/K
Short to Vbat		Vbat	$<I_{OUT}/K$
Open load		Vbat	0 V
Short to GND		L	V_{SENSEH}
Overload		PWM Power limitation	V_{SENSEH}
		Vbat No power limitation	>nominal
Overtemperature		L	V_{SENSEH}

- Overtemperature, overload and short to GND can be distinguished from an open load condition without the need of offstate diagnostics – no switchable pull up resistor is required.
- Detailed diagnostics without external components is possible.

1.4.7 Indication of power limitation, the advantages

- The system reaction time on overload/short circuit events depends on various aspects. The most important one is the first link in the chain: the diagnostics feedback of the smart power device.

Figure 23. System reaction time comparison



- Indication of power limitation as diagnostics feedback allows almost instantaneous overload/short circuit detection, as soon as the deltaT exceeds 60 K.

2 Analogue current sense

2.1 Introduction

With the introduction of the novel VIPower M0-5 technology, important improvements have been introduced to the analog current sense operation.

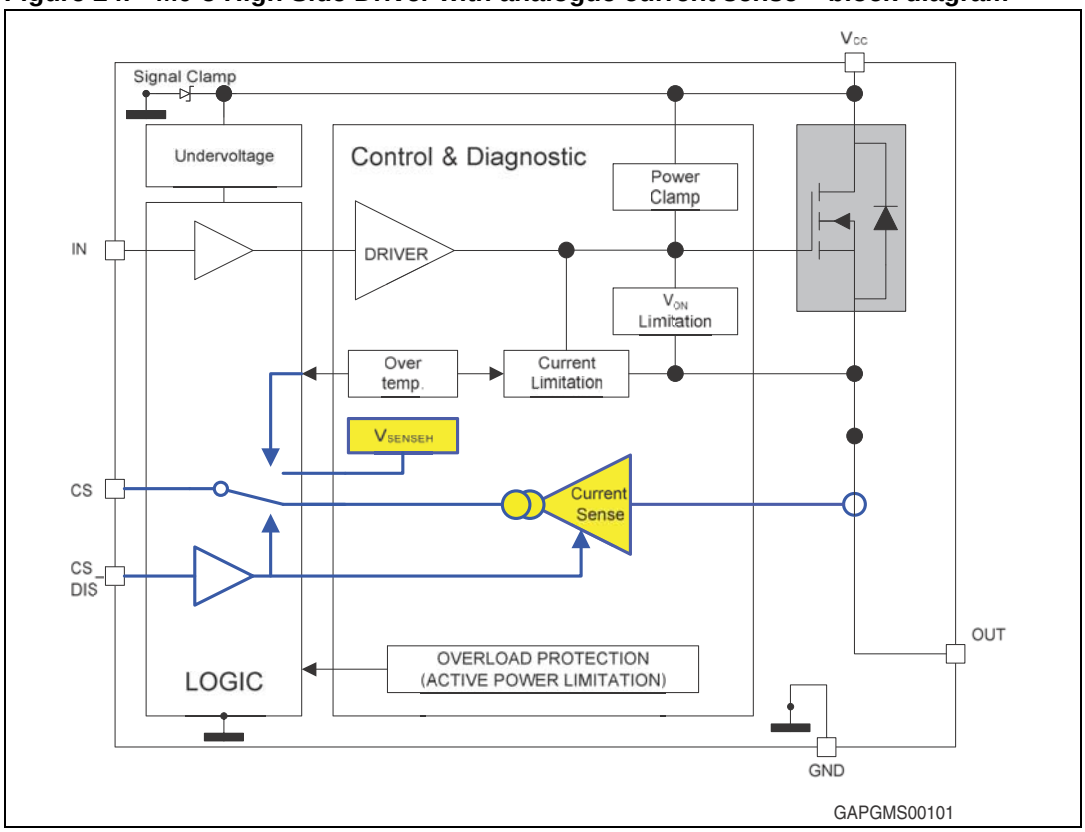
The block diagram of a M0-5 High Side Drive with analog current sense is reported in *Figure 24*.

In line with the previous generations, the current sense block has a double function:

- Current mirror of the load current in normal operation. This delivers a current proportional to the load current according to a known ratio named K
- Diagnostics flag in fault conditions. This delivers a fixed voltage with a certain current capability in case of overtemperature conditions.

The current delivered by the current sense circuit can be easily converted to a voltage by means of an external sense resistor, thus allowing continuous load monitoring and abnormal-condition detection.

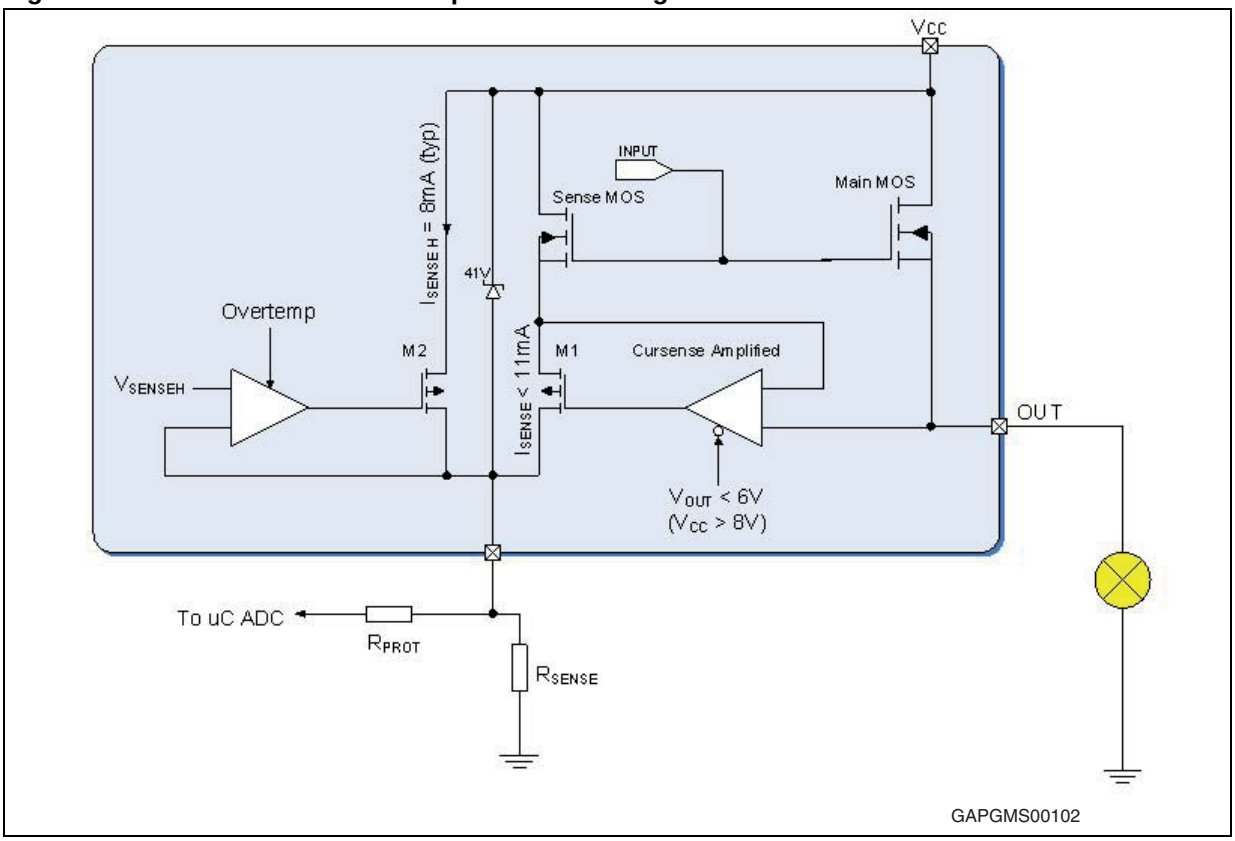
Figure 24. M0-5 High Side Driver with analogue current sense – block diagram



2.2 Simplified principle of operation

The simplified block diagram of the M0-5 analog current sense is shown in *Figure 25*.

Figure 25. M0-5 current sense simplified block diagram



The SenseMOS is scaled down copy of the MainMOS according to a defined geometric ratio, driven by the same gate control circuit as the MainMOS.

2.3 Normal operation (channel ON, CS_DIS low)

The current flowing through the MainMOS is mirrored by the SenseMOS.

The current delivered by the current sense pin is regulated by the current sense amplifier through the P channel MOSFET M1 so that:

Equation 4

$$V_{DS\_Main} = V_{DS\_Sense} \rightarrow R_{ds\_sense} \cdot I_{sense} = R_{DS\_Main} \cdot I_{out}$$

and consequently

Equation 5

$$V_{sense} = R_{sense} \cdot I_{out} / K$$

where

$$K \propto R_{ds\_sense} / R_{DS\_Main}$$

encloses the geometric ratio, the current sense amplifier offset and various process parameter spreads.

Care must be taken in order to ensure the I_{SENSE} is proportional to I_{OUT}. Indeed, the maximum drop across the R_{SENSE} is internally limited to approx. 7.5 V as specified in the datasheet by the parameter V_{SENSE} “maximum analog sense output voltage” (5 V minimum @ 8 V < Vcc < 16 V; - 40 °C < Tj < 150 °C).

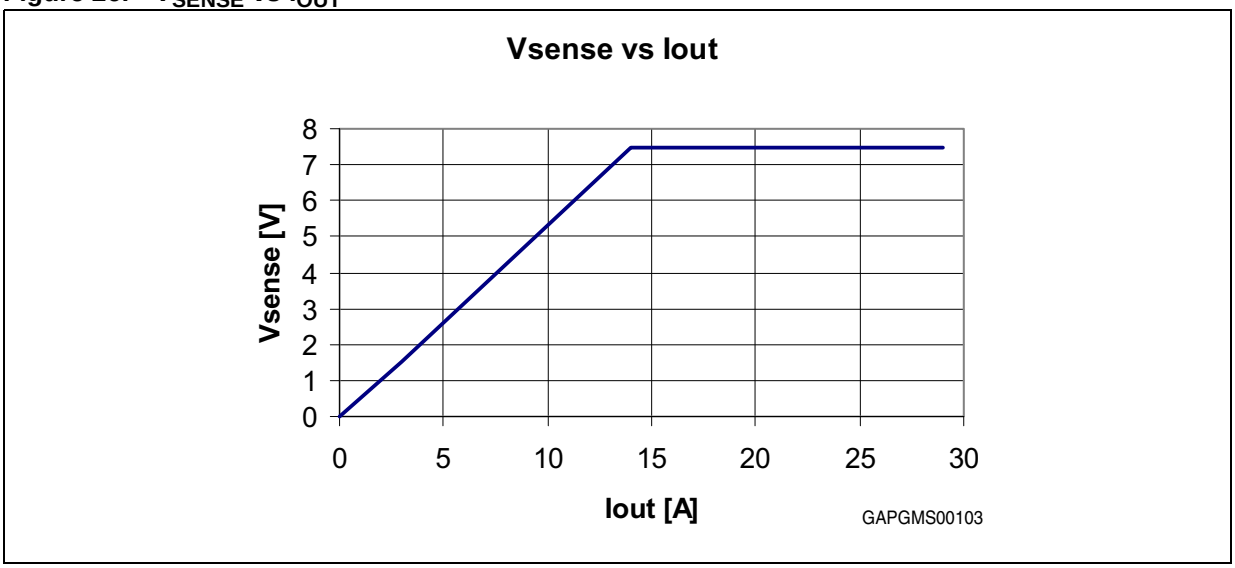
Example 1: VND5025AK with R_{SENSE} selected to have V_{SENSE} = 1.5 V @ I_{OUT} = 3 A

Considering (for sake of simplicity) K_2 @ 3 A = 2790 (typical value) → I_{SENSE} = 1 mA→ R_{SENSE} = 1.5 k

Assuming a typical V_{SENSE} saturation of 7.5 V → maximum I_{SENSE} = 5 mA to maintain linearity → maximum I_{OUT} = 14 A.

In other words, with the selected R_{SENSE} any load current greater than 14 A produces the same V_{SENSE} (see *Figure 26*).

Figure 26. V_{SENSE} vs I_{OUT}



On the other hand, care must be taken to prevent the P channel MOSFET M1 from saturation, causing the I_{SENSE} to again be disproportional with I_{OUT}. This normally happens when the maximum current that M1 is able to supply is reached (11 mA typ.)

This value is consistent with the current sense operating range and current limitation value.

Example 2: VND5025AK with R_{SENSE} selected in order to have V_{SENSE} = 1.5 V @ I_{OUT} = 10 A

Considering (for sake of simplicity) K3 @ 10 A = 2760 (typical value) → I_{SENSE} = 3.6 mA → R_{SENSE} = 414 Ω

Assuming K to remain approx. 2760 for I_{OUT} > 10 A, the maximum load current which can be detected is:

$$I_{OUT} = I_{SENSE\_MAX} \cdot K \cong 29A$$

still compatible with the minimum I_{LimH}.

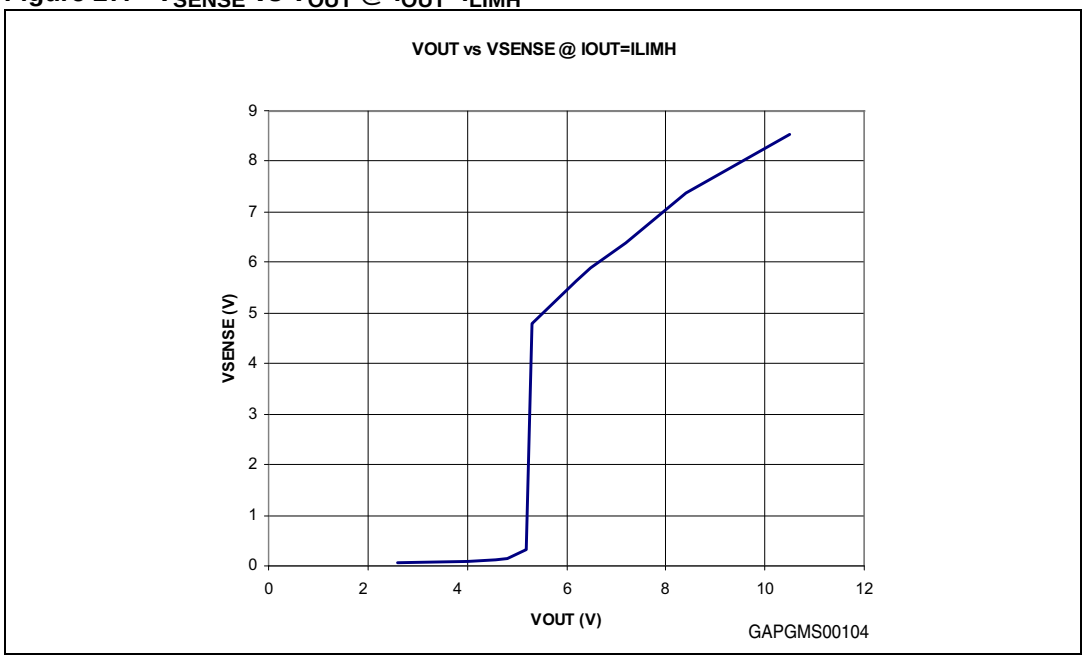
With the selected R_{SENSE}, the maximum V_{SENSE} which can be developed to maintain linearity is approx. 4.3 V.

However, the current sense operation for load current approaching the current limitation is neither guaranteed nor predictable. Indeed, because of the intervention of the current limiter, the output voltage can drop significantly: up to approximately 0 V in the extreme case of a hard short circuit.

As the whole circuit is referred to V_{OUT}, ambiguous and unreliable current values can derive from the CS under such conditions.

In order to bring the CS into a well defined state, a dedicated circuit section shuts down the current sense circuitry when V_{OUT} drops below a certain threshold (6 V typ, see *Figure 27*).

Figure 27. V_{SENSE} vs V_{OUT} @ I_{OUT}=I_{LIMH}



Once again, this value is consistent with the current sense operating range and current limitation value.

Example 3: VND5025AK

At the edge of current limitation $I_{OUT} = I_{LimH}$ = 29 A, the maximum drop on the output MOSFET is

$$V_{DS} = R_{DS\_MAX} \cdot I_{LimH} \cong 1.45V$$

Therefore, at Vcc = 8 V, V_{OUT} is still sufficient to ensure correct CS function up to the current limited region.

In conclusion, in normal operation the current sense works properly within the described border conditions. For a given device, the I_{SENSE} is a single value monotonic function of the I_{OUT} as long as the maximum I_{SENSE} (1^{st} example) or the current sense saturation (2^{nd} example) are reached, i.e., there's no chance of having the same I_{SENSE} for different I_{OUT} within the given range.

The current sense may still work above the current limited region depending on the V_{OUT}. In this latter case, however, the intervention of protection mechanisms such as power limitation and saturation of the circuit (depending on the R_{SENSE} choice) might cause the information provided by the current sense to not be processable.

Finally, the CS switch-off in case of a hard short circuit renders this latter condition indistinguishable from an open load triggered switch-off.

2.4 Overtemperature indication (channel ON, CS_DIS low)

In case of overtemperature, the fault is indicated by the CS pin which is switched to a "current limited" voltage souce.

Indeed, with reference to *Figure 25*, whenever an overtemperature condition is reached, the branch circuit on the left side is activated.

The P channel MOSFET M2 is controlled in such a way as to develop 9 V typ (v_{SENSEH} in the datasheet) across the external sense resistor.

In any case, the current sourced by the CS in this condition is limited to 8 mA typ (I_{SENSEH} in the datasheet).

Example 4 VND5025AK and minimum sense resistance for v_{SENSEH} > 5 V

Considering typical I_{SENSEH} = 8 mA $\rightarrow$ R_{SENSE_MIN} = 625 Ω

2.5 Current sense ESD and spikes protection

An additional improvement brought to the current sense circuit with the M0-5 is related to the ESD and voltage transient protection of the CS pin.

With reference to *Figure 25*, this protection is now obtained thanks to the active clamping structure connected between Vcc and the CS pad, represented in a simplified way by a zener.

Consequently, the absolute maximum rating on V_{CSENSE} now ranges from Vcc - 41 V to Vcc.

This novel solution has removed the inaccuracy at very low V_{SENSE} experienced by the M0-3 drivers due to the offset caused by some leakage in the previous ESD protection structure.

This offset increases when V_{SENSE} is lower than V_{GND} because of the ground network which protects against reverse battery.

With M0-5, the current sense is able to function correctly with the accuracy given by the K factor spread for V_{SENSE} up to -1 V (with reference to the device GND).

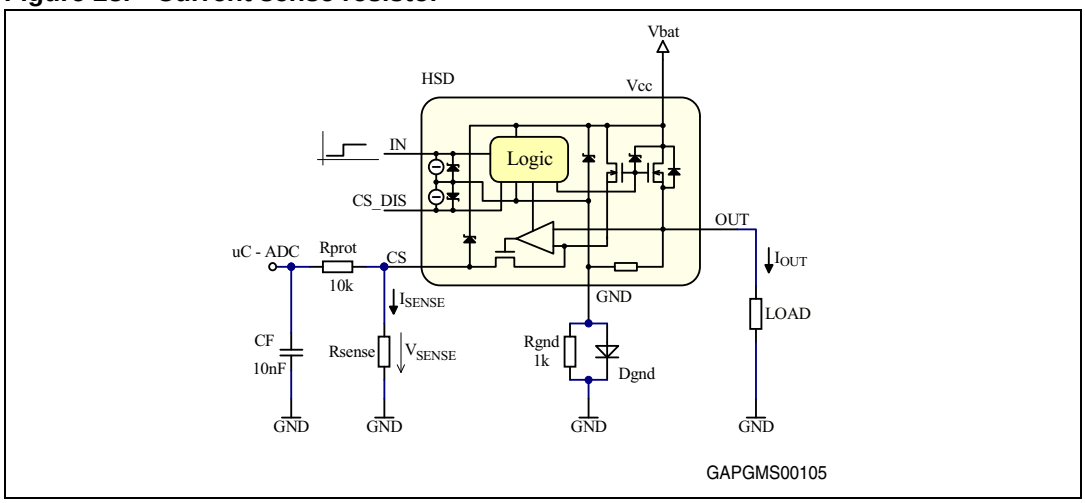
2.6 Current sense resistor calculation

The analogue M0-5 HSDs integrate a current sense which under normal circumstances provides a voltage across an external shunt resistor (R_{SENSE}), which is proportional to the load current with an N/n ratio (the so-called K factor):

$$V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot \frac{I_{OUT}}{K}[V]$$

This allows monitoring of the current which flows through the load and the detection of fault conditions such as open load, overload and short-circuit to GND leading to a thermal shutdown. In case of a thermal shutdown (M0-5, M0-5Enhanced) or a Power Limitation (M0-5Enhanced), the C_{SENSE} pin is switched to a voltage source V_{SENSEH} (V_{SENSEH} = 9 V typ, $I_{SENSEHmax}$ = 8 mA) for as long as the device remains in the thermal shutdown (Power Limitation) mode. The voltage from the current sense resistor is usually connected through a 10 kΩ protection resistor to the ADC input of the µC. For the V_{SENSEH} level, the voltage is limited by the µC internal ESD protection (~5.6 V) and the ADC shows maximum value (0xFF in case of 8 bit resolution). The capacitor CF is used to improve the accuracy of the ADC. This capacitor plus a 10 kΩ serial resistor function as a low pass filter (>10 kHz) for potential HF noise on the C_{SENSE} line (especially if there is a long wire route to the microcontroller).

Figure 28. Current sense resistor



The R_{SENSE} value definition example:

Consider the VN5016AJ (16 mΩ) with a nominal load current I_N = 5 A@V_{SENSE} = 2 V and typ K = 5000 (datasheet):

$$R_{SENSE} = K \cdot \frac{V_{SENSE}}{I_{OUT}} = 5000 \cdot \frac{2}{5} = 2\kappa\Omega$$

2.7 Diagnostics with different load configurations

2.7.1 Diagnostics with paralleled loads

A HSD with current sensing allows the detection of individual bulb failures when in a parallel arrangement. However, if we consider the bulb wattage spread, the HSD K-factor tolerance, variations of bulb currents vs. V_{BAT} and ADC resolution, it is clear that accurate failure determination can be difficult in some cases. For example, if there is a largeand small bulb on the output, the detection limit for the lowest power bulb is lost in the tolerances.

In order to achieve better current sense accuracy, one or both of the strategies listed below can be adopted:

1. Current sense calibration (K-factor measurement) of each HSD
2. V_{BAT} measurement →bulb current compensation by appropriate software

Table 6. Paralleling bulbs – overview

5+5W	OK without calibration
7+7W	
21+21W	
27+27W	
21+5W	Calibration and V_{BAT} monitoring recommended
27+7W	
21+21+5W	Calibration and V_{BAT} monitoring necessary
27+27+7W	

2.7.2 Diagnostics with different load options

In some cases, the requirement profile asks for alternative loads to be driven with one and the same High Side Driver. These load alternatives may be a bulb lamp alternating with an LED (-cluster). In this case the driver:

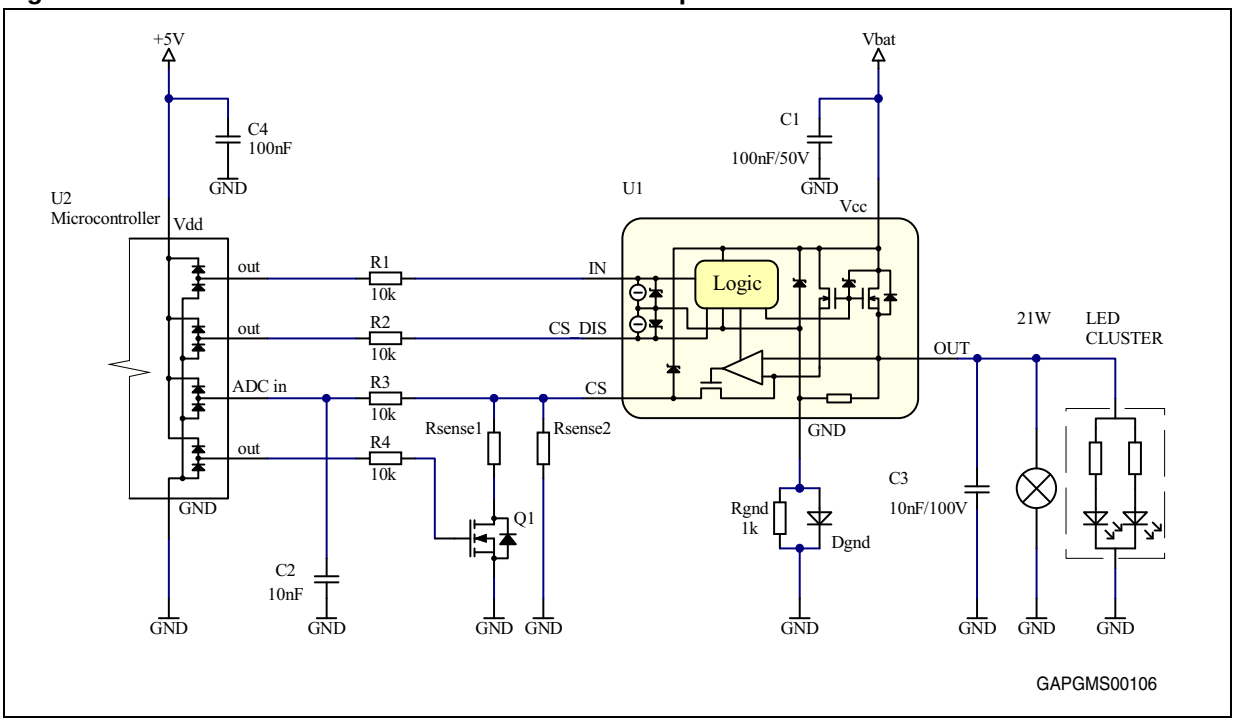
- must handle the high inrush current of the bulb load
- must provide sufficiently low power dissipation during continuous operation
- must not indicate an open load in case an LED (-cluster) is applied instead of a bulb.

M0-5 drivers today offer an open load threshold (in case of drivers with digital status output) that is usually low enough to prevent an open load detection in case an LED is connected.

If an analog current sense device is used, different sense resistors have to be used in order to have the current sense band in the appropriate range matching the different load currents.

An example of a current sense resistor switching circuit can be seen in the *Figure 29*. The measured scale can be extended by R_{SENSE1}, switched in parallel to R_{SENSE2} by MOSFET Q1.

Figure 29. Switchable current sense resistor – example



2.7.3 K-factor calibration method

In order to reduce the V_{SENSE} spread, it is possible to reduce the K spread and eliminate the R_{SENSE} variation by adding a simple test (calibration test) at the end of the module production line.

How the calibration works

"To calibrate" on a specific device soldered in a module signifies measuring the K ratio at a given output current by a V_{SENSE} reading. Since the relation of $I_{OUT} = I_{SENSE} \times K$ is known, it is straightforward to calculate the K ratio. However, even if the K ratio measured at a single point eliminates the parametric spread, it doesn't eliminate the V_{SENSE} variation due to the K variation produced by the output current variation.

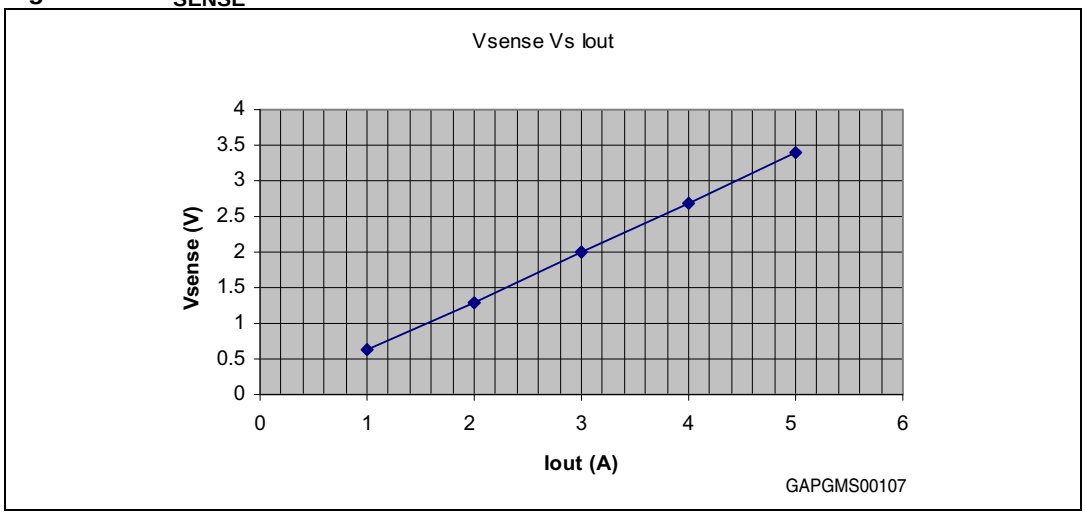
This variation can be eliminated given the following considerations:

Table 7 and *Figure 30* show a V_{SENSE} measurement in a random VND5E025AK with R_{SENSE} = 1.8 kΩ.

Table 7. V_{SENSE} measurement

I_{OUT}[A]	V_{SENSE}[V]
1	0.64
2	1.29
3	1.99
4	2.69
5	3.39

Figure 30. V_{SENSE} measurement



The trend is almost linear in the application range and so we can approximate the V_{SENSE} trend with the following equation:

Equation 6

$$V_{sense} = m*I_{out} + a$$

Where *m* [ohm] is the rectangular coefficient and *a* is a constant.

The output current can be calculated by inverting this equation:

Equation 7

$$I_{out} = M*V_{sense} + b$$

Instead of $I_{OUT} = I_{SENSE} \times K$, once M[S] and b are known, it is possible to evaluate the I_{OUT} with a high accuracy, leaving only the spread due to temperature variation.

The current sense fluctuation due temperature variation is expressed in the datasheet with the parameter dK/K.

How to calculate M and b

To calculate M and b two simple measurements performed at the end of the production line are required. Chose two reference output currents (I_{ref1} and I_{ref2}) and measure the respective V_{SENSE1} and V_{SENSE2}. These four values must thenbe stored in an EEPROM in order to let the µC use this information to calculate K and b using the simple formulas reported below.

Since we defined:

$$I_{out} = M*V_{sense} + b$$

it is also true that:

Equation 8

$$I_{ref1} = M*V_{sense1} + b$$

and

$$I_{ref2} = M*V_{sense2} + b$$

Solving these two equations we get the following formulas:

Equation 9

$$M = (I_{ref1} - I_{ref2})/(V_{sense1} - V_{sense2})$$

$$b = (I_{ref2}*V_{sense1} - I_{ref1}*V_{sense2})/(V_{sense1} - V_{sense2})$$

Example for the chosen device:

Setting I_{ref1} = 2 A and I_{ref2} = 4 A according to *Table 7* we get V_{SENSE1} = 1.29 V and V_{SENSE2} = 2.69 V then

M = 1.43 [S]

b = 0.16 [A]

I_{OUT} is then:

Equation 10

$$I_{out} = 1.43 \cdot V_{sense} + 0.16$$

After calibration, the current sense variation is still affected by the device temperature. *Equation 10* remains affected by an error proportional to the sense current thermal drift.

This drift is reported in the datasheet as dK/K.

dK_1/K_1 (1)	Currente sense drift	I_{OUT}=2 A; V_{SENSE}=4 V V_{CSD}=0 V; T_j=-40°C to 150 °C	-13		13	%

1. The drift decreases when increasing the output current, e.g. in the VND5E025AK datasheet the drift is +/- 13 % at 2 A and it decreases down to +/-6 % when the output current is 10 A.

2.8 Analogue current sense diagnostics

Table 8 summarizes all failure conditions, the V_{SENSE} signal behavior and recommendations for diagnostics sampling for M0-5 in comparison with M0-5Enhanced.

Table 8. Analogue HSD diagnostics

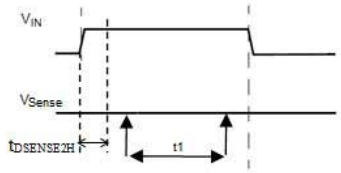
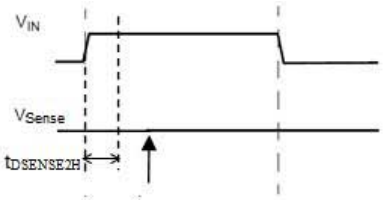
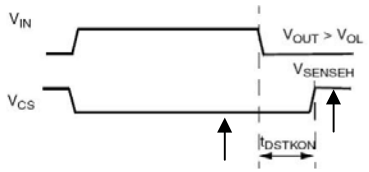
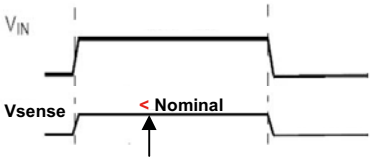
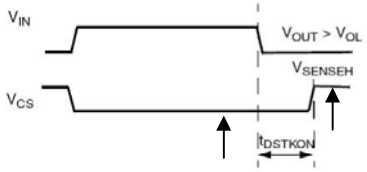
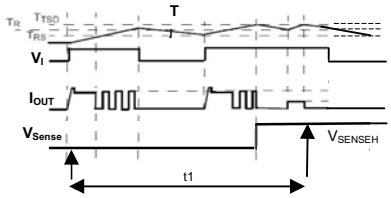
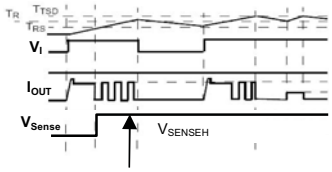
Diagnostics	Symbol	M0-5	M0-5*Enhanced*	
		Value	Value	
Open load (without pull-up)	V_{IN}	H	H	
	V_{SENSE}	L → L	L	
	Condition	1st sample after V_{IN} = H with a minimum delay of 600us, and wait to t1 (see SC to GND) for 2nd sample to distinguish between SC to GND – see (1).	Delay response time from rising edge of INPUT pin must be considered (minimum 300 µs).	
	Waveform			
Open load (with pull-up)	V_{IN}	H	H	L
	V_{SENSE}	L → L	L	V_{SENSEH}
	Condition	Same as open load without pull-up (No diagnostics in off-state)	N/A	
	Waveform			
Short circuit to V_{BAT}	V_{IN}	H	H	L
	V_{SENSE}	< Nominal	< Nominal	V_{SENSEH}
	Condition	N/A	N/A	
	Waveform			

Table 8. Analogue HSD diagnostics (continued)

Diagnostics	Symbol	M0-5	M0-5*Enhanced*
		Value	Value
SC to GND	V_{IN}	H	H
	V_{SENSE}	L → V_{SENSEH} (V_{SENSEH} ⇒ thermal shutdown)	V_{SENSEH} (V_{SENSEH} ⇒ *Power Limitation* or thermal shutdown)
	Condition	1st sample after V_{IN}=H with a minimum delay of 600 µs, and wait until thermal shutdown (t1) for 2nd sample to distinguish between open load. t1 depends on package, cooling area, SC resistance, ambient temperature, etc (range of 50 – 1000 ms) – see (1). $T_j > T_{TSD}$ (Typ=175 °C)	
	Waveform		

1. V_{SENSE} = 0 V condition explanation (M0-5 only):

Under normal conditions, the V_{SENSE} is a mirror of the HSD output current, therefore just one sample gives us information about the HSD. However, we should consider the status signal delay response time from the rising edge of the INPUT pin: $t_{DSENSE2H}$ = max 600 µs (see datasheet).

If the device is in a thermal shutdown condition the V_{SENSE} is pulled to V_{SENSEH}.

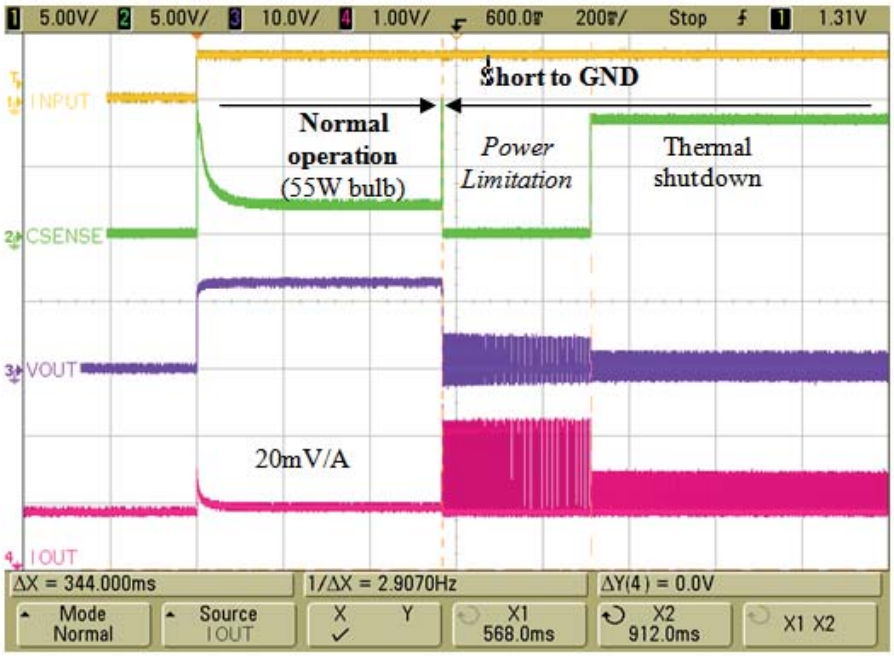
If V_{SENSE} = 0 V we have to be careful because there are two possible states:

a) Open Load

b) Hard short to GND, the device is still not in thermal shutdown

If a hard short to GND occurs, the V_{SENSE} first goes to 0 V (the internal current mirror is not working because V_{OUT} is close to 0V). After the device reaches thermal shutdown the V_{SENSE} is pulled to V_{SENSEH}. The time between SC to GND and thermal shutdown depends on the package, cooling area, SC resistance, ambient temperature etc. Normally this time is in the range of 50 - 1000 ms. See *Figure 31*.

Figure 31. VND5012A current sense voltage behavior – hard short to GND occurred (20 mΩ), thermal shutdown was reached 344 ms after short-circuit to GND



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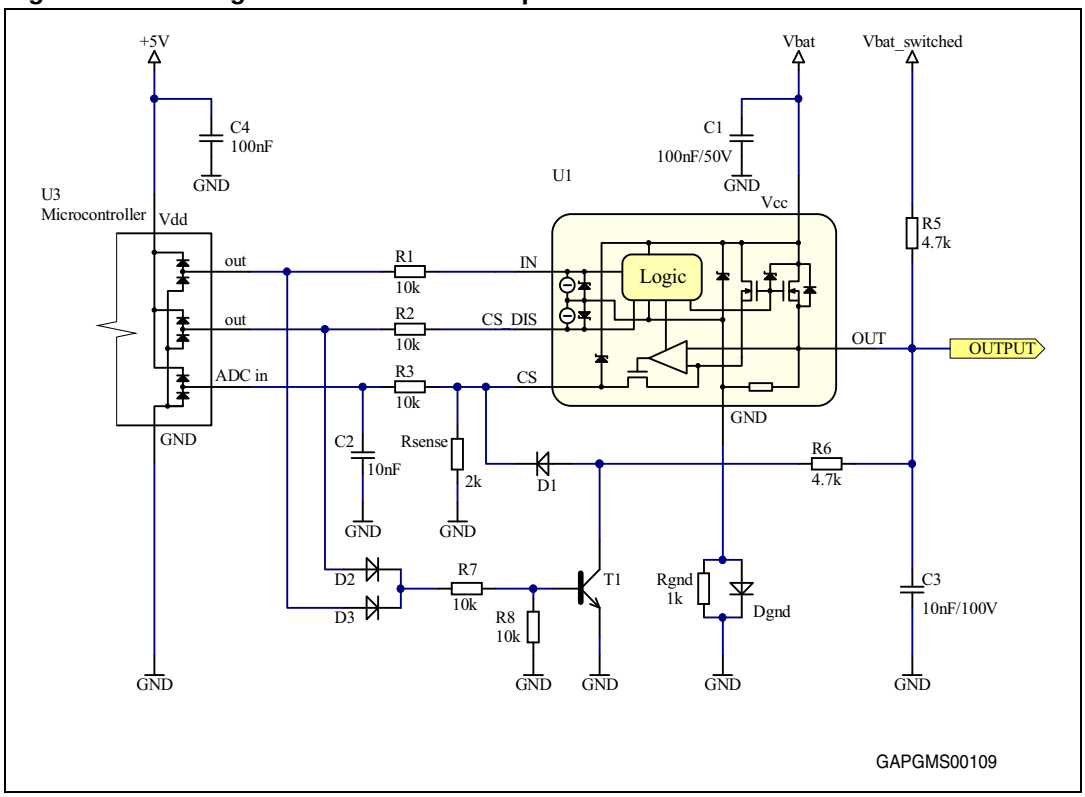
2.9 Open load detection in off-state – external circuitry for analogue M0-5 HSD

The following schematic shows a simple way to perform an open-load diagnostics in off-state for analogue HSDs. In case of a missing load in off-state the R_{SENSE} resistor is supplied through R5, R6 and D1. Then the voltage increase on R_{SENSE} is about 2 V (divider R5, R6, R_{SENSE}), which can be recognized by a µC as open-load in off-state.

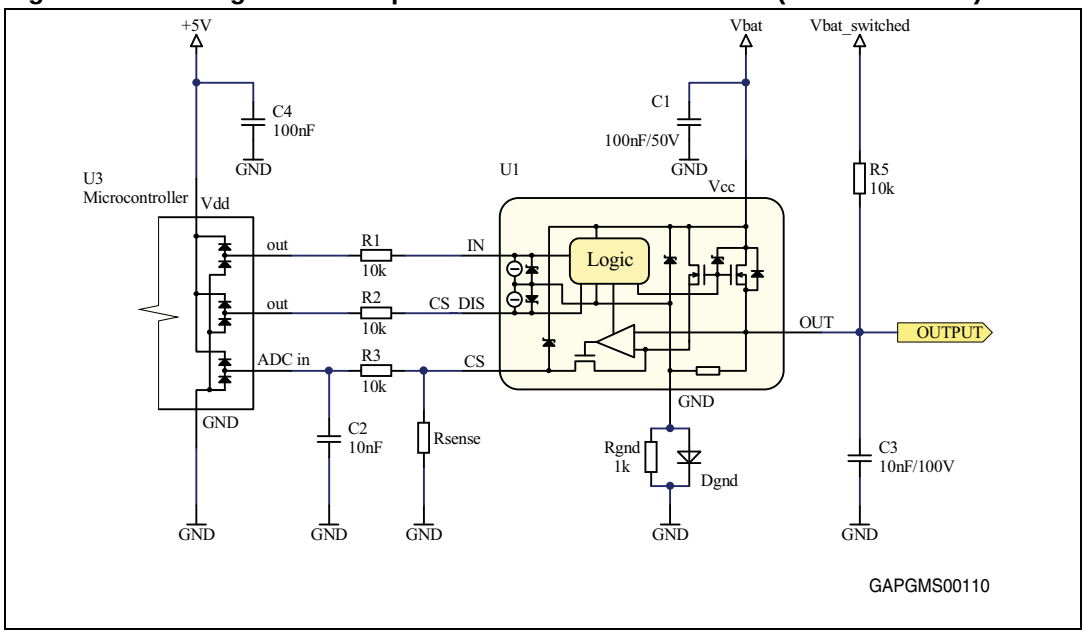
In on-state conditions (or if current sense disable signal is high) the influence of R5, R6 is suppressed by the conducting transistor T1 (anode of D1 is shorted to GND).

Figure 32. Analogue HSD – Circuit for open load detection in off-state



2.10 Open Load detection in off-state – M0-5Enhanced HSD

Figure 33. Analogue HSD – Open load detection in off-state (M0-5Enhanced)



3 Digital status output

3.1 Digital HSD diagnostics

The diagnostics of digital M0-5 devices is based on a logical level on the status pin.

The table below summarizes all failure conditions, the STATUS signal behavior and recommendations for diagnostics sampling for M0-5 in comparison with M0-5Enhanced.

Table 9. Digital HSD diagnostics

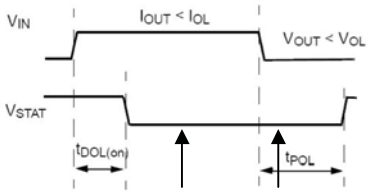
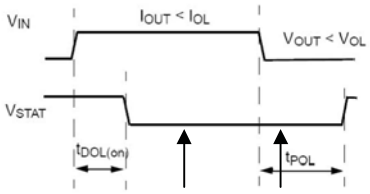
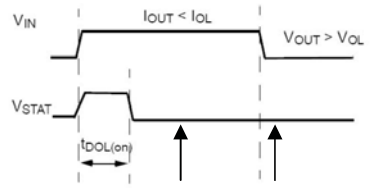
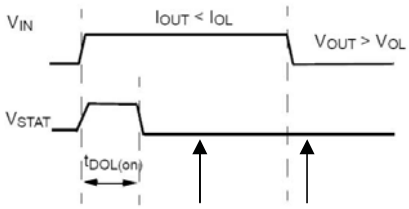
Diagnostics	Symbol	M0-5		M0-5*Enhanced*	
		Value		Value	
Open load (without pull-up)	V_{IN}	H	L	H	L
	V_{STAT}	L	L	L	L
	Condition	$I_{OUT} < I_{OL}$ (see datasheet) $V_{OUT} > V_{OL}$ (Typ=3 V) Without external pull-up		$I_{OUT} < I_{OL}$ (see datasheet) $V_{OUT} > V_{OL}$ (Typ=3 V) Without external pull-up	
	Waveform				
Open load (with pull-up)	V_{IN}	H	L	H	L
	V_{STAT}	L	L	L	L
	Condition	$I_{OUT} < I_{OL}$ (see datasheet) $V_{OUT} > V_{OL}$ (Typ=3 V) With external pull-up		$I_{OUT} < I_{OL}$ (see datasheet) $V_{OUT} > V_{OL}$ (Typ=3 V) With external pull-up	
	Waveform				

Table 9. Digital HSD diagnostics (continued)

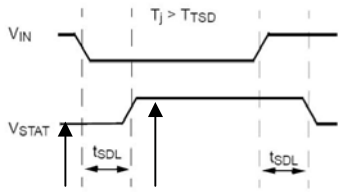
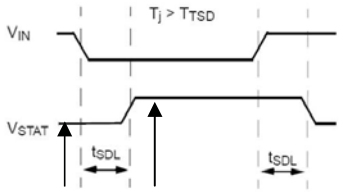
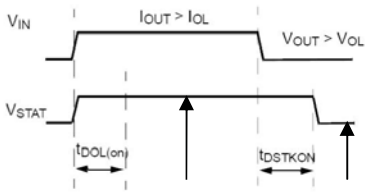
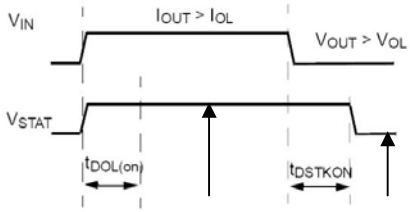
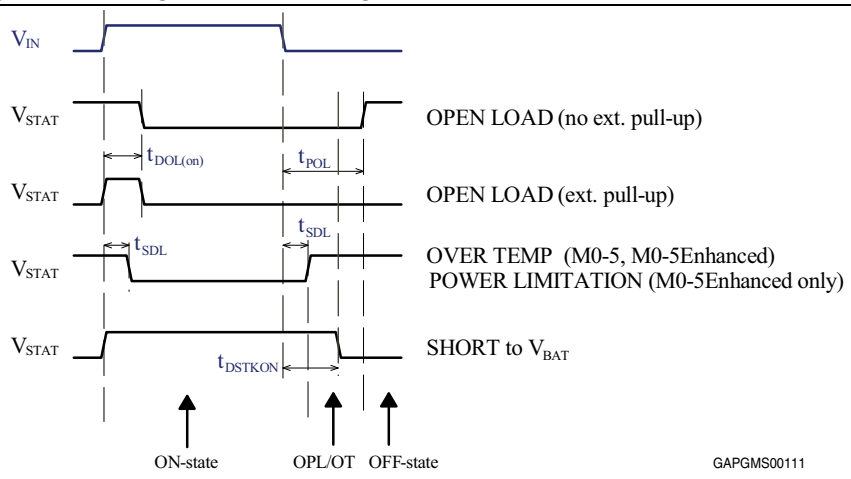
Diagnostics	Symbol	M0-5		M0-5*Enhanced*	
		Value		Value	
Overtemp / Overload	V_{IN}	H	L	H	L
	V_{STAT}	L	H	L	H
	Condition	$Tj > T_{TSD}$ (Typ=175 °C) (Thermal shutdown)		– Active Power Limitation – $Tj > T_{TSD}$ (Typ=175 °C) (Thermal shutdown)	
	Waveform				
Short circuit to V_{BAT}	V_{IN}	H	L	H	L
	V_{STAT}	H	L	H	L
	Condition	$I_{OUT} > I_{OL}$ (see datasheet) $V_{OUT} > V_{OL}$ (Typ = 3 V)		$I_{OUT} > I_{OL}$ (see datasheet) $V_{OUT} > V_{OL}$ (Typ = 3 V)	
	Waveform				

Figure 34. Digital HSD diagnostics – timing overview



4 Switching inductive loads

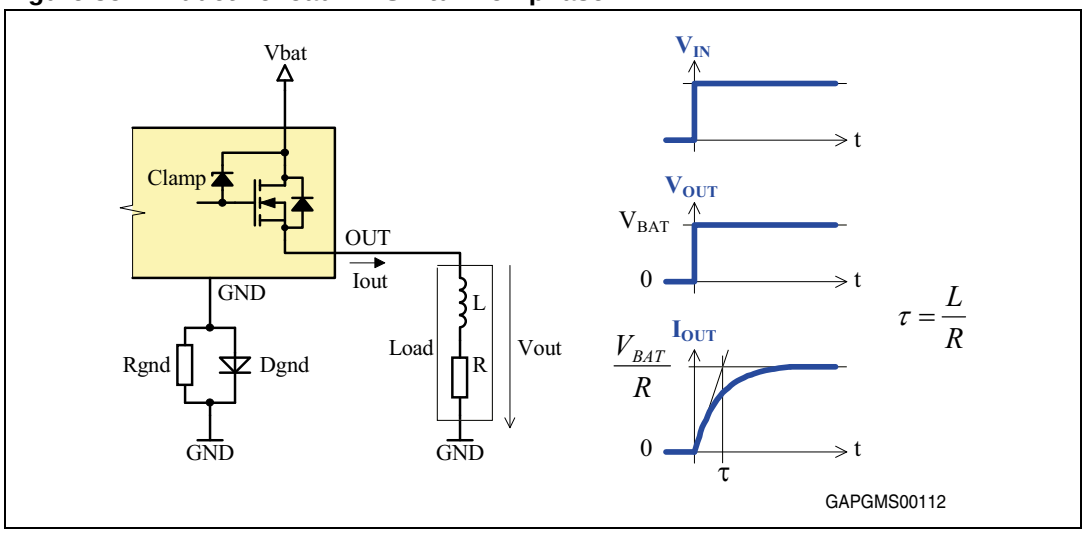
Switching inductive loads such as relays, solenoids, motors etc. can generate transient voltages of many times the steady-state value. For example, turning off a 12 volt relay coil can easily create a negative spike of several hundred volts. The M0-5/M0-5E high side drivers are well designed to drive such loads, in most cases without any external protection. Nevertheless, there are physical limits for each component that have to be respected in order to decide whether external protection is necessary or not.

An attractive feature of the M0-5/M0-5E drivers is that a relatively high output voltage clamping leads to a fast demagnetization of the inductive load.

The purpose of this chapter is to provide a simple guide on how to check the conditions during demagnetization and how to select a proper HSD (and the external clamping if necessary) according to the given load.

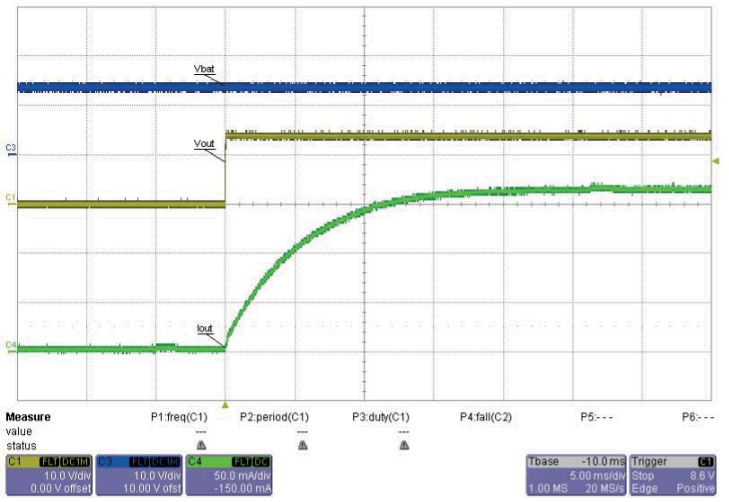
4.1 Turn-on phase behaviour

Figure 35. Inductive load – HSD turn-on phase



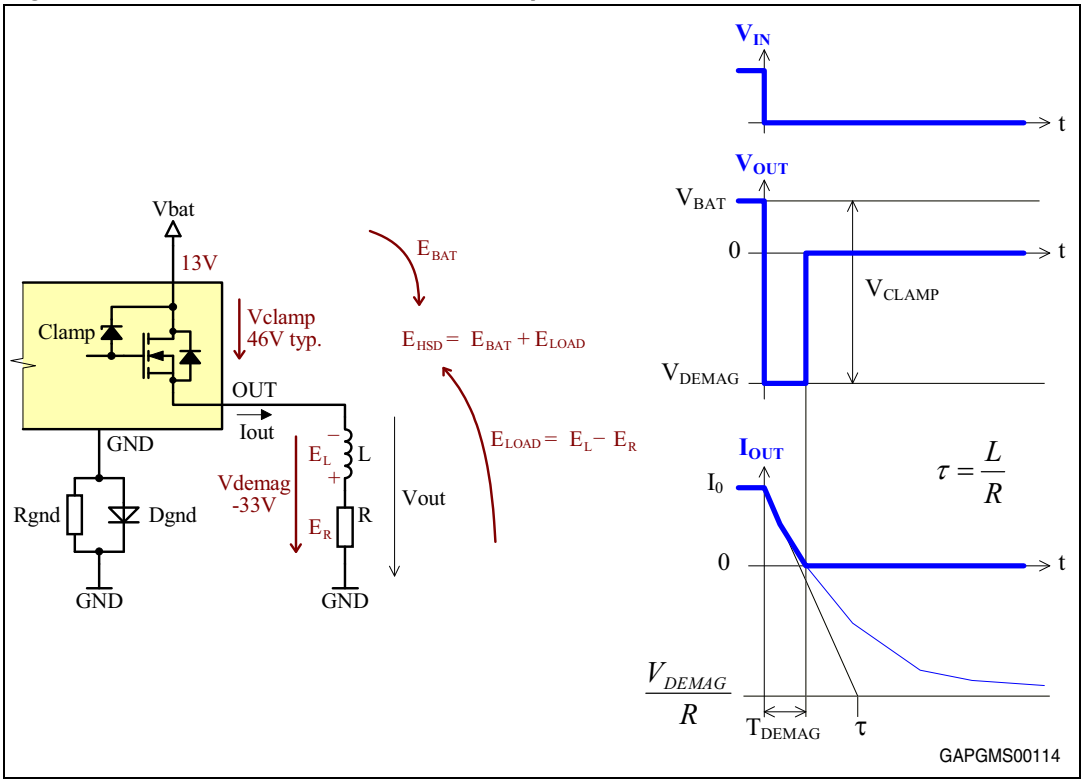
When an HSD turns on an inductive load, the current increases with a time constant given by L/R values, so the nominal load current is not reached immediately. This fact should be considered in diagnostics software (i.e. to avoid false open load detection).

Figure 36. Inductive load – turn-on example: VNQ5E050AK, L=260 mH, R=81 Ω



4.2 Turn-off phase behavior

Figure 37. Inductive load – HSD turn-off phase



The HSD turn-off phase with inductive load is explained in *Figure 37*. The inductance reverses the output voltage in order to be able to continue driving the current in the same

direction. This voltage (so called demagnetization voltage) is limited to the value given by the clamping voltage of the HSD and the battery voltage:

Equation 11

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} =$$

$$= 13V - 46V \text{ typ.}$$

The load current decays exponentially (linearly if R→0) and reaches zero when all energy stored in the inductor is dissipated in the HSD and the load resistance.

Since the HSD output clamp is related to the V_{BAT} pin, the energy absorbed by the HSD increases with increasing battery voltage (the battery is in series with the high side switch and load so the energy contribution of the battery increases with the battery voltage).

4.2.1 Calculation of energy dissipated in the HSD

The energy dissipated in the High Side Driver is given by the integral of the actual power on the MOSFET through the demagnetization time:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot i_{OUT}(t)dt$$

To integrate the above formula we need to know the current response $i_{OUT}(t)$ and the demagnetization time T_{DEMAG}. The $I_{OUT}(t)$ can be obtained from the well known formula, R/L circuit current response using the initial current I_0 and the final current V_{DEMAG}/R considering i_{OUT} >= 0 condition (see *Figure 37*):

$$I_{OUT}(t) = I_0 - \left(\left(I_0 + \frac{|V_{DEMAG}|}{R} \right) \cdot \left(1 - e^{\frac{-tR}{L}} \right) \right)$$

$(0 < t < T_{DEMAG} \rightarrow i_{OUT} \geq 0)$

Inserting i(t) = 0 we can calculate the demagnetization time:

Equation 12

$$T_{DEMAG} = \frac{L}{R} \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right)$$

Equation 13

$$\lim_{R \to 0} T_{DEMAG} = L \cdot \frac{I_0}{V_{DEMAG}}$$

(simplified for R→0)

Substituting the T_{DEMAG} and $i_{OUT}(t)$ by the formulas above we can calculate the energy dissipated in the HSD:

$$E_{HSD} = \int_0^{T_{DEMAG}} V_{CLAMP} \cdot I_{OUT}(t)dt = \int_0^{T_{DEMAG}} (V_{BAT} + |V_{DEMAG}|) \cdot I_{OUT}(t)dt$$

then

Equation 14

$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) \right]$$

Equation 15

$$\lim_{R \to 0} E_{HSD} = \frac{1}{2} \cdot L \cdot I_0^2 \cdot \frac{V_{BAT} + |V_{DEMAG}|}{|V_{DEMAG}|}$$

(simplified for R→0)

4.2.2 Calculation example

This example shows how to use above equations to calculate the demagnetization time and energy dissipated in the HSD.

Conditions:

- Battery voltage: V_{BAT} = 13.5 V
- HSD: VNQ5E050AK-E
- Clamping voltage: V_{CLAMP} = 46 V (typical for M0-5/M0-5E)
- Load resistence: R = 81 Ω
- Load inductance: L = 260 mH
- Load current (before turn-off event): $I_0 = V_{BAT}/R$ = 167 mA

Step 1) Demagnetization voltage calculation using *Equation 11*:

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 13.5 - 46 = -32.5V$$

Step 2) Demagnetization time calculation using *Equation 12:*

$$T_{DEMAG} = \frac{L}{R} \cdot \left(\log \frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) = \frac{0.260}{81} \cdot \log\left(\frac{32.5 + 0.167 \cdot 81}{32.5} \right) = 1.12ms$$

Step 3) Calculation of energy dissipated in the HSD using *Equation 14*:

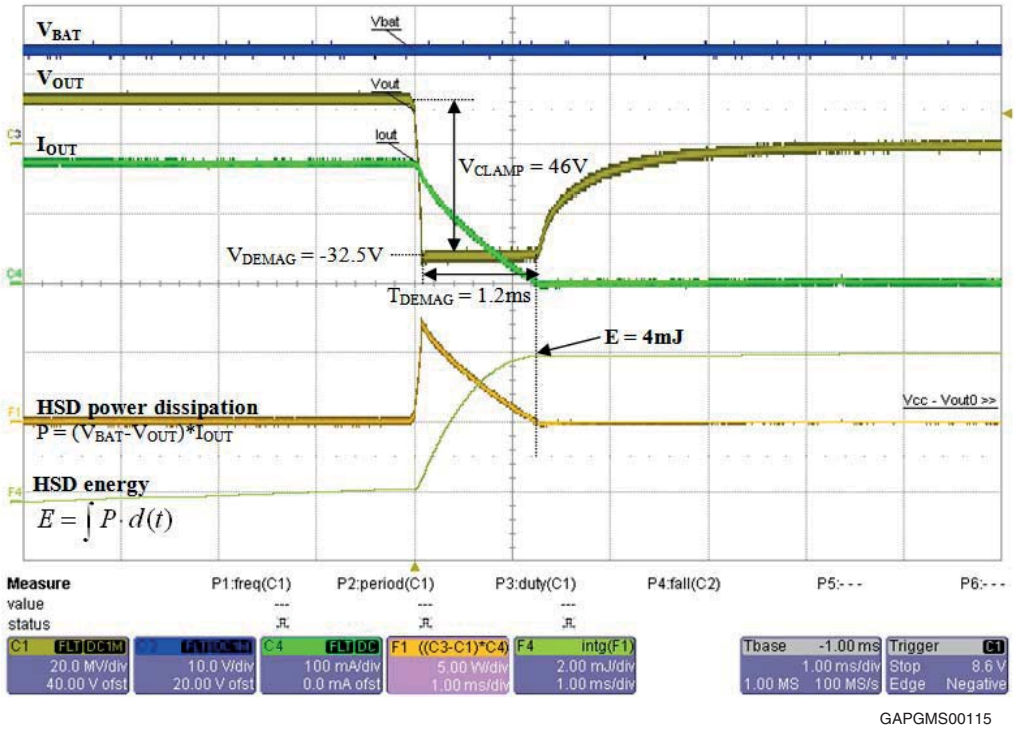
$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{V_{DEMAG}} \right) \right] =$$

$$= \frac{13.5 + 32.5}{81^2} \cdot 0.260 \cdot \left[(81 \cdot 0.167 - 32.5) \cdot \log\left(\frac{32.5 + 0.167 \cdot 81}{32.5} \right) \right] = 4.04mJ$$

Step 4) Measurement (comparison with theory):

(see *Figure 38*)

Figure 38. Inductive load – turn off example: VNQ5E050AK, L=260 mH, R=81 Ω



The demagnetization energy dissipated in the HSD was measured by an oscilloscope with mathematical functions. The first function (F1) shows the actual power dissipation on the HSD $(V_{BAT} - V_{OUT}) \times I_{OUT}$, the second function (F4) shows the HSD energy (integral of F1).

As seen from the oscillogram the measured values are very close to the theoretical calculations.

4.3 Proper HSD selection

Even if the device is internally protected against break down during the demagnetization phase, the energy capability is limited and has to be taken into account during the design of the application.

It is possible to identify two main mechanisms that can lead to the device failure:

1. The temperature during the demagnetization rises quickly (depending on the inductance) and the uneven energy distribution on the power surface can cause the presence of a hot spot causing the device failure with a single shot.
2. As in normal operation, the life time of the device is affected by the fast thermal variation as described by the Coffin-Manson law. Repetitive demagnetization energy causing temperature variations above 60 K causes a shorter life time.

These considerations lead to two simple design rules:

1. The energy has to be below the energy the device can withstand at a given inductance.
2. In case of a repetitive pulse, the average temperature variation of the device should not exceed 60 K at turn-off.

To fulfill these rules, the designer has to calculate the energy dissipated in the HSD at turn-off, and then compare this number with the datasheet values as shown in the following examples.

4.3.1 Example of VND5E160AJ driving relays

The purpose of this example is to evaluate if a VND5E160AJ device can safely drive a relay under following conditions:

– Battery voltage: V_{BAT} = 16 V

– HSD: VND5E160AJ
  Clamping voltage: V_{CLAMP} = 46 V (typical for M0-5/M0-5E)

– Relay: NVF4-4C-Z60a
  Resistance: R = 62 Ω@-40°C(1)
  Inductance (coil not powered): L = 260 mH(2)

– Load current (before turn-off event): $I_0 = V_{BAT}/R$ = 258 mA

1. The relay datasheet usually specifies a coil resistance at 20 °C. For the worst case evaluation we should consider the resistance at -40 °C which can be calculated as:

$$R_{-40} = R_{20} \cdot (1 + 0.0039 \cdot (-40 - 20))$$

2. Not every relay datasheet specifies the coil inductance. In this case it can be determined by measurement. The inductance value is different with armature seated (relay powered) than when unseated (relay not powered). The inductance measurement should be done with relay powered (armature seated) because this better represents the application conditions. The inductance of a typical 12 V automotive relay is in the range of 200-800 mH.

Step 1) Demagnetization voltage calculation using *Equation 11*:

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 16 - 46 = -30V$$

Step 2) Demagnetization time calculation using *Equation 12:*

$$T_{DEMAG} = \frac{L}{R} \cdot \left(\log \frac{|V_{DEMAG}| + I_0 \cdot R}{V_{DEMAG}} \right) = \frac{0.260}{62} \cdot \log\left(\frac{30 + 0.258 \cdot 62}{30} \right) = 1.8ms$$

Step 3) Calculation of energy dissipated in HSD using *Equation 14:*

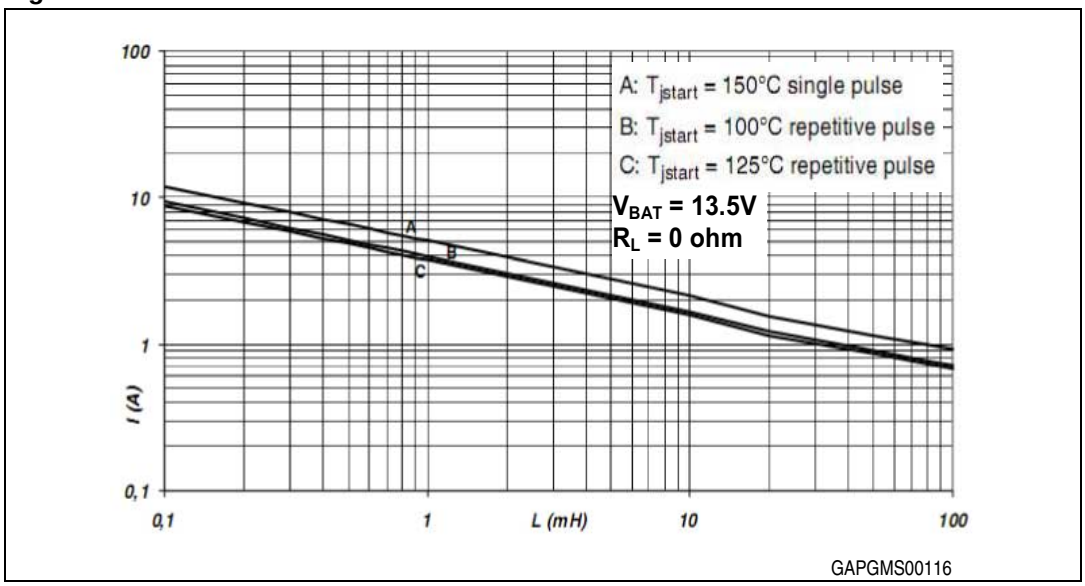
$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) \right] =$$

$$= \frac{16 + 30}{62^2} \cdot 0.260 \cdot \left[62 \cdot 0.258 - 30 \cdot \log\left(\frac{30 + 0.258 \cdot 62}{30} \right) \right] = 9.9mJ$$

Step 4) HSD datasheet analysis:

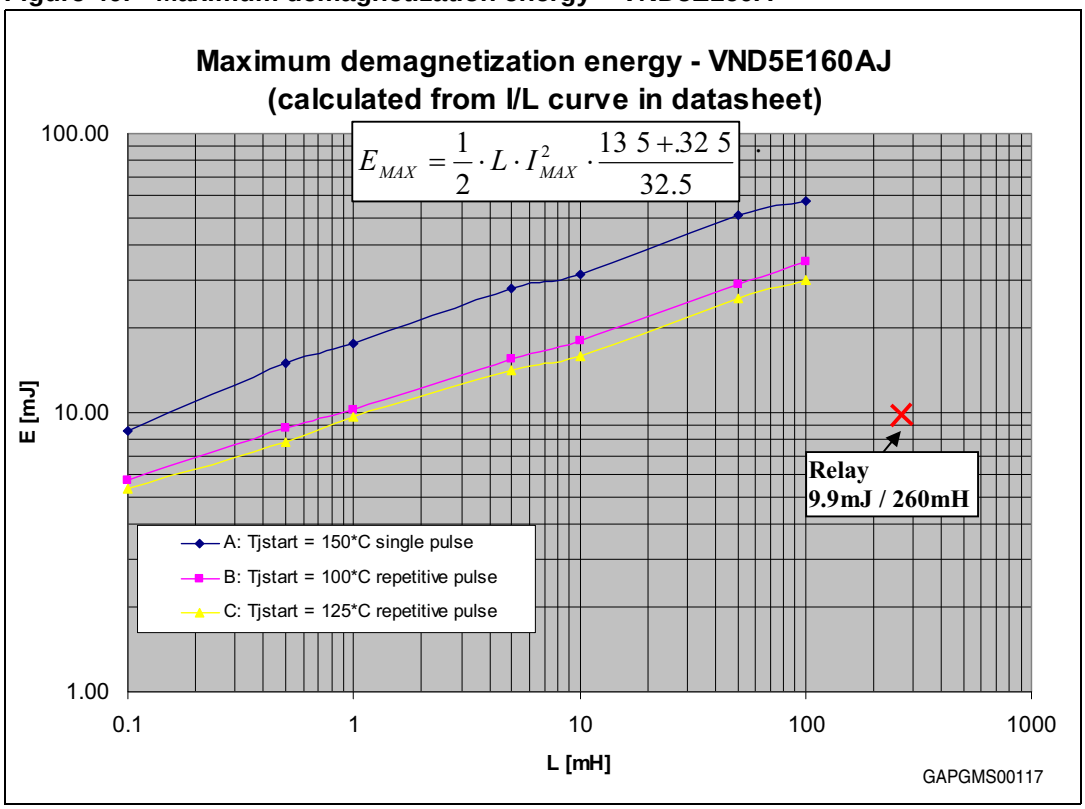
The maximum demagnetization energy is specified by I/L diagram in the datasheet. This diagram shows the maximum turn-off current versus inductance for R_L = 0 Ω and V_{BAT} = 13.5 V (see *Figure 39*). These conditions are different from conditions considered in our example (R_L = 62 Ω, V_{BAT} = 16 V) and inductance 260 mH is not covered by the diagram.

Figure 39. Maximum turn-off current versus inductance – VND5E160AJ datasheet



Therefore it is convenient to translate I/L chart to E/L chart. This can be easily done using *Equation 15* for the calculation of energy on the HSD considering R_L = 0, V_{BAT} = 13.5 V (see *Figure 40*).

Figure 40. Maximum demagnetization energy – VND5E160A



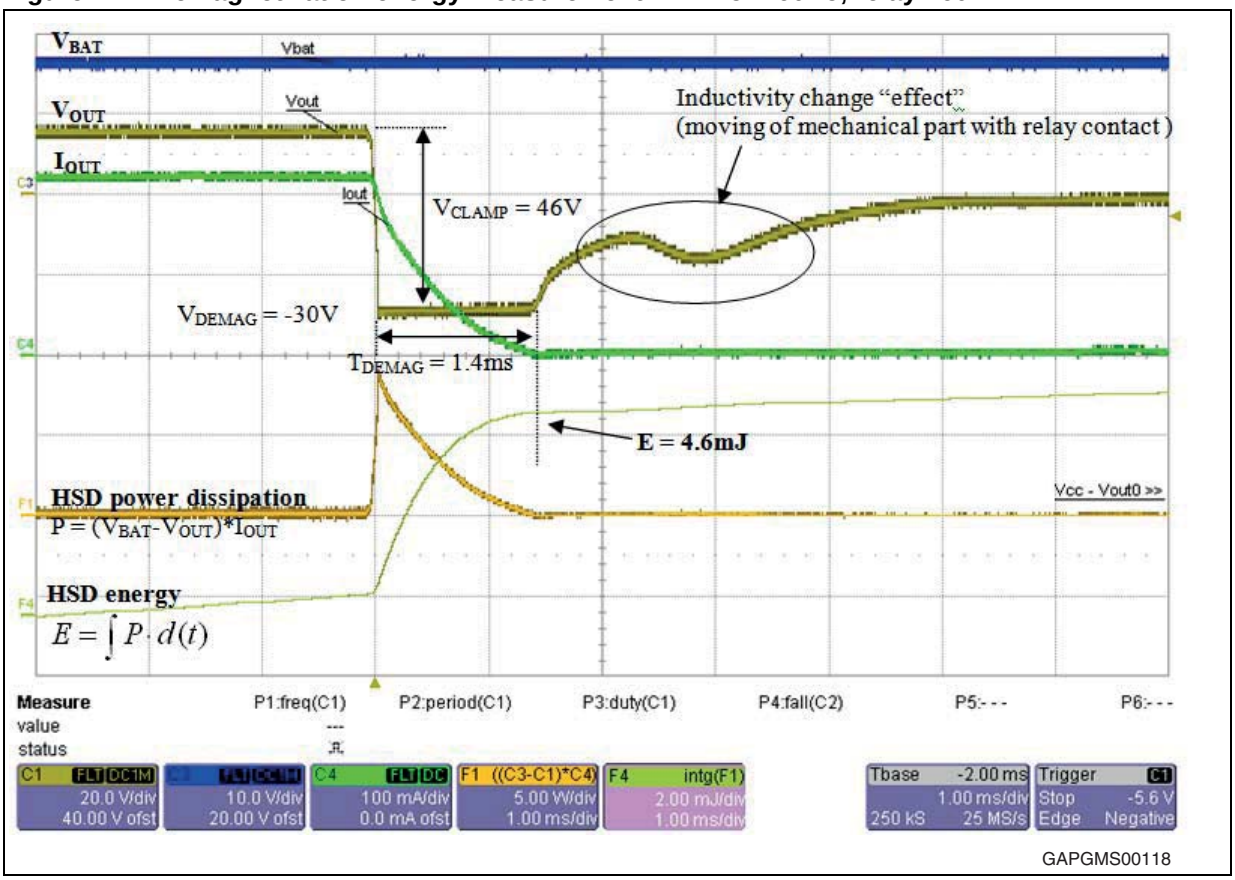
Waveform A represents the max energy the device can withstand in a single pulse. A second pulse with the same energy can destroy the part. Waveforms B and C represent the max energy to ensure the junction temperature variation to stay below 60 K.

Putting the energy value of 9.9 mJ @ 260 mH calculated in Step 3) to this diagram we can see that we are clearly in the safe area. Although the energy curve is introduced only up to 100 mH inductance, the calculated energy is below the limit even at 100 mH.

Step 5) Measurement (calculation check):

(see *Figure 41*).

Figure 41. Demagnetization energy measurement – VND5E160AJ, relay 260 mH



The measured energy is lower by a factor of two than calculated (4.6 mJ measured versus 9.9 mJ calculated). This difference can be explained by measurement at ambient temperature when the coil resistance is ~25 % higher than the resistance at -40 °C used in the calculations. Another factor is the coil inductance decrease due to the magnetic saturation (the inductance value used for calculation was measured at a low current).

Conclusion: the device can safely drive the load without additional protection. The worst case demagnetization energy is clearly below the device limit.

4.4 External clamping selection

The main function of external clamping circuitry is to clamp the demagnetization voltage and dissipate the demagnetization energy in order to protect the HSD. It can be used as a cost

effective alternative in case the demagnetization energy exceeds the energy capability of a given HSD. A typical example is driving DC motors (high currents in combination with high inductance).

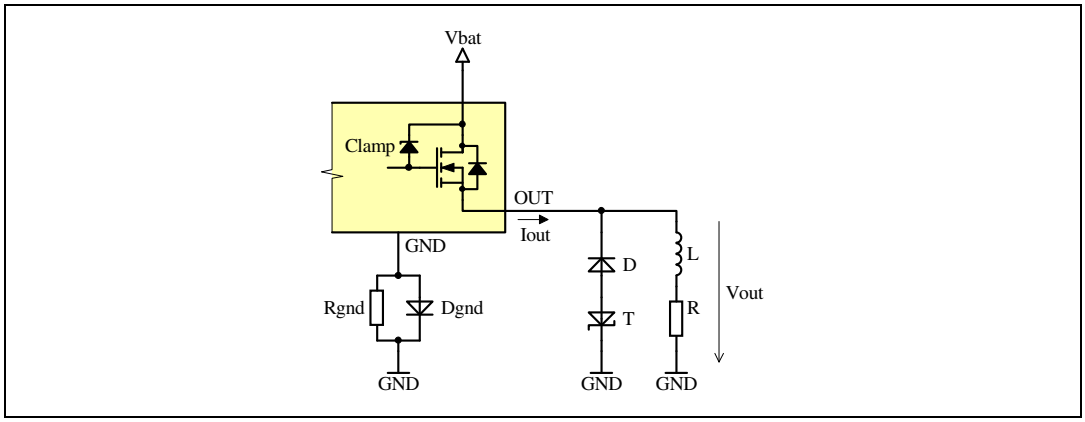
During the selection of a suitable HSD for such an application, we usually end up in the situation that a given HSD fits perfectly in terms of current profile, but the worst case demagnetization energy is too high (turn-off from stall condition at 16 V, -40 °C). Rather than selecting a larger HSD, the use of an external clamp can be the more economical choice.

External clamping circuitry – requirements summary:

- Proper negative output voltage clamping to protect the HSD
- No conduction at:
  - Normal operation (0-16 V)
  - Reverse battery condition (-16 V@60 s)
  - Jump start (27 V@60 s)
  - Load dump (36 V@400 ms)
- Proper energy capability
  - Single demagnetization pulse
  - Repetitive demagnetization pulse

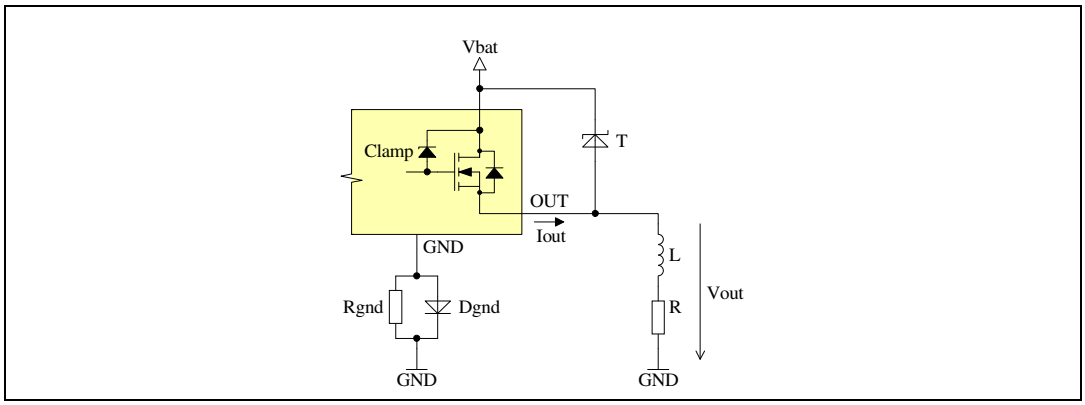
4.4.1 Clamping circuitry examples

1) Transil and diode protection circuitry (in parallel with the load):



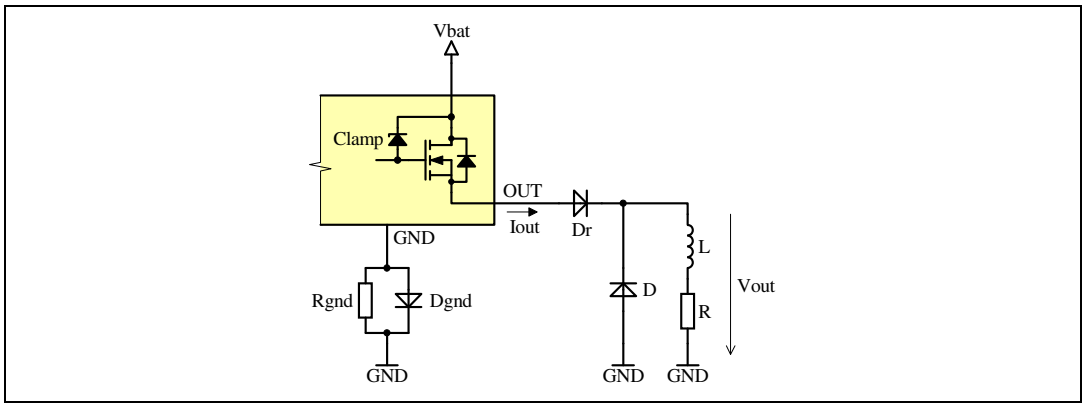
The transil (T) clamps the demagnetization voltage to a safe level. The clamping voltage of the transil should be selected in a way that the voltage across the HSD channel is below the minimum specified clamping voltage of the HSD (41 V). The diode (D) is included to protect the transil during normal operation (positive output voltage).

2) Transil protection circuitry (in parallel with the HSD)



The HSD channel is protected directly by the parallel transil. The clamping voltage of the transil should be below the minimum clamping voltage of the HSD (41 V). Such transils (V_{CL} < 41 V) usually start conducting at 30 V, therefore there is a high probability that it is damaged during the clamped load dump pulse (36 V). For that reason it is usually better to use the previously described solution (1).

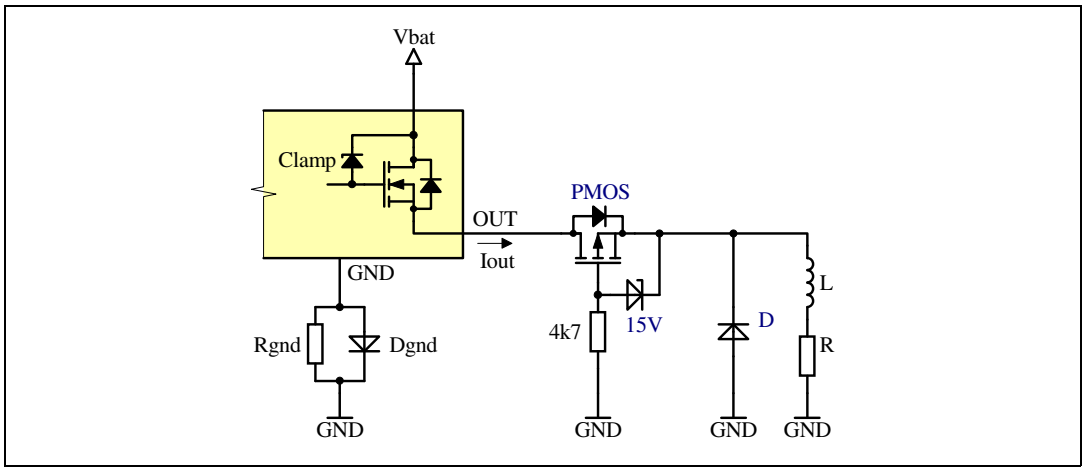
3) Freewheeling diode and reverse battery diode



A general purpose diode connected in parallel with the load provides a conductive path for proper demagnetization. Relatively small demagnetization voltage (1 diode voltage drop in forward direction) leads to a very slow demagnetization. This can have a negative influence when driving the relay, for example. A slow movement of the armature (slow opening of contacts) can have a negative influence on the lifetime of the relay contacts (depending on the switching current).

In order to protect the freewheeling diode against the reverse battery condition, there is an additional diode (Dr) required in series with the output. This circuitry is suitable only for small loads because of permanent voltage drop (→ power dissipation) on Dr during normal operation.

4) Freewheeling diode and reverse battery P-channel MOS circuitry



This circuitry is an improvement of the previous example. The reverse battery protection of the freewheeling diode (and load) is solved by a PMOS circuitry with negligible voltage drop at nominal current (to avoid undesired power dissipation in on-state)

The peak power dissipation of the freewheeling diode during the demagnetization phase is very low in comparison with the transil protection because of low demagnetization voltage (1 diode voltage drop). Furthermore, the average power dissipation is much lower, assuming non-zero load resistance (the part of demagnetization energy dissipated in the load resistance is higher at lower demagnetization voltage).

Therefore, this circuitry is suitable for high current inductive loads such as DC motors, where the transil protection is usually not able to handle the average power dissipation caused by repetitive turn-on/off cycles (the HSD usually goes in thermal cycling when the motor is blocked so there are a lot of demagnetization cycles in a short time).

External clamping circuitry examples

Table 10. External clamping circuitry examples (1/2)

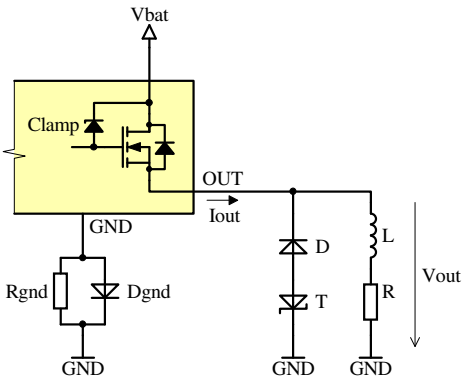
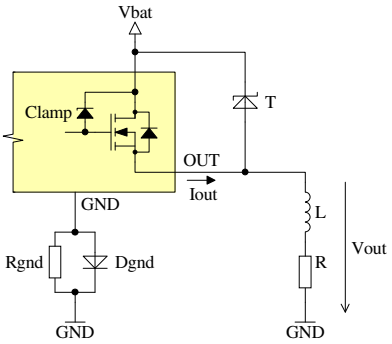
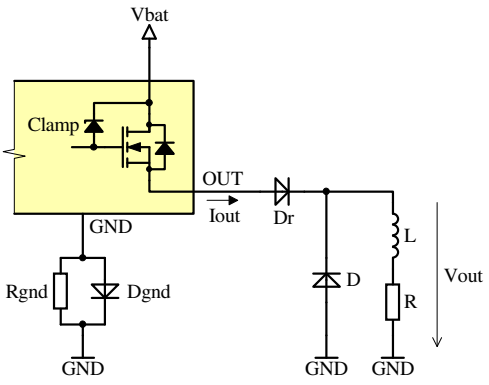
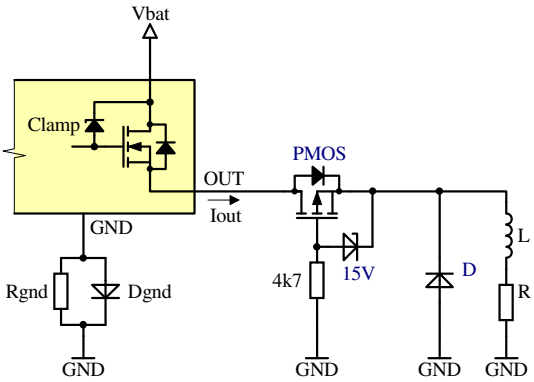
External clamping circuitry	+	–
1) Transil and diode (in parallel with the load) 	Fast demagnetization	The peak voltage across the HSD channel depends also on V_{BAT} (maximum V_{BAT} should be considered)
2) Transil (in parallel with the HSD) 	Fast demagnetization Direct (parallel) protection of the HSD - independent from V_{BAT}	Load dump pulse: (The transil with V_{CL} < 41 V is starting to conduct already at ~30 V → transil can be damaged during the load dump pulse) Higher peak power dissipation on transil in comparison with circuitry 1) (contribution of power supply)
3) Freewheeling diode and reverse battery diode 	Low cost Load is reverse battery protected	Only for small loads (voltage drop and power dissipation on reverse battery protection diode Dr) Slow demagnetization

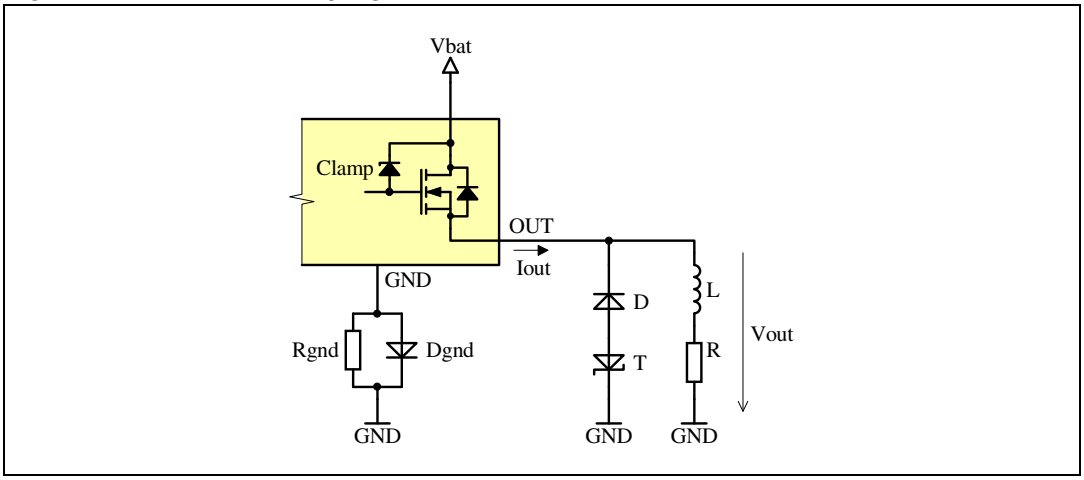
Table 11. External clamping circuitry examples (2/2)

External clamping circuitry	+	–
4) Freewheeling diode and reverse battery FET 	Load is reverse battery protected Low peak power dissipation on D during demag. phase (suitable for high current inductive loads such as DC motors)	High number of ext. components (cost) Slow demagnetization

4.4.2 Component selection guide for external transil-diode clamping

This chapter shows how to select proper a diode (D) and transil (T) for external clamping circuitry 1).

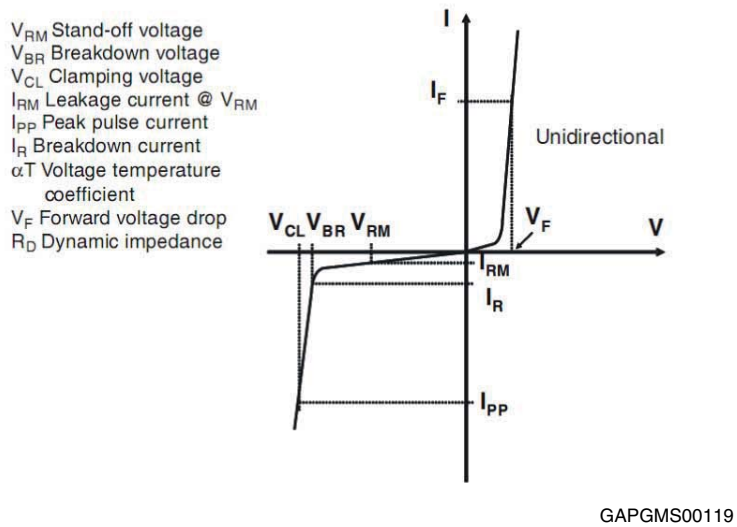
Figure 42. External clamping - transil and diode



Transil selection

- Clamping voltage, V/A characteristic

Figure 43. Transil – V/A characteristic



Considering the worst case values (V_{BAT} = 16 V, $V_{HSDClampMin}$ = 41 V) the demagnetization voltage should be limited at least to 16 – 41 = -25 V. Assuming 1 V voltage drop on the protection diode (D) we need a transil with V_{CL} < 24 V at the given current level (load current at switch-off event). The clamping voltage is usually specified only at the maximum peak power limit of the device. To determine the voltage at a given current level, apply a linear approximation using V_{BR}/I_R and V_{CL}/I_{PP} data or estimate the value using V_{CL}/I_{PP} diagram in the datasheet.

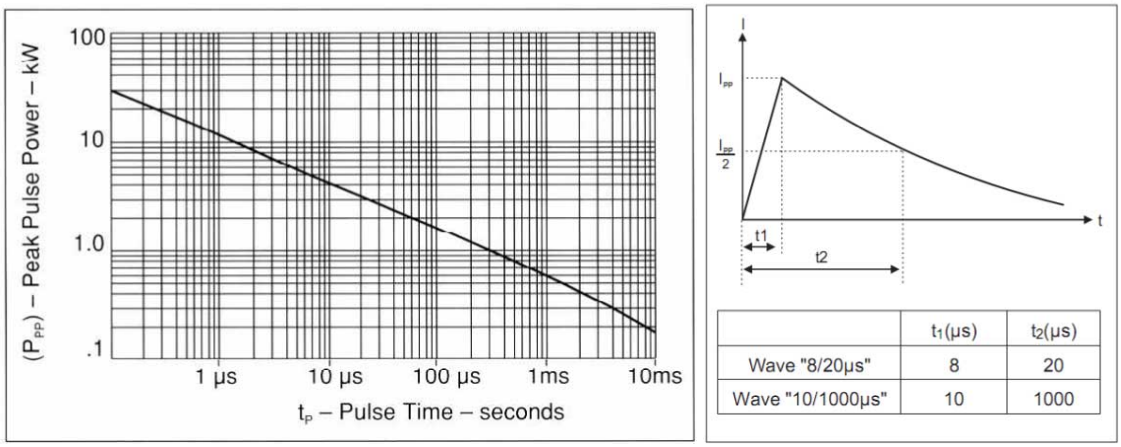
The transil must not conduct during a reverse battery condition. Assuming V_{BAT} = -16 V, a 0.5 V drop on the HSD channel and a 0.5 V drop on the protection diode, we have -15 V across the transil. We can find the parameter V_{RM} (Stand-off voltage) in the transil specification. V_{RM} is the maximum operation voltage with low leakage current (valid in the whole temperature range).

V_{RM}>15 V
VCL<24 V (at given I_0)

- Single pulse energy capability

The maximum nonrepetitive transient power and current capability of transils is specified mostly for 10/1000 µs exponential pulse at 25 °C. A real application condition is usually different. In our case, the pulse length is given by the demagnetization time, while the current waveform is close to the sawtooth shape (depending on L/R ratio of the load). To check if the transil can safely operate under the desired conditions we can use the translation diagrams in *Figure 44*, *Figure 45* and *Figure 46*.

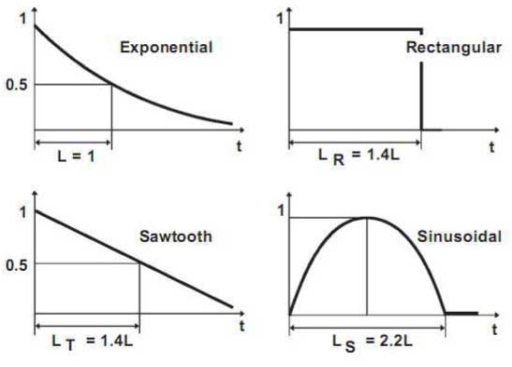
Figure 44. Peak pulse power vs pulse time (for transil 600 W@10/1000 µs series)



	t_1(µs)	t_2(µs)
Wave "8/20µs"	8	20
Wave "10/1000µs"	10	1000

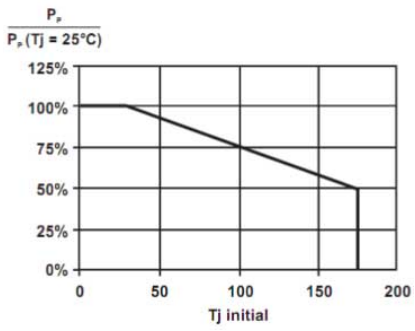
GAPGMS00120

Figure 45. Equivalent pulses giving the same power dissipation



GAPGMS00121

Figure 46. Maximum peak power as a function of initial temperature of the transil



GAPGMS00122

- Repetitive pulse energy capability

Depending on the application (PWM, HSD thermal cycling), the transil should be able to withstand repetitive operation and the most important parameter is the average power dissipation:

Equation 16

$$P_{AVG} = f \cdot E$$

valid when

$$T_{DEMAG} < \frac{1}{f}$$

f: switching frequency;

E: energy dissipated in transil at each demag. pulse.

Equation 17

$$E = \frac{|V_{CL}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{CL}| \cdot \log\left(\frac{|V_{CL}| + I_0 \cdot R}{|V_{CL}|} \right) \right]$$

V_{CL}: transil clamping voltage;

R: load resistance;

L: load inductance;

I_0: load current at turn-off event.

The junction temperature T_J calculated from P_{AVG} should never exceed the maximum specified junction temperature:

Equation 18

$$T_j = T_{Amb} + R_{th(j-a)} \cdot P_{AVG}$$

T_{Amb}: ambient temperature;

$R_{th(j-a)}$: thermal resistance between the junction and ambient;

P_{AVG}: average power dissipation.

Transil selection summary:

1. Determine the length of equivalent exponential pulse:

$$T_P = 0.5 \cdot \frac{T_{DEMAG}}{1.4}$$

(see *Figure 45* – considering sawtooth demagnetization current)

2. Determine maximum peak power (P_P) for T_P(using *Figure 44*)
3. Correct P_P value according to worst case T_j (using *Figure 46*)
4. Check if corrected

$$P_P > V_{CL} \cdot I_0$$

5. Check P_{AVG} and T_J in repetitive operation (*Equation 16* - *Equation 18*)

Diode selection:

- Reverse voltage > 52 V
  (Must not conduct during positive voltage on the HSD output →maximum possible output voltage is limited by $V_{HSDClampMax}$ = 52 V)

- Peak forward current > I_0 @ T_{DEMAG}
  (I_0: load current at switch-off event, T_{DEMAG}: demagnetization time)

4.4.3 Examples of VN5E025AJ for DC motor driving with external clamp)

The purpose of this example is to evaluate if a VN5E025AJ can safely drive a specific DC motor in terms of demagnetization energy and to determine a suitable external clamping circuitry if needed.

Battery voltage:	V_{BAT} = 16 V
HSD:	VN5E025AJ
– Clamping voltage:	V_{CLAMP} = 46 V (typical for M0-5/M0-5E)
DC Motor:	
– Nominal current:	I_{nom} = 1.5 A
– Resistance:	R = 0.6Ω@-40 °C
– Inductance:	L = 0.73 mH
– Stall current:	I_0 = 25 A@-40 °C, 16 V

Step 1) Demagnetization voltage calculation using *Equation 11*:

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} = 16 - 46 = -30V$$

Step 2) Demagnetization time calculation using *Equation 12*:

$$T_{DEMAG} = \frac{L}{R} \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.00073}{0.6} \cdot \log\left(\frac{30 + 25 \cdot 0.6}{30}\right) = 0.49ms$$

Step 3) Calculation of energy dissipated in HSD using *Equation 14*:

$$E_{HSD} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right)\right] =$$

$$= \frac{16 + 30}{0.6^2} \cdot 0.00073 \cdot \left[0.6 \cdot 25 - 30 \cdot \log\left(\frac{30 + 25 \cdot 0.6}{30}\right)\right] \cdot = 264.5mJ$$

Step 4) HSD datasheet analysis:

Looking at the I/L diagram in the datasheet, the maximum turn-off current specified for 0.73 mH inductance is 16 A (single pulse, V_{BAT} = 13.5 V, R_L = 0). The worst case current in

our example (a motor stall condition 25 A@16 V/-40 °C) is much higher. For better comparison of the calculated energy (264.5 mJ) with the device limits, it is useful to translate the current values at 0.73 mH (I_{MAX_A} = 16 A, I_{MAX_B} = 12 A, I_{MAX_C} = 11 A) to energy values using *Equation 15*:

$$E_{MAX-A} = \frac{1}{2} \cdot L \cdot I^2_{MAX} \cdot \frac{V_{BAT} + |V_{DEMAG}|}{|V_{DEMAG}|} = \frac{1}{2} \cdot 0.00073 \cdot 16^2 \cdot \frac{13.5 + 32.5}{32.5} = 132mJ$$

E_{MAX_B} = 74 mJ

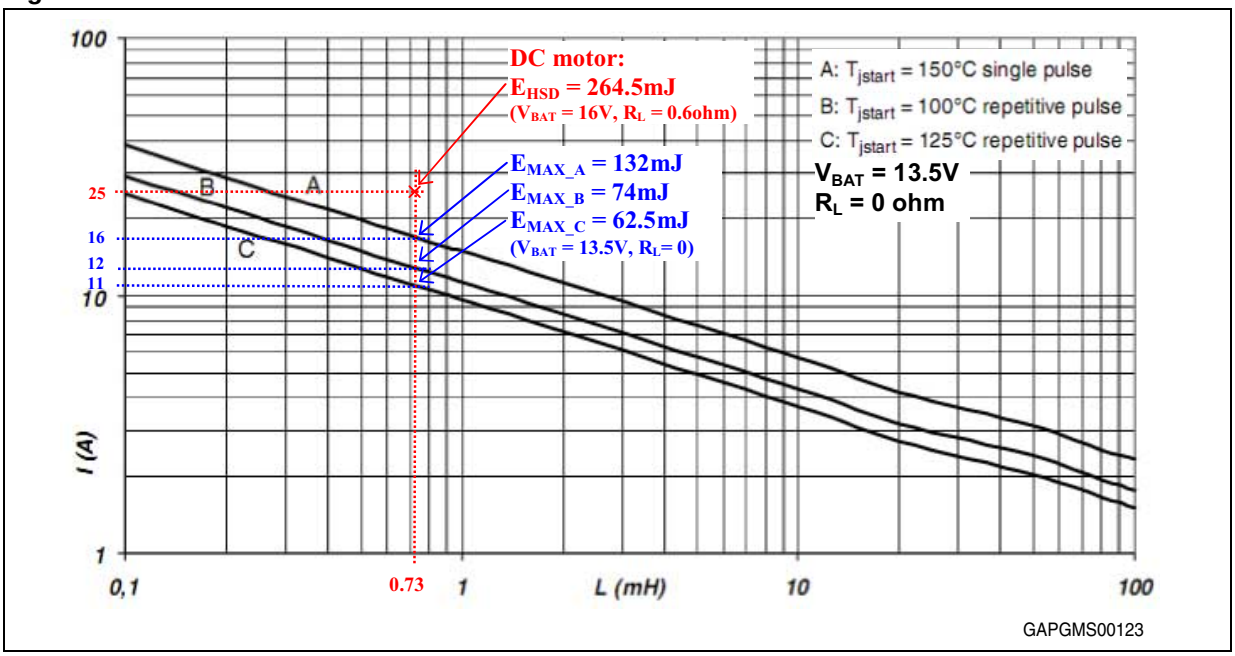
E_{MAX_C} = 62.5 mJ

single pulse @ T_{jstart} = 150 °C

repetitive pulse @ T_{jstart} = 100 °C

repetitive pulse @ T_{jstart} = 125 °C

Figure 47. Maximum turn-off current versus inductance – VN5E025AJ datasheet



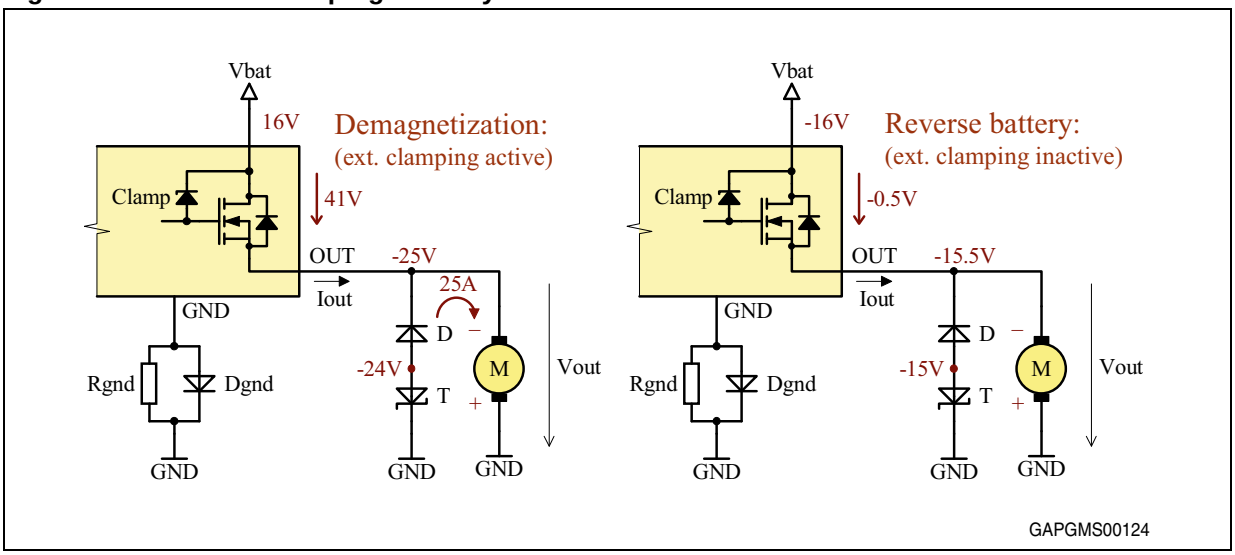
The demagnetization energy is by a factor of 2 higher than the device is able to withstand, therefore additional protection/clamping is necessary.

The evaluation of an appropriate protection/clamping is described in the following Step 5).

Step 5) External clamping selection (transil and diode):

The external circuitry is selected according to *Table 10*. We start with the evaluation of the circuitry with transil and diode as shown in *Figure 48*:

Figure 48. External clamping circuitry – border conditions



The diode (D) selection:

- Reverse voltage > 52 V
  (Must not conduct during positive voltage on the output →maximum possible output voltage is limited by $V_{HSDClampMax}$ = 52 V)
- Peak forward current > 25 A @ 0.49 ms
  (I_0 @ T_{DEMAG})

→1N4002 (V_{RRM} = 100 V, I_{FSM} = 30 A @ 8.3 ms)

The transil (T) selection:

- Stand-off voltage > 15 V
  (Must not conduct during the reverse battery condition at
  16 V → $V_{BATreverse}$–$V_{HSDdrop}$–V_{Ddrop} = 16 V–0.5 V–0.5 V = 15 V)
- Clamping voltage < 24 V@25 A
  (To be sure that the HSD clamp is not activated
  → $V_{HSDClampMin}$–V_{BAT}–V_{Ddrop} = 41 V–16 V–1 V = 24 V)
- Energy capability requirement (single pulse):
  Peak power: 600 W (considering V_{CL} = 24 V → 24 V*25A = 600 W)
  Pulse duration: 0.49 ms (considering V_{CL} = 24 V)
  Pulse waveform: sawtooth demag. current considered
  Equivalent exponential pulse duration: 0.175 ms

$$0.5 \cdot \frac{0.49\text{ms}}{1.4} = 0.175\text{ms}$$

(see *Figure 45*)

Choice 1) Single pulse consideration:

According to required energy capability (600 W@0.175 ms), we can find a suitable transil in the SMBJ series (ST devices 600 W@10/1000 µs). Maximum peak power of these devices is ~ 825 W@0.175 ms considering 105 °C initial temperature (see *Figure 44* and *Figure 46*).

The first device closest to the reverse battery requirement (stand-off voltage V_{RM} > 15 V) is SMBJ16A:

Type	I_{RM}@V_{RM}		V_{BR}@IR min(1)		V_{CL}@I_{PP} 10/1000 µs		V_{CL}@I_{PP} 8/20 µs		αT(2)
	max		min		max		max		max
	µA	V	V	mA	V	A	V	A	10-4/°C
SMBJ16A/CA	1	16	17.8	1	26	23.1	34.4	116	8.8

1. Pulse test : t_p<50 ms.
2. To calculate V_{BR} or V_{CL} versus junction temperature, use the following formulas:

$V_{BR}@T_j=V_{BR}@25\ °C \times (1 + \alpha T \times (T_j-25))$

$VCL@Tj=V_{CL}@25\ °C \times (1 + \alpha T \times (T_j-25))$

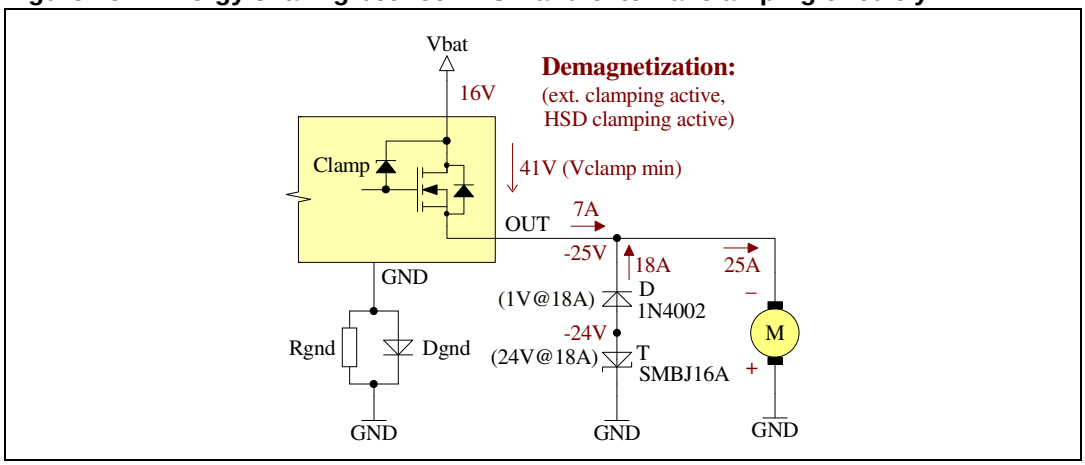
V_{CL}= 24 V@18 A (estimated from V_{CL}/I_{PP} diagram)

V_{CL}= 27 V@25 A (estimated from V_{CL}/I_{PP} diagram)

Then we check the V_{CL}/I_{PP} parameters. As seen from the V_{CL}/I_{PP} characteristics, this transil does not fit with our 24 V@25 A requirement.

Nevertheless, we can decide to use this device given that the HSD can also go in clamp to safely dissipate the remaining energy (see *Figure 49*):

Figure 49. Energy sharing between HSD and external clamping circuitry



The output voltage during the demagnetization phase is -25 V (considering a worst case HSD $V_{ClampMin}$ = 41 V, V_{BAT} = 16 V).

Under these conditions, the external clamping circuitry provides 18 A according to the transil characteristics at 24 V (1 V drop on the protection diode), so the HSD is loaded by the remaining current (25-18 = 7 A). Looking at the I/L diagram, we are clearly in the safe area.

In addition to single pulse energy considerations, the “repetitive energy capability” also needs to be checked – see *Choice 2) Single pulse consideration*.

Choice 2) Single pulse consideration

In the second choice, we select a more powerful transil from the SMCJ series (ST devices 1500 W@10/1000 µs) with a more flat V_{CL}/I_{PP} characteristics:

→ SMCJ18A:

Type	$I_{RM}@V_{RM}$		$V_{BR}@IR$ min(1)		$V_{CL}@I_{PP}$ 10/1000 µs		$V_{CL}@I_{PP}$ 8/20 µs		αT(2)
	max		min		max		max		max
	µA	V	V	mA	V	A	V	A	10-4/°C
SMCJ18A/CA	1	18	20.0	1	29.2	53	39.3	254	9.2

1. Pulse test : t_p<50 ms.
2. To calculate V_{BR} or V_{CL} versus junction temperature, use the following formulas:

$V_{BR}@T_j=V_{BR}@25\ °C \times (1 + \alpha T \times (T_j-25))$

$VCL@Tj=V_{CL}@25\ °C \times (1 + \alpha T \times (T_j-25))$

V_{CL} = 23 V@25 A (estimated from V_{CL}/I_{PP} diagram)

As seen in the datasheet, the selected device is able to fulfill the 24 V/25 A clamping requirement together with a safe stand-off voltage of 18 V (no conduction at reverse battery condition). It means that the HSD is fully protected and does not see any demagnetization energy.

In addition to single pulse energy considerations, the “repetitive energy capability” also needs to be checked.

- Repetitive energy capability check (HSD cycling):

Assuming that the HSD is in a thermal shutdown condition with autorestart (frequency assumed to be ~500 Hz) and $I_0 = I_{limL}$ → 15 A.

One pulse energy – according to *Equation 17* :

$$E = \frac{|V_{CL}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{CL}| \cdot \log\left(\frac{|V_{CL}| + I_0 \cdot R}{|V_{CL}|} \right) \right] =$$

$$= \frac{23}{0.6^2} \cdot 0.00073 \cdot \left[0.6 \cdot 15 - 23 \cdot \log\left(\frac{23 + 15 \cdot 0.6}{23} \right) \right] = 65.5\text{mJ}$$

Demagnetization time check *Equation 12 :*

$$T_{DEMAG} = \frac{L}{R} \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) = \frac{0.00073}{0.6} \cdot \log\left(\frac{25 + 15 \cdot 0.6}{23} \right) = 0.4\text{ms}$$

Average power dissipation on transil during HSD cycling – *Equation 16*):

$$P_{AVG} = f \cdot E$$

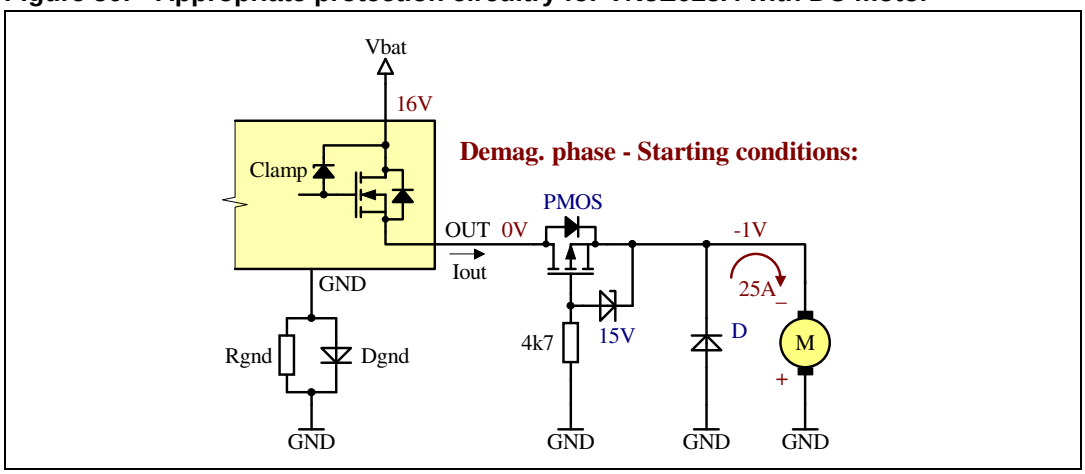
→ 500*0.0655 = 32.8 W

The calculated average power dissipation of 32.8 W is very high - clearly above the capability of standard transil diodes. Therefore this protection can be used only if no PWM control is used and proper diagnostics is implemented to switch-off the HSD in case of overload.

Step 5 – continued) External clamping selection (freewheeling diode)

The following evaluation is conducted on circuitry with a freewheeling diode, as shown in *Figure 50*. In this case, the average power dissipation on the freewheeling diode is not so high. The demagnetization voltage is about -1 V, therefore most of the energy stored in the load inductance is dissipated in the load resistance (0.6 Ω). Relatively slow demagnetization does not cause any problems when driving motors.

Figure 50. Appropriate protection circuitry for VN5E025A with DC motor



Demagnetization time - *Equation 12* (Assuming V_{DEMAG} = -1 V) :

$$T_{DEMAG} = \frac{L}{R} \cdot \log\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \frac{0.00073}{0.6} \cdot \log\left(\frac{1 + 25 \cdot 0.6}{1}\right) = 3.37ms$$

The freewheeling diode selection:

- •Reverse voltage > 52 V
  (Must not conduct during positive voltage on the output →maximum possible output voltage is limited by $V_{HSDClampMax}$ = 52 V)

- Peak forward current: > 25 A @ 3.37 ms
  (I_0 @ T_{DEMAG})
- Average power dissipation (repetitive turn-off)

Assuming that the HSD is in a thermal shutdown condition, with autorestart (frequency assumed to be ~500 Hz) and $I_0 = I_{limL} \Rightarrow$ 15 A.

Energy dissipated in the freewheeling diode - *Equation 17 :*

(HSD turn off: $I_0 = I_{limL}$ = 15 A):

$$E = \frac{|V_{CL}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{CL}| \cdot \left(\log \frac{|V_{CL}| + I_0 \cdot R}{|V_{CL}|} \right) \right] =$$

$$= \frac{1}{0.6^2} \cdot 0.00073 \cdot \left[0.6 \cdot 15 - 1 \cdot \log \left(\frac{1 + 15 \cdot 0.6}{1} \right) \right] = 13.6\text{mJ}$$

Demagnetization time for $I_0 = I_{limL}$ = 15 A - *Equation 12* :

$$T_{DEMAG} = \frac{L}{R} \cdot \log \left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \right) = \frac{0.00073}{0.6} \cdot \log \left(\frac{1 + 15 \cdot 0.6}{1} \right) = 2.8\text{ms}$$

The demagnetization time (2.8 ms) is higher than the assumed HSD cycling frequency period (2 ms). Therefore the average power dissipation on the freewheeling diode cannot be easily calculated using *Equation 16* : P_{AVG}=f.E $\Rightarrow$ 500 × 0.0136 = 6.8 W (real value is significantly lower).

As a rough estimation, we can use the average power dissipation during one demagnetization pulse:

$$P_{AVG} = \frac{E}{T_{DEMAG}} = \frac{0.0136}{0.0028} = 4.9\text{W}$$

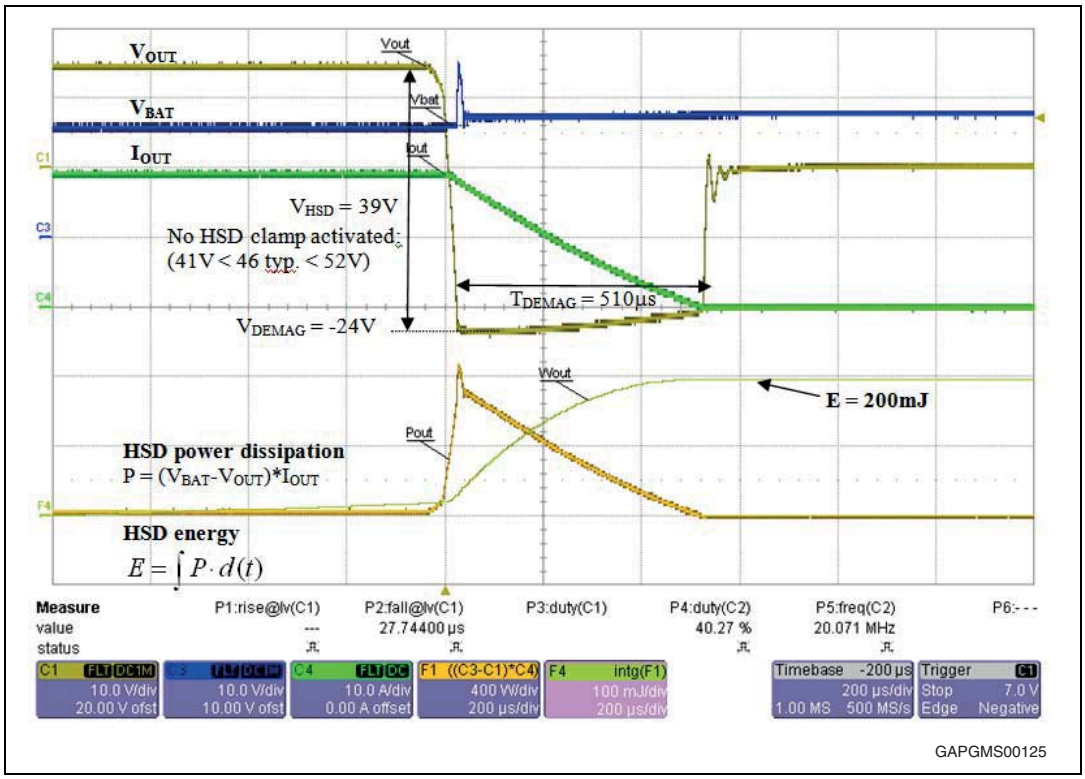
$\rightarrow$1N5401 (V_{RRM}=100 V, I_{FSM}=200 A@8.3 ms, P_D= 6.25 W)

Step 6) Measurement (confirmation of theoretical analysis)

- Transil diode protection circuitry: SMBJ16A + 1N4002

The measurement was done at room temperature on VND5E025AK loaded with a blocked DC motor (as specified in the beginning) and with external protection regarding Choice 1) SMBJ16A + 1N4002:

Figure 51. Demagnetization energy measurement – VND5E025AK, Motor, SMBJ16A and 1N4002



The measured energy is significantly lower than the calculated one (200 mJ measured versus 260 mJ calculated), while the demagnetization time fits well. This difference can be explained by measurement at ambient temperature when coil resistance is ~25 % higher than the resistance at -40 °C used in the calculations.

Measured stall current was 19 A (versus 25 A specification at -40 °C). As seen from the screenshot, the external clamping circuitry (SMBJ16A + 1N4002) limits the demagnetization voltage to -24 V, so the voltage across the HSD is maximum 39 V (below internal clamp activation).

Reverse battery test:

The measured break down voltage of the external clamping circuitry is:

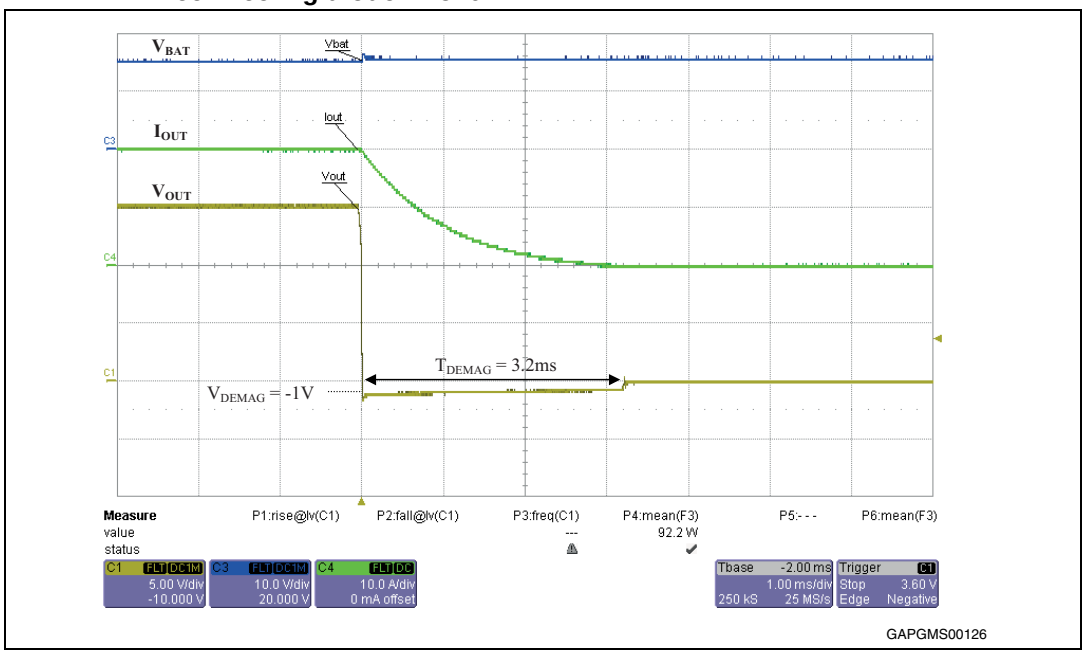
-19 V@-1 mA → fitting the -16 V@60 s reverse battery requirement.

The transil diode failed (overheating) during HSD thermal shutdown cycling (as expected in theoretical calculation).

- Freewheeling diode protection circuitry: 1N5401

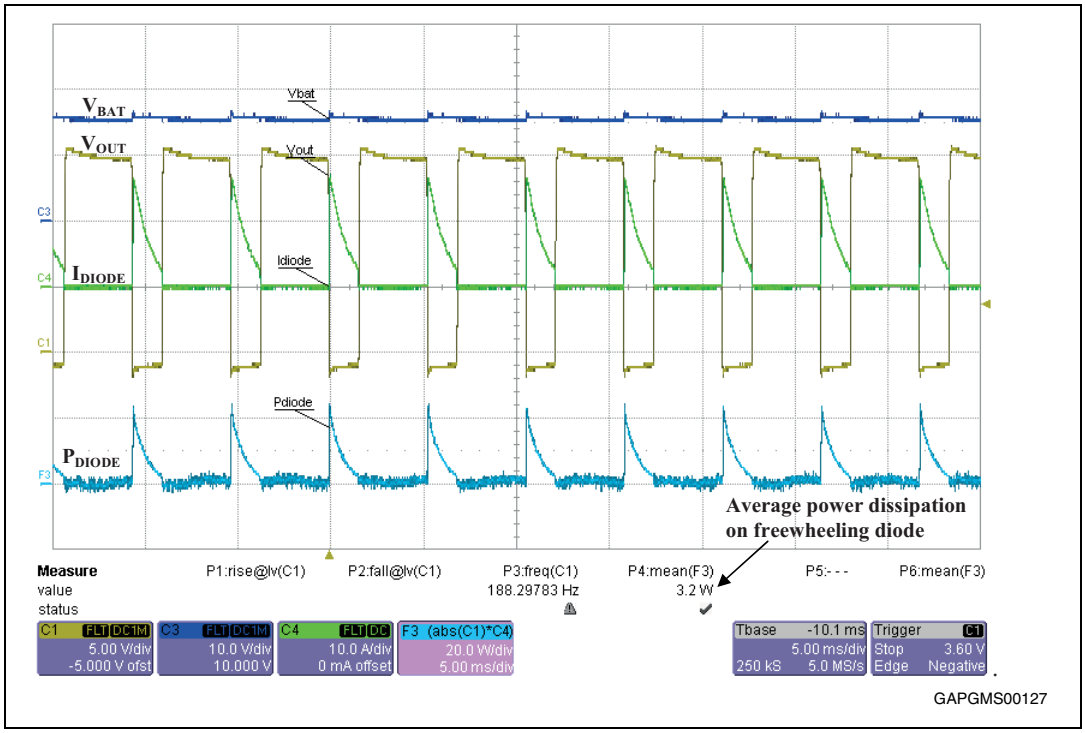
The measurement was done at room temperature on VND5E025AK loaded with a blocked DC motor (as specified in the beginning) and with external freewheeling diode 1N5401.

Figure 52. Demagnetization phase – VND5E025AK, DC motor (blocked), freewheeling diode 1N5401



The measured demagnetization time of 3.2 ms is very close to the calculated value (3.37 ms). Due to the measurement at room temperature, the stall current was only 20 A (versus 25 A specified at -40 °C).

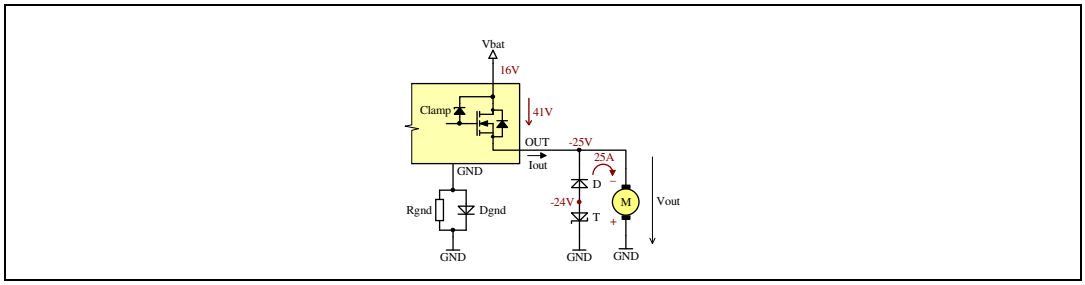
Figure 53. Repetitive demagnetization – VND5E025AK (TSD cycling), DC motor, 1N5401



The average power dissipation measured on the freewheeling diode is 3.2 W, while the HSD thermal shutdown cycling frequency was 188 Hz. These values are below theoretical calculations. Real HSD cycling frequency is much lower than the frequency assumed in the calculation (500 Hz – based on simulation with resistive load).

Conclusion:

The demagnetization energy is two times higher than the device is able to withstand, therefore additional protection/clamping is necessary. Two different external protection circuits were analyzed:

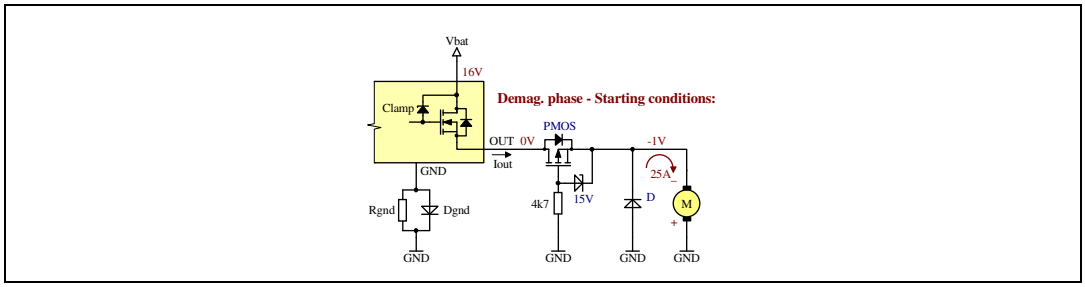


- Transil and diode (SMBJ16A or SMCJ18A and 1N4002)

The transil is not able to withstand the repetitive energy when the HSD is in a thermal cycling condition. Therefore this protection can by used only if no PWM control is used and proper diagnostics is implemented to switch-off the HSD in case of overload.

- Freewheeling diode (1N5401) and reverse battery protection circuitry with MOSFET

With this external protection circuitry, the repetitive energy capability requirement is also fulfilled.



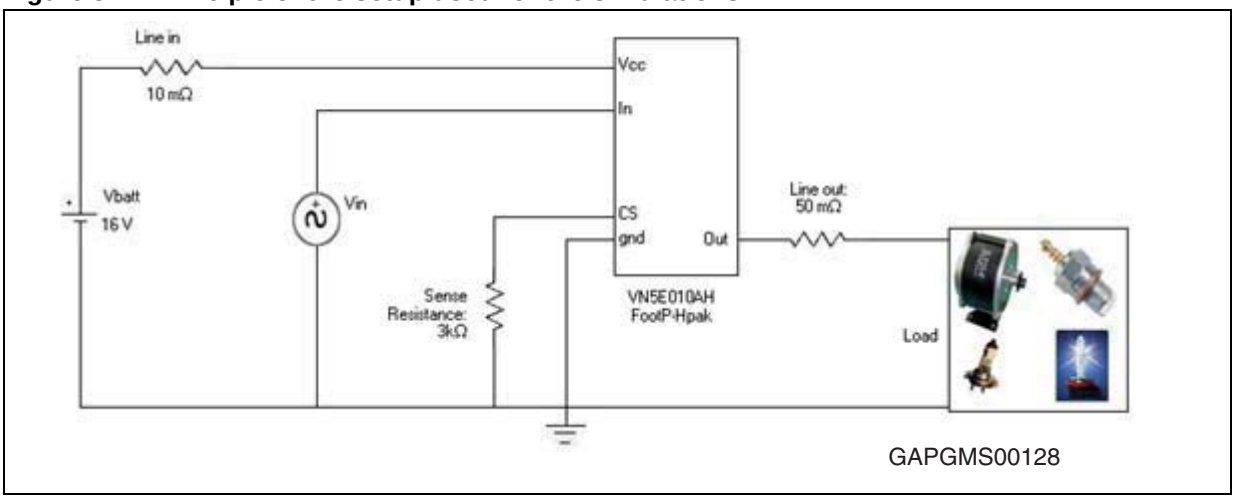
5 High Side Driver selection for lamp loads

This chapter proposes drivers that can be used for typical automotive lamp loads or typical combinations of lamps.

A properly selected driver should allow the safe turning on of the bulb without any restrictions under normal conditions. Under worst case conditions, the driver should still be able to turn on the bulb even if some protection of the driver may be triggered temporarily. However, the driver's long term integrity should not be jeopardized.

In order to decide which driver is suitable to turn on a lamp, three conditions are first defined - see a), b) and c) below. Afterwards a simulation is performed with the pre-selected bulb/driver combination, in order to verify the driver matches the requirements under the defined conditions. The tool used for this simulation is based on Matlab/Simulink.

Figure 54. Principle of the setup used for the simulations

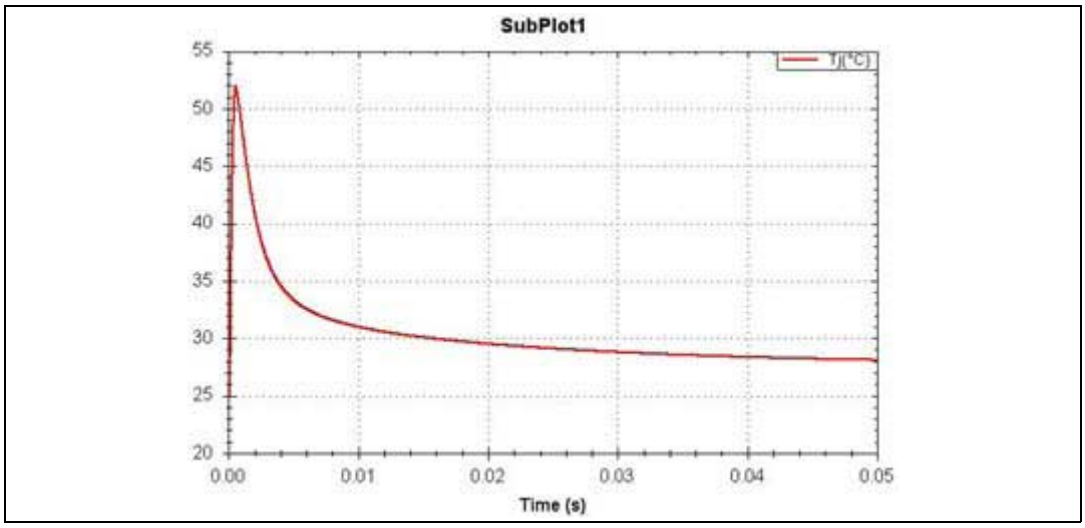


The prerequisite to appear in *Table 12*, *Table 13*,*Table 14*, *Table 15* is that the driver has to fulfill all of the following three requirements:

a) Normal condition

V_{batt} = 13.5 V; T_c = 25 °C; T_{bulb} = 25 °C

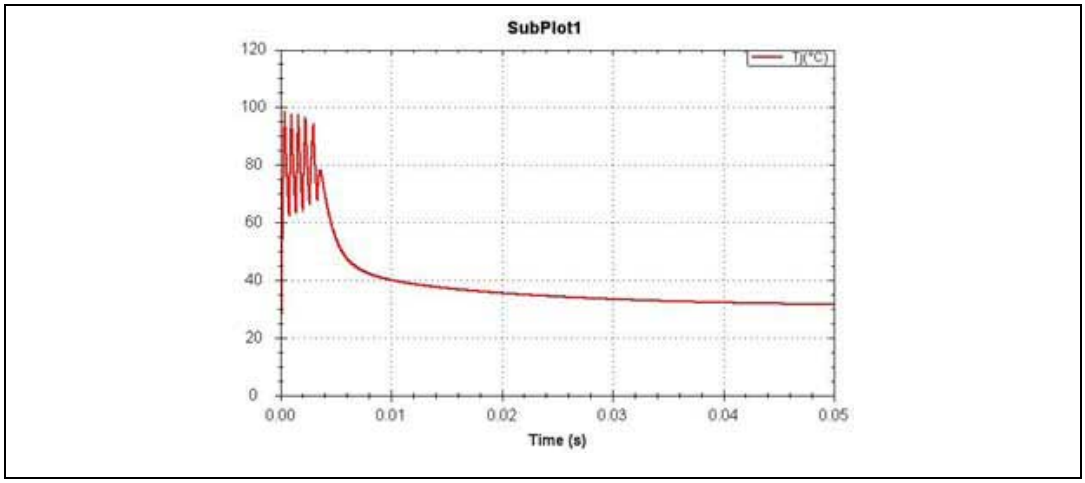
Requirement: none of the protection functions must be triggered.



b) Cold condition

V_{batt} = 16 V; T_c = 25 °C; T_{bulb} = -40 °C

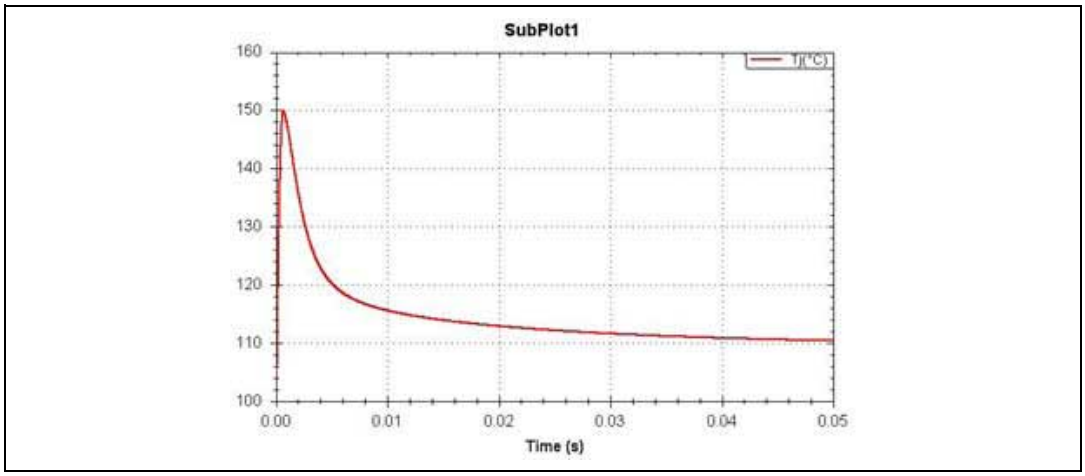
Requirement: power limitation allowed for durations of less than 20 ms.



c) Hot condition

V_{batt} = 16 V; T_c = 105 °C; T_{bulb} = 25 °C

Requirement: driver must not run into thermal shutdown.



Note: The mentioned criteria only refer to the inrush current at turn-on of a cold bulb. The steady state power dissipation and, in case PWM is applied, the additional switching losses of the driver also have to be considered in order not to exceed the maximum possible power dissipation. This obviously becomes more important with a larger number of channels per package (i.e. dual or quad channel drivers) and high power loads applied to more than one channel.

Table 12. List of suggested bulb/driver combinations(1/4)

Bulb load [W]	Driver ron [mΩ]	Single channel part #	Dual channel part #	Quad channel part #
65	10	VN5010AK VN5E010AH		
	12	VN5012AK	VND5012AK VND5E012AY	
	16	VN5016AJ VN5E016AH		

Table 12. List of suggested bulb/driver combinations(1/4) (continued)

Bulb load [W]	Driver ron [mΩ]	Single channel part #	Dual channel part #	Quad channel part #
60	10	VN5010AK VN5E010AH		
	12	VN5012AK	VND5012AK VND5E012AY	
	16	VN5016AJ VN5E016AH		
55	10	VN5010AK VN5E010AH		
	12	VN5012AK		
	16	VN5016AJ VN5E016AH	VND5012AK VND5E012AY	

Table 13. List of suggested bulb/driver combinations(2/4)

Bulb load [W]	Driver ron [mΩ]	Single channel part #	Dual channel part #	Quad channel part #
3x27 + 7	10	VN5010AK VN5E010AH		
	12	VN5012AK		
	16	VN5016AJ VN5E016AH	VND5012AK VND5E012AY	
2x27 + 7	12	VN5012AK	VND5012AK VND5E012AY	
	16	VN5016AJ VN5E016AH		
	25	VN5025AJ VN5E025AJ	VND5025AK VND5E025AK	
	27			VNQ5027AK

Table 13. List of suggested bulb/driver combinations(2/4) (continued)

Bulb load [W]	Driver ron [mΩ]	Single channel part #	Dual channel part #	Quad channel part #
27 + 7	25	VN5025AJ VN5E025AJ	VND5025AK VND5E025AK	
	27			VNQ5027AK
27	25	VN5025AJ VN5E025AJ	VND5025AK VND5E025AK	
	27			VNQ5027AK
	50	VN5E050AJ	VND5E050J/AJ VND5E050K/AK	VNQ5E050K/AK

Table 14. List of suggested bulb/driver combinations(3/4)

Bulb load [W]	Driver ron [mΩ]	Single channel part #	Dual channel part #	Quad channel part #
3x21 + 5	10	VN5010AK VN5E010AH		
	12	VN5012AK	VND5012AK VND5E012AY	
	16	VN5016AJ VN5E016AH		
	25	VN5025AJ VN5E025AJ	VND5025AK VND5E025AK	
	27			VNQ5027AK
2x21 + 5	16	VN5016AJ VN5E016AH		
	25	VN5025AJ VN5E025AJ	VND5025AK VND5E025AK	
	27			VNQ5027AK

Table 14. List of suggested bulb/driver combinations(3/4) (continued)

Bulb load [W]	Driver ron [mΩ]	Single channel part #	Dual channel part #	Quad channel part #
21 + 5	25	VN5025AJ VN5E025AJ	VND5025AK VND5E025AK	
	27			VNQ5027AK
	50	VN5E050J/AJ	VND5E050J/AJ VND5E050K/AK	VNQ5E050K/AK
21	25	VN5025AJ VN5E025AJ	VND5025AK VND5E025AK	
	27			VNQ5027AK
	50	VN5050J/AJ VN5E050J/AJ	VND5050J/AJ VND5050K/AK VND5E050J/AJ VND5E050K/AK	VNQ5050K/AK VNQ5E050K/AK

Table 15. List of suggested bulb/driver combinations(4/4)

Bulb load [W]	Driver ron [mΩ]	Single channel part #	Dual channel part #	Quad channel part #
10	50	VN5050J/AJ VN5E050J/AJ	VND5050J/AJ VND5050K/AK VND5E050J/AJ VND5E050K/AK	VNQ5050K/AK VNQ5E050K/AK
	160	VN5E160S/AS	VND5E160J/AJ	VNQ5E160K/AK
7	160	VN5160S VN5E160S/AS	VND5160J/AJ VND5E160J/AJ	VNQ5160K/AK VNQ5E160K/AK
5	160	VN5160S VN5E160S/AS	VND5160J/AJ VND5E160J/AJ	VNQ5160K/AK VNQ5E160K/AK

6 Paralleling of HSDs

6.1 Paralleling of CS_DIS (current sense disable) and IN (input)

The following chapters describe the paralleling of CS_DIS and IN pins of HSDs, taking into account device technology (monolithic HSDs or hybrid HSDs) and supply line configuration (either the same or separate supply lines for each HSD).

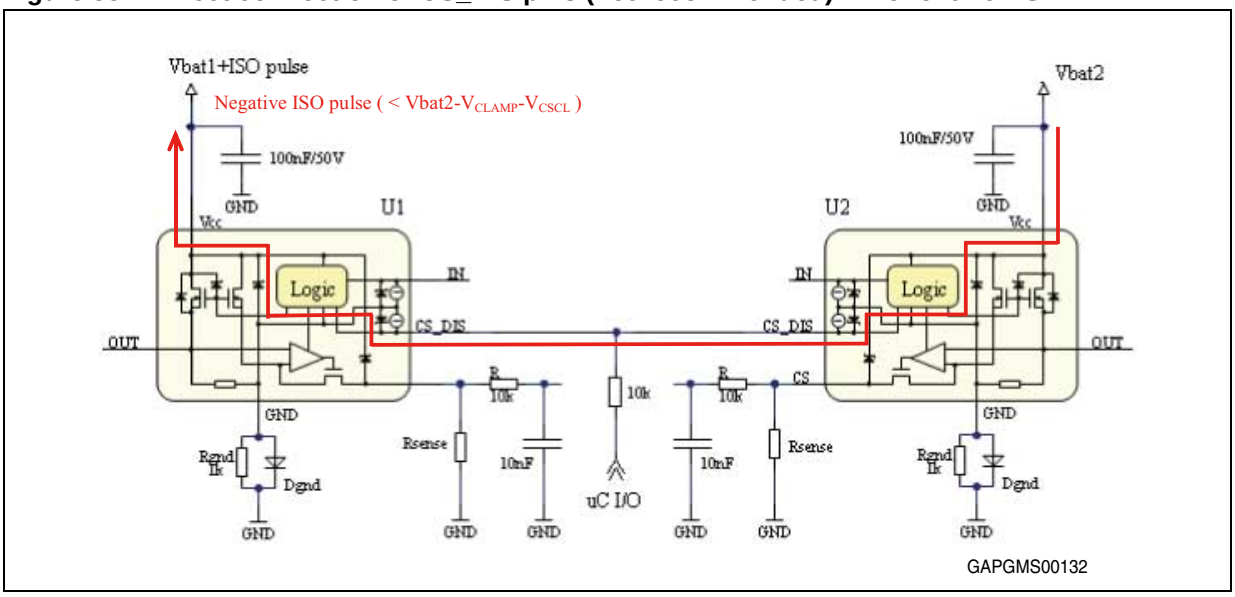
Direct connection of CS_DIS or IN pins is generally allowed with devices designed with the same technology (monolithic or hybrid) supplied from one supply line. In all other cases (like the combination of monolithic with hybrid technology or different supply lines, or both), we should use additional components to ensure safe operation under conditions in automotive environments (ISO pulses, reverse battery …).

The clamp structure on the CS_DIS pin is the same as on the IN pin, therefore all the explanations related to the paralleling of the CS_DIS pins are also applicable to paralleling of IN pins.

6.1.1 Monolithic HSDs supplied from different supply lines

Paralleling CS_DIS pins of monolithic HSDs is possible, however some precautions in schematics should be applied if the HSDs are supplied from different supply lines. In this case, the direct connection of CS_DIS pins (as shown in *Figure 55*) is not safe.

Figure 55. Direct connection of CS_DIS pins (not recommended) – Monolithic HSD



Direct connection of CS_DIS pins is not safe in following cases:

- Negative voltage surge on either on Vbat1 or Vbat2
- Positive voltage surge either on Vbat1 or Vbat2 while:
  - Device GND pin disconnected;
  - Dgnd not used (resistor protection only);
  - Positive pulse energy higher than HSD (or D_{gnd}) capability - all paralleled devices can be damaged

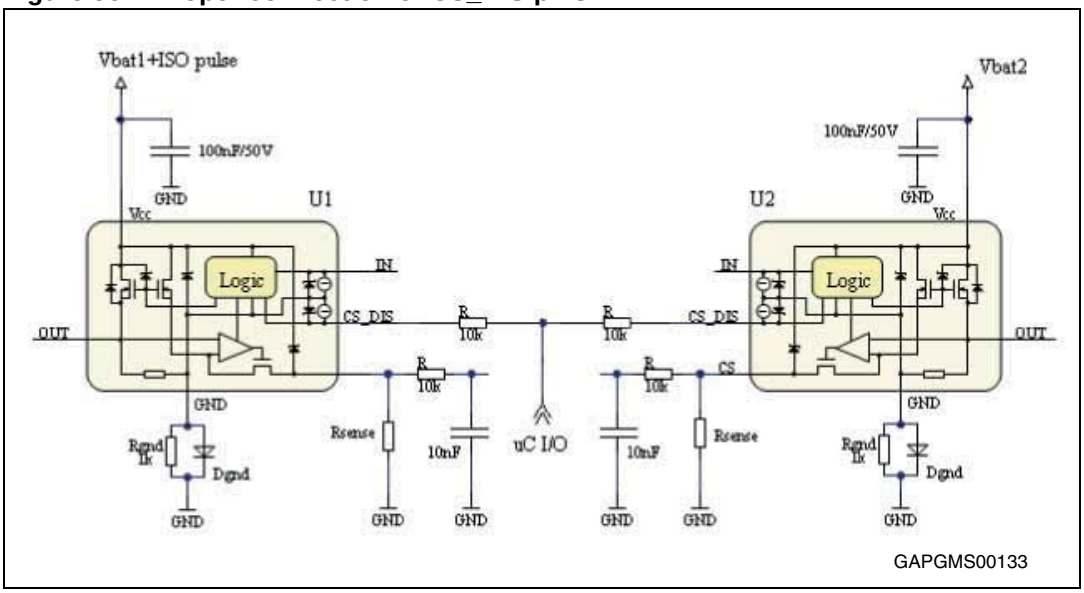
A negative voltage surge (ISO7637-2 pulse 1, 3a) either on Vbat1 or Vbat2 is directly coupled to the HSD GND pin through the involved Vcc-GND clamp structure. As soon as this occurs and the negative voltage on GND pin is large enough to activate all involved clamp structures, there may be an unlimited current flow through both CS_DIS pins (supported by current from Vcc through the associated parasitic bipolar structure). This current can lead to malfunction or even failure of one or both of the HSDs.

A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on Vbat1 or Vbat2 may lead to the HSD GND pin to rise in voltage (in case of missing Dgnd, Dgnd failure or GND pin disconnected). As soon as this occurs, the voltage on CS_DIS pin also rises (the CS_DIS pin clamp structure is linked with the GND). If the voltage on the CS_DIS line reaches ~6.3 V (clamp voltage on CS_DIS pin) there may be an unlimited current flow through both CS_DIS pins (supported by current from Vcc through the associated parasitic bipolar structure). This current can lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such failures add a 10 KΩ resistor in series to each CS_DIS pin (see *Figure 56*).

In principle, the same applies to the input pins (the clamp structure is the same as on the CS_DIS pin).

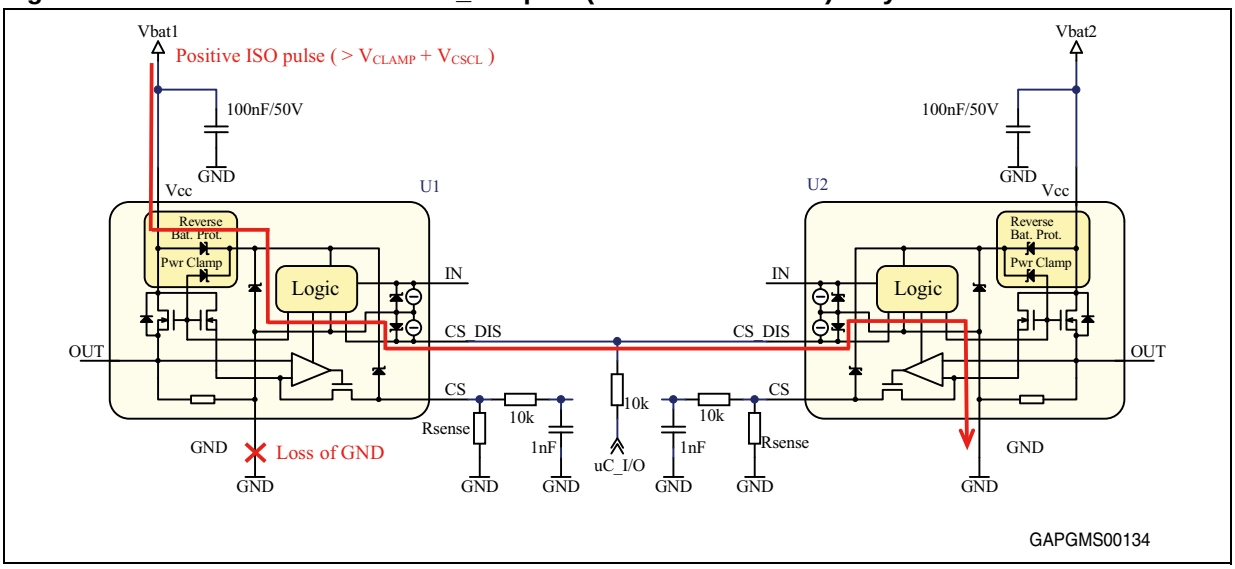
Figure 56. Proper connection of CS_DIS pins



6.1.2 Hybrid HSDs supplied from different supply lines

Paralleling of CS_DIS pins of hybrid HSDs is possible, however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of CS_DIS pins (as shown in *Figure 57*) is not safe.

Figure 57. Direct connection of CS_DIS pins (not recommended) – Hybrid HSD



Direct connection of CS pins is not safe in the following cases:

- Loss of GND connection

If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are no longer clamped (considering no other devices are connected to this supply line). If the transient voltage is large enough to activate involved clamp structures, there may be unlimited current flow between both supply lines through the CS_DIS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

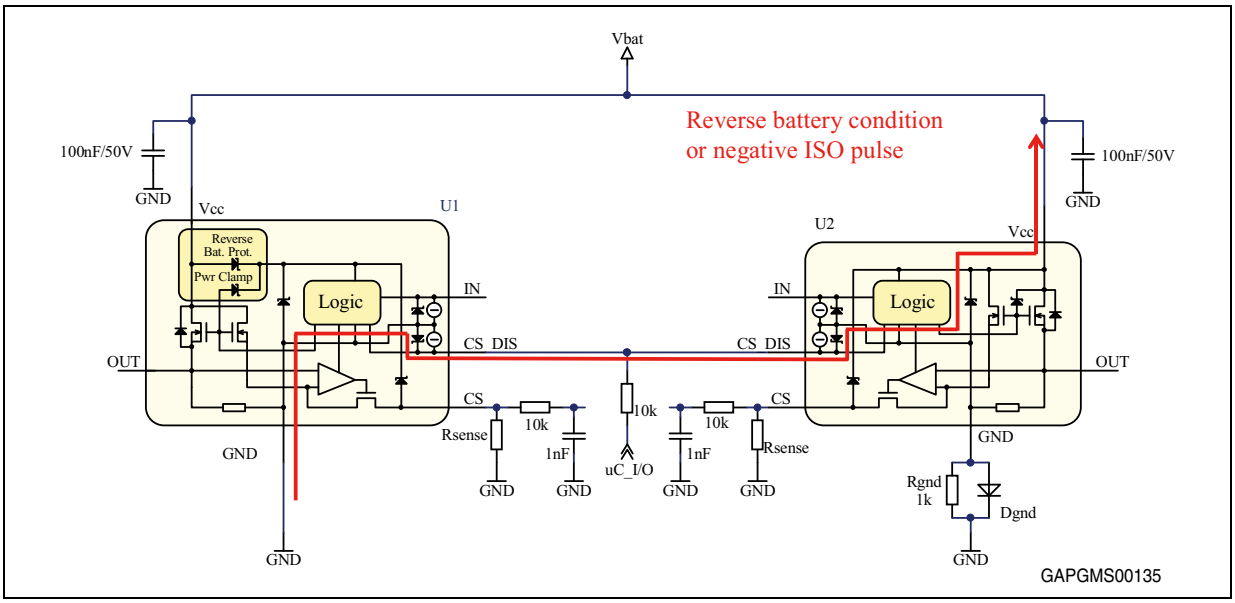
In order to avoid such failures, add a 10 KΩ resistor in series to each CS_DIS pin (as already described in case of monolithic devices – see *Figure 6.1.1: Monolithic HSDs supplied from different supply lines on page 72*).

In principle, the same applies to the input pins (the clamp structure is the same as on the CS_DIS pin).

6.1.3 Mix of monolithic and hybrid HSDs

Paralleling of CS_DIS pins of monolithic and hybrid HSD is possible, however some precautions in schematics must be applied. The direct connection of CS_DIS pins (as shown in *Figure 58*) is not safe (even if we consider the same power supply for both devices).

Figure 58. Direct connection of CS_DIS pins (not recommended) – Mix of monolithic and hybrid HSD



Direct connection of CS pins is not safe in the following cases (single supply line considered):

- Reverse battery
- Negative ISO pulse

Due to the different concepts of reverse battery protection of hybrid and monolithic devices, there is a way for unlimited current flow between both devices in case of reverse battery conditions. The hybrid device has an integrated reverse battery protection in the Vcc line, while the monolithic device needs an external diode/resistor in series with the GND pin (refer to *Section 1.2: Reverse battery protection*). The different potential on each GND pin (hybrid: ~ 0 V, monolithic: Vbat - 0.7 V) leads to the activation of both CS_DIS clamp structures when V_{BAT} is below ~ -7.5 V (V_{CSCL} and two diode voltage drop). The resulting current can lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such failure, add a 10 KΩ resistor in series to each CS_DIS pin (as already described in case of paralleling of monolithic devices – see *Figure 6.1.1: Monolithic HSDs supplied from different supply lines on page 72*).

In principle, the same applies to the input pins (the clamp structure is the same as on CS_DIS pin).

6.2 Paralleling of CS pins (current sense)

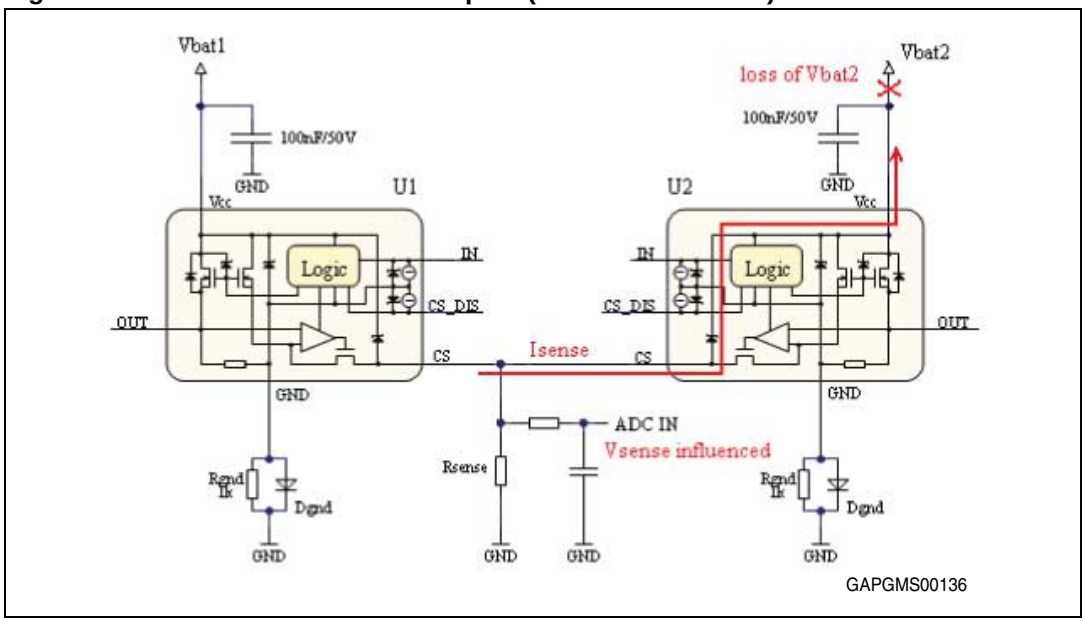
The following chapters describe the paralleling of CS pins of HSDs, taking into account device technology (monolithic HSDs or hybrid HSDs) and supply line configuration (either the same or separate supply line for each HSD).

Direct connection of CS pins is generally allowed when the devices are supplied from one supply line. In case of separated supply lines, we should use additional components to ensure a safe operation under conditions in automotive environments (ISO pulses, reverse battery …).

6.2.1 Monolithic HSDs supplied from different supply lines

Paralleling CS pins of monolithic HSDs is possible, however some precautions in schematics should be applied if the HSDs are supplied from different supply lines. Direct connection of CS pins (as shown in the next picture) is not safe.

Figure 59. Direct connection of CS pins (not recommended) – Monolithic HSD



Direct connection of CS pins is not safe in following cases:

- Negative voltage surge on either on Vbat1 or Vbat2
- Positive voltage surge either on Vbat1 or Vbat2 while:
  - Device GND pin disconnected;
  - Dgnd not used (resistor protection only);
  - Positive pulse energy higher than the HSD (or Dgnd) capability - all paralleled devices can be damaged
- Loss of Vbat1 or Vbat2

A negative voltage surge (ISO7637-2 pulse 1, 3a) either on Vbat1 or Vbat2 is directly coupled to the CS pin through the internal Vcc-CS clamp structure. If the negative voltage on the CS line is high enough to activate the Vcc-CS clamp structure, there may be an unlimited current flow through both CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

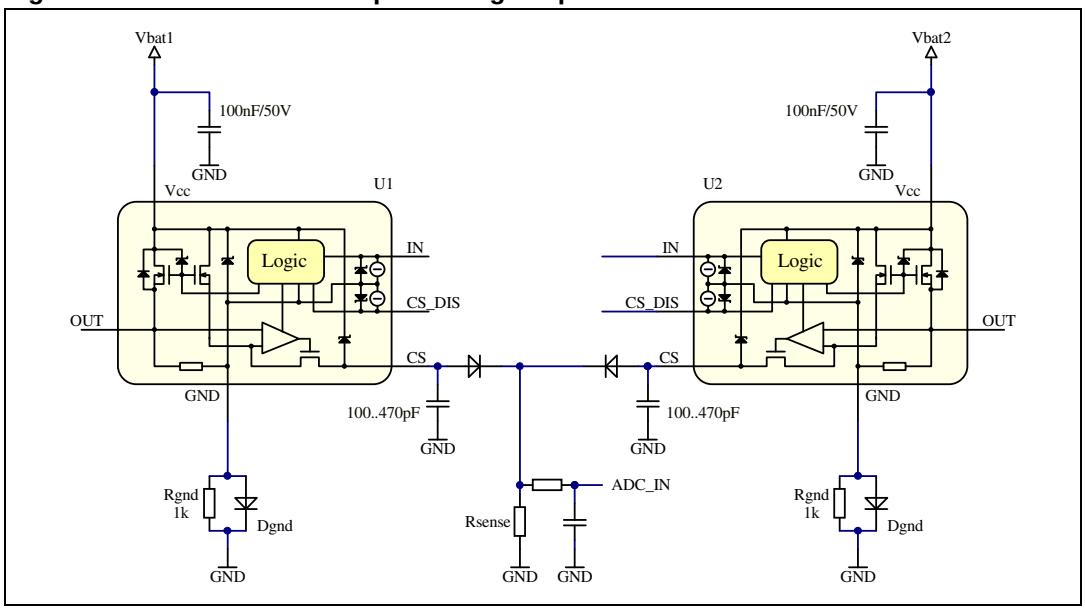
A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on Vbat1 or Vbat2 together with missing Dgnd (Dgnd not used, Dgnd failure or GND pin disconnected) can activate the Vcc-CS clamp structure (clamp voltage similar to Vcc-GND clamp). As soon as this occurs there may be an unlimited current flow through both CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

Loss of either Vbat1 or Vbat2 leads to an incorrect current sense signal. If Vbat2 is lost, U2 (and other components connected to Vbat2) is supplied by U1 current sense signal through the internal Vcc-CS clamp structure. Therefore, the voltage on CS bus drops to almost 0V resulting in an invalid V_{SENSE} reading.

In order to protect the devices during ISO pulses and to ensure a valid current sense signal, we can add a diode in series to each CS pin (as shown in the following schematics). In order to suppress the rectification of noise injected to the sense line, add a ceramic filter capacitor between each CS pin and ground.

However, the voltage drop on diodes in series with the CS pin can have an influence on the dynamic range of current sense, temperature and current sense accuracy.

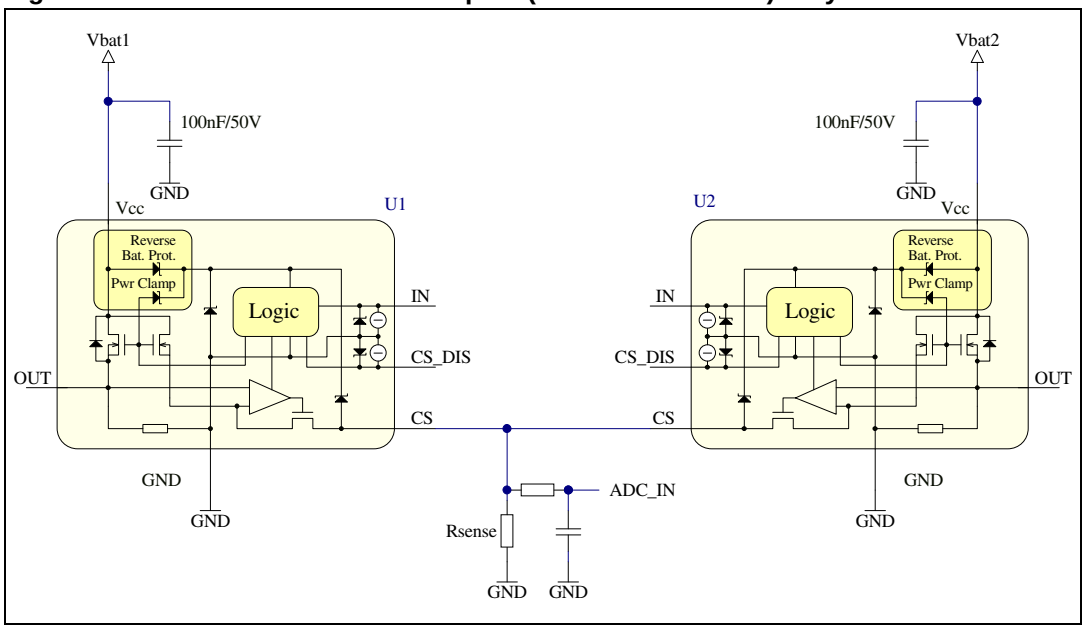
Figure 60. Safe solution for paralleling CS pins



6.2.2 Hybrid HSDs supplied from different supply lines

Paralleling CS pins of hybrid HSDs is possible, however some precautions in schematics should be applied if the HSDs are supplied from different supply lines. Direct connection of CS pins (as shown in the next picture) is not safe.

Figure 61. Direct connection of CS pins (not recommended) – Hybrid HSD



Direct connection of CS pins is not safe in following cases:

- Loss of Vbat1 or Vbat2
- Loss of GND connection

Loss of either Vbat1 or Vbat2 leads to an incorrect current sense signal. If Vbat2 is lost, U2 logic part is supplied by U1 current sense signal through the internal Vcc-CS clamp structure. Therefore the voltage on CS bus drops and we no longer have an accurate V_{SENSE} reading.

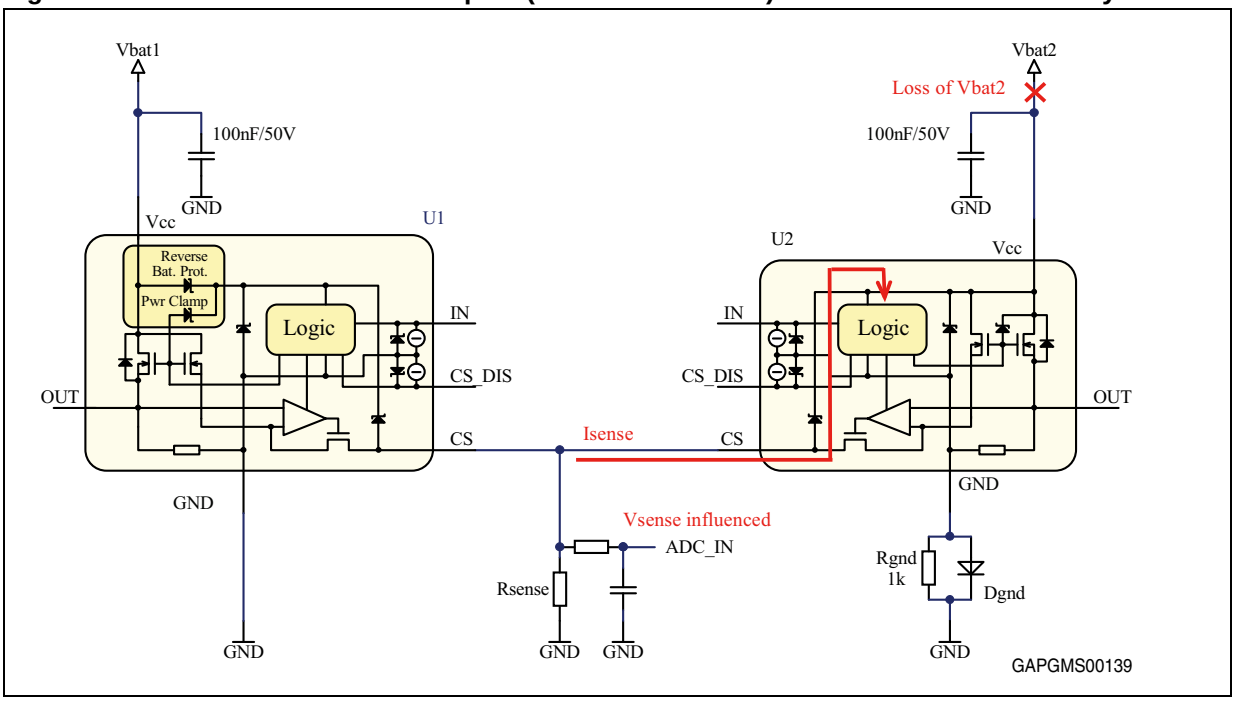
If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are no longer clamped (considering no other devices connected on this supply line). If the transient voltage is high enough to activate involved clamp structures, there may be an unlimited current flow between both supply lines through the CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

In order to ensure a valid current sense signal and to protect devices in all previously described cases, we can add a diode in series to each CS pin (as previously described in the case of monolithic devices – see *Section 6.2.1: Monolithic HSDs supplied from different supply lines*).

6.2.3 Mix of monolithic and hybrid HSDs supplied from different supply lines

Paralleling CS pins of monolithic and hybrid HSDs is possible, however some precautions in schematics should be applied if the HSDs are supplied from different supply lines. Direct connection of CS pins (as shown in *Figure 62*) is not safe.

Figure 62. Direct connection of CS pins (not recommended) – Mix of monolithic and hybrid HSD



Direct connection of CS pins is not safe in following cases:

- Negative ISO pulse on Vbat2
- Loss of Vbat1 or Vbat2
- Loss of GND connection

A negative voltage surge (ISO7637-2 pulse 1, 3a) on Vbat2 is directly coupled to the CS pin through the internal Vcc-CS clamp structure. If the negative voltage on the CS line is high enough to activate the Vcc-CS clamp structure, there may be an unlimited current flow through both CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

Loss of either Vbat1 or Vbat2 leads to an incorrect current sense signal. If Vbat2 is lost, U2 logic part is supplied by U1 current sense signal through the internal Vcc-CS clamp structure. Therefore the voltage on CS bus drops, resulting in an inaccurate V_{SENSE} reading.

If the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are no longer clamped (considering no other devices connected to this supply line). If the transient voltage is high enough to activate the involved clamp structures, there can be an unlimited current flow between both supply lines through the CS pins. This current can lead to malfunction or even failure of one or both of the HSDs.

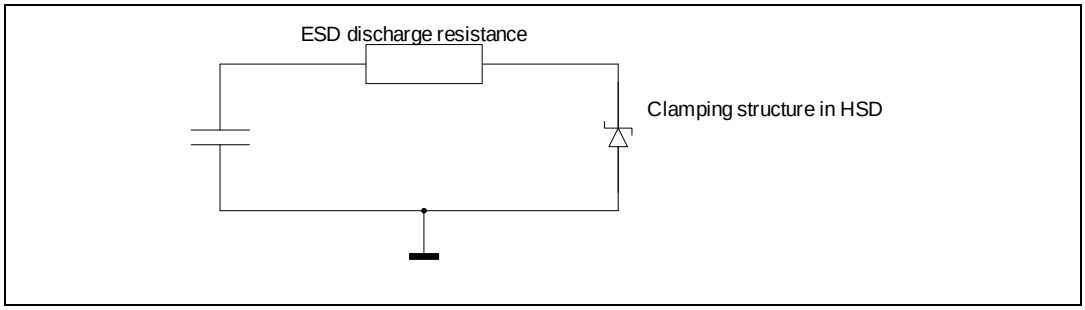
In order to ensure a valid current sense signal and to protect devices in all previously described cases, we can add a diode in series to each CS pin (as previously described in the case of monolithic devices – see previous *Section 6.2.1: Monolithic HSDs supplied from different supply lines*).

7 ESD protection

7.1 ESD protection of HSD – calculations

The ESD robustness of a typical M0-5 HSD is rated at 5000 V on the output- as well as Vcc-pin according to the Human Body Model (100 pF, 1.5 kΩ). This applies to positive as well as negative ESD pulses. For any ESD pulse beyond these values, external protection is required.

Calculation of the energy capability of the HSD output without external protection (negative ESD pulse)



The energy content of the ESD pulse is:

Equation 19

$$V_{EDS} = \frac{1}{2} \cdot C_{ESD} \cdot V^2_{ESD}$$

The energy dissipated by the resistance is:

Equation 20

$$W_R = \frac{1}{2} \cdot C_{ESD} \cdot (V_{ESD} - V_{DEMAG})^2$$

The energy dissipated by the HSD is:

Equation 21

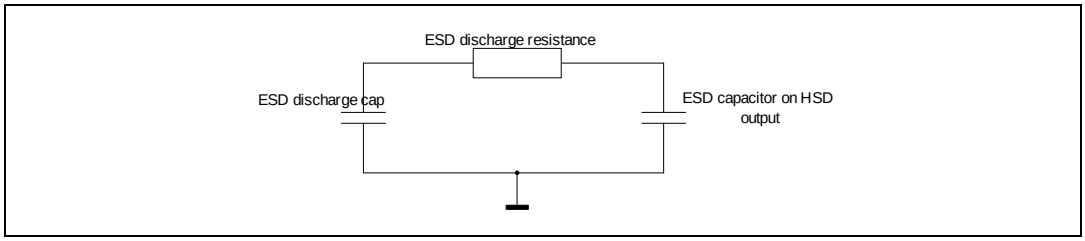
$$W_{HSD} = (V_{ESD} - V_{DEMAG}) \cdot V_{clamp} \cdot C_{ESD}$$

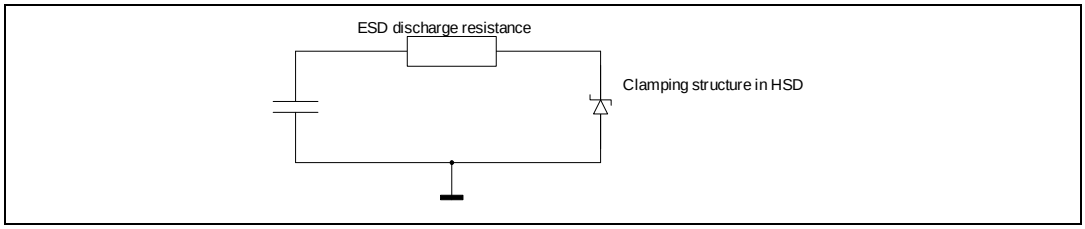
The maximum ESD pulse energy capability of the HSD can be calculated using *Equation 21* and the data sheet parameters (typical example):

$$W_{HSDMAX} = 4954V \cdot 46V \cdot 100pF \cong 23\mu J$$

Calculation of external protection (negative ESD pulse)

When the ESD pulse amplitude or the ESD capacitance is increased or the discharging resistance is decreased, the HSD needs external protection because the energy discharged in the HSD exceeds the limit calculated in *Equation 21*. If we add a ceramic capacitor on the output, the ESD pulse initially only charges the capacitor without impacting the HSD until the voltage reaches the HSD active clamping voltage. Then the voltage stays constant (without further impact on the capacitor), and excessive energy is absorbed by the ESD discharge resistance and by the HSD.





If in the first step we neglect the HSD, the final voltage becomes:

Equation 22

$$V_{Final} = V_{ESD} \cdot \left(\frac{C_{ESD}}{C_{ESD} + C_{EXT}} \right)$$

with V_{ESD}=8 KV, C_{ESD}=330 pF and F_{Final}=50 V, C_{EXT} should be >53 nF.

Since the HSD can absorb some ESD energy on its own, the external capacitor can actually be smaller.

The time t_1 defines the point in time when the external capacitor reaches the demagnetisation voltage of the HSD and does not charge further.

The time constant for discharging the ESD capacitor is:

Equation 23

$$\tau = R_{ESD} \cdot C_{ESD} \cdot \frac{C_{EXT}}{C_{EXT} + C_{ESD}}$$

with $C_{EXT} >> C_{ESD} \rightarrow$

$$\tau \approx R_{ESD} \cdot C_{ESD}$$

Equation 24

$$I(t) = \frac{V_{ESD}}{R_{ESD}} \cdot e^{\frac{-t}{\tau}}$$

Equation 25

$$V_{C_{ESD}}(t) = V_{ESD} \cdot e^{\frac{-t}{\tau}} + V_{Final} \cdot \left(1 - e^{\frac{-t}{\tau}}\right)$$

Equation 26

$$V_{C_{EXT}}(t) = V_{Final} \cdot \left(1 - e^{\frac{-t}{\tau}}\right)$$

Equation 27

$$t_1 = -\tau \cdot \log\left(1 - \frac{V_{DEMAG}}{V_{Final}}\right)$$

The residual voltage at the ESD capacitor when the external capacitor is charged to the HSD clamping voltage becomes:

Equation 28

$$V_{C_{ESD}}(t1) = V_{ESD} - V_{DEMAG} \cdot \frac{C_{EXT}}{C_{ESD}}$$

Therefore the energy absorbed by the HSD becomes:

Equation 29

$$W_{HSD} = \left(V_{ESD} - V_{DEMAG} \cdot \left(1 + \frac{C_{EXT}}{C_{ESD}}\right)\right) \cdot V_{clamp} \cdot C_{ESD}$$

Once we know the maximum ESD energy capability of the HSD (calculated with *Equation 21*), we can calculate the necessary external capacitor:

Equation 30

$$C_{EXT} > \frac{V_{ESD} - V_{DEMAG}}{V_{DEMAG}} \cdot C_{ESD} - \frac{W_{HSDMAX}}{V_{DEMAG} \cdot V_{clamp}}$$

Of course, the external capacitor needs a voltage capability larger than the maximum clamping voltage of the HSD.

In addition, it must be ensured that the ESD discharge current cannot exceed the maximum current capability of the HSD:

Equation 31

$$I(t_1) < I_{LIMHmax}$$

And therefore

Equation 32

$$C_{EXT} > C_{ESD} \cdot \left(\frac{(V_{ESD} - R_{ESD} \cdot I_{LIMHmax})}{V_{DEMAG}} - 1 \right)$$

Example 1:

Contact discharge 8 kV, 330 pF, 2 kW, $I_{LIMH\ max}$=14 A (VNx5E160 HSD), battery not supplied (Vcc=0 V)

→according to *Equation 30* C_{EXT} > 46 nF

→according to *Equation 32* C_{EXT} > -143 nF

→C_{EXT} > 46 nF fulfils both requirements.

Example 2:

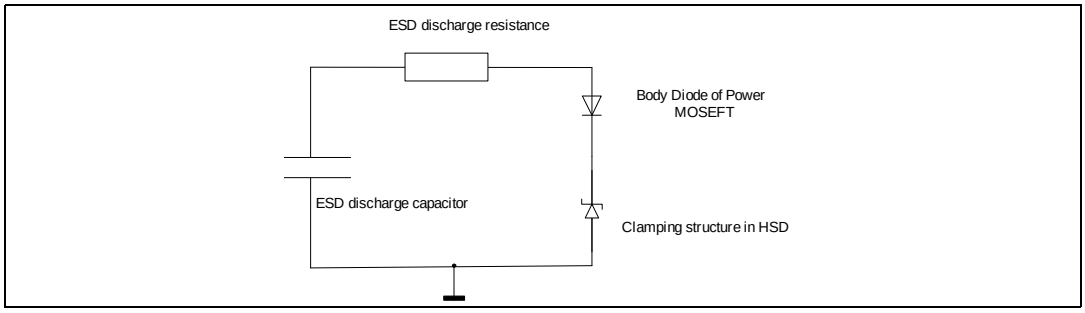
Contact discharge 6 kV, 150 pF, 330 Ω, battery not supplied (Vcc=0 V)

→according to *Equation 30*: C_{EXT} > 9 nF

→according to *Equation 32*: C_{EXT} > 4.4 nF

→C_{EXT} > 9 nF fulfils both requirements.

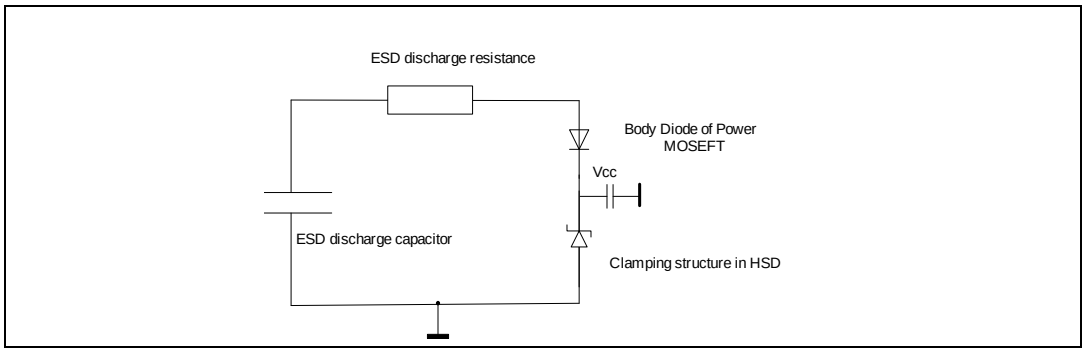
Positive ESD pulses without external protection



A positive ESD pulse on the output is transferred through the body diode of the power MOSFET to the Vcc pin of the HSD, stressing the Vcc-GND clamping structure. The ESD ratings of the Vcc-GND clamping structure is the same for the output clamping structure.

Therefore the same considerations and calculations apply for negative ESD pulses on the output.

Positive ESD pulses with external protection

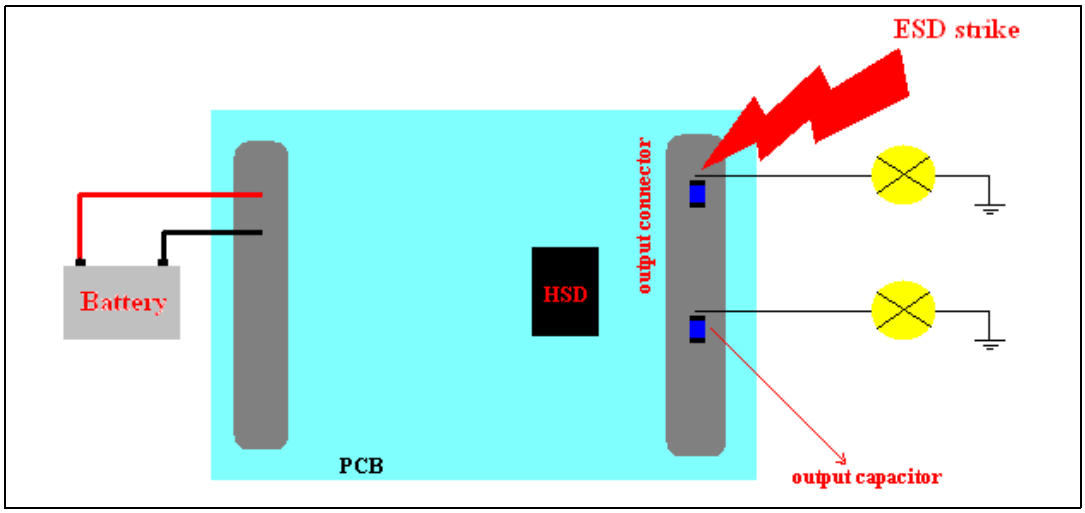


A positive ESD pulse on the output is transferred through the body diode of the power MOSFET to the Vcc pin of the HSD,so the same requirements to dimension the external capacitor apply as the negative ESD pulses on the output.

7.2 ESD protection – ECU level (layout consideration)

An ESD pulse on a powered ECU output connector is an expected event during the life of a car.

Typically, contact and air discharge tests are performed during module qualification. (Ref. IEC61000-4-2). The possible risk at application level is an early failure of the HSD with a following resistive short circuit between Vcc and OUT. The ESD pulse destruction value strongly depends on the module layout. To make the module pass the required stress level, add a 100 V ceramic capacitor with a value in the order of tens of nF to the output close to the connector. This capacitor decreases both the applied dv/dt and the maximum output voltage seen by the HSD.



8 Robust design

8.1 Design suggestions for HSDs and relays on the same PCB

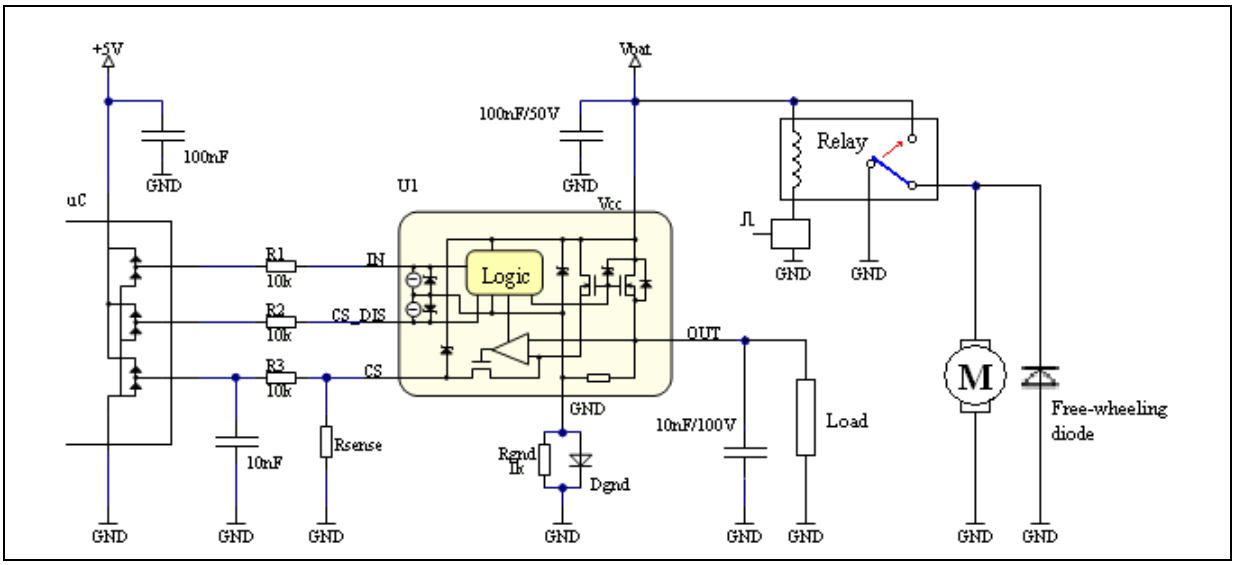
A typical ECU today still employs, along with the smart power HSDs and LSDs, a certain number of electromechanical relays. The activation of these relays, being on the same PCB and supplied by the same battery line as the HSDs, may lead to fast dv/dt on the battery line due to bouncing of the contacts when inductive loads are driven. Even a standard high frequency capacitor (typ. value 100 nF) across the local battery and ground is not enough to smoothen these pulses. The possible risk at application level is an early failure of the HSD with a following resistive short between Vcc and OUT. In order to avoid this, add a free-wheeling diode across the inductive load terminals (see below diagram) in order to minimize the effects of the relay bouncing.

Some suggestions above those already mentioned to help render the HSDs less sensitive when used with relays on the same board are:

a) the usage of four-layer PCBs where the inner layers are used as low resistance shields (one should be connected to module GND, the other to the battery connector);

b) the CS pin circuitry as recommended in the datasheet;

c) the use of separate connectors to supply the HSDs.



9 Revision history

Table 16. Document revision history

Date	Revision	Changes
01-Aug-2012	1	Initial release.
18-Sep-2013	2	Updated disclaimer

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