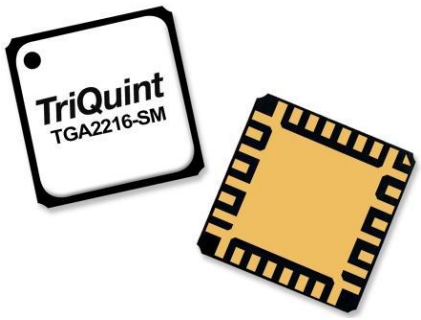
TGA2216-SM

0.1 – 3.0GHz 10W GaN Power Amplifier

Applications

- Commercial and military radar
- Communications
- Electronic Warfare

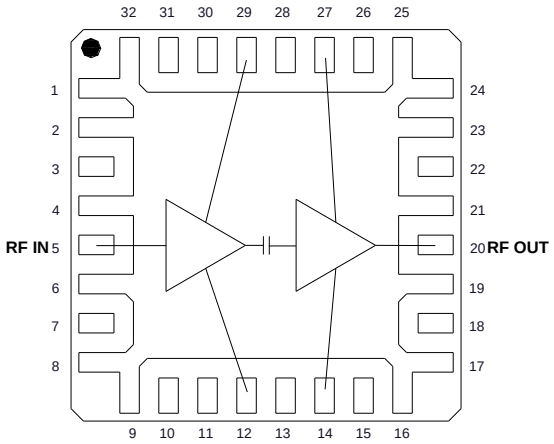


QFN 5x5 mm 32L

Product Features

- Frequency Range: 0.1 – 3.0GHz
- P_{SAT}: >40dBm at P_{IN} = 27dBm
- P1dB: >35dBm
- PAE: 50% @ midband
- Large Signal Gain: >13dB
- Small Signal Gain: 21dB
- Bias: V_D = 40V, I_{DQ} = 360mA, V_{G1} = -2.4V Typical, V_{G2} = +17.7V Typical
- Wideband Flat Gain and Power
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Functional Block Diagram



General Description

TriQuint's TGA2216-SM is a wideband cascode amplifier fabricated on TriQuint's production 0.25um GaN on SiC process. The cascode configuration offers exceptional wideband performance as well as supporting 40V operation. The TGA2216-SM operates from 0.1 - 3.0GHz and provides greater than 10W of saturated output power with greater than 13dB of large signal gain and greater than 40% power-added efficiency.

The TGA2216-SM is available in a low-cost, surface mount 32 lead 5x5 AIN QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2216-SM is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1-2, 4, 6, 8-9, 16-17, 19, 21, 23-25, 32	GND
3, 7, 10-11, 13, 15, 18, 22, 26, 28, 30-31	NC
5	RF IN
12, 29	GATE1
14, 27	GATE 2
20	RF OUT, DRAIN

Ordering Information

Part	ECCN	Description
TGA2216-SM	EAR99	0.1 – 3.0GHz 10W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	80V
Gate Voltage Range (V_{G1})	-8 to 0V
Gate Voltage Range (V_{G2})	0 to 40V
Drain Current (I_D)	760mA
Gate Current (I_{G1})	-5 to 5.6mA
Gate Current (I_{G2})	-5 to 5.6mA
Power Dissipation (P_{DISS}), 85°C	28W
Input Power (P_{IN}), CW, 50 Ω, 85°C,	33dBm
Input Power (P_{IN}), CW, VSWR 10:1, V_D = 40V, 85°C	27dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	320°C
Storage Temperature	-55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	40V
Drain Current (I_{DQ})	360mA
Gate Voltage (V_{G1})	-2.4V (Typ.)
Gate Voltage (V_{G2})	+17.7V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25^{0}C, V_D = 40V, I_{DQ} = 360mA, V_{G1} = -2.4V Typical, V_{G2} = +17.7V Typical

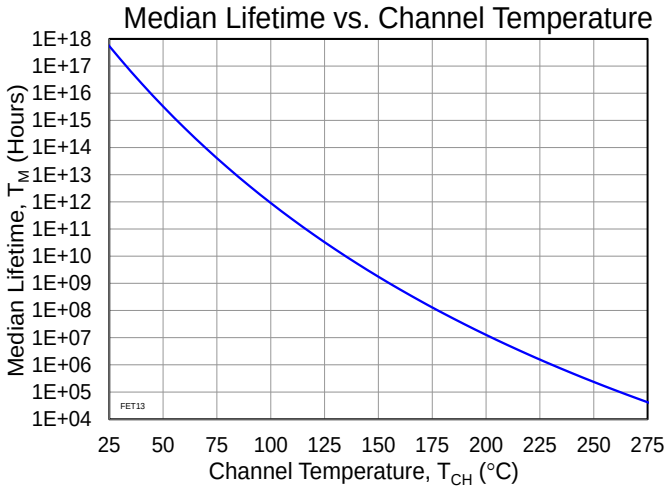
Parameter	Min	Typical	Max	Units
Operational Frequency Range	0.1		3.0	GHz
Small Signal Gain		21		dB
Input Return Loss		> 8		dB
Output Return Loss		> 11		dB
Output Power (Pin = 27dBm)		> 40		dBm
Power Added Efficiency (Pin = 27dBm)		50 (mid band)		%
Power @ 1dB Compression (P1dB)		> 35		dBm
IM3 @ 120mA, POUT/tone = 30dBm		-25		dBc
IM5 @ 120mA, POUT/tone = 30dBm		-33		dBc
Small Signal Gain Temperature Coefficient		-0.03		dB/°C
Output Power Temperature Coefficient		-0.007		dBm/°C
Recommended Operating Voltage:		40	48	V

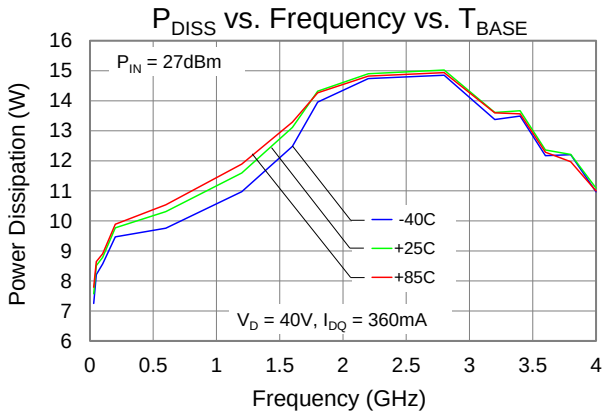
Thermal and Reliability Information

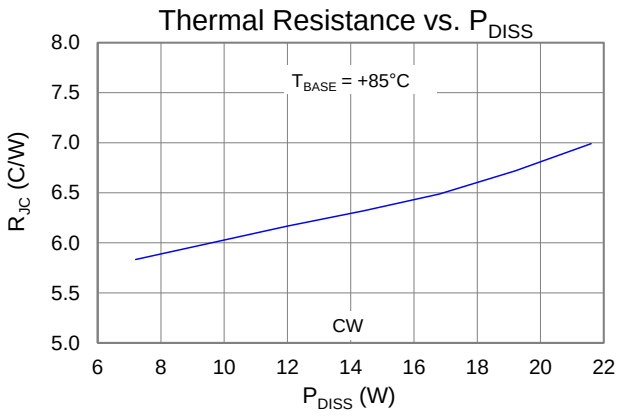
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, **V_D(2) = 40V (CW)**	6.32	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	I_{DQ} = 360mA, $I_{D\ Drive}$ = 610mA	179	°C
Median Lifetime (T_M)	P_{IN} = 27dBm, P_{OUT} = 40dBm, P_{DISS} = 15W	7.99 x 10^7	Hrs

Notes:
1. Thermal resistance measured to back of package.
2. The drain voltage for Cascode amplifier transistor is ½ of the V_D.

Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in I_{D_MAX}



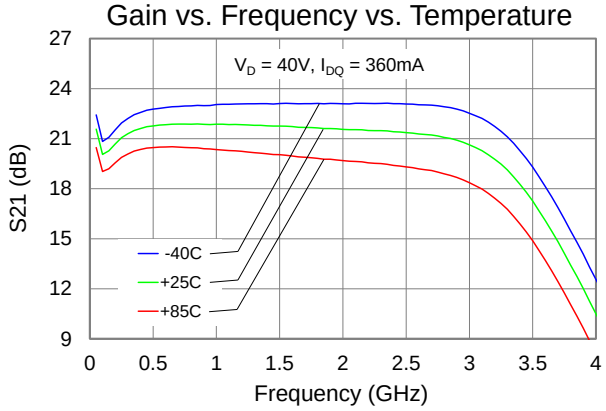




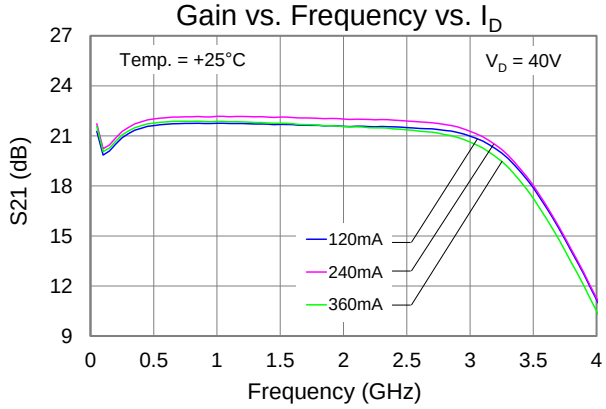
Typical Performance: Small Signal

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

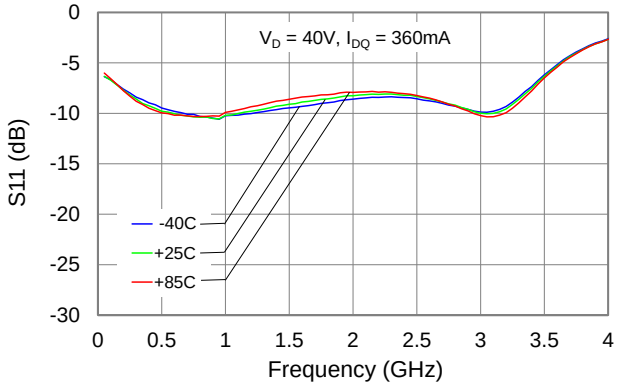
Gain vs. Frequency vs. Temperature



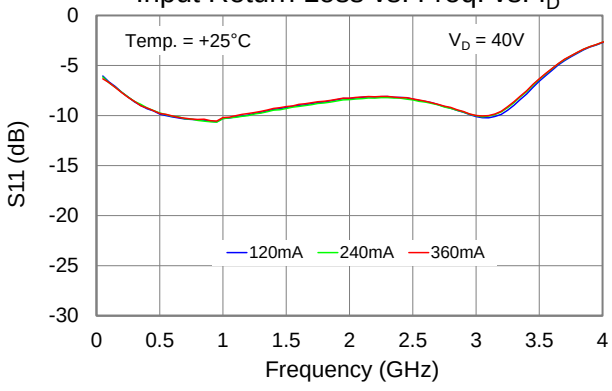
Gain vs. Frequency vs. I_D



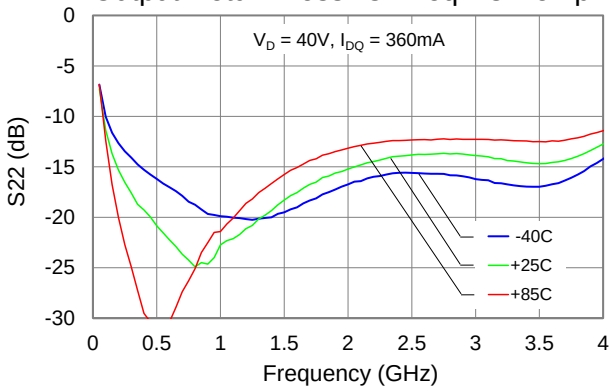
Input Return Loss vs. Freq. vs. Temp.



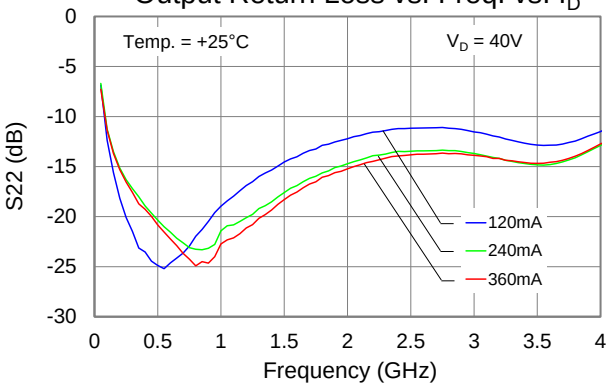
Input Return Loss vs. Freq. vs. I_D



Output Return Loss vs. Freq. vs. Temp.



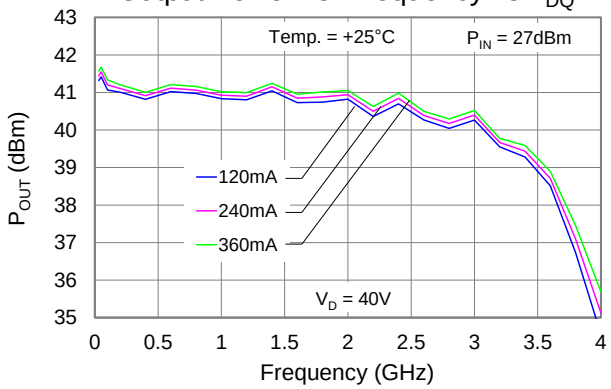
Output Return Loss vs. Freq. vs. I_D



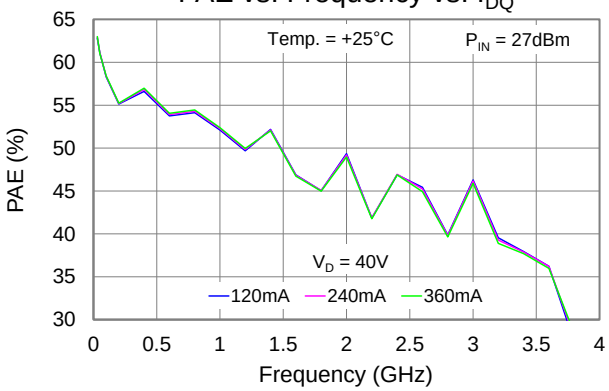
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

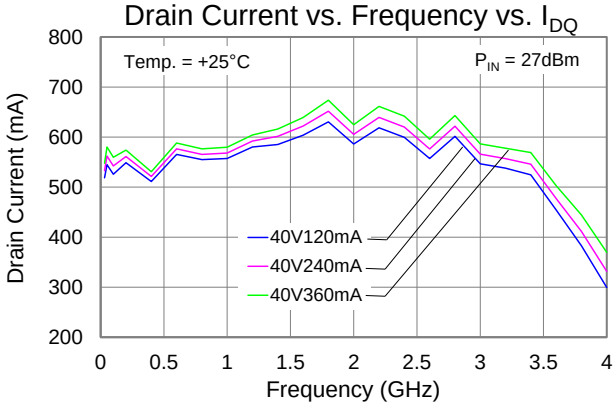
Output Power vs. Frequency vs. I_{DQ}



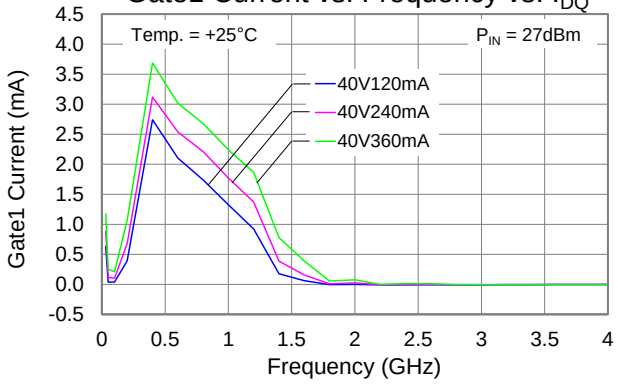
PAE vs. Frequency vs. I_{DQ}



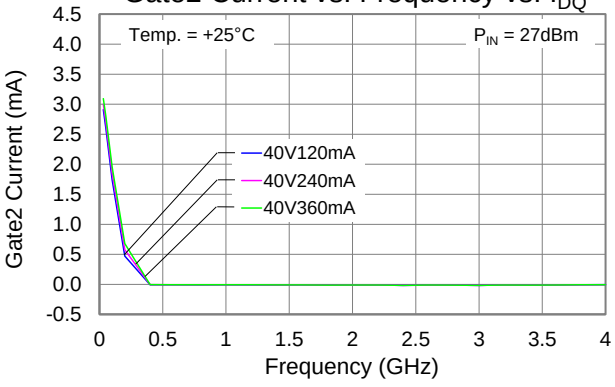
Drain Current vs. Frequency vs. I_{DQ}



Gate1 Current vs. Frequency vs. I_{DQ}



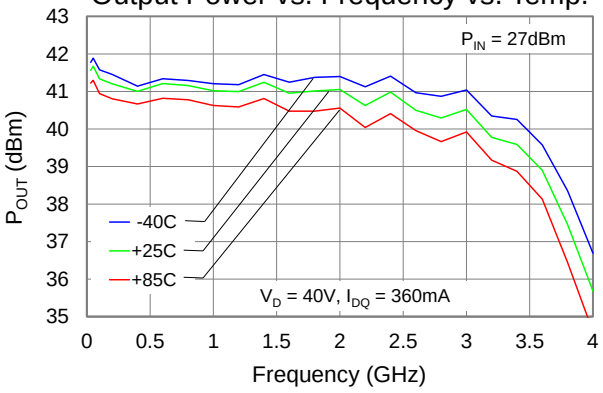
Gate2 Current vs. Frequency vs. I_{DQ}



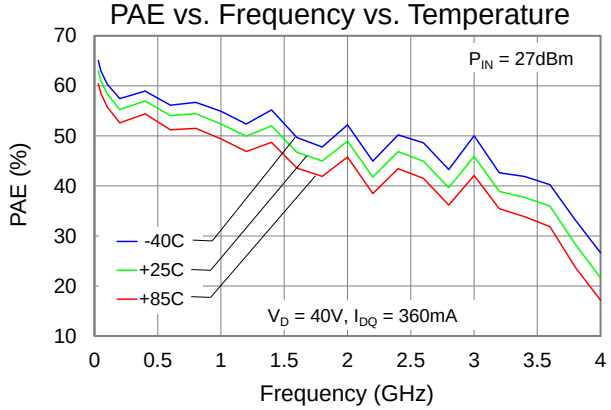
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

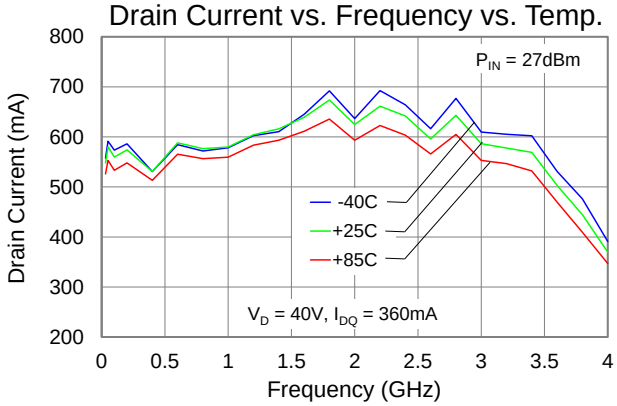
Output Power vs. Frequency vs. Temp.



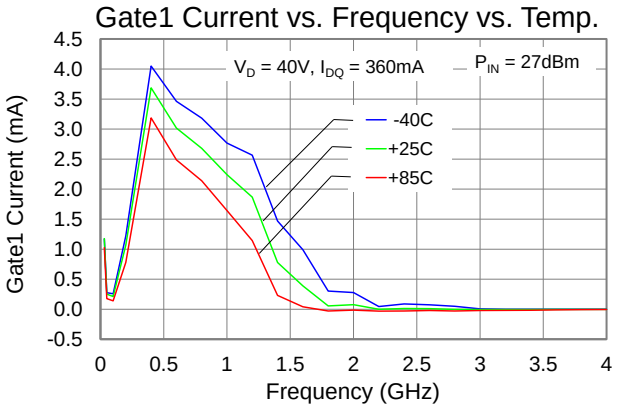
PAE vs. Frequency vs. Temperature



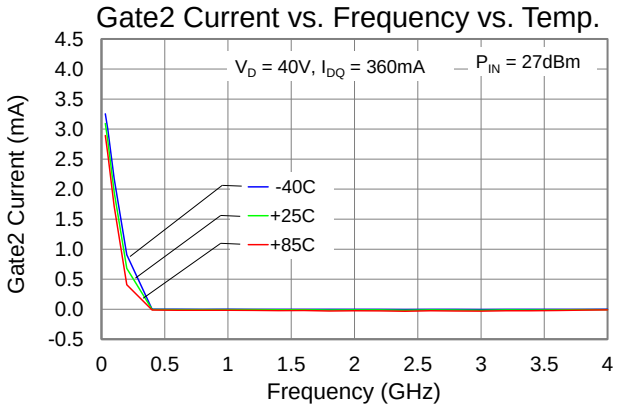
Drain Current vs. Frequency vs. Temp.



Gate1 Current vs. Frequency vs. Temp.



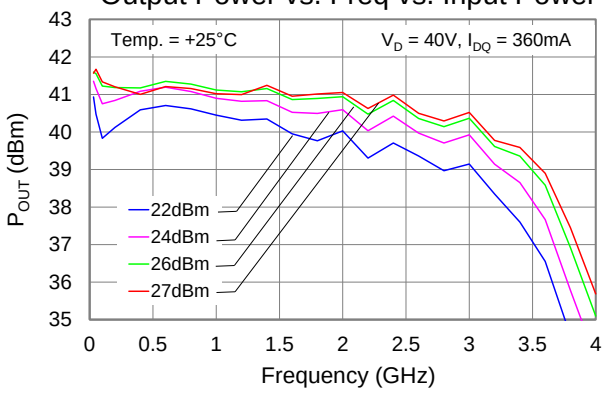
Gate2 Current vs. Frequency vs. Temp.



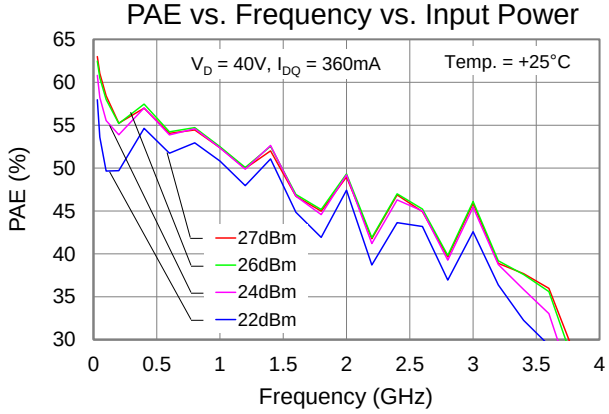
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

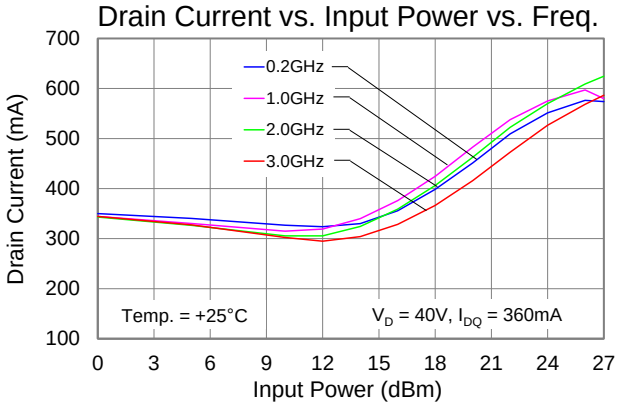
Output Power vs. Freq vs. Input Power



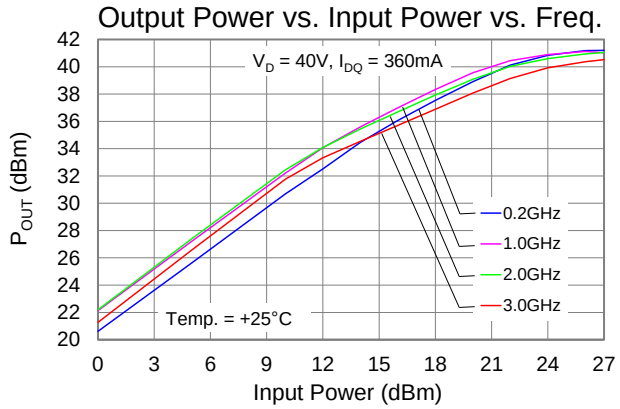
PAE vs. Frequency vs. Input Power



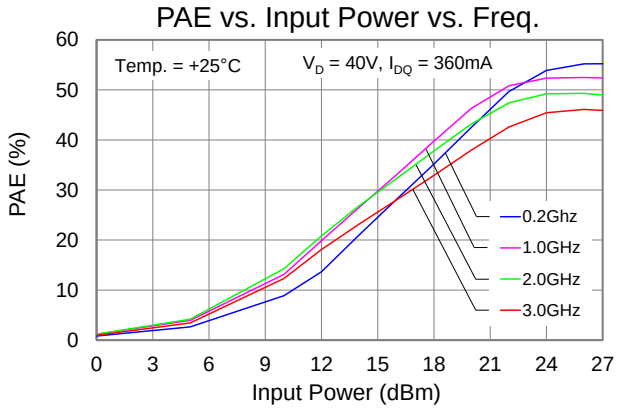
Drain Current vs. Input Power vs. Freq.



Output Power vs. Input Power vs. Freq.



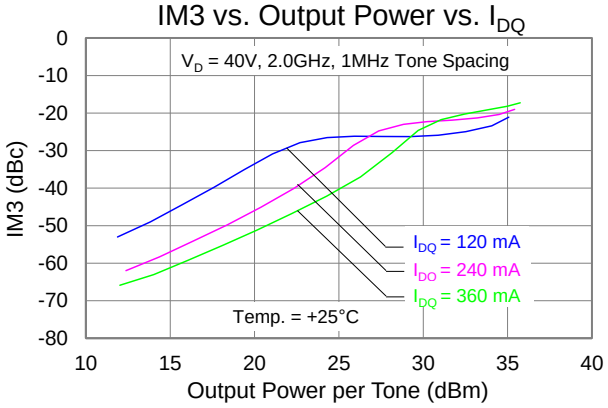
PAE vs. Input Power vs. Freq.



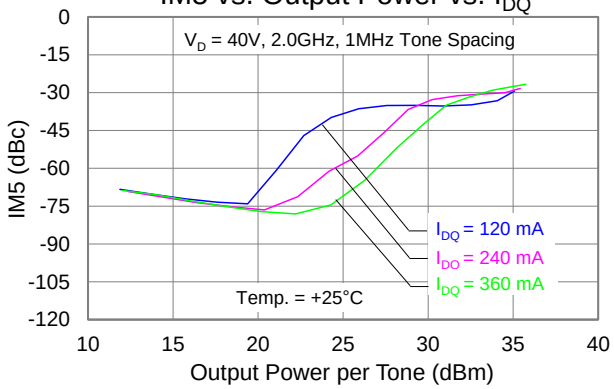
Typical Performance: Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

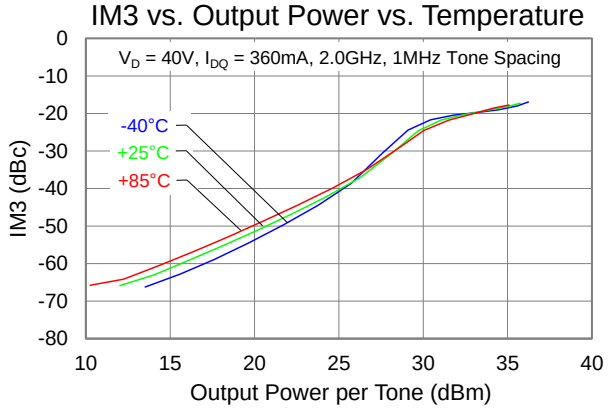
IM3 vs. Output Power vs. I_{DQ}



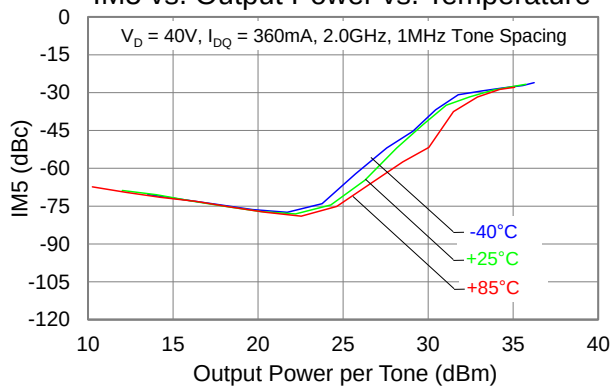
IM5 vs. Output Power vs. I_{DQ}



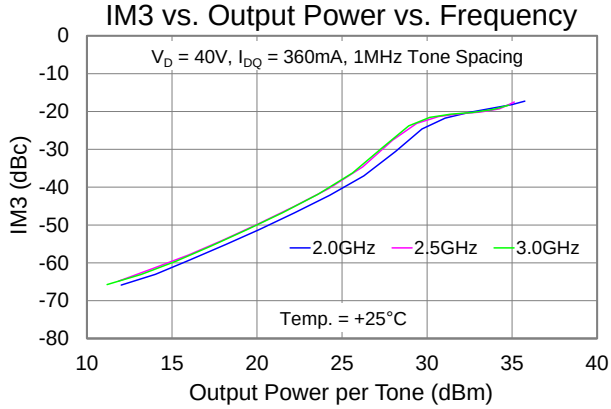
IM3 vs. Output Power vs. Temperature



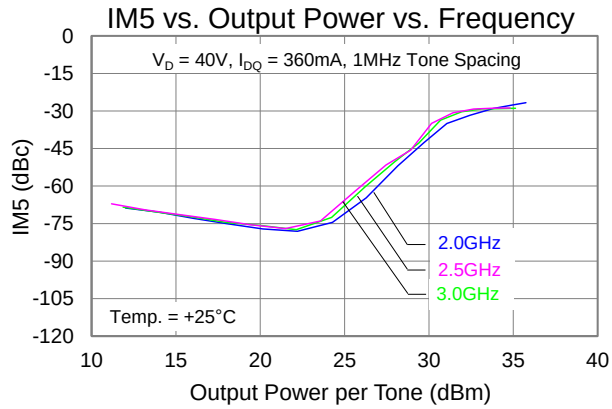
IM5 vs. Output Power vs. Temperature



IM3 vs. Output Power vs. Frequency



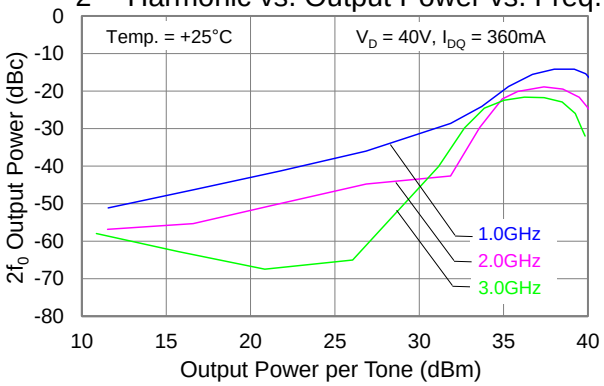
IM5 vs. Output Power vs. Frequency



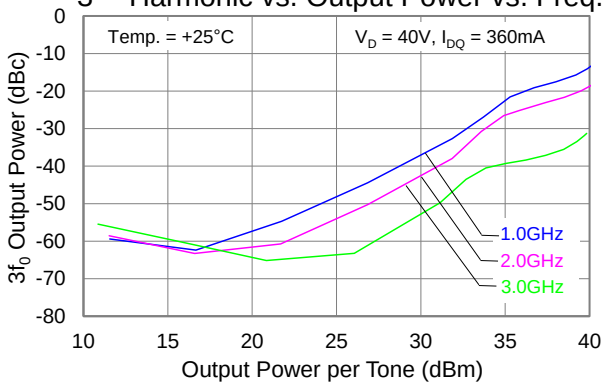
Typical Performance: Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

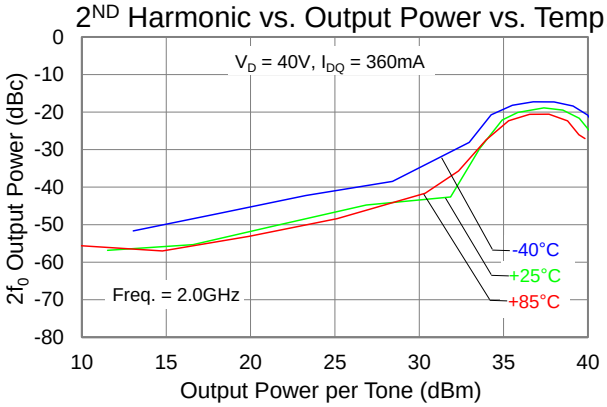
2ND Harmonic vs. Output Power vs. Freq.



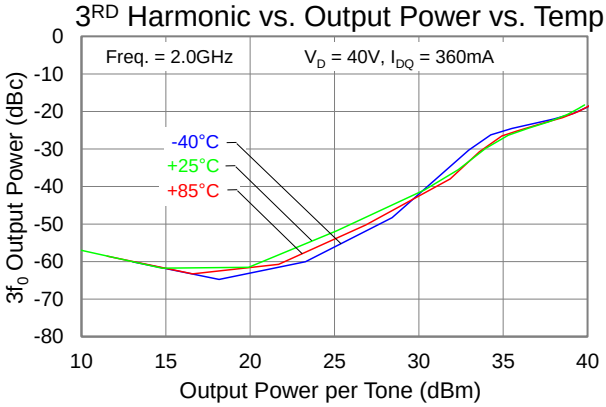
3RD Harmonic vs. Output Power vs. Freq.



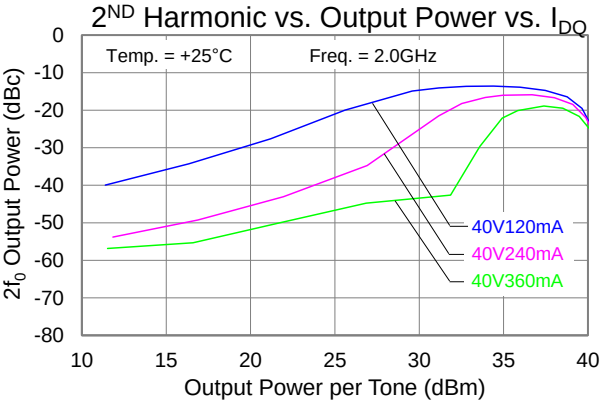
2ND Harmonic vs. Output Power vs. Temp.



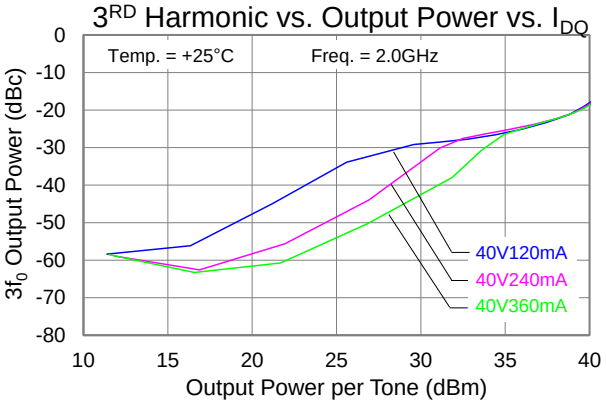
3RD Harmonic vs. Output Power vs. Temp.



2ND Harmonic vs. Output Power vs. I_{DQ}



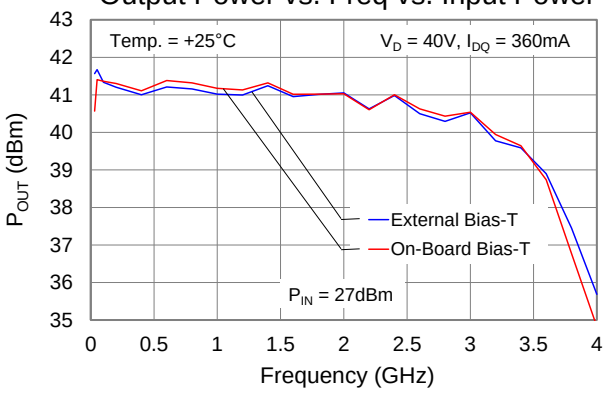
3RD Harmonic vs. Output Power vs. I_{DQ}



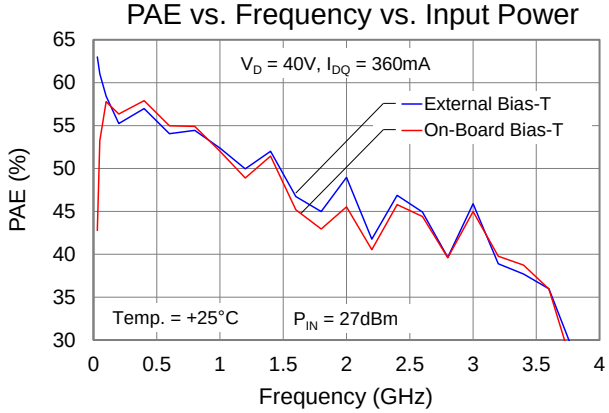
Typical Performance: Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 11 and 13)

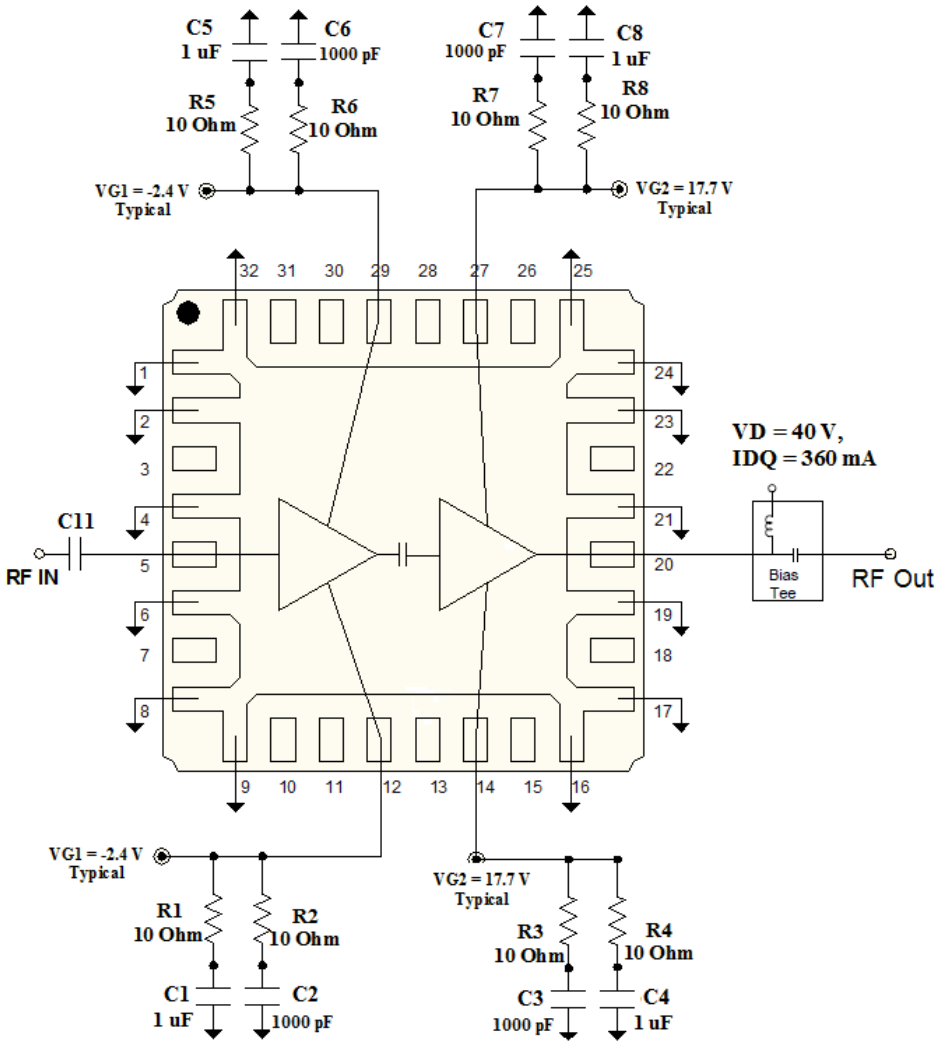
Output Power vs. Freq vs. Input Power



PAE vs. Frequency vs. Input Power



Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)
2. Coaxial input DC block (C11) is used for input port (RF In.)
3. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee.

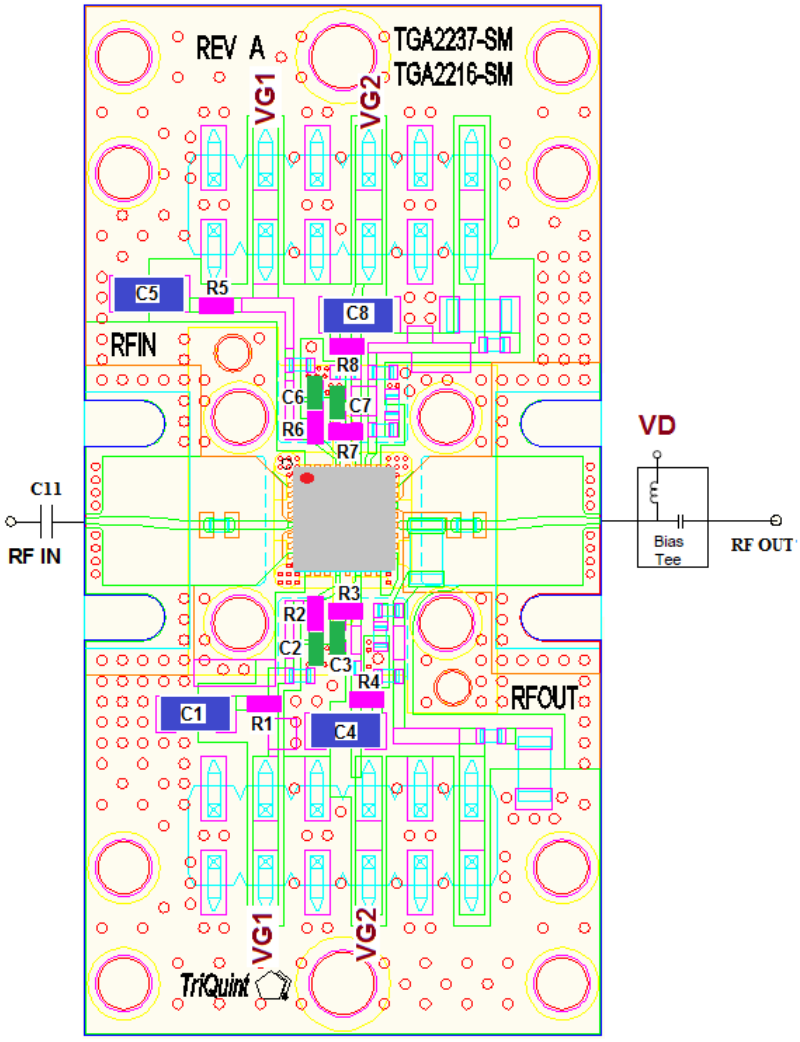
Bias-up Procedure

1. Set I_D limit to 720mA, I_{G1} & I_{G2} limit to 5mA
2. Set V_{G1} to -5.0V
3. Set V_{G2} to (V_D/2) - 2.7V or 40V/2 - 2.7V = 17.3V
4. Set V_D +40V
5. Adjust V_{G1} more positive until I_{DQ} = 360mA (V_{G1} ~ -2.4V Typical)
6. Adjust V_{G2} to (V_D/2) + V_{G1}; (V_{G2} ~ +17.7V Typical)
7. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_{G1} to -5.0V. Ensure I_{DQ} ~ 0mA
3. Reduce V_{G2} to 0V.
4. Set V_D to 0V
5. Turn off V_D supply
6. Turn off V_{G2} supply
7. Turn off V_{G1} supply

Assembly Drawing (Coaxial input DC block and coaxial output bias tee)

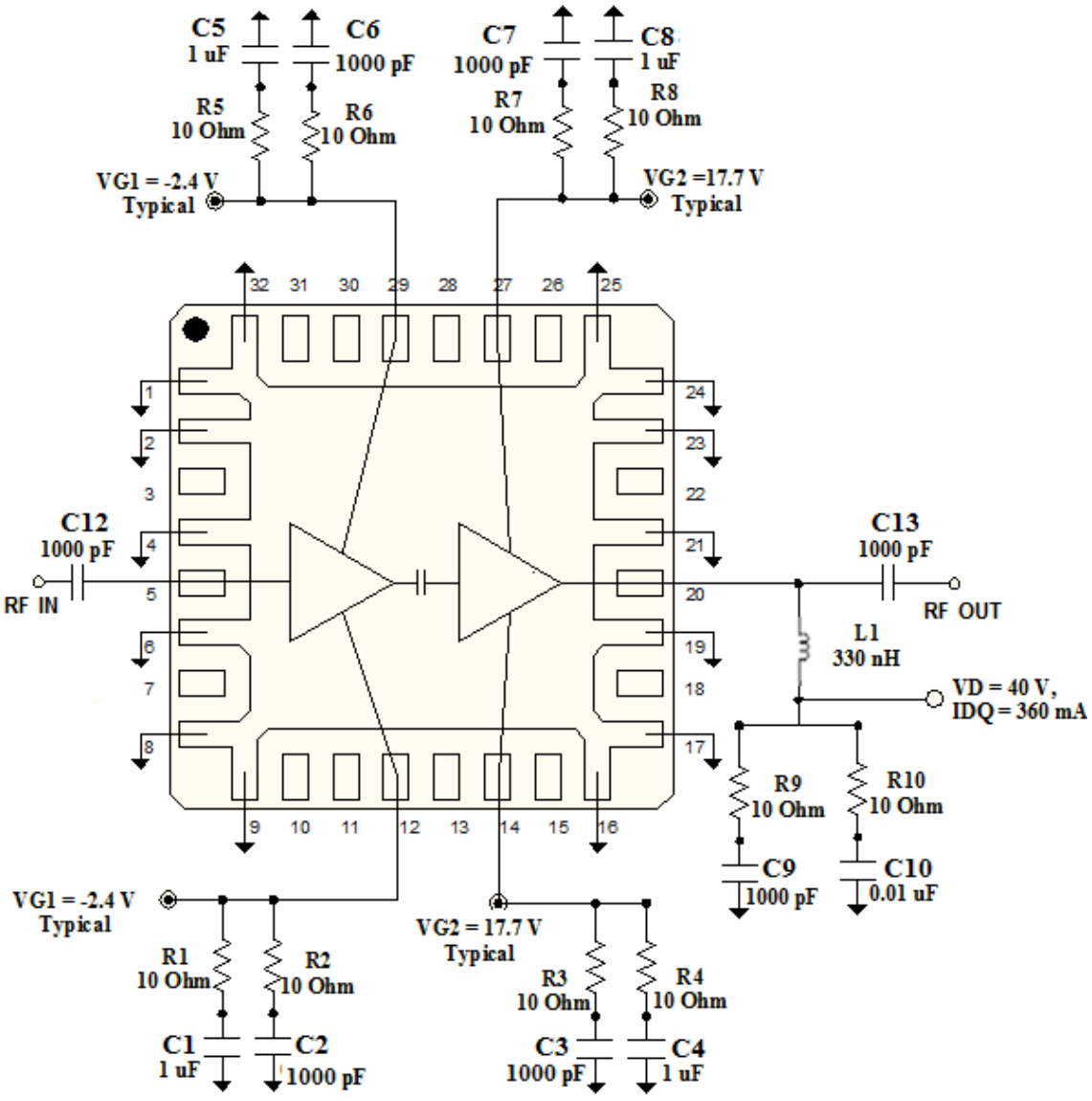


Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1, C4, C5, C8	1uF	Cap, 1206, 50V, 10%, X7R	Various	
C2, C3, C6, C7	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C11		DC Block	Various	
R1 – R8	10Ω	Res, 0402	Various	

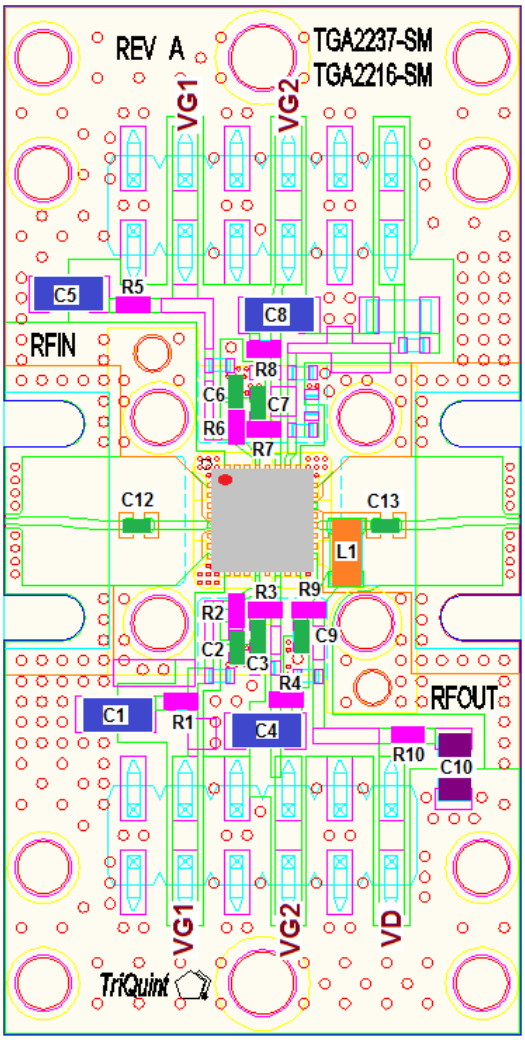
Notes:

Application Circuit (Option with board-level DC blocks and output bias tee)



1. Performance of the DUT with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.
2. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)

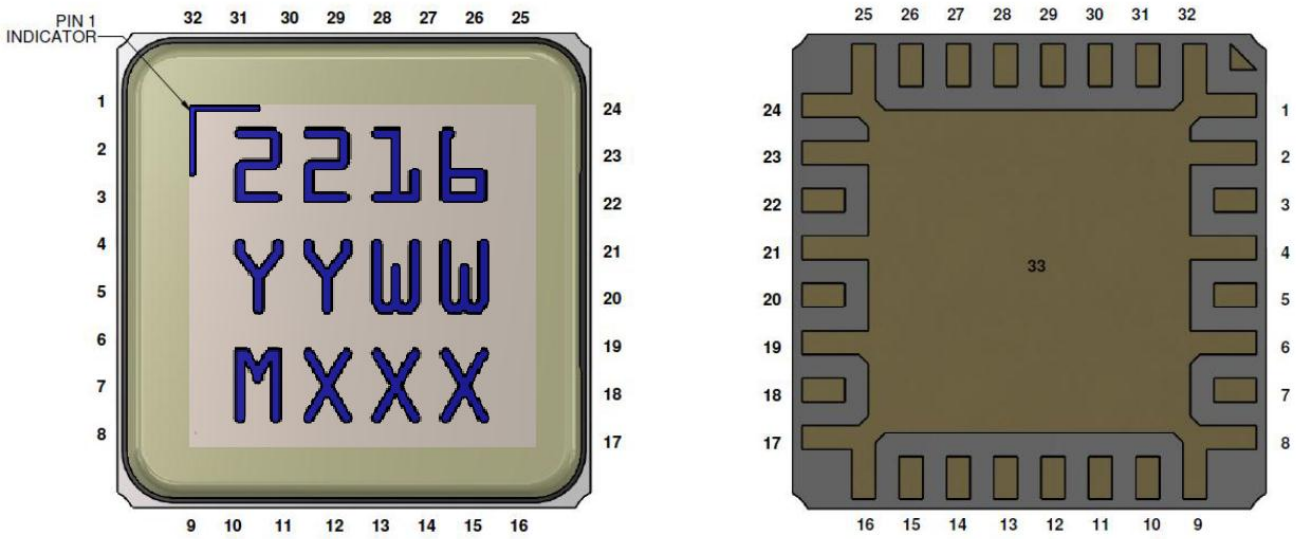
Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option



Bill of Materials For On-Board Bias-Tee

Reference Design	Value	Description	Manufacturer	Part Number
C1, C4, C5, C8	1uF	Cap, 1206, 50V, 10%, X7R		
C2-C3, C6-C7, C9, C12, C13	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C10	0.01uF	Cap, 1206, 100V, 10%, X7R	Various	
L1	330nH	Ind, 1206, 100V, 10%, X7R	Various	
R1 – R10	10Ω	Res, 0402	Various	

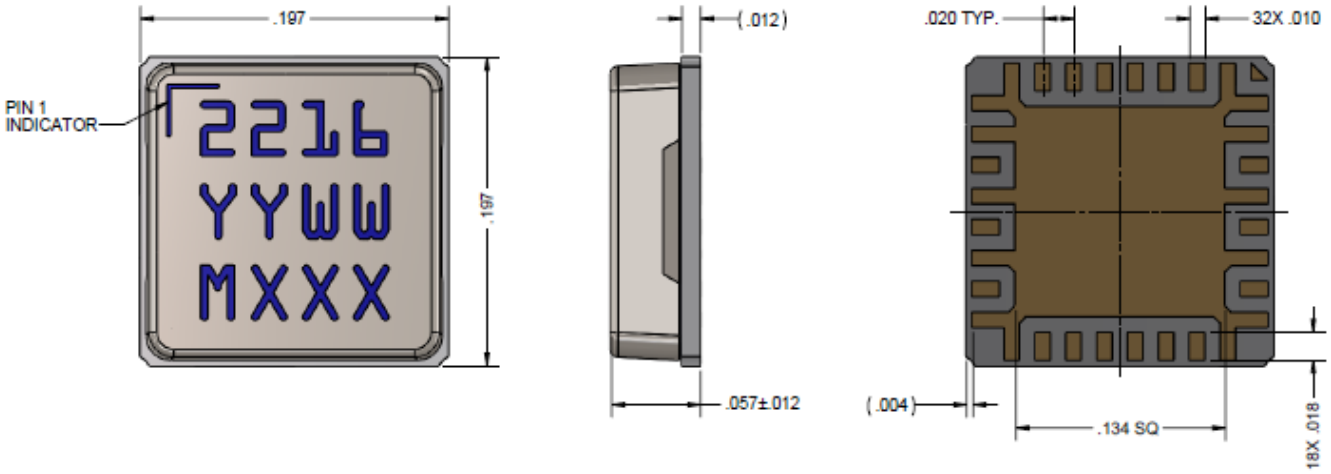
Pin Layout



Pin Description

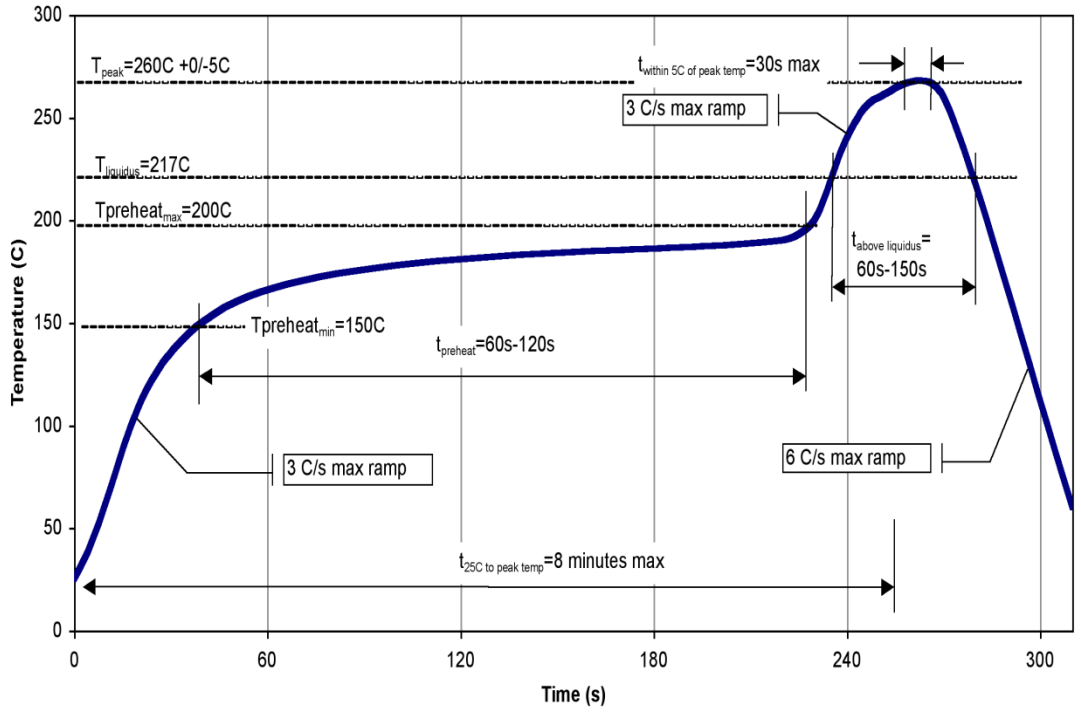
Pin No.	Symbol	Description
1-2, 4, 6, 8-9, 16-17, 19, 21, 23-25, 32	GND	Connected to ground paddle (pin 33); must be grounded on PCB.
3, 7, 10-11, 13, 15, 18, 22, 26, 28, 30-31	NC	No connection.
5	RF IN	Input; matched to 50 Ω.
12, 29	GATE1	GATE voltage1; bias network is required; see recommended Application Information on page 11.
14, 27	GATE2	Gate voltage2; bias network is required; see recommended Application Information on page 11.
20	RF OUT/ DRAIN	Output; matched to 50 Ω.
33	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Mechanical Information



Units: inches
Tolerances: unless specified
x.xx = ± 0.01
x.xxx = ± 0.005
Materials:
Base: Ceramic
Lid: Plastic
All metalized features are gold plated
Part is epoxy sealed
Marking:
2216: Part number
YY: Part Assembly year
WW: Part Assembly week
MXXX: Batch ID

Recommended Soldering Temperature Profile



Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

Solderability

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

ECCN

US Department of Commerce: EAR99

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.972.994.8465
Email: info-sales@triquint.com **Fax:** +1.972.994.8504

For technical questions and application information: **Email:** info-products@triquint.com

Important Notice

The information contained herein is believed to be reliable. TriQuint makes no warranties regarding the information contained herein. TriQuint assumes no responsibility or liability whatsoever for any of the information contained herein. TriQuint assumes no responsibility or liability whatsoever for the use of the information contained herein. The information contained herein is provided "AS IS, WHERE IS" and with all faults, and the entire risk associated with such information is entirely with the user. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for TriQuint products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information.

TriQuint products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.