

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TO-252 saves board space
- Fast switching speed
- High performance trench technology

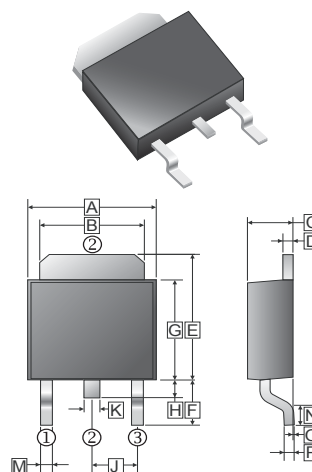
APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

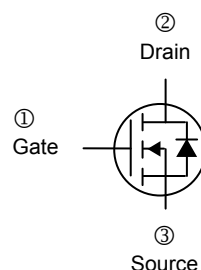
PACKAGE INFORMATION

Package	MPQ	LeaderSize
TO-252	2.5K	13' inch

TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30	REF.
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	20	A
$T_C = 25^\circ\text{C}$			
Pulsed Drain Current ²	I_{DM}	36	A
Continuous Source Current (Diode Conduction) ¹	I_S	30	A
Power Dissipation ¹	P_D	50	W
$T_C = 25^\circ\text{C}$			
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	$^\circ\text{C}$
Thermal Resistance Ratings			
Maximum Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	50	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3.0	$^\circ\text{C} / \text{W}$

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0	-	-	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS}=0$, $V_{GS}=20\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS}=80\text{V}$, $V_{GS}=0$
		-	-	25		$V_{DS}=80\text{V}$, $V_{GS}=0$, $T_J=55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(ON)}$	34	-	-	A	$V_{DS}=5\text{V}$, $V_{GS}=10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	50	m Ω	$V_{GS}=10\text{V}$, $I_D=9.2\text{A}$
		-	-	59		$V_{GS}=4.5\text{V}$, $I_D=6.1\text{A}$
Forward Transconductance ¹	g_{fs}	-	4.4	-	S	$V_{DS}=40\text{V}$, $I_D=5.5\text{A}$
Diode Forward Voltage	V_{SD}	-	1.1	-	V	$I_S=9\text{A}$, $V_{GS}=0$
Dynamic ²						
Total Gate Charge	Q_g	-	25	-	nC	$I_D=9\text{A}$ $V_{DS}=25\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	Q_{gs}	-	5	-		
Gate-Drain Change	Q_{gd}	-	19	-		
Turn-on Delay Time	$T_{d(on)}$	-	9	-	nS	$V_{DD}=100\text{V}$ $I_D=9\text{A}$ $R_L=25\Omega$ $V_{GEN}=10\text{V}$
Rise Time	T_r	-	15	-		
Turn-off Delay Time	$T_{d(off)}$	-	45	-		
Fall Time	T_f	-	39	-		

Notes:

1. Pulse test : $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.