27C203
FAST PIPELINED 256K (16K x 16) EPROM

- **Pipelined Interface**
  - **Clock for Data Latching**
  - **Optional Synchronous Chip Select**
- **Quick-Pulse Programming™**
  - **4 Second Throughput for Automated Manufacturing**
- **Very High Speed**
  - **Supports up to 20MHz Pipelined 80386/376's at Zero Wait-States**
- **Excellent Drive Capability**
  - **4 mA Source/16 mA Sink Current Handles Large Fanout**
- **System Initialize Feature**
  - **Initialization Register Forces Startup Vector for State Machine Applications**
- **High-Performance/Low Power CMOS**
  - **High Density Memory With 100 mA I_{CC} Maximum**
- **Versatile Package Options**
  - **Standard DIP**
  - **Compact Surface-Mount Cerquad**
  - **Compact Surface-Mount PLCC****

The Intel 27C203 is a high performance 262,144-bit erasable programmable read-only memory organized as 16K words of 16 bits each. Its density and word-wide configuration, combined with its pipelined bus interface, provides a high integration firmware solution for today's speed-critical applications.

The 27C203 supports the pipelined bus architectures of the Intel 80376 and 80386 microprocessors. Pipelining relaxes memory interface requirements by utilizing an overlapping "early address," effectively stretching the read operation an additional bus cycle. Thus, much higher bus bandwidths are achievable than with a standard interface. An 80386/376 design employing the 27C203 can accommodate system clock rates up to 20 MHz at zero wait-states, while utilizing slower, less expensive interface logic in 16 MHz versions. The 256K bit capacity is well suited for high-end embedded control applications. The 27C203's simple interface and X16 organization help minimize overall chip count.

State machine designers can also use the 27C203 as a synchronous logic element, especially where the designer needs a pipelined "data-flow-through" transfer function. For example, it can be applied to weighting or summing functions in high frequency filters using digital signal processing techniques. To simplify system design and debugging, the 27C203 contains a hardware-controlled initial condition vector through the INIT function pin.

The 27C203 is available in three package versions. The standard 40-pin Dual-In-Line Package (DIP) provides for conventional device handling and socketing. The 44-lead OTP™ (One-Time-Programmable) Plastic Leaded Chip Carrier (PLCC) allows lowest cost, automated, surface-mount manufacturing. The 44-lead Cerquad Package allows reprogramming within the same compact dimensions as the PLCC package.

The 27C203 is manufactured on Intel's advanced CHMOS* III-E, a process optimized for high performance.

The 27C203 will be replaced by the 27C203C mid 1990. The 27C203C will be functionally identical to the 27C203 in the read mode. The 27C203C's memory array will use a I-transistor cell, versus the 27C203's 2-transistor cell, and will program with a standard one-pass algorithm.

*CHMOS is a patented process of Intel Corporation.

**PLCC package availability TBD

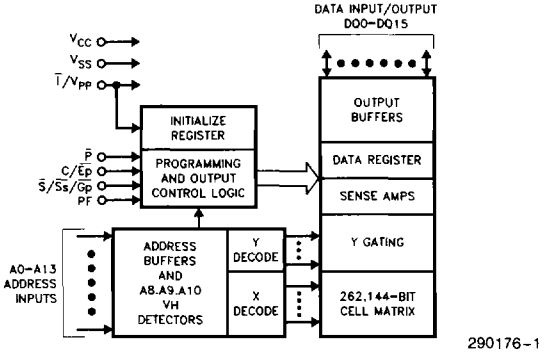


Figure 1. 27C203 Block Diagram

October 1989
Order Number: 290176-002

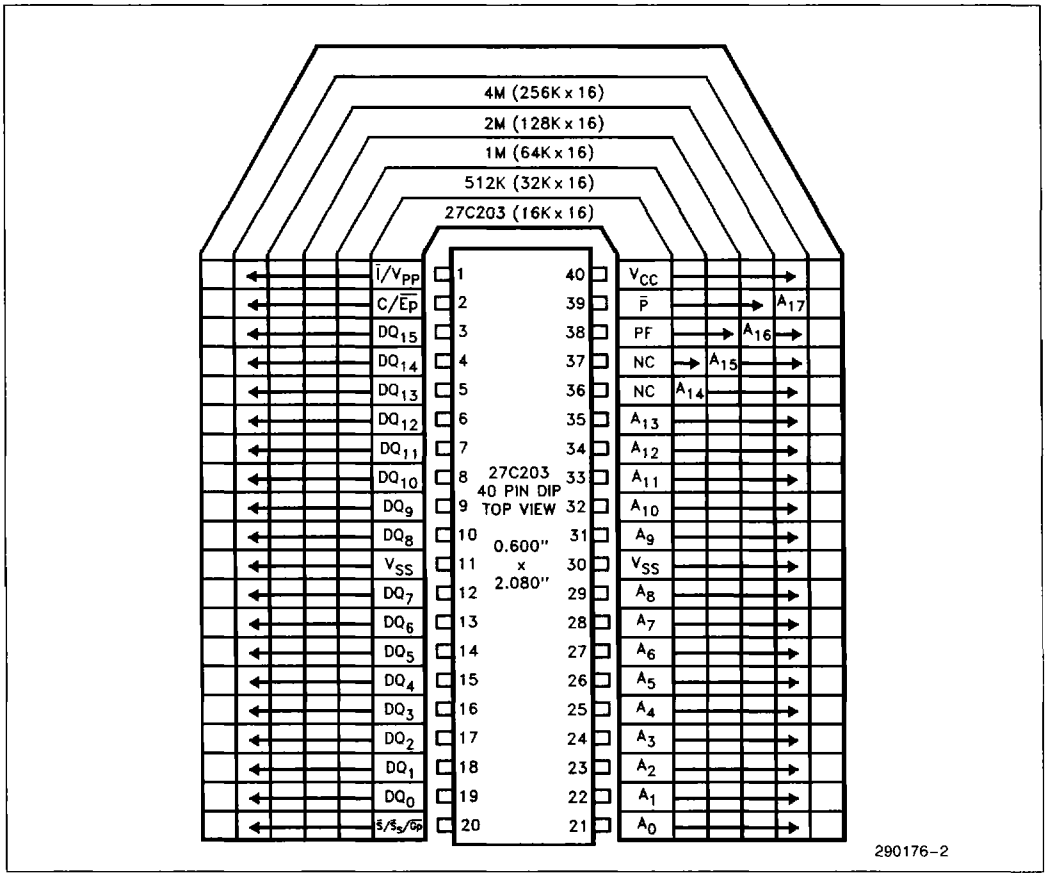


Figure 2a. DIP Pin Configuration

27C203 Pin Names

A0–A13	Address
DQ0–DQ15	Data Inputs/Outputs
C/$\overline{Ep}$	Clock/Program Chip Enable
$\overline{S}$/$\overline{Ss}$/$\overline{Gp}$	Chip Select/Program Output Enable
$\overline{P}$	Programming Enable
PF	Program Function
$\overline{I}/V_{PP}$	Initialize Register Enable/V_{PP}
NC	No Connect

NOTE:
1. Each 27C203 V_{CC} and V_{SS} pin specified must be tied individually to their respective power supplies. See System Design Considerations.

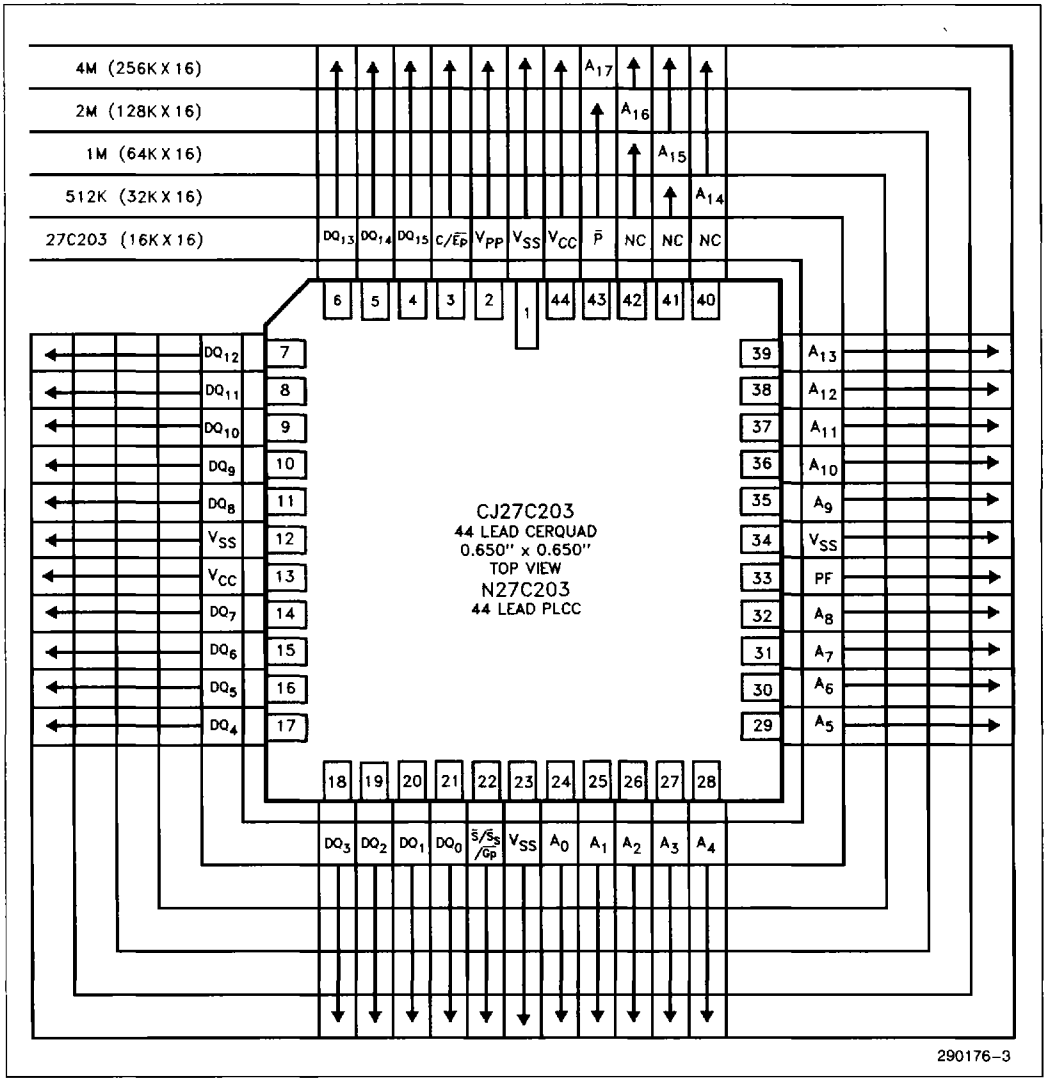


Figure 2b. Cerquad/PLCC Lead Configuration

ABSOLUTE MAXIMUM RATINGS*

Operating temperature during read . . . 0°C to +70°C

Temperature under bias . . . . . −55°C to +125°C

Storage temperature . . . . . −65°C to +125°C

All input or output voltages with respect to ground . . . . . −2V to +7V(1)

Voltage on A9 with with respect to ground . . . . . −2V to +14V(1)

V_{PP} supply voltage with respect to ground during programming . . −2V to +14V(1)

V_{CC} supply voltage with respect to ground . . . . . −2V to +7V(1)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

EXTENDED TEMPERATURE (EXPRESS) EPROMS

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS EPROMs are available with 168 +/− 8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process meets or exceeds most industry burn-in specifications. The standard EXPRESS EPROM operating temperature range is 0°C to +70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are also available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

EXPRESS OPTIONS

Versions

Speed Versions	Packaging Options	
	DIP	Cerquad
−45V05	Q, T, L	Q, T, L
−45V10	Q, T, L	Q, T, L
−55V05	Q, T, L	Q, T, L
−55V10	Q, T, L	Q, T, L

EXPRESS EPROM PRODUCT FAMILY

Product Definitions

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ± 8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ± 8

NOTE:
1. Minimum D.C. input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} +2V for periods less than 20 ns.

D.C. CHARACTERISTICS

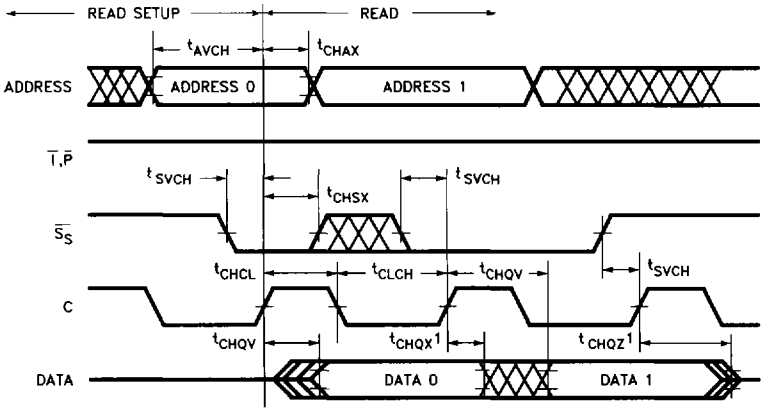
Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Units	
I_{LI}	Input Load Current			10	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.5V
I_{PP1}	V_{PP} Load Current Read			10	µA	V_{PP} = 5.5V
I_{CC}(1)	V_{CC} Current Active		60	100	mA	
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL} = 16 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −4mA

A.C. CHARACTERISTICS

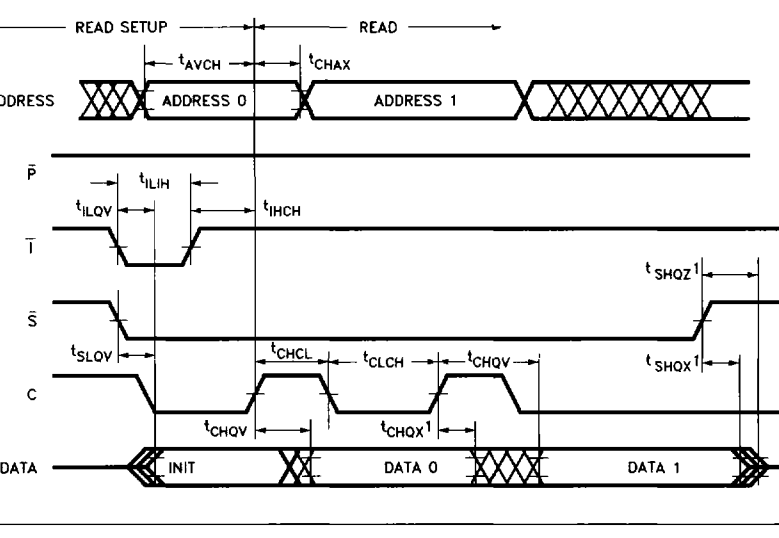
Versions (2)	V_{CC} ± 5% (5.0 ± 0.25V)	C27C203-45V05 CJ27C203-45V05		C27C203-55V05 CJ27C203-55V05		Units
	V_{CC} ± 10% (5.0 ± 0.50V)	C27C203-45V10 CJ27C203-45V10		C27C203-55V10 CJ27C203-55V10		
Symbol	**Characteristics**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{AVCH}	Address Valid to Clock	45		55		ns
t_{CHAX}	Address Hold from Clock	0		0		ns
t_{CHQV}(3)	Clock to Valid Output		40		50	ns
t_{CHQZ}(4)	Clock to Output Tri-state for Synchronous Chip Deselect, S_S		15		15	ns
t_{CHCL}, t_{CLCH}	Clock Pulse Width	25		25		ns
t_{SVCH}	Setup Time to Clock for Synchronous Chip Select, $\overline{S_S}$.	10		10		ns
t_{CHSX}	Hold Time for Sync. Select	10		10		ns
t_{CHQX}(4)	Data Hold Time From Clock	0		0		ns
t_{SHQX}(4)	Data Hold Time From Select	0		0		ns
t_{SLQV}(3)	Valid Output Delay from Asynchronous Chip Select, $\overline{S}$.		35		40	ns
t_{SHQZ}(4)	Output Tri-state from Asynchronous Chip Deselect, $\overline{S}$.		10		10	ns
t_{ILQV}(3)	Initialize Register Valid Output Delay		35		40	ns
t_{ILIH}	Initialize Pulse Width	20		25		ns
t_{IHCH}	Recovery Time from Initialize to Clock	5		5		ns

NOTES:
1. V_{CC} current assumes no output loading, i.e., I_{OH} = I_{OL} 0mA
2. Packaging options: C = Ceramic Side-Brazed, CJ = Cerquad.
3. A derating factor of 6 ns/100 pF should be used with output loading greater than 30 pF. This derating factor is only sampled and not 100% tested.
4. These parameters are only sampled and not 100% tested.

A.C. WAVEFORMS—PIPELINED BUS APPLICATION (80376/80386)



A.C. WAVEFORMS—STATE MACHINE APPLICATION (ASYNCHRONOUS CHIP SELECT)

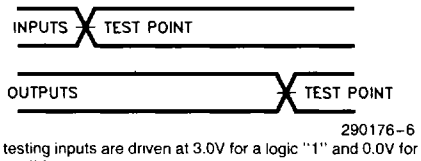


NOTE:
1. These parameters are only sampled and not 100% tested.

CAPACITANCE(1) T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	12	15	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	15	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Input Capacitance		75	pF	V_{PP} = 0V

A.C. TESTING INPUT/OUTPUT WAVEFORM



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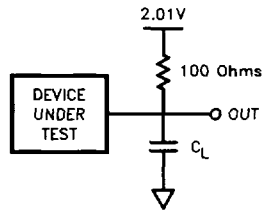
A.C. testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0." Timing measurements are made at 1.5V. Rise and fall times are 5 ns. or less.

A.C. TESTING LOAD CURRENT



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C_L = 30 pF
C_L includes Jig Capacitance

Table 1. Mode Table

Mode	Pins	$\overline{S}/\overline{S_s}/\overline{G_p}$	$C/\overline{E_p}$	pF	A10	A9	A8	A0	$\overline{P}$	$\overline{I}/V_{PP}$	V_{CC}	DQ
Read Setup	Asynchronous Chip Select	X	⌐	V_{IH}	A10	A9	A8	A0	V_{IH}	V_{IH}	V_{CC}	DQ Prior
	Synchronous Chip Select	V_{IL}	⌐	V_{IH}	A10	A9	A8	A0	V_{IH}	V_{IH}	V_{CC}	DQ Prior
Read	Asynchronous Chip Select	V_{IL}	X	X	X	X	X	X	V_{IH}	V_{IH}	V_{CC}	Q_{OUT}
	Synchronous Chip Select	X	⌐	X	X	X	X	X	V_{IH}	V_{IH}	V_{CC}	Q_{OUT}
Initialize Register Read	Asynchronous Chip Select	V_{IL}	X	X	X	X	X	X	V_{IH}	V_{IL}	V_{CC}	Q_{OUT}
	Synchronous Chip Select	V_{IL}	⌐	X	X	X	X	X	V_{IH}	V_{IL}	V_{CC}	Q_{OUT}
Deselect	Asynchronous Chip Select	V_{IH}	X	X	X	X	X	X	V_{IH}	V_{IH}	V_{CC}	High Z
	Synchronous Chip Select	V_{IH}	⌐	X	X	X	X	X	V_{IH}	V_{IH}	V_{CC}	High Z
Int$_e$ligent Identifier	Manufacturer	V_{IL}	V_{IL}	X	X	V_H	X	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Q_{OUT} = 0089H
	Device	V_{IL}	V_{IL}	X	X	V_H	X	V_{IH}	V_{IH}	V_{IH}	V_{CC}	Q_{OUT} = 66F6H
Blank Check	Ones	V_{IL}	V_{IL}	V_{IH}	A10	A9	A8	A0	V_{IH}	V_{PP}	(Note 2)	Zeros
	Zeros	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8	A0	V_{IH}	V_{PP}	(Note 2)	Ones
Program	Ones	V_{IH}	V_{IL}	V_{IH}	A10	A9	A8	A0	V_{IL}	V_{PP}	(Note 2)	D_{IN}
	Zeros	V_{IH}	V_{IL}	V_{IL}	A10	A9	A8	A0	V_{IL}	V_{PP}	(Note 2)	D_{IN}

Table 1. Mode Table (Continued)

Mode	Pins	$\overline{S}/\overline{S_s}/\overline{G_p}$	$C/\overline{E_p}$	pF	A10	A9	A8	A0	$\overline{P}$	$\overline{i}/V_{PP}$	V_{CC}	DQ
Program Verify	Ones	V_{IL}	V_{IL}	V_{IH}	A10	A9	A8	A0	V_{IH}	V_{PP}	(Note 2)	Ones
	Zeros	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8	A0	V_{IH}	V_{PP}	(Note 2)	Zeros
Synchronous Chip Select Program		V_{IH}	V_{IL}	X	X	X	V_H	X	V_{IL}	V_{PP}	(Note 2)	High Z
Initialize Register Program		V_{IH}	V_{IL}	X	V_H	X	X	X	V_{IL}	V_{PP}	(Note 2)	D_{IN}
Initialize Register Read		V_{IL}	V_{IL}	X	X	X	X	X	V_{IH}	V_{IL}	(Note 2)	Q_{OUT}
Program Inhibit		X	V_{IH}	X	X	X	X	X	X	V_{PP}	(Note 2)	High Z

NOTES:
1. Refer to A.C. Test Points for V_{IH} and V_{IL} levels. A V_{IH} to V_{IL} transition is represented by ⌝, and a V_{IL} to V_{IH} transition is represented by ⌜. X represents either V_{IH} or V_{IL}. See D.C. programming characteristics for V_H and V_{PP}.
2. V_{CC} = 6.25V ±0.25V during programming.

READ MODE

The 27C203 read operation is synchronous. Data registers on the output buffers (Figure 3) allow high-bandwidth, pipelined read operations without the additional components that would normally be required. By using these data registers along with a programmable initial word feature, state machine designs can be implemented without the use of external latches.

The chip select (output enable) can be programmed to be synchronous ($\overline{Ss}$) or left in the default asynchronous state ($\overline{S}$) (Figure 3). The chip select is programmed to be synchronous in pipelined bus applications so the data output triggers off the rising edge of the clock (C) signal. In state machine applications, the chip select can be programmed or left unprogrammed, depending on the needs of the design. Pipelined and state machine applications are detailed below.

PIPELINED BUS APPLICATION (80376 OR 80386)

The 27C203 pipelined EPROM interfaces with the 80376/80386 pipelined bus when programmed in the synchronous chip select mode. Figure 4 shows a 376™ embedded processor with the 27C203 in a simple embedded system.

Valid address information must be stable for the minimum address setup time (t_{AVCH}) before the data can be shifted to the outputs. The data is loaded in the data registers on the rising edge of the 27C203's C. The same C edge latches the synchronous chip select state into the chip select register. To activate the next output, the $\overline{Ss}$ input must be low before the C rising edge. Following the rising edge of the C, the outputs become valid (t_{CHQV}).

To deselect the device in the next output state, the $\overline{Ss}$ must be high for at least the synchronous select setup time (t_{SVCH}) before the C rising edge. Follow-

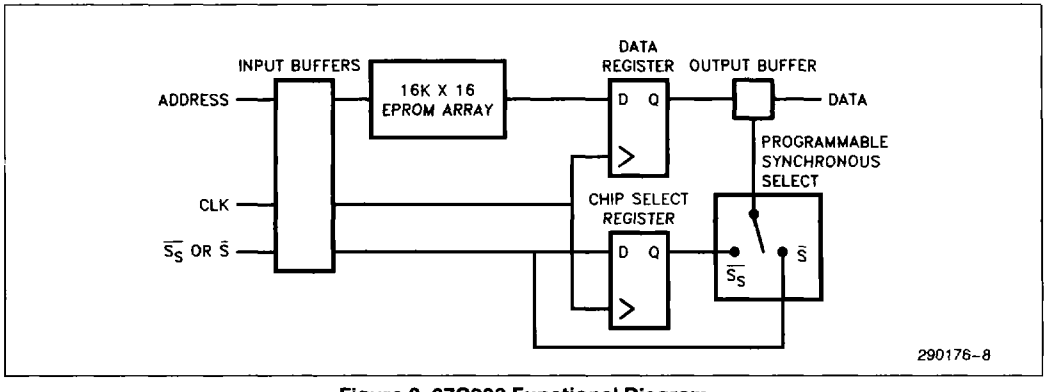


Figure 3. 27C203 Functional Diagram

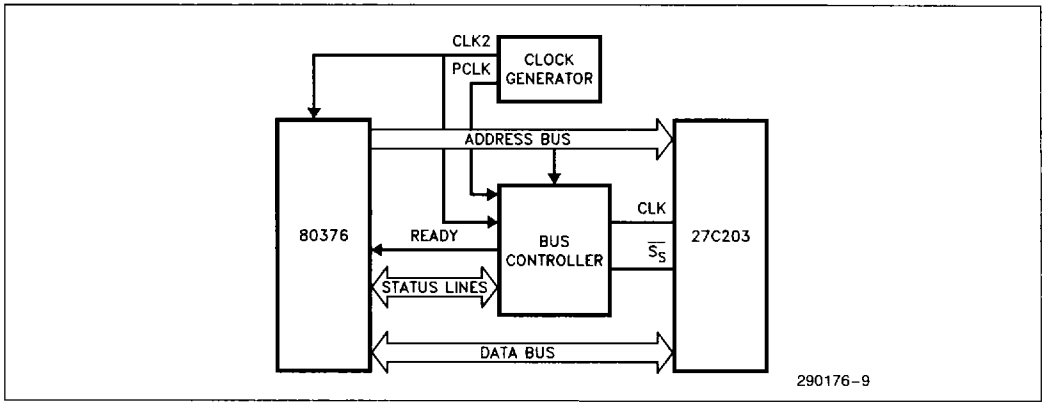


Figure 4. 27C203 in Simple 80376 Embedded System

ing the rising edge of the C, the outputs become tri-stated (t_{CHQZ}).

Buffering may be needed to avoid bus contention when different types of pipelined memories are bussed together. For common 27C203's with synchronous chip selects, the chip deselect times are sufficiently fast to minimize active output overlap. The synchronization of one device's selection with another's deselection is accomplished through common clock inputs (C must be common with multiple synchronously selected devices).

STATE MACHINE APPLICATION

A programmable initial word feature, combined with the data registers, optimize the 27C203 for state machine designs. The 16-bit initial word is active (t_{ILQV}) when the Initialize Register Enable pin ($\overline{I}$) is brought low for a minimum pulse width (t_{ILIH}). A recovery time (t_{IHCH}) is required before the next C rising edge.

The chip select can be programmed to be either synchronous ($\overline{Ss}$) or left in the default asynchronous state ($\overline{S}$), depending on the needs of the application. With asynchronous operation, data is read when chip select ($\overline{S}$) is brought low. The registered data will then become valid in the chip select access time (t_{SLQV}). To deselect the device, $\overline{S}$ must be raised high and the outputs will become tri-stated (t_{SHQZ}).

SYSTEM DESIGN CONSIDERATIONS

The 27C203 is a high performance memory with exceptionally strong output drive capability for fast output response. Input levels are sensitive to power supply stability. Special considerations must be given to the large supply current swings associated with switching 16 powerful output drivers. Minimizing power supply inductance is critical. Wide, short traces with low inductance must be connected from the circuit board's ground and V_{CC} plane to each device. V_{CC} transients must be suppressed with high-frequency 0.1 μF capacitors. Where the solid ground plane of a multilayer board is not available, bulk electrolytic capacitors (typically 4.7μF) should decouple the V_{CC} and the ground supplies for each group of four 27C203 devices.

The 30pF load capacitance specified in the A.C. Test Conditions is not a system design limitation. The 27C203 has the output drive capability to handle the capacitive loading of large memory arrays. However, access times must be appropriately derated for loading in excess of 30pF. t_{CHQV}, t_{SLQV} and t_{ILQV} should be derated 6ns/100pF with output loading greater than 30pF.

PROGRAMMING MODE

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

To minimize data access time delays, the 27C203 utilizes a 2-transistor cell with differential sensing. The 2-transistor cells are partitioned into "ONES" and "ZEROS" arrays. Programming is done in two passes; once in the "ONES" half of the memory array and once in the "ZEROS" half. The same data word must be presented to the device in both passes. A program function (PF) pin is provided to control this partitioning (see Figure 5).

When V_{PP} and V_{CC} are raised to their programming voltage (Table 2), the 27C203 becomes asynchronous and the programming mode is entered. Chip Select ($\overline{S}/\overline{Ss}$) becomes a programming output enable ($\overline{Gp}$), and Clock (C) becomes a chip enable ($\overline{Ep}$). The programming pin ($\overline{P}$) is brought to the TTL-low level to activate the EPROM programming pulse while the programming output enable ($\overline{Gp}$) is held at a TTL-high level.

Outputs are active whenever $\overline{Gp}$ and $\overline{Ep}$ are low. $\overline{Ep}$ does not need to be toggled as it does while serving the read mode Clock function. This facilitates gang programming by allowing $\overline{Gp}$ to be a common verify control line while $\overline{Ep}$ controls individual device selection, eliminating bus contention.

PROGRAM INHIBIT

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{P}$ or $\overline{Ep}$ prevents devices from being programmed.

Except for $\overline{Ep}$, all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{P}$ input, with V_{PP} at programming voltage, $\overline{Ep}$ at a TTL-low level and $\overline{G_p}$ at V_{IH} will program the selected device.

PROGRAM VERIFY/BLANK CHECK

The program verify mode is activated when the programming output enable pin ($\overline{Gp}$) is at a TTL-low level, V_{PP} and V_{CC} are at their programming levels, and the program control line ($\overline{P}$) is at a TTL-high level. Blank Check individually confirms unprogrammed status of both arrays **(a blank check cannot be done with a normal read operation with the 2-transistor cell)**. Program verify is used to check programmed status. The elevated V_{CC} voltage used during Program Verify ensures high programming margins and long-term data retention with maximum noise immunity.

The program/verify cycle begins with the "ONES" array; the Program Function pin (PF) is held at a TTL-high level. The "ONES" programming is completed when the desired "ONES" bits are verified changed from their unprogrammed state ("ZEROS")

Programming is not complete, however, until the "ZEROS" array program/verify cycle is also finished. The "ZEROS" cycle begins when PF is brought to a TTL-low level. The "ZEROS" programming is completed when the desired "ZEROS" bits are verified changed from their unprogrammed state ("ONES").

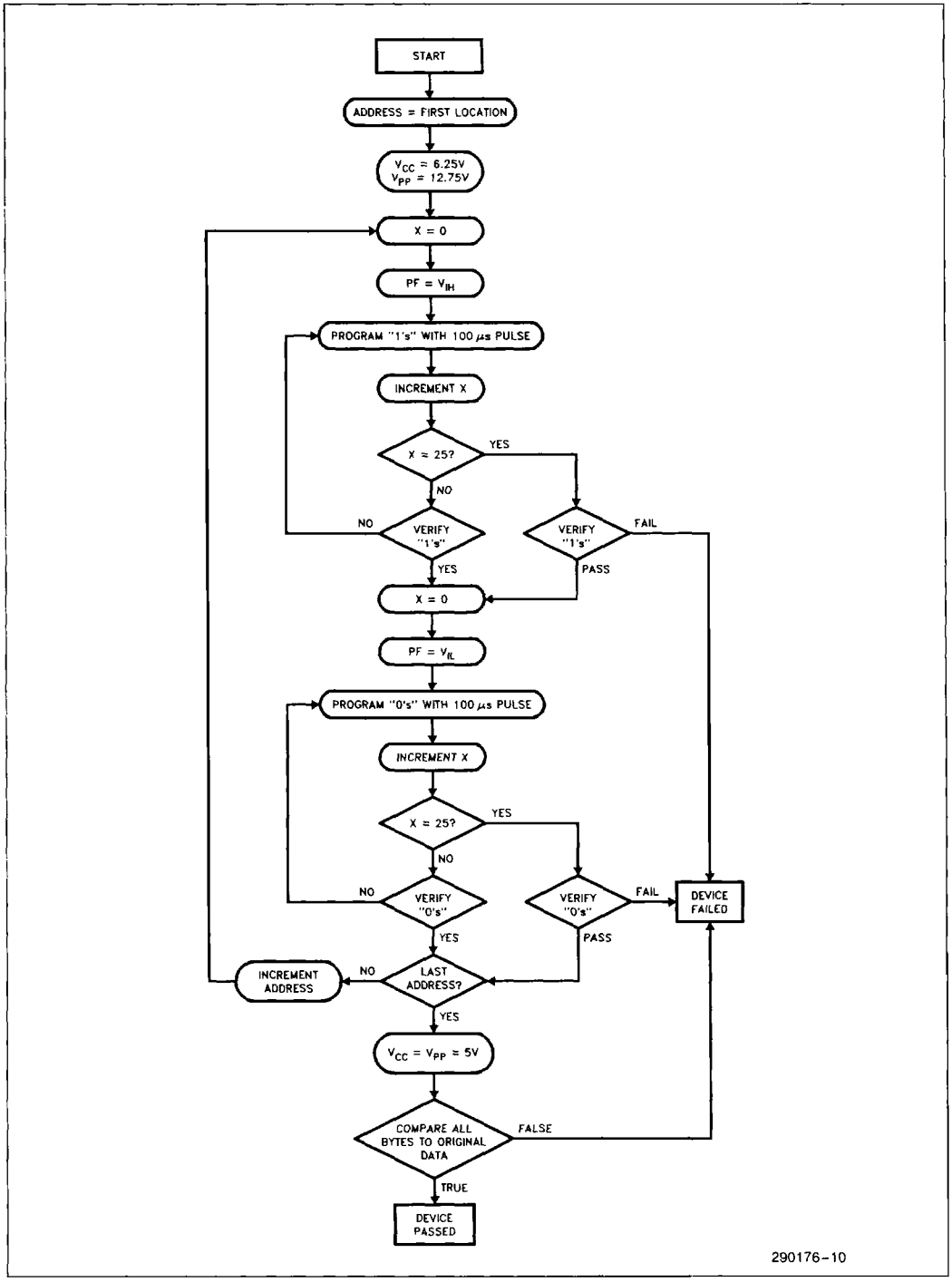


Figure 5. 27C203 Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Operations

The Quick-Pulse Programming algorithm is used to program Intel's 27C203. Developed to substantially reduce production programming throughput time, this algorithm can program a 27C203 in under four seconds. Actual programming time depends on the PROM programmer used.

The Quick-Pulse Programming algorithm uses a 100 microsecond initial-pulse followed by a word verification to determine when the addressed word is correctly programmed. The algorithm terminates if 25 100 μs pulses fail to program a word. This is repeated for both the "ONES" and "ZEROS" programming. Figure 5 shows the 27C203 Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/word-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. When programming is complete, all words should be compared to the original data in a standard read mode with V_{CC} = 5.0V.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type. Programming equipment can automatically match a device with its proper programming algorithm.

The Identifier mode is activated when A9 is at high voltage (V_H). A0 determines the information being accessed. The first address (A0 = V_{IL}) accesses the manufacturer code and the second (A0 = V_{IH}) accesses the device code.

SPECIAL FEATURE PROGRAMMING

The Chip Select synchronous state ($\overline{Ss}$) and the initialize register contents are both UV-erasable and user-programmable. Programming operations for these special 27C203 features are described below and waveforms are shown in Figure 7.

SYNCHRONOUS CHIP SELECT PROGRAMMING

The chip select pin's default (erased) state is asynchronous ($\overline{S}$). The synchronous state ($\overline{Ss}$) is programmed by raising A8 to V_H (Figure 7) for twenty five 100 microsecond program pulses. Program verify is accomplished with a functionality check; when $\overline{Ss}$ is programmed, the state of the outputs, valid or tri-state, can only be changed with a clock (C) rising edge.

INITIALIZE REGISTER CONTENTS PROGRAMMING

When the initialize register enable pin is brought low, the initialize register contents override the output generated by normal read oprations. The contents are all "ZEROS" in the erased state. To program the register, A10 is raised to V_H (Figure 7). The remaining setup and programming parameters are the same as the program "ONES" mode, with the data inputs set to the desired initial-condition-vector data. The initialize register read mode or the initialize register verify mode allow programming verification.

Erasure Characteristics (for UV-Window Packages)

Light with wavelengths shorter than 4000 Angstroms (Å) causes EPROM erasure. Sunlight and some florescent lamps have wavelengths in the 3000Å–4000Å range. Constant exposure to room-level florescent light can erase an EPROM in about three years while direct sunlight erasure can occur within one week. Covering windowed EPROMs with opaque labels prevents such unintended erasure.

The recommended erasure procedure is to expose the EPROM to a 2537Å ultraviolet (UV) source for a minimum integrated dose (intensity x exposure time) of 15 W-sec/cm^2. The EPROM should be placed within one inch of the light source and will erase in 15-20 minutes with a typical 12000 μW/cm^2 lamp.

Overexposure to high-intensity UV light can cause permanent device damage. The maximum integrated dose allowed is 7258 W-sec/cm^2 (approximately 1 week at 12000 μW/cm).

D.C. Programming Characteristics $T_A = 25°C \pm 5°C$

Table 2

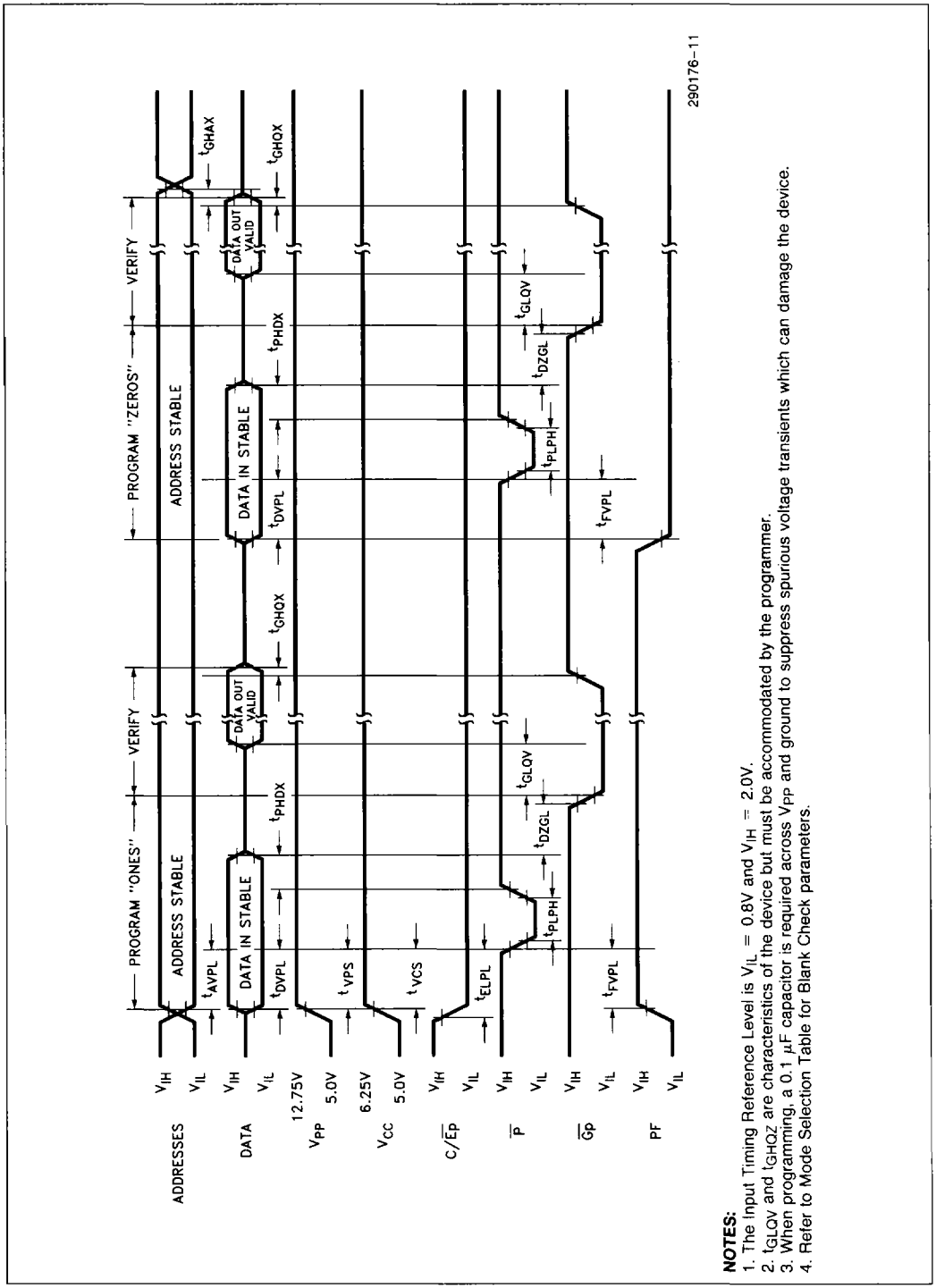
Symbol	Parameter	Limits			Conditions
		Min	Max	Units	
I_{IL}	Input Low Load Current		10	μA	$V_{IN} = 0V$
I_{IH}	Input High Load Current		10	μA	$V_{IN} = 6V$
I_{OZL}	Tri-state Low Leakage		10	μA	$V_{OUT} = 0V$
I_{OZH}	Tri-state High Leakage		15	μA	$V_{OUT} = 6V$
I_{CC}(1)	V_{CC} Current Active		100	mA	$\overline{Ep} = \overline{P} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Verify Output Low Volt.		0.45	V	$I_{OL} = 16$ mA
V_{OH}	Verify Output High Volt.	2.4		V	$I_{OH} = -4$ mA
I_{PP}	V_{PP} Supply Current		50	mA	$\overline{Ep} = \overline{P} = V_{IL}$
V_H	Input High Voltage	11.5	12.5	V	$V_{CC} = 5V$
V_{PP}	V_{PP} Supply Voltage	12.5	13.0	V	
V_{CC}	V_{CC} Supply Voltage	6.0	6.5	V	

A.C. Programming Characteristics $T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Conditions
		Min	Max	Units	
t_{AVPL}	Address Setup Time	1		μs	
t_{DZGL}	$\overline{Gp}$ Setup Time	1		μs	
t_{DVPL}	Data Setup Time			μs	
t_{FVPL}	PF Setup Time	1		μs	
t_{GHAX}	Address Hold Time	0		μs	
*t_{PHDX}	Data Hold Time	1		μs	
t_{GHQX}	Output Deselect Time	0	50	ns	(Note 2)
t_{VPS}	V_{PP} Setup time	1		μs	
t_{VCS}	V_{CC} Setup Time	1		μs	
t_{ELPL}	$\overline{Ep}$ Setup Time	1		μs	
t_{AHPL}	Special Functions Address Setup Time	1		μs	A8 or A10 = V_H
t_{PLPH}	Program ($\overline{P}$) Pulse Width	95	105	μs	Quick-Pulse™ Programming
t_{GLQV}	Data Valid from $\overline{OE}$		50	μs	
t_{AVQV}	Intelligent Identifier Valid from Address Valid		100	ns	A9 = V_H Other A's = V_{IL}
t_{ILQV}	Initialize Register Verify from $\overline{I}$ Low		100	ns	$A_{10} = V_H$
t_{PLPH2}	Synchronous Chip Select Program Pulse Width	95	105	μs	$A_8 = V_H$

NOTES:
1. The maximum current value is with outpus DQ0–DQ15 unloaded.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

***AC Conditions of Test**
Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V



NOTES:
1. The Input Timing Reference Level is V_{IL} = 0.8V and V_{IH} = 2.0V.
2. t_{GLQV} and t_{GHQZ} are characteristics of the device but must be accommodated by the programmer.
3. When programming, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. Refer to Mode Selection Table for Blank Check parameters.

Figure 6. Programming Waveforms

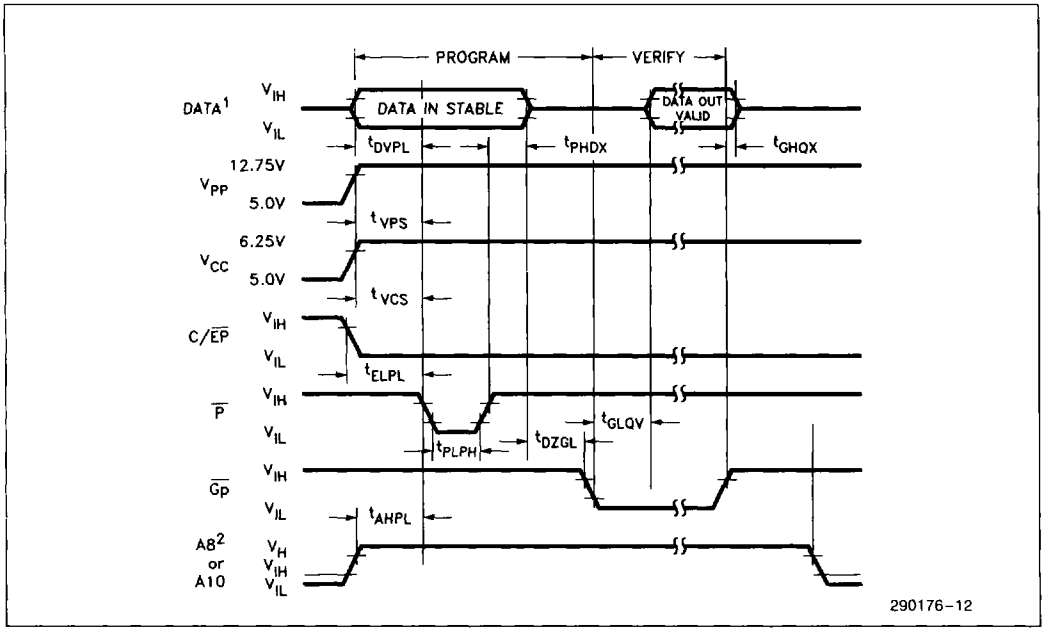


Figure 7. Synchronous Chip Select and Initial Word Programming Waveforms

NOTES:
1. Data waveform applies to initial word programming function only.
2. Waveform applies to A8 when programming the Synchronous Chip Select function. A10 programs the Initialize register.